EXAR ...the analog plus company™

Data Acquisition Products 1995

EXAR ...the analog plus company

About The Company

EXAR Corporation manufactures and markets standard products and application specific integrated circuits emphasizing the company's mixed-signal design and test expertise. A pioneer in analog circuits since 1971, EXAR is strongly positioned as a key supplier for the worldwide mixed-signal IC market. EXAR calls itself the "analog plus"™ company in reference to its long history in analog, and its mixed-signal capability of combining analog, digital, EEPROM and switched capacitor filter (SCF) designs on the same silicon substrate. This capability, along with the company's in-depth system expertise, allows EXAR to provide its customers with system level solutions.

EXAR Corporation expanded its product offerings to include data converter products with the acquisition of Micro Power Systems Inc. in June 1994. Micro Power Systems, a recognized and innovative leader in the development of high-performance data-acquisition circuits, achieved market-share leader status as a supplier of data converters to the document-imaging industry for products such as scanners, digital cameras and digital copiers.

As a company, EXAR focuses on the communications, consumer, computer peripheral and document imaging markets. EXAR addresses these markets with proprietary and alternate sourced standard products, and custom designs. The Company supports standard cell, full custom, standard cell/full custom and semi-custom designs technologies. EXAR has a wide variety of processes, such as a 6 micron high voltage bipolar, a 0.8 micron BiCMOS, and a 0.6 micron CMOS, to maximize circuit performance.

EXAR is dedicated to providing its customers with a competitive advantage by delivering innovative high quality mixed-signal system solutions in the shortest time. EXAR supports its customers through experienced IC designers with systems knowledge, as well as an established worldwide Field Application Engineering (FAE) organization and an Application Engineering staff located at headquarters.

EXAR is committed to the principal of Total Quality Management and the philosophy of continuous improvement. All employees have been trained in this area and the Company has full participation and support. Examples of EXAR's quality goals include 95% on-time delivery and an out-going PPM level of less than 25.

EXAR is ISO 9001 registered. The accrediting bodies are the Dutch Council for Certification (RVC) of the Netherlands, and the Registrar Accreditation Board (RAB) of the United States.

EXAR Corporation is headquartered in San Jose, California with sales offices across the USA, Europe, Asia and Japan.

Ordering Information

Orders may be placed through your local EXAR office, authorized sales representatives or distributors. Call them for current pricing and availability or for any other questions you may have regarding EXAR products. The list of EXAR offices, Sales Representatives and Distributors are provided in Section 11.

EXAR Corporation

Data Acquisition Products

Data Book

1995

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein are only for illustration purposes and may vary upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

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Analog-to-Digital Converter Overview

Part No.	Resolution (Bits)	Speed	Max Power	# Chan.	Track/ Hold	V_{REF} Range	µP Bus P–Parallel S–Serial	Pkg
MP8790	12	2 MSPS	225	1	Y	1 to 5 V	12, P/S	PQFP
MP8791	12	2 MSPS	225	1	Y	1 to 5 V	12, P	PDIP, SOIC
MP3274	12	15µS	200	32	Y	4 V	8/12, µP, P/S	PGA, PLCC
MP3275	12	15µS	200	16	Y	4 V	S	PQFP
MP3276	12	15µS	200	16	Y	4 V	8/12, µP, P/S	PGA, PLCC
MP87091	12	750 KSPS	225	1	Y	1 to 5 V	12, P	PDIP, SOIC
MP87092	12	750 KSPS	225	1	Y	1 to 5 V	S	PDIP, SOIC
MP8782	10	5 MSPS	200	1	Y	1 to 5 V	10, P	PQFP
MP8784	10	5 MSPS	200	1	Y	1 to 5 V	10, P	PDIP, SOIC
**MP8784A	10	15 MSPS	200	1	Y	1 to 5 V	10, P	PDIP, SOIC
MP7695	10	1 MSPS	60	1	Y	1 to 5 V	10, P	PDIP, CDIP, SOIC
MP8795	10	1 MSPS	50	1	Y	1 to 5 V	10, P	PDIP, SOIC
MP8796	10	1 MSPS	50	1	Y	1 to 5 V	10, P	SOIC
MP8798	10	1 MSPS	50	4	Y	1 to 5 V	10, P	PDIP, SOIC, SSOP
MP8799	10	1 MSPS	50	8	Y	1 to 5 V	10, P	PQFP
MP87198	10	1 MSPS	50	4	Y	1 to 5 V	10, P	PDIP, SOIC, SSOP
MP87095	10	750 KSPS	50	1	Y	1 to 5 V	10, P	PDIP, SOIC
MP87098	10	750 KSPS	50	4	Y	1 to 5 V	10, P	PDIP, SOIC, SSOP
MP87099	10	750 KSPS	50	8	Y	1 to 5 V	10, P	PQFP
MP7696	9	2 MSPS	50	1	Y	1 to 5 V	9, P	PDIP, SOIC
MP8775	8	20 MSPS	125	1	Y	1 to 5 V	8, P	PDIP, SOIC, SSOP
MP8776	8	20 MSPS	150	1	Y	1 to 5 V	8, P	PDIP, SOIC, SSOP
MP8785	8	20 MSPS	125	1	Y	1 to 5 V	8, P	SOIC, PDIP
MP8786	8	20 MSPS	150	1	Y	1 to 5 V	8, P	SOIC, PDIP, SSOP
MP8780	8	15 MSPS	425	1	Y	1 to 5 V	8, P	PDIP, SOIC
MP7684A	8	14 MSPS	425	1	Y	1 to 5 V	8, P	PDIP, CDIP, SOIC
MP7690A	8	14 MSPS	425	1	Y	1 to 5 V	8, P	CDIP
MP7684	8	10 MSPS	450	1	Y	1 to 5 V	8, P	PDIP, CDIP, SOIC
MP7690	8	10 MSPS	450	1	Y	1 to 5 V	8, P	CDIP
MP7683	8	3 MSPS	180	1	Y	1 to 5 V	8, P	PDIP, CDIP, SOIC, SSOP
MP7693	8	3 MSPS	180	1	Y	1 to 5 V	8, P	PDIP, SOIC, PLCC
MP7783	8	2.5 MSPS	180	1	Y	1 to 5 V	8, P	PDIP, SOIC
MP8820	8	1.6 MSPS	225	8	Y	0.5 to 1.5 V	µP, P	SOIC, SSOP
MP7686	6	20 MSPS	200	1	Y	1 to 5 V	6, P	PDIP, CDIP, SOIC
MP7682	6	15 MSPS	250	1	Y	1 to 5 V	6, P	PDIP, CDIP, SOIC, LCC

Analog-to-Digital Converters with Gain and Offset Control

Part No.	Resolution (Bits)	Speed	Max Power	# Chan.	Track /Hold	Gain Control (Bits)	Offset Control (Bits)	V_{REF} Range	µP Bus P–Parallel S–Serial	Pkg
MP8830	10	1.25 MSPS	700	3***	Y	9	6	1 V	P	PQFP
**MP8831	10	1.25 MSPS	250	1	Y	9	6	1 V	P	SOIC

**Planned ***3 Independent Channels

Digital-to-Analog Converter Overview

Part #	Resolution (Bits)	# DACs	I or V/ FIX or MUL	Buffered or Double Buffered	Parallel or Serial	Operating Voltage Range	Pkg
MP7616	16	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7626	16	1	I/M 4Q	B	P	4.5 to 16.5 V	PDIP, CDIP, PLCC
MP7636A	16	1	I/M 4Q	DB	P	4.5 to 16.5 V	SOIC
MP7610	14	8	V/F	DB	S	+12/–12 V	PDIP, SOIC
MP7611	14	8	V/F	DB	P	+12/–12 V	PQFP, PGA, PLCC
MP7614	14	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7612	12	8	V/F	DB	S	+12/–12 V	PDIP, SOIC
MP7613	12	8	V/F	DB	P	+12/–12 V	PQFP, PGA, PLCC
MP7680	12	4	I/M 4Q	DB	P	4.5 to 5.5 V	PDIP, CDIP, PQFP
MP1208	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1209	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1210	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1230	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1230A	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP1231	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP1231A	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP1232	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1232A	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7541B	12	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7542	12	1	I/M 4Q	DB	P	4.5 to 5.5 V	PDIP, CDIP, SOIC
MP7543	12	1	I/M 4Q		S	4.5 to 5.5 V	PDIP, CDIP, SOIC, PLCC
MP7545	12	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7545B	12	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, SOIC, PLCC
MP7645B	12	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP
MP7533	10	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7633	10	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7641	8	8	V/M 2Q	B	S	±5, +5, +10 V	PDIP, SOIC
MP7651	8	8	V/M 2Q	B	S	±5 V	PDIP, SOIC
MP7670	8	8	V/M 4Q	B	S	–5, +5 V	PDIP, SOIC
MP8840	8	8	V/M 4Q	B	S	–5, +5 V	PDIP, SOIC
MP7643	8	4	V/M 2Q	B	P	±5, +5, +10 V	PDIP, SOIC
MP7652	8	4	V/M 2Q	B	S	±5, +5, +10 V	PDIP, SOIC
MP7226	8	4	V/F	DB	P	±5/15 V	PDIP, SOIC, PLCC
MP7628	8	4	I/M 4Q	B	P	4.5 to 5.5 V	PDIP, CDIP, SOIC, PLCC
MP7528	8	2	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7529A	8	2	I/M 4Q	B	P	4.5 to 16 V	PDIP, SOIC, PLCC
MP7529B	8	2	I/M 4Q	B	P	4.5 to 5.5 V	PDIP, SOIC, PLCC
MP7228	8	8	V/F	DB	P	±5/15 V	PDIP, CDIP, PLCC, SOIC
MP7523	8	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7524	8	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7524A	8	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, SOIC

Definitions

I = Current Output, V = Voltage Output, F = Fixed Reference, M 2Q = Two Quadrant Multiplying, M 4Q = Four Quadrant Multiplying

Low Voltage Converter Overview

Low Voltage 3.3 V Digital-to-Analog Converters (3.0 to 3.6 V Operation, Tested at 3.0 V. For Performance at 2.7 V, Contact Local Sales Representative)

Part #	*Resolution (Bits)*	*# DACs*	*I or V/ FIX or MUL*	*Buffered or Double Buffered*	*Parallel or Serial*	*Operating Voltage Range*	*Pkg*
MP75L24	8	1	I/M 4Q	B	P	3.0 to 3.6 V	PDIP, SOIC
MP75L43	12	1	I/M 4Q		S	3.0 to 3.6 V	PDIP, SOIC
MP75L45	12	1	I/M 4Q	B	P	3.0 to 3.6 V	PDIP, SOIC, SSOP

Definitions
I = Current Output
M 4Q = Four Quadrant Multiplying

Low Voltage 3.3 V Analog-to-Digital Converters (3.0 to 3.6 V Operation, Tested at 3.0 V. For Performance at 2.7 V, Contact Local Sales Representative)

Part #	*Resolution (Bits)*	*Speed*	*Max Power*	*# Chan.*	*Track/ Hold*	*V_{REF} Range*	*µP Bus*	*Pkg*
MP87L91	12	1 MSPS	50	1	Y	1 to 3 V	12	PDIP, SOIC
MP87L92	12	0.5 MSPS	50	1	Y	1 to 3 V	12	PDIP, SOIC
MP87L82	10	2 MSPS	50	1	Y	1 to 3 V	10	PQFP
MP87L84	10	2 MSPS	50	1	Y	1 to 3 V	10	PDIP, SOIC
MP87L95	10	0.25 MSPS	10	1	Y	1 to 3 V	10	PDIP, SOIC
MP87L98	10	0.25 MSPS	10	4	Y	1 to 3 V	10	PDIP, SOIC, SSOP
MP87L99	10	0.25 MSPS	10	8	Y	1 to 3 V	10	PQFP
MP76L90	8	5 MSPS	45	1	Y	1 to 3 V	8	PDIP, SOIC
MP87L75	8	10 MSPS	35	1	Y	1 to 3 V	8	PDIP, SOIC, SSOP
MP87L85	8	10 MSPS	35	1	Y	1 to 3 V	8	PDIP, SOIC
MP87L76	8	10 MSPS	35	1	Y	1 to 3 V	8	PDIP, SOIC, SSOP
MP76L86	6	6 MSPS	25	1	Y	1 to 3 V	8	PDIP, SOIC

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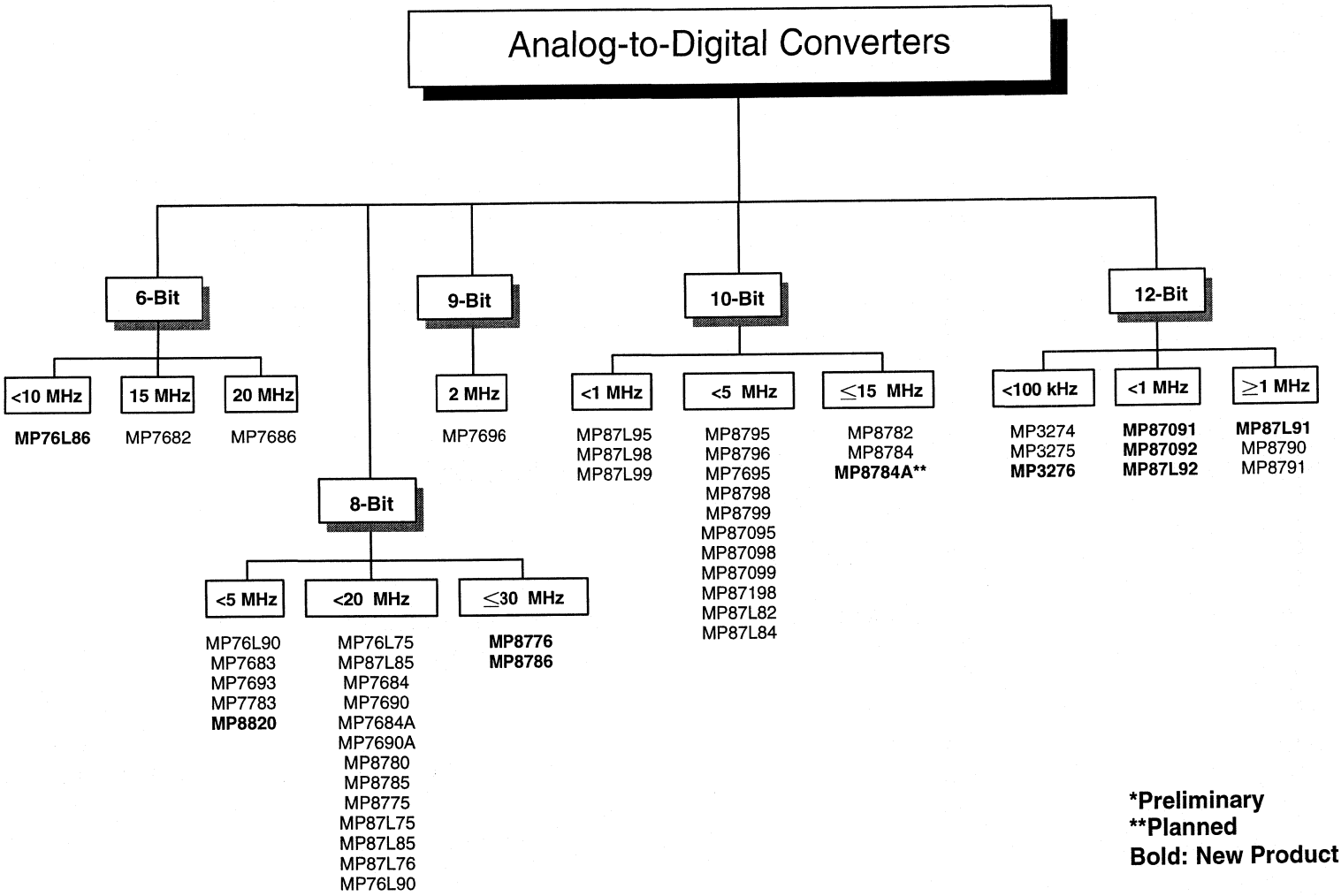

***Preliminary**
****Planned**
Bold: New Product

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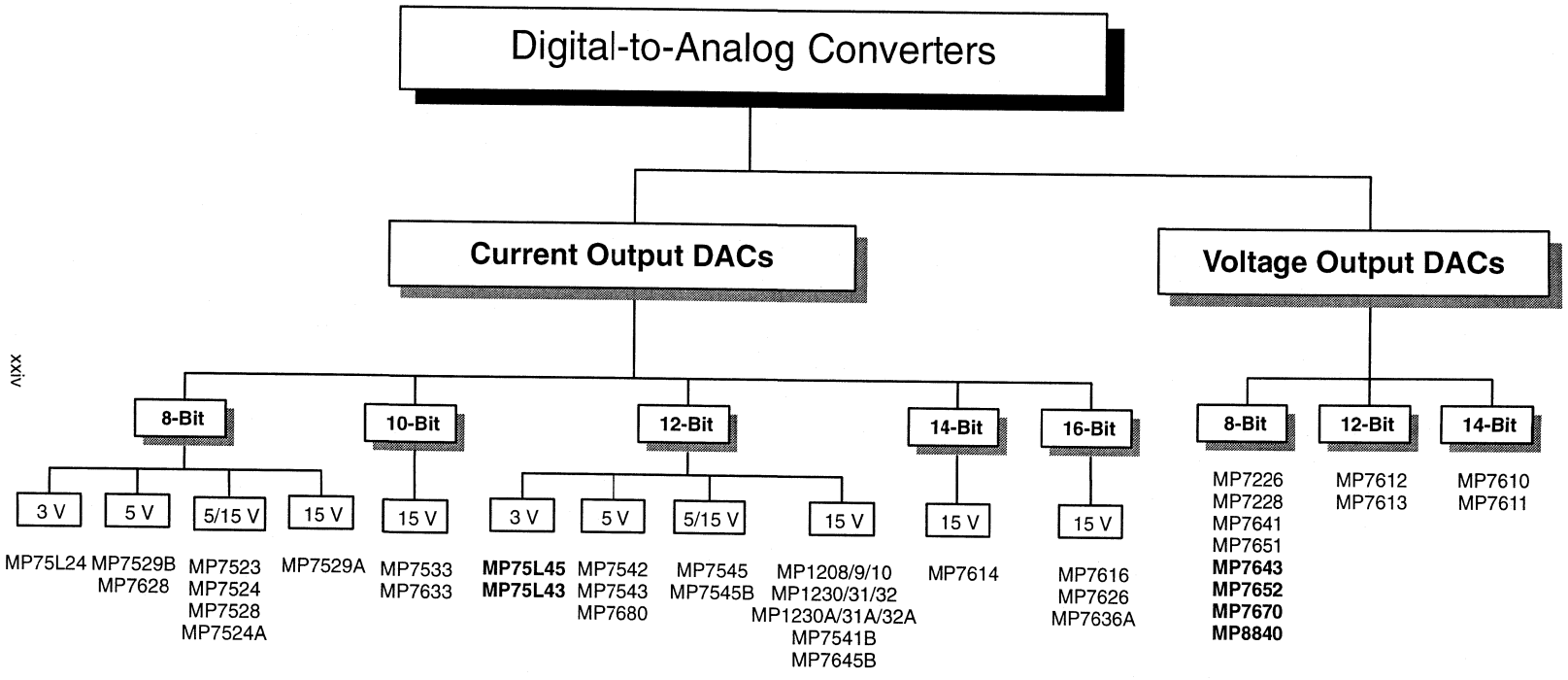

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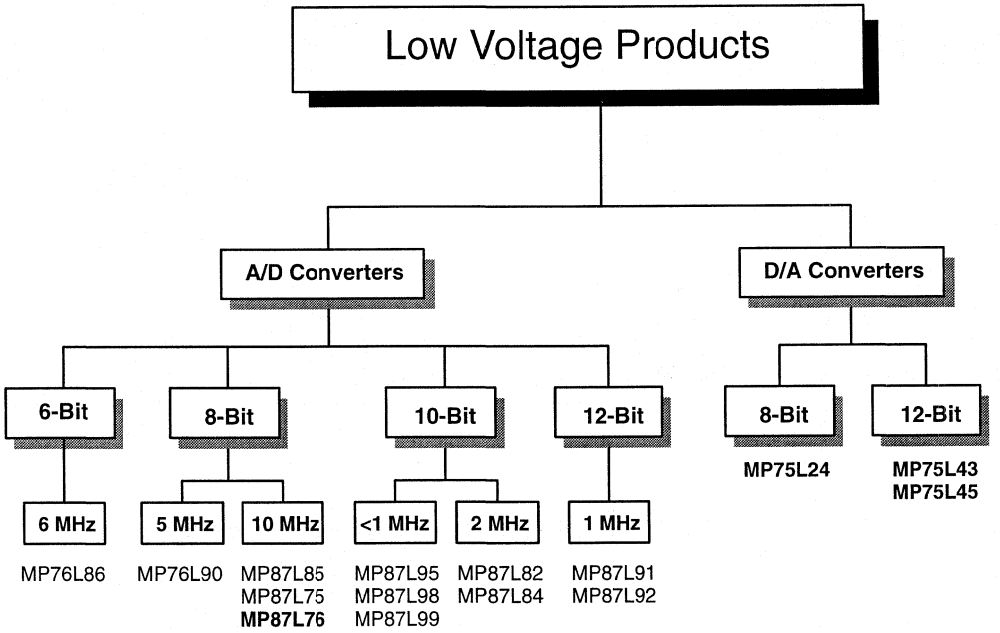

***Preliminary**
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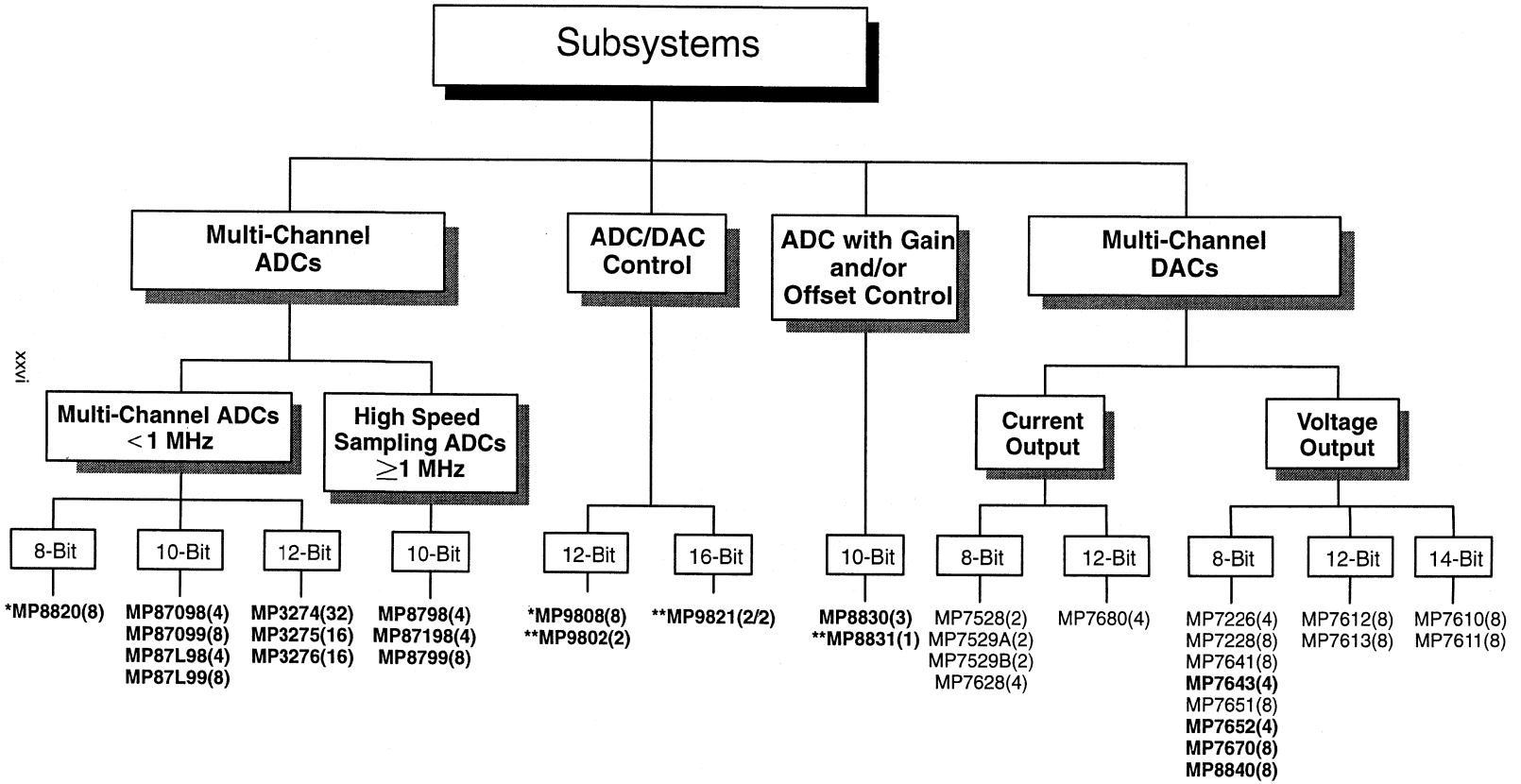
EXAR ...the analog plus company



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Section 1

General Information

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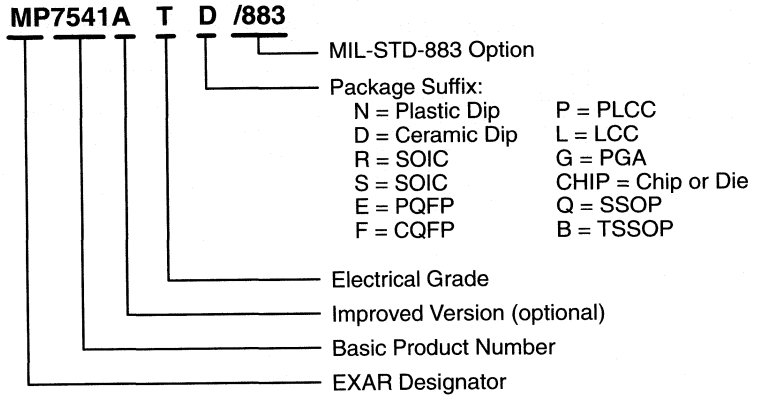
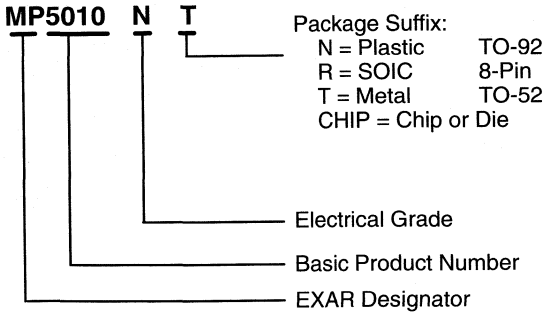
Data Acquisition Products

D/A and A/D Converters



Voltage References



EXAR supplies its products in chip or die form for hybrid or multichip applications. Contact your sales representative for information or quotation. EXAR products are also available through chip processor, Chip Supply Inc.

Cross Reference

Pin-for-Pin & Functional Equivalents

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
Analog Devices		
AD1341	MP3274	FE
	MP3275	FE
	MP3276	FE
AD1671	MP8790	FE
	MP8791	FE
	MP8792	FE
AD363	MP3274	FE
	MP3275	FE
	MP3276	FE
AD364	MP3274	FE
	MP3275	FE
	MP3276	FE
AD390	MP7613	FE
AD392	MP7613	FE
AD567	MP1230	FE
	MP1231	FE
	MP1232	FE
AD574A	MP574A	PP
AD589	MP5010	PP
AD671	MP8790	FE
	MP8791	FE
	MP8792	FE
AD674	MP674	PP
AD7226	MP7226	PP
	MP8840	FE
AD7228	MP7228	PP
	MP8840	FE
AD7237	MP7613	FE
AD7244	MP7610	FE
AD7247	MP7613	FE
AD75069	MP7613	FE
AD7520	MP7533	PP(P1)
	MP7633	PP(P1)
AD7521	MP7541B	PP(P2)
AD7522	MP7522	PP
AD7523	MP7523	PP
AD7524	MP7524A	PP(P1)
AD7528	MP7528	PP
AD7530	MP7633	PP(P1)
	MP7533	FE
AD7531	MP7541B	PP(P2)
AD7533	MP7533	PP
AD7541	MP7541B	PP(P2)
AD7542	MP7542	PP
	MP1208	FE
	MP1209	FE
	MP1210	FE
AD7543	MP7543	PP
AD7545	MP7545B	PP(P2)
	MP1208	FE
	MP1209	FE
	MP1210	FE
AD7548	MP1230	FE

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
Analog Devices (Cont'd)		
AD7548	MP1231	FE
	MP1232	FE
AD7574	MP7574	PP
AD7581	MP7581	PP
AD7586	MP8790	FE
	MP8791	FE
	MP8792	FE
AD7628	MP7529A	PP(P2)
	MP7529B	FE
AD774B	MP774	PP
AD7776	MP87095	FE
AD7777	MP87098	FE
AD7778	MP87099	FE
AD7820	MP0820	PP
	MP7683	FE
	MP7693	FE
	MP7783	FE
AD7821	MP7683	FE
	MP7693	FE
	MP7783	FE
AD7824	MP0820	FE
AD7828	MP0820	FE
AD7886	MP87091	FE
	MP87092	FE
AD875	MP8784	FE
AD9003	MP8790	FE
	MP8791	FE
	MP8792	FE
AD9005A	MP8791	FE
	MP8792	FE
ADC0820	MP0820	PP
ADC574	MP5010	PP
ADC674	MP674	PP
ADC774	MP774	PP
DAC8408	MP7628	FE
DAC8229	MP7670	FE
DAC8412	MP7613	FE
DAC8426	MP7652	FE
DAC8800	MP7641	FE
DAC8840	MP8840	PP
DAC8841	MP8840	FE
PM7226	MP7226	PP
PM7226A	MP7643	FE
PM7524	MP7524	PP
PM7528	MP7528	PP
PM7533	MP7533	PP
PM7533	MP7533	PP
PM7541	MP7541B	PP(P2)
PM7542	MP7542	PP
PM7543	MP7543	PP
PM7545	MP7545B	PP(P2)
PM7574	MP7574	PP
PM7628	MP7529	PP

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
Analog Devices (Cont'd)		
PM7645	MP7645B	PP(P2)
Burr Brown		
ADC603	MP8791	FE
ADS574	MP574A	PP
ADS674	MP674	PP
ADS774	MP774	PP
ADS7810	MP87091	FE
	MP87092	FE
ADS7819	MP87091	FE
	MP87092	FE
DAC4813	MP7613	FE
DAC4814	MP7612	FE
DAC700	MP7616	FE
	MP7626	FE
	MP7636	FE
DAC702	MP7616	FE
	MP7626	FE
	MP7636	FE
DAC703	MP7616	FE
DAC708	MP7616	FE
	MP7626	FE
	MP7636	FE
DAC7528	MP7643	FE
DAC7541	MP7541B	PP(P2)
DAC7545A	MP7545B	PP(P2)
	MP7542	FE
DAC7800	MP7612	FE
DAC7801	MP7613	FE
DAC7802	MP7613	FE
Crystal Semiconductor		
CS5412	MP8790	FE
	MP8791	FE
EXAR		
MP7520	MP7633	PP(P1)
MP7521	MP7541B	PP(P2)
MP7530	MP7633	PP(P1)
MP7531	MP7541B	PP(P2)
MP7682	MP7686	PP
Harris		
AD7523	MP7523	PP
	MP7524	FE
AD7533	MP7533	PP
	MP7633	FE
AD7541	MP7541B	PP(P2)

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
Harris (Cont'd)		
AD7545	MP7545B	PP(P2)
CA3300	MP7686	PP(P3)
	MP3306	PP
	MP7682	PP
CA3306	MP7686	PP(P3)
	MP3306A	PP
HI1175	MP8785	PP
	MP8775	FE
	MP8776	FE
	MP8786	FE
HI1176	MP8775	FE
	MP8776	FE
	MP8785	FE
	MP8786	FE
HI-5700A	MP7684A	PP(P3)
HI-5701	MP7686	FE
HI1-574A	MP574A	PP
HI1-674A	MP674	PP
HI1-774	MP774	PP
HI5800	MP8790	FE
	MP8791	FE
	MP8792	FE
HI5801	MP8790	FE
	MP8791	FE
ICL8069	MP5010	PP
Linear Technology		
LT1004	MP5010	PP
LT1290	MP3274	FE
	MP3275	FE
	MP3276	FE
LT1293	MP3274	FE
	MP3275	FE
	MP3276	FE
LT1294	MP3274	FE
	MP3275	FE
	MP3276	FE
LT1296	MP3274	FE
	MP3275	FE
	MP3276	FE
LTC1282	MP87L90	FE
	MP87L91	FE
LTC1283	MP87L99	FE
LTC1287	MP87L92	FE
Maxim		
ADC0820	MP0820	PP
MAX120	MP87091	FE
MAX122	MP87091	FE
MAX150	MP0820	FE

TQM™

Notes:
(1) EXAR has a Plastic DIP lower cost version for this product, which is supplied only in Ceramic by the "industry" source.
(2) EXAR warrants these devices over the industrial temp range of –40 to +85°C.
(P) P indicates the preferred device. Some industry part numbers have multiple EXAR part numbers of equal or better performance. All are listed for maximum availability.
P1 = Preferred, ESD < 1500 V, P2 = Preferred, ESD 2000 V, P3 = Preferred, ESD 4000 V

Pin-for-Pin & Functional Equivalents

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
Maxim (Cont'd)		
MAX152	MP76L90	FE
	MP87L75	FE
	MP87L85	FE
	MP87L86	FE
MAX153	MP7683	FE
	MP7693	FE
	MP7783	FE
MAX160	MP7574	PP(2)
MAX161	MP7581	PP
MAX162	MP87091	FE
MAX176	MP87092	FE
MAX180	MP3274	FE
	MP3275	FE
	MP3276	FE
MAX181	MP3274	FE
	MP3275	FE
	MP3276	FE
MAX183	MP87091	FE
MAX186	MP3274	FE
	MP3275	FE
	MP3276	FE
MAX500	MP7652	FE
MAX510	MP7652	FE
MAX526	MP7613	FE
MAX527	MP7613	FE
MAX528	MP8840	FE
	MP7670	FE
MAX529	MP8840	FE
	MP7670	FE
MAX536	MP7612	FE
MAX537	MP7612	FE
MAX7837	MP7613	FE
MAX7847	MP7613	FE
MX574	MP574	PP
MX667	MP7643	FE
MX674	MP674	PP
MX7224	MP7643	FE
MX7225	MP7643	FE
MX7226	MP7226	PP
	MP7643	FE
MX7228	MP7228	PP
	MP7643	FE
MX7520	MP7533	PP(P1)
	MP7541B	PP(P2)
MX7521	MP7541B	PP(P2)
MX7523	MP7523	PP
MP7524	MP7524A	PP(P1)
MX7528	MP7528	PP
MX7530	MP7633	PP(P1)
	MP7533	PP
MX7531	MP7541B	PP(P2)
MX7533	MP7533	PP
MX7541	MP7541B	PP(P2)
MX7542	MP7542	PP
MX7543	MP7543	PP
MX7545	MP7545B	PP(P2)
MX7574	MP7574	PP
MX7581	MP7581	PP

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
Maxim (Cont'd)		
MX767	MP7643	FE
MX7820	MP7683	FE
	MP7693	FE
	MP7783	FE
MX7821	MP7683	FE
	MP7693	FE
	MP7783	FE
MX7824	MP0820	FE
MX7828	MP0820	FE
National		
ADC08061	MP7683	FE
	MP7693	FE
	MP7783	FE
ADC08161	MP7683	FE
	MP7693	FE
	MP7783	FE
ADC0820	MP0820	PP
ADC10061	MP7695	FE
	MP8795	FE
	MP8796	FE
ADC10064	MP87198	FE
	MP8798	FE
ADC10461	MP7695	FE
	MP8795	FE
	MP8796	FE
ADC10464	MP87198	FE
	MP8798	FE
ADC1061	MP87095	FE
ADC10664	MP87198	FE
	MP8798	FE
ADC12038	MP3274	FE
	MP3275	FE
	MP3276	FE
ADC12062	MP87091	FE
	MP8790	FE
	MP8791	FE
ADC12662	MP8790	FE
	MP8791	FE
ADC12L030	MP87L92	FE
DAC0800	MP7523	FE
	MP7524	FE
DAC0801	MP7523	FE
	MP7524	FE
DAC0802	MP7523	FE
	MP7524	FE
DAC0830	MP7523	FE
	MP7524	FE
DAC0831	MP7523	FE
	MP7524	FE
DAC0832	MP7523	FE
	MP7524	FE
DAC0854	MP7652	FE
DAC0890	MP7643	FE
DAC1020	MP7633	PP(P1)
	MP7533	PP

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
National (Cont'd)		
DAC1021	MP7633	PP(P1)
	MP7533	PP
DAC1022	MP7633	PP(P1)
	MP7533	PP
DAC1208	MP1208	PP
	MP7542	FE
	MP7543	FE
	MP7545B	FE
DAC1209	MP1209	PP
	MP7542	FE
	MP7543	FE
	MP7545B	FE
DAC1210	MP1210	PP
	MP7542	FE
	MP7543	FE
	MP7545B	FE
DAC1218	MP7541B	PP(P2)
DAC1219	MP7541B	PP(P2)
DAC1220	MP7541B	PP(P2)
DAC1221	MP7541B	PP(P2)
DAC1222	MP7541B	PP(P2)
DAC1230	MP1230	PP
	MP7542	FE
	MP7543	FE
DAC1231	MP1231	PP
	MP7542	FE
	MP7543	FE
DAC1232	MP1232	PP(1,2)
	MP7542	FE
	MP7543	FE
DAC7541	MP7541B	PP(P2)
DAC7545	MP7545B	PP(P2)
LM113	MP5010	PP
LM185	MP5010	PP
Philips		
ADC0820	MP0820	PP
TDA8703	MP8785	FE
	MP8775	FE
TDA8713	MP8776	FE
	MP8786	FE
Raytheon		
TDC1038	MP8775	FE
	MP8776	FE
	MP8785	FE
	MP8786	FE
TDC1046	MP7686	FE
TDC1048	MP8775	FE
	MP8776	FE
	MP8785	FE
	MP8786	FE
TDC1058	MP8775	FE
	MP8776	FE

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
Raytheon (Cont'd)		
MP8785	FE	
	MP8786	FE
TMC1173-05	MP76L90	FE
TMC1173-10	MP87L75	PP
	MP87L85	PP
	MP76L90	FE
	MP87L86	FE
TMC1175-20	MP8785	PP
	MP8775	FE
	MP8776	FE
	MP8786	FE
Sipex		
HS1068	MP8775	FE
	MP8776	FE
	MP8785	FE
	MP8786	FE
HS3210C-0	MP7645	FE
HS3120B-0	MP7645	FE
HS3120B-2	MP7645	FE
HS3120C-2	MP7645	FE
HS3140B-3	MP7614	PP
HS3140C-3	MP7614	PP
HS574A	MP574A	PP
HS7528	MP7528	PP
HS7541	MP7541B	PP(P2)
HS7542	MP7542	PP
HS7543	MP7543	PP
HS7545	MP7545B	PP(P2)
HS7584	MP7680	PP(P1)
HS9331	MP7626	PP
SP674	MP674	PP
SP7514	MP7614	FE
SP7545	MP7545	PP
SP7645	MP7645	PP
SP774	MP774	PP
SP7800A	MP87091	FE
SP7800	MP87092	FE
SP7802	MP87091	FE
	MP87092	FE
SP9316C	MP7626	PP
Sony		
CXD1172	MP7686	FE
CXD1175A	MP8785	PP(P2)
CXD1176	MP8775	FE
	MP8776	FE
	MP8785	FE
	MP8786	FE

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(2) EXAR warrants these devices over the industrial temp range of –40 to +85°C.
(P) P indicates the preferred device. Some industry part numbers have multiple EXAR part numbers of equal or better performance. All are listed for maximum availability.
P1 = Preferred, ESD < 1500 V, P2 = Preferred, ESD 2000 V, P3 = Preferred, ESD 4000 V

Pin-for-Pin & Functional Equivalents

Industry P/N	EXAR P/N	Pin for Pin Funct. Equiv.
SPT		
HADC674	MP674	PP
HDAC574	MP574A	PP
HDAC7541	MP7541B	PP(P2)
HDAC7542	MP7542	PP
HDAC7543	MP7543	PP
HDAC7545	MP7545B	PP(P2)
SPT1175	MP8775	PP
	MP8785	PP
SPT (Cont'd)		
MP8776	FE	
	MP8786	FE
SPT774	MP774	PP
SPT7920	MP8791	FE
SPT9950	MP8790	FE
	MP8791	FE
	MP8792	FE
Texas Instruments		
AD7628	MP7529	PP
TLC0820	MP0820	PP
TLC5502-5	MP7690	FE
	MP8780	FE
TLC5503-2	MP8775	FE
	MP8776	FE
	MP8785	FE
	MP8786	FE
TLC5503-5	MP7690	FE
Texas Instruments (Cont'd)		
TLC5503-5	MP8780	FE
TLC7524	MP7524	PP(2)
TLC7528	MP7528	PP
TLC7528	MP7528	PP
TLC7528	MP7529B	FE
TLC7533	MP7533	PP(2)
TLC7533C	MP7533	PP
TLC7628	MP7529	FE

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Analog-to-Digital Converters

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP3274		32	12	8/12, µP	N	A	G	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	2	1	15 µs	200
MP3274		32	12	8/12, µP	N	A	G	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	2	1	15 µs	200
MP3274		32	12	8/12, µP	N	A	P	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	1/2	1/2	15 µs	200
MP3274		32	12	8/12, µP	N	S	G	0.900"	MIL*	68	+10V INT	+5 to +10/0 to +20 V	1/2	1/2	15 µs	200
MP3275		16	12	8/12, µP	N	A	E	0.600"	IND	44	+10V INT	+5 to +10/0 to +20 V	1	1	15 µs	200
MP3276	New	16	12	8/12, µP	N	A	G	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	2	2	15 µs	200
MP3276	New	16	12	8/12, µP	N	A	P	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	2	2	15 µs	200
MP7682		1	6	6	Y	J	N	0.300"	IND	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	J	S	0.300"	IND	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	K	N	0.300"	IND	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7682		1	6	6	Y	K	S	0.300"	IND	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7682		1	6	6	Y	S	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	T	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7683		1	8	8	Y	J	N	0.600"	IND	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	J	Q	0.200"	IND	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	J	S	0.335"	IND	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	K	N	0.600"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7683		1	8	8	Y	K	S	0.335"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7683		1	8	8	Y	S	D	0.600"	MIL*	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	T	D	0.600"	MIL*	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7684		1	8	8	Y	J	D	0.600"	IND	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	J	N	0.600"	IND	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	J	S	0.335"	IND	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	K	D	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684		1	8	8	Y	K	N	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684		1	8	8	Y	K	S	0.335"	IND	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684		1	8	8	Y	S	D	0.600"	MIL*	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	T	D	0.600"	MIL*	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684A		1	8	8	Y	J	D	0.600"	IND	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	J	N	0.600"	IND	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	J	S	0.335"	IND	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	K	D	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7684A		1	8	8	Y	K	N	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7684A		1	8	8	Y	K	S	0.335"	IND	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7684A		1	8	8	Y	S	D	0.600"	MIL*	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	T	D	0.600"	MIL*	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400

TQM™

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PACKAGE CODES *– D = Cerdip, N = PDIP, P = PLCC, S = SOIC, L = LCC, E = Plastic Flat Pack, G = PGA, Q = SSOP, R = SOIC, W = PDIP*
TEMP *– IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*
***Preliminary Product*

Analog-to-Digital Converters

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP7686		1	6	6	Y	J	D	0.300"	IND	18	+4.1 V	0 to 5 V	2	1 1/4	20 MSPS	170
MP7686		1	6	6	Y	J	N	0.300"	IND	18	+4.1 V	0 to 5 V	2	1 1/4	20 MSPS	170
MP7686		1	6	6	Y	J	S	0.300"	IND	18	+4.1 V	0 to 5 V	2	1 1/4	20 MSPS	170
MP7686		1	6	6	Y	K	D	0.300"	IND	18	+4.1 V	0 to 5 V	1 1/4	1	20 MSPS	170
MP7686		1	6	6	Y	K	N	0.300"	IND	18	+4.1 V	0 to 5 V	1 1/4	1	20 MSPS	170
MP7686		1	6	6	Y	K	S	0.300"	IND	18	+4.1 V	0 to 5 V	1 1/4	1	20 MSPS	170
MP7690		1	8	8	Y	J	D	0.300"	IND	24	+4.1 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7690		1	8	8	Y	K	D	0.300"	IND	24	+4.1 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7690		1	8	8	Y	S	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7690		1	8	8	Y	T	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7690A		1	8	8	Y	A	D	0.300"	IND	24	+4.1 V	0 to 5 V	2	1	14 MSPS	400
MP7690A		1	8	8	Y	B	D	0.300"	IND	24	+4.1 V	0 to 5 V	1 3/4	3/4	14 MSPS	400
MP7690A		1	8	8	Y	S	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	2	1	14 MSPS	400
MP7690A		1	8	8	Y	T	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	1 3/4	3/4	14 MSPS	400
MP7693		1	8	8	Y	B	N	0.300"	IND	20	+5 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7693		1	8	8	Y	B	P	0.350"	IND	20	+5 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7693		1	8	8	Y	B	S	0.300"	IND	20	+5 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7695		1	10	10	Y	A	D	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7695		1	10	10	Y	A	N	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7695		1	10	10	Y	A	S	0.335"	IND	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7695		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7696		1	9	9	Y	A	N	0.300"	IND	24	+4.1 V	0 to 5 V	1	1	2 MSPS	50
MP7696		1	9	9	Y	A	S	0.335"	IND	24	+4.1 V	0 to 5 V	1	1	2 MSPS	50
MP76L86		1	6	6	Y	A	N	0.300"	IND	18	+3 V	0 to 3.3 V	1	1	6 MSPS	20
MP76L86		1	6	6	Y	A	S	0.300"	IND	18	+3 V	0 to 3.3 V	1	1	6 MSPS	20
MP76L90		1	8	8	Y	A	N	0.300"	IND	24	+3 V	0 to 3.3 V	1	1	5 MSPS	45
MP76L90		1	8	8	Y	A	S	0.300"	IND	24	+3 V	0 to 3.3 V	1	1	5 MSPS	45
MP7783		1	8	8	Y	J	N	0.300"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7783		1	8	8	Y	J	S	0.300"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP87091	New	1	12	12	Y	A	N	0.600"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175
MP87091	New	1	12	12	Y	A	S	0.335"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175

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MP87092	New	1	12	1	Y	A	N	0.600"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175
MP87092	New	1	12	1	Y	A	S	0.335"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175
MP87095		1	10	10	Y	A	D	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87095		1	10	10	Y	A	N	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87095		1	10	10	Y	A	S	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87095		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	D	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	Q	0.200"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	S	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87099		8	10	10	Y	A	E	0.550"	IND	44	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	D	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	Q	0.200"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	S	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP8775		1	8	8	Y	A	N	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8775		1	8	8	Y	A	Q	0.200"	IND	20	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8775		1	8	8	Y	A	S	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8776	New	1	8	8	Y	A	N	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8776	New	1	8	8	Y	A	Q	0.200"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8776	New	1	8	8	Y	A	S	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8780		1	8	8	Y	J	N	0.300"	IND	24	+2.5 V	0 to 5 V	1 1/2	1	15 MSPS	400
MP8780		1	8	8	Y	J	S	0.300"	IND	24	+2.5 V	0 to 5 V	1 1/2	1	15 MSPS	400
MP8782		1	10	10	Y	A	E	0.550"	IND	44	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784		1	10	10	Y	A	N	0.300"	IND	24	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784		1	10	10	Y	A	S	0.300"	IND	24	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784		1	10	10	Y	S	D	0.300"	MIL*	24	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784A	New**	1	10	10	Y	S	D	0.300"	MIL*	24	+1.0 to 4.0 V	0 to 5 V				
MP8785		1	8	8	Y	A	N	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8785		1	8	8	Y	A	R	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8785		1	8	8	Y	A	S	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125

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TEMP *– IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*
***Preliminary Product*

Analog-to-Digital Converters

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP8786	New	1	8	8	Y	A	N	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8786	New	1	8	8	Y	A	Q	0.200"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8786	New	1	8	8	Y	A	R	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8786	New	1	8	8	Y	A	S	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8790		1	12	12	Y	A	E	0.550"	IND	52	+5.0 V	0 to 5 V	2 1/2	1	2 MSPS	200
MP8791		1	12	12	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	2 1/2	1	2 MSPS	200
MP8791		1	12	12	Y	A	S	0.335"	IND	28	+4.6 V	0 to 5 V	2 1/2	1	2 MSPS	200
MP8795		1	10	10	Y	A	D	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8795		1	10	10	Y	A	N	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8795		1	10	10	Y	A	S	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8795		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8796		1	10	10	Y	A	S	0.300"	IND	20	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	D	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	Q	0.200"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	S	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8799		8	10	10	Y	A	E	0.450"	IND	44	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP87L75		1	8	8	Y	A	N	0.300"	IND	20	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L75		1	8	8	Y	A	R	0.300"	IND	20	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L75		1	8	8	Y	A	S	0.300"	IND	20	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L76	New	1	8	8	Y	A	Q	0.200"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP87L76	New	1	8	8	Y	A	S	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP87L82		1	10	10	Y	A	E	0.550"	IND	44	+0.6 to 2.4 V	0 to 3.3 V	2	1	2 MSPS	25
MP87L84		1	10	10	Y	A	N	0.300"	IND	24	+0.6 to 2.4 V	0 to 3.3 V	2	1	2 MSPS	25
MP87L84		1	10	10	Y	A	S	0.300"	IND	24	+0.6 to 2.4 V	0 to 3.3 V	2	1	2 MSPS	25
MP87L85		1	8	8	Y	A	N	0.300"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L85		1	8	8	Y	A	R	0.300"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L85		1	8	8	Y	A	S	0.300"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L85		1	8	8	Y	A	W	0.400"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30

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**Contact Factory for Non-Compliant Military Processing*
***Preliminary Product*

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP87L91		1	12	12	Y	A	N	0.300"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L91		1	12	12	Y	A	S	0.335"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L92		1	12	12	Y	A	N	0.300"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L92		1	12	12	Y	A	S	0.335"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L95		1	10	10	Y	A	N	0.300"	IND	24	+3.0 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L95		1	10	10	Y	A	S	0.300"	IND	24	+3.0 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	D	0.300"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	N	0.300"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	Q	0.200"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	S	0.300"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L99		8	10	10	Y	A	E	0.550"	IND	44	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP8820	New	8	8	8	Y	A	Q	0.200"	IND	28	0 V to 1.5 V	0 V to 1.5 V	1	–1, 2	1.6 MSPS	75
MP8820	New	8	8	8	Y	A	S	0.300"	IND	28	0 V to 1.5 V	0 V to 1.5 V	1	–1, 2	1.6 MSPS	75
MP8830	New	3	10	10	Y	A	E	0.670"	COM	64	0 V to 1.5 V	0 V to 1.5 V	1 1/2	3/4	1.25 MSPS	500
MP8831	New**	1	10	10	Y	A	S	0.300"	COM		0 V to 1.5 V	0 V to 1.5 V	1 1/2	3/4	0.6 MSPS	180

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**Contact Factory for Non-Compliant Military Processing*
***Preliminary Product*

Analog-to-Digital Converters (Non-Compliant Flow)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP3274		32	12	8/12, µP	N	S	G	0.900"	MIL*	68	+10V INT	+5 to +10/0 to +20 V	1/2	1/2	15 µs	200
MP7682		1	6	6	Y	S	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	T	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7683		1	8	8	Y	S	D	0.600"	MIL*	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	T	D	0.600"	MIL*	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7684		1	8	8	Y	S	D	0.600"	MIL*	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	T	D	0.600"	MIL*	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684A		1	8	8	Y	S	D	0.600"	MIL*	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	T	D	0.600"	MIL*	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7690		1	8	8	Y	S	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7690		1	8	8	Y	T	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7690A		1	8	8	Y	S	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	2	1	14 MSPS	400
MP7690A		1	8	8	Y	T	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	1 3/4	3/4	14 MSPS	400
MP7695		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP8784		1	10	10	Y	S	D	0.300"	MIL*	24	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784A	New*	1	10	10	Y	S	D	0.300"	MIL*	24	+1.0 to 4.0 V	0 to 5 V				
MP8795		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50

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**Contact Factory for Non-Compliant Military Processing*

Analog-to-Digital Converters (5 Volt)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP3274		32	12	8/12, µP	N	A	G	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	2	1	15 µs	200
MP3274		32	12	8/12, µP	N	A	P	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	1/2	1/2	15 µs	200
MP3274		32	12	8/12, µP	N	S	G	0.900"	MIL*	68	+10V INT	+5 to +10/0 to +20 V	1/2	1/2	15 µs	200
MP3275		16	12	8/12, µP	N	A	E	0.600"	IND	44	+10V INT	+5 to +10/0 to +20 V	1	1	15 µs	200
MP3276	New	16	12	8/12, µP	N	A	G	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	2	2	15 µs	200
MP3276	New	16	12	8/12, µP	N	A	P	0.900"	IND	68	+10V INT	+5 to +10/0 to +20 V	2	2	15 µs	200
MP7682		1	6	6	Y	A	D	0.300"	IND	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	B	D	0.300"	IND	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7682		1	6	6	Y	J	N	0.300"	IND	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	J	S	0.300"	IND	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	K	N	0.300"	IND	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7682		1	6	6	Y	K	S	0.300"	IND	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7682		1	6	6	Y	S	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	2	2	15 MSPS	150
MP7682		1	6	6	Y	T	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	1	1	15 MSPS	150
MP7683		1	8	8	Y	A	D	0.600"	IND	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	B	D	0.600"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7683		1	8	8	Y	J	N	0.600"	IND	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	J	Q	0.200"	IND	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	J	S	0.335"	IND	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	K	N	0.600"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7683		1	8	8	Y	K	S	0.335"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7683		1	8	8	Y	S	D	0.600"	MIL*	24	+4.1 V	0 to 5 V	1 1/4	1 1/4	3 MSPS	100
MP7683		1	8	8	Y	T	D	0.600"	MIL*	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7684		1	8	8	Y	J	D	0.600"	IND	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	J	N	0.600"	IND	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	J	S	0.335"	IND	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	K	D	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684		1	8	8	Y	K	N	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684		1	8	8	Y	K	S	0.335"	IND	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684		1	8	8	Y	S	D	0.600"	MIL*	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	S	L	0.450"	MIL*	28	+4 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7684		1	8	8	Y	T	D	0.600"	MIL*	28	+4 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7684A		1	8	8	Y	J	D	0.600"	IND	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	J	N	0.600"	IND	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	J	S	0.335"	IND	28	+4 V	0 to 5 V	2	1	14 MSPS	400

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**Contact Factory for Non-Compliant Military Processing*
***Preliminary Product*

Analog-to-Digital Converters (5 Volt)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP7684A		1	8	8	Y	K	D	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7684A		1	8	8	Y	K	N	0.600"	IND	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7684A		1	8	8	Y	K	S	0.335"	IND	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7684A		1	8	8	Y	S	D	0.600"	MIL*	28	+4 V	0 to 5 V	2	1	14 MSPS	400
MP7684A		1	8	8	Y	T	D	0.600"	MIL*	28	+4 V	0 to 5 V	1 1/2	3/4	14 MSPS	400
MP7686		1	6	6	Y	J	D	0.300"	IND	18	+4.1 V	0 to 5 V	2	1 1/4	20 MSPS	170
MP7686		1	6	6	Y	J	N	0.300"	IND	18	+4.1 V	0 to 5 V	2	1 1/4	20 MSPS	170
MP7686		1	6	6	Y	J	S	0.300"	IND	18	+4.1 V	0 to 5 V	2	1 1/4	20 MSPS	170
MP7686		1	6	6	Y	K	D	0.300"	IND	18	+4.1 V	0 to 5 V	1 1/4	1	20 MSPS	170
MP7686		1	6	6	Y	K	N	0.300"	IND	18	+4.1 V	0 to 5 V	1 1/4	1	20 MSPS	170
MP7686		1	6	6	Y	K	S	0.300"	IND	18	+4.1 V	0 to 5 V	1 1/4	1	20 MSPS	170
MP7686		1	6	6	Y	S	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	2	1 1/4	20 MSPS	170
MP7686		1	6	6	Y	T	D	0.300"	MIL*	18	+4.1 V	0 to 5 V	1 1/4	1	20 MSPS	170
MP7690		1	8	8	Y	J	D	0.300"	IND	24	+4.1 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7690		1	8	8	Y	K	D	0.300"	IND	24	+4.1 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7690		1	8	8	Y	S	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	2	1 1/2	10 MSPS	375
MP7690		1	8	8	Y	T	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	1 1/2	1	10 MSPS	375
MP7690A		1	8	8	Y	A	D	0.300"	IND	24	+4.1 V	0 to 5 V	2	1	14 MSPS	400
MP7690A		1	8	8	Y	B	D	0.300"	IND	24	+4.1 V	0 to 5 V	1 3/4	3/4	14 MSPS	400
MP7690A		1	8	8	Y	S	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	2	1	14 MSPS	400
MP7690A		1	8	8	Y	T	D	0.300"	MIL*	24	+4.1 V	0 to 5 V	1 3/4	3/4	14 MSPS	400
MP7693		1	8	8	Y	B	N	0.300"	IND	20	+5 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7693		1	8	8	Y	B	P	0.350"	IND	20	+5 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7693		1	8	8	Y	B	S	0.300"	IND	20	+5 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7695		1	10	10	Y	A	D	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7695		1	10	10	Y	A	N	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7695		1	10	10	Y	A	S	0.335"	IND	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7695		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/4	1	1 MSPS	50
MP7696		1	9	9	Y	A	N	0.300"	IND	24	+4.1 V	0 to 5 V	1	1	2 MSPS	50
MP7696		1	9	9	Y	A	S	0.335"	IND	24	+4.1 V	0 to 5 V	1	1	2 MSPS	50
MP7783		1	8	8	Y	J	N	0.300"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP7783		1	8	8	Y	J	S	0.300"	IND	24	+4.1 V	0 to 5 V	3/4	3/4	3 MSPS	100
MP87091	New	1	12	12	Y	A	N	0.600"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175
MP87091	New	1	12	12	Y	A	S	0.335"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*
***Preliminary Product*

Analog-to-Digital Converters (5 Volt)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP87092	New	1	12	1	Y	A	N	0.600"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175
MP87092	New	1	12	1	Y	A	S	0.335"	IND	28	+4.1 V	0 to 5 V	2 1/2	1	750 KSPS	175
MP87095		1	10	10	Y	A	D	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87095		1	10	10	Y	A	N	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87095		1	10	10	Y	A	S	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87095		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	D	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	Q	0.200"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87098		4	10	10	Y	A	S	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87099		8	10	10	Y	A	E	0.550"	IND	44	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	D	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	Q	0.200"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP87198		4	10	10	Y	A	S	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	0.75 MSPS	50
MP8775		1	8	8	Y	A	N	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8775		1	8	8	Y	A	Q	0.200"	IND	20	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8775		1	8	8	Y	A	S	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8776	New	1	8	8	Y	A	N	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8776	New	1	8	8	Y	A	Q	0.200"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8776	New	1	8	8	Y	A	S	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8780		1	8	8	Y	J	N	0.300"	IND	24	+2.5 V	0 to 5 V	1 1/2	1	15 MSPS	400
MP8780		1	8	8	Y	J	S	0.300"	IND	24	+2.5 V	0 to 5 V	1 1/2	1	15 MSPS	400
MP8782		1	10	10	Y	A	E	0.550"	IND	44	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784		1	10	10	Y	A	N	0.300"	IND	24	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784		1	10	10	Y	A	S	0.300"	IND	24	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784		1	10	10	Y	S	D	0.300"	MIL*	24	+1.0 to 4.0 V	0 to 5 V	2	1	5 MSPS	200
MP8784A	New**	1	10	10	Y	S	D	0.300"	MIL*	24	+1.0 to 4.0 V	0 to 5 V				
MP8785		1	8	8	Y	A	N	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8785		1	8	8	Y	A	R	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125

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TEMP *– IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

***Preliminary Product*

Analog-to-Digital Converters (5 Volt)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP8785		1	8	8	Y	A	S	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8785		1	8	8	Y	A	W	0.400"	IND	24	+0.6 to 2.6 V	0 to 5 V	1 1/2	3/4	20 MSPS	125
MP8786	New	1	8	8	Y	A	N	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8786	New	1	8	8	Y	A	Q	0.200"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8786	New	1	8	8	Y	A	R	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8786	New	1	8	8	Y	A	S	0.300"	IND	24	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP8790		1	12	12	Y	A	E	0.550"	IND	52	+5.0 V	0 to 5 V	2 1/2	1	2 MSPS	200
MP8791		1	12	12	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	2 1/2	1	2 MSPS	200
MP8791		1	12	12	Y	A	S	0.335"	IND	28	+4.6 V	0 to 5 V	2 1/2	1	2 MSPS	200
MP8795		1	10	10	Y	A	D	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8795		1	10	10	Y	A	N	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8795		1	10	10	Y	A	S	0.300"	IND	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8795		1	10	10	Y	S	D	0.300"	MIL*	24	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8796		1	10	10	Y	A	S	0.300"	IND	20	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	D	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	N	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	Q	0.200"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8798		4	10	10	Y	A	S	0.300"	IND	28	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8799		8	10	10	Y	A	E	0.450"	IND	44	+4.6 V	0 to 5 V	1 1/2	1	1 MSPS	50
MP8820	New	8	8	8	Y	A	Q	0.200"	IND	28	0 V to 1.5 V	0 V to 1.5 V	1	–1, 2	1.6 MSPS	75
MP8820	New	8	8	8	Y	A	S	0.300"	IND	28	0 V to 1.5 V	0 V to 1.5 V	1	–1, 2	1.6 MSPS	75
MP8830	New	3	10	10	Y	A	E	0.670"	COM	64	0 V to 1.5 V	0 V to 1.5 V	1 1/2	3/4	1.25 MSPS	500
MP8831**	New	1	10	10	Y	A	S	0.300"	COM		0 V to 1.5 V	0 V to 1.5 V	1 1/2	3/4	0.6 MSPS	180

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**Contact Factory for Non-Compliant Military Processing*
***Preliminary Product*

Analog-to-Digital Converters (3 Volt)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP76L86		1	6	6	Y	A	N	0.300"	IND	18	+3 V	0 to 3.3 V	1	1	6 MSPS	20
MP76L86		1	6	6	Y	A	S	0.300"	IND	18	+3 V	0 to 3.3 V	1	1	6 MSPS	20
MP76L90		1	8	8	Y	A	N	0.300"	IND	24	+3 V	0 to 3.3 V	1	1	5 MSPS	45
MP76L90		1	8	8	Y	A	S	0.300"	IND	24	+3 V	0 to 3.3 V	1	1	5 MSPS	45
MP87L75		1	8	8	Y	A	N	0.300"	IND	20	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L75		1	8	8	Y	A	R	0.300"	IND	20	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L75		1	8	8	Y	A	S	0.300"	IND	20	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L76	New	1	8	8	Y	A	Q	0.200"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP87L76	New	1	8	8	Y	A	S	0.300"	IND	20	+0.6 to 2.6 V	0 to 5 V	1	1/2	30 MSPS	110
MP87L82		1	10	10	Y	A	E	0.550"	IND	44	+0.6 to 2.4 V	0 to 3.3 V	2	1	2 MSPS	25
MP87L84		1	10	10	Y	A	N	0.300"	IND	24	+0.6 to 2.4 V	0 to 3.3 V	2	1	2 MSPS	25
MP87L84		1	10	10	Y	A	S	0.300"	IND	24	+0.6 to 2.4 V	0 to 3.3 V	2	1	2 MSPS	25
MP87L85		1	8	8	Y	A	N	0.300"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L85		1	8	8	Y	A	R	0.300"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L85		1	8	8	Y	A	S	0.300"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L85		1	8	8	Y	A	W	0.400"	IND	24	+0.5 to 2.5 V	0 to 3.3 V	1 1/2	1/2	10 MSPS	30
MP87L91		1	12	12	Y	A	N	0.300"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L91		1	12	12	Y	A	S	0.335"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L92		1	12	12	Y	A	N	0.300"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L92		1	12	12	Y	A	S	0.335"	IND	28	+3.0 V	0 to 3.3 V	2	1	1 MSPS	25
MP87L95		1	10	10	Y	A	N	0.300"	IND	24	+3.0 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L95		1	10	10	Y	A	S	0.300"	IND	24	+3.0 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	D	0.300"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	N	0.300"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	Q	0.200"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L98		4	10	10	Y	A	S	0.300"	IND	28	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10
MP87L99		8	10	10	Y	A	E	0.550"	IND	44	+2.6 V	0 to 3.3 V	1 1/2	1	0.25 MSPS	10

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Analog-to-Digital Converters (Subsystems)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	V_{REF} Tested	V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)
MP8820	New	8	8	8	Y	A	Q	0.200"	IND	28	0 V to 1.5 V	0 V to 1.5 V	1	–1, 2	1.6 MSPS	75
MP8820	New	8	8	8	Y	A	S	0.300"	IND	28	0 V to 1.5 V	0 V to 1.5 V	1	–1, 2	1.6 MSPS	75
MP8830	New	3	10	10	Y	A	E	0.670"	COM	64	0 V to 1.5 V	0 V to 1.5 V	1 1/2	3/4	1.25 MSPS	500
MP8831	New**	1	10	10	Y	A	S	0.300"	COM		0 V to 1.5 V	0 V to 1.5 V	1 1/2	3/4	0.6 MSPS	180

Digital-to-Analog Converters

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP1208		12	1	I	4Q	DB	Y	4/8, µP	B	D	0.600"	IND	24	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1208		12	1	I	4Q	DB	Y	4/8, µP	K	N	0.600"	IND	24	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1208		12	1	I	4Q	DB	Y	4/8, µP	T	D	0.600"	MIL*	24	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1209		12	1	I	4Q	DB	Y	4/8, µP	A	D	0.600"	IND	24	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1209		12	1	I	4Q	DB	Y	4/8, µP	J	N	0.600"	IND	24	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1209		12	1	I	4Q	DB	Y	4/8, µP	S	D	0.600"	MIL*	24	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1210		12	1	I	4Q	DB	Y	4/8, µP	H	N	0.600"	IND	24	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1210		12	1	I	4Q	DB	Y	4/8, µP	R	D	0.600"	MIL*	24	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1230		12	1	I	4Q	DB	Y	8/4, µP	B	D	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1230		12	1	I	4Q	DB	Y	8/4, µP	K	N	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1230A		12	1	I	4Q	DB	Y	8/4, µP	B	N	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1230A		12	1	I	4Q	DB	Y	8/4, µP	B	S	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	A	D	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	J	N	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	J	S	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	S	D	0.300"	MIL*	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231A		12	1	I	4Q	DB	Y	8/4, µP	B	N	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231A		12	1	I	4Q	DB	Y	8/4, µP	B	S	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1232		12	1	I	4Q	DB	Y	8/4, µP	H	N	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1232		12	1	I	4Q	DB	Y	8/4, µP	Z	D	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1232A		12	1	I	4Q	DB	Y	8/4, µP	B	N	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1232A		12	1	I	4Q	DB	Y	8/4, µP	B	S	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP7226		8	4	V	2Q	DB		8, µP	K	N	0.300"	IND	20	15 V	1	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	K	P	0.350"	IND	20	15 V	1	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	K	S	0.300"	IND	20	15 V	1	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	L	N	0.300"	IND	20	15 V	1/2	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	L	P	0.350"	IND	20	15 V	1/2	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	L	S	0.300"	IND	20	15 V	1/2	1/2	1 1/2 LSB	20	5000
MP7228		8	8	V	2Q	DB		8, µP	K	N	0.300"	IND	24	–5/15 V	1	1/2	1 LSB	5 Typ	7000
MP7228		8	8	V	2Q	DB		8, µP	K	P	0.450"	IND	28	–5/15 V	1	1/2	1 LSB	5 Typ	7000
MP7228		8	8	V	2Q	DB		8, µP	L	N	0.300"	IND	24	–5/15 V	1/2	1/2	1/2 LSB	5 Typ	7000
MP7228		8	8	V	2Q	DB		8, µP	L	P	0.450"	IND	28	–5/15 V	1/2	1/2	1/2 LSB	5 Typ	7000

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP7523		8	1	I	4Q		Y	8	J	N	0.300"	IND	16	5 to 16 V	1/2	1	1.8% FSR	35	150
MP7523		8	1	I	4Q		Y	8	J	S	0.300"	IND	16	5 to 16 V	1/2	1	1.8% FSR	35	150
MP7523		8	1	I	4Q		Y	8	K	N	0.300"	IND	16	5 to 16 V	1/4	1	1.8% FSR	35	150
MP7523		8	1	I	4Q		Y	8	K	S	0.300"	IND	16	5 to 16 V	1/4	1	1.8% FSR	35	150
MP7524		8	1	I	4Q	B	Y	8	A	D	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	B	D	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	C	D	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	N	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	P	0.350"	IND	20	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	R	0.150"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	S	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	N	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	P	0.350"	IND	20	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	R	0.150"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	S	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	L	N	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	L	P	0.350"	IND	20	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	L	S	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	S	D	0.300"	MIL*	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	T	D	0.300"	MIL*	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	U	D	0.300"	MIL*	16	15 V	1/8	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	A	N	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	A	R	0.150"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	B	N	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	B	R	0.150"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	C	N	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	C	R	0.150"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7528		8	2	I	4Q	B	Y	8	A	D	0.300"	IND	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	B	D	0.300"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	C	D	0.300"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	J	N	0.300"	IND	20	4.5 to 15.75V	1 1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	J	P	0.350"	IND	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	J	S	0.300"	IND	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	K	N	0.300"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	K	P	0.350"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	K	S	0.300"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	L	N	0.300"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	L	P	0.350"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200

All Ratings Max Unless Otherwise Noted

PACKAGE CODES *– D = Cerdip, N = PDIP, P = PLCC, S = SOIC, L = LCC, E = Plastic Flat Pack, G = PGA, Q = SSOP, R = SOIC, W = PDIP*

TEMP *– IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP7528		8	2	I	4Q	B	Y	8	L	S	0.300"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	S	D	0.300"	MIL*	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	T	D	0.300"	MIL*	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7529A		8	2	I	4Q	B	Y	8	J	N	0.300"	IND	20	10.8 to 15.75 V	1	1	5 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	J	P	0.350"	IND	20	10.8 to 15.75 V	1	1	5 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	J	S	0.300"	IND	20	10.8 to 15.75 V	1	1	5 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	K	N	0.300"	IND	20	10.8 to 15.75 V	1/2	1	3 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	K	P	0.350"	IND	20	10.8 to 15.75 V	1/2	1	3 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	K	S	0.300"	IND	20	10.8 to 15.75 V	1/2	1	3 LSB	35	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	J	N	0.300"	IND	20	4.5 to 5.5 V	1	1	5 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	J	P	0.350"	IND	20	4.5 to 5.5 V	1	1	5 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	J	S	0.300"	IND	20	4.5 to 5.5 V	1	1	5 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	K	N	0.300"	IND	20	4.5 to 5.5 V	1/2	1	3 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	K	P	0.350"	IND	20	4.5 to 5.5 V	1/2	1	3 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	K	S	0.300"	IND	20	4.5 to 5.5 V	1/2	1	3 LSB	15	200 Typ
MP7533		10	1	I	4Q	B	Y	10	A	D	0.300"	IND	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	B	D	0.300"	IND	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	C	D	0.300"	IND	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	J	N	0.300"	IND	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	J	S	0.300"	IND	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	K	N	0.300"	IND	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	K	S	0.300"	IND	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	L	N	0.300"	IND	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	L	S	0.300"	IND	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	S	D	0.300"	MIL*	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	T	D	0.300"	MIL*	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	U	D	0.300"	MIL*	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7541		12	1	I	4Q		Y	12	A	D	0.300"	IND	18	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7541		12	1	I	4Q		Y	12	B	D	0.300"	IND	18	4.5 to 16 V	1/2	1	0.4% FSR	2	500 Typ
MP7541		12	1	I	4Q		Y	12	J	N	0.300"	IND	18	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7541		12	1	I	4Q		Y	12	J	S	0.300"	IND	18	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7541		12	1	I	4Q		Y	12	K	N	0.300"	IND	18	4.5 to 16 V	1/2	1	0.4% FSR	2	500 Typ
MP7541		12	1	I	4Q		Y	12	K	S	0.300"	IND	18	4.5 to 16 V	1/2	1	0.4% FSR	2	500 Typ
MP7541		12	1	I	4Q		Y	12	S	D	0.300"	MIL*	18	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7541		12	1	I	4Q		Y	12	T	D	0.300"	MIL*	18	4.5 to 16 V	1/2	1	0.4% FSR	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	A	D	0.300"	IND	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	B	D	0.300"	IND	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ

TQM™

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/- LSB)	DNL (+/- LSB)	Gain Error (+/-)	Gain T.C.	Settling Time (ns)
MP7541B		12	1	I	4Q		Y	12	J	N	0.300"	IND	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	J	S	0.300"	IND	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	K	N	0.300"	IND	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	K	S	0.300"	IND	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	S	D	0.300"	MIL*	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	T	D	0.300"	MIL*	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	A	D	0.300"	IND	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	B	D	0.300"	IND	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	J	N	0.300"	IND	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	J	S	0.300"	IND	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	K	N	0.300"	IND	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	K	S	0.300"	IND	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	S	D	0.300"	MIL*	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	T	D	0.300"	MIL*	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	A	D	0.300"	IND	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	B	D	0.300"	IND	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	J	N	0.300"	IND	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	J	P	0.350"	IND	20	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	J	S	0.300"	IND	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	K	N	0.300"	IND	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	K	P	0.350"	IND	20	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	K	S	0.300"	IND	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	S	D	0.300"	MIL*	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	T	D	0.300"	MIL*	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	A	D	0.300"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	B	D	0.300"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	C	D	0.300"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	J	N	0.300"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	J	P	0.350"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	J	S	0.300"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	K	N	0.300"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	K	P	0.350"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	K	S	0.300"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	L	N	0.300"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	L	P	0.350"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	L	S	0.300"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	S	D	0.300"	MIL*	20	5 to 15 V	2	4	25 LSB	2	2000 Typ

TQM™

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

Digital-to-Analog Converters

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP7545		12	1	I	4Q	B	Y	12, µP	T	D	0.300"	MIL*	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	U	D	0.300"	MIL*	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	K	N	0.300"	IND	20	5 to 15 V	1	1	3 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	K	P	0.350"	IND	20	5 to 15 V	1	1	3 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	K	S	0.300"	IND	20	5 to 15 V	1	1	3 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	L	N	0.300"	IND	20	5 to 15 V	1	1	1 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	L	P	0.350"	IND	20	5 to 15 V	1	1	1 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	L	S	0.300"	IND	20	5 to 15 V	1	1	1 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	T	D	0.300"	MIL*	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	U	D	0.300"	MIL*	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP75L24	New	8	12	I	4Q	B	Y	8	A		0.300"	IND	16	3.0 to 3.6 V	1	1	3 LSB		100
MP75L24	New	8	12	I	4Q	B	Y	8	A		0.150"	IND	16	3.0 to 3.6 V	1	1	3 LSB		100
MP75L43	New	12	1	I	4Q	B	Y	Serial, uP	J	N	0.300"	IND	16	3.0 to 3.6 V	1	1			2
MP75L43	New	12	1	I	4Q	B	Y	Serial, uP	J	S	0.300"	IND	16	3.0 to 3.6 V	1	1			2
MP75L45		12	1	I	4Q	B	Y	12, µP	K	N	0.300"	IND	20	3.0 to 3.6 V	1	1	10 LSB	2	TBD
MP75L45		12	1	I	4Q	B	Y	12, µP	K	S	0.300"	IND	20	3.0 to 3.6 V	1	1	10 LSB	2	TBD
MP7610		14	8	V	2Q	DB		Serial, µP	A	N	0.400"	IND	28	+12/–12 V	8	4	32 LSB		50000
MP7610		14	8	V	2Q	DB		Serial, µP	A	S	0.300"	IND	28	+12/–12 V	8	4	32 LSB		50000
MP7610		14	8	V	2Q	DB		Serial, µP	B	N	0.400"	IND	28	+12/–12 V	4	3	24 LSB		50000
MP7610		14	8	V	2Q	DB		Serial, µP	B	S	0.300"	IND	28	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	A	E	0.550"	IND	44	+12/–12 V	8	4	32 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	A	G	0.600"	IND	44	+12/–12 V	8	4	32 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	A	P	0.550"	IND	44	+12/–12 V	8	4	32 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	B	E	0.550"	IND	44	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	B	G	0.600"	IND	44	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	B	P	0.550"	IND	44	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	S	G	0.600"	MIL*	44	+12/–12 V	8	4	32 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	A	N	0.400"	IND	28	+12/–12 V	2	1	8 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	A	S	0.300"	IND	28	+12/–12 V	2	1	8 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	B	N	0.400"	IND	28	+12/–12 V	1	0.75	6 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	B	S	0.300"	IND	28	+12/–12 V	1	0.75	6 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	S	D	0.300"	IND	28	+12/–12 V	1	0.75	6 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	A	E	0.550"	IND	44	+12/–12 V	2	1	8 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	A	G	0.600"	IND	44	+12/–12 V	2	1	8 LSB		50000

TQM™

All Ratings Max Unless Otherwise Noted

PACKAGE CODES – D = Cerdip, N = PDIP, P = PLCC, S = SOIC, L = LCC, E = Plastic Flat Pack, G = PGA, Q = SSOP, R = SOIC, W = PDIP

TEMP – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C

**Contact Factory for Non-Compliant Military Processing*

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP7613		12	8	V	2Q	DB		Parallel, µP	A	P	0.550"	IND	44	+12/–12 V	2	1	8 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	B	E	0.550"	IND	44	+12/–12 V	1	0.75	6 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	B	G	0.600"	IND	44	+12/–12 V	1	0.75	6 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	B	P	0.550"	IND	44	+12/–12 V	1	0.75	6 LSB		50000
MP7614		14	1	I	4Q		Y	14	J	N	0.300"	IND	20	4.5 to 16 V	4	4	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	K	D	0.300"	IND	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	K	N	0.300"	IND	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	K	S	0.300"	IND	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	T	D	0.300"	MIL*	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	J	D	0.400"	IND	22	4.5 to 16 V	14	16	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	J	N	0.400"	IND	22	4.5 to 16 V	14	16	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	J	S	0.300"	IND	24	4.5 to 16 V	14	16	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	K	D	0.400"	IND	22	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	K	N	0.400"	IND	22	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	K	S	0.300"	IND	24	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	T	D	0.400"	MIL*	22	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	J	D	0.600"	IND	24	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	J	N	0.600"	IND	24	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	J	P	0.450"	IND	28	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	K	D	0.600"	IND	24	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	K	N	0.600"	IND	24	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	K	P	0.450"	IND	28	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	L	D	0.600"	IND	24	4.5 to 16.5 V	2	1	0.1% FSR	2	2000 Typ
MP7628		8	4	I	4Q	B	Y	8, µP	A	D	0.600"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	B	D	0.600"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	J	N	0.600"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	J	P	0.450"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	J	S	0.300"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	K	N	0.600"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	K	P	0.450"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	K	S	0.300"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	S	D	0.600"	MIL*	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	T	D	0.600"	MIL*	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7633		10	1	I	4Q	B	Y	10	A	D	0.300"	IND	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	B	D	0.300"	IND	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	C	D	0.300"	IND	16	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP7633		10	1	I	4Q	B	Y	10	J	N	0.300"	IND	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	J	P	0.350"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	J	S	0.300"	IND	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	K	N	0.300"	IND	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	K	P	0.350"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	K	S	0.300"	IND	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	L	N	0.300"	IND	16	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	L	P	0.350"	IND	20	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	L	S	0.300"	IND	16	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	S	D	0.300"	MIL*	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	T	D	0.300"	MIL*	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	J	D	0.300"	IND	20	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	J	S	0.300"	IND	20	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q	DB	Y	8, UP	K	D	0.300"	IND	20	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	K	S	0.300"	IND	20	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	L	D	0.300"	IND	20	4.5 to 16.5 V	2	1	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	S	D	0.300"	MIL*	20	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	T	D	0.300"	MIL*	20	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7641		8	8	V	2Q	DB	Y	Serial µP	A	N	0.300"	IND	28	–5, +5, +10 V	1	0.8	1.5% FSR		500
MP7641		8	8	V	2Q	DB	Y	Serial µP	A	S	0.335"	IND	28	–5, +5, +10 V	1	0.8	1.5% FSR		500
MP7643	New	8	4	V	2Q	DB	Y	8, µP	A	N	0.335"	IND	28	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7643	New	8	4	V	2Q	DB	Y	8, µP	A	S	0.300"	IND	28	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7645B		12	1	I	4Q	B	Y	12, µP	B	D	0.300"	IND	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q	B	Y	12, µP	C	D	0.300"	IND	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q	B	Y	12, µP	K	N	0.300"	IND	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q	B	Y	12, µP	L	N	0.300"	IND	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q	B	Y	12, µP	T	D	0.300"	MIL*	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q	B	Y	12, µP	U	D	0.300"	MIL*	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7651		8	8	V	2Q		Y	Serial µP	A	N	0.300"	IND	28	–5, +5 V	1	0.8	1.5% FSR		500
MP7651		8	8	V	2Q		Y	Serial µP	A	S	0.335"	IND	28	–5, +5 V	1	0.8	1.5% FSR		500
MP7652	New	8	4	V	2Q	DB	Y	Serial	A	N	0.300"	IND	24	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7652	New	8	4	V	2Q	DB	Y	Serial	A	S	0.300"	IND	24	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7670	New	8	8	V	4Q	DB	Y	Serial	A	N	0.300"	IND	24	–5, +5 V	1	1	1/2 LSB		5 µs
MP7670	New	8	8	V	4Q	DB	Y	Serial	A	S	0.300"	IND	24	–5, +5 V	1	1	1/2 LSB		5 µs

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TEMP *– IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP7680		12	4	I	4Q	DB	Y	4/8, µP	J	D	0.600"	IND	40	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	J	E	0.550"	IND	44	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	J	N	0.600"	IND	40	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	K	D	0.600"	IND	40	4.5 to 5.5 V	1	2	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	K	E	0.550"	IND	44	4.5 to 5.5 V	1	2	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	K	N	0.600"	IND	40	4.5 to 5.5 V	1	2	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	L	E	0.550"	IND	44	4.5 to 5.5 V	1/2	1	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	L	N	0.600"	IND	40	4.5 to 5.5 V	1/2	1	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q	DB	Y	4/8, µP	S	D	0.600"	MIL*	40	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP8840	New	8	8	V	4Q	DB	Y	Serial	A	N	0.300"	IND	24	–5, +5 V	1	1			6 µs
MP8840	New	8	8	V	4Q	DB	Y	Serial	A	S	0.300"	IND	24	–5, +5 V	1	1			6 µs

Digital-to-Analog Converters (Non-Compliant Flow)

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP1208		12	1	I	4Q	DB	Y	4/8, µP	T	D	0.600"	MIL*	24	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1209		12	1	I	4Q	DB	Y	4/8, µP	S	D	0.600"	MIL*	24	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1210		12	1	I	4Q	DB	Y	4/8, µP	R	D	0.600"	MIL*	24	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	S	D	0.300"	MIL*	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP7524		8	1	I	4Q	B	Y	8	S	D	0.300"	MIL*	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	T	D	0.300"	MIL*	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	U	D	0.300"	MIL*	16	15 V	1/8	1	0.6% FSR	35	100
MP7528		8	2	I	4Q	B	Y	8	S	D	0.300"	MIL*	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	T	D	0.300"	MIL*	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7533		10	1	I	4Q	B	Y	10	S	D	0.300"	MIL*	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	T	D	0.300"	MIL*	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	U	D	0.300"	MIL*	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7541B		12	1	I	4Q		Y	12	S	D	0.300"	MIL*	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	T	D	0.300"	MIL*	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	S	D	0.300"	MIL*	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	T	D	0.300"	MIL*	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	S	D	0.300"	MIL*	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	T	D	0.300"	MIL*	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	S	D	0.300"	MIL*	20	5 tc 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	T	D	0.300"	MIL*	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	U	D	0.300"	MIL*	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	T	D	0.300"	MIL*	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	U	D	0.300"	MIL*	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7611		14	8	V	2Q	DB		Parallel, µP	S	G	0.600"	MIL*	44	+12/–12 V	8	4	32 LSB		50000
MP7614		14	1	I	4Q		Y	14	T	D	0.300"	MIL*	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	T	D	0.400"	MIL*	22	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters (Non-Compliant Flow)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits		Track/ Hold		Grade		Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed		Power (mW)
MP7628		8	4	I	4Q		B	Y		8, µP	S	D	0.600"	MIL*	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q		B	Y		8, µP	T	D	0.600"	MIL*	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7633		10	1	I	4Q		B	Y		10	S	D	0.300"	MIL*	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q		B	Y		10	T	D	0.300"	MIL*	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7636A		16	1	I	4Q		DB	Y		8, µP	S	D	0.300"	MIL*	20	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q		DB	Y		8, µP	T	D	0.300"	MIL*	20	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y		12, µP	T	D	0.300"	MIL*	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y		12, µP	U	D	0.300"	MIL*	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7680		12	4	I	4Q		DB	Y		4/8, µP	S	D	0.600"	MIL*	40	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ

Digital-to-Analog Converters (5 V)

Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP1208		12	1	I	4Q	DB	Y	4/8, µP	B	D	0.600"	IND	24	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1208		12	1	I	4Q	DB	Y	4/8, µP	K	N	0.600"	IND	24	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1208		12	1	I	4Q	DB	Y	4/8, µP	T	D	0.600"	MIL*	24	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1209		12	1	I	4Q	DB	Y	4/8, µP	A	D	0.600"	IND	24	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1209		12	1	I	4Q	DB	Y	4/8, µP	J	N	0.600"	IND	24	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1209		12	1	I	4Q	DB	Y	4/8, µP	S	D	0.600"	MIL*	24	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1210		12	1	I	4Q	DB	Y	4/8, µP	H	N	0.600"	IND	24	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1210		12	1	I	4Q	DB	Y	4/8, µP	R	D	0.600"	MIL*	24	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1230		12	1	I	4Q	DB	Y	8/4, µP	B	D	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1230		12	1	I	4Q	DB	Y	8/4, µP	K	N	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1230A		12	1	I	4Q	DB	Y	8/4, µP	B	N	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1230A		12	1	I	4Q	DB	Y	8/4, µP	B	S	0.300"	IND	20	4.5 to 16 V	1/2	3/4	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	A	D	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	J	N	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	J	S	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231		12	1	I	4Q	DB	Y	8/4, µP	S	D	0.300"	MIL*	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231A		12	1	I	4Q	DB	Y	8/4, µP	B	N	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1231A		12	1	I	4Q	DB	Y	8/4, µP	B	S	0.300"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	1000 Typ
MP1232		12	1	I	4Q	DB	Y	8/4, µP	H	N	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1232		12	1	I	4Q	DB	Y	8/4, µP	Z	D	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1232A		12	1	I	4Q	DB	Y	8/4, µP	B	N	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP1232A		12	1	I	4Q	DB	Y	8/4, µP	B	S	0.300"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	1000 Typ
MP7226		8	4	V	2Q	DB		8, µP	K	N	0.300"	IND	20	15 V	1	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	K	P	0.350"	IND	20	15 V	1	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	K	S	0.300"	IND	20	15 V	1	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	L	N	0.300"	IND	20	15 V	1/2	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	L	P	0.350"	IND	20	15 V	1/2	1/2	1 1/2 LSB	20	5000
MP7226		8	4	V	2Q	DB		8, µP	L	S	0.300"	IND	20	15 V	1/2	1/2	1 1/2 LSB	20	5000
MP7228		8	8	V	2Q	DB		8, µP	K	N	0.300"	IND	24	–5/15 V	1	1/2	1 LSB	5 Typ	7000
MP7228		8	8	V	2Q	DB		8, µP	K	P	0.450"	IND	28	–5/15 V	1	1/2	1 LSB	5 Typ	7000

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**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters (5 V)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits		Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)	
MP7228		8	8	V	2Q		DB	8, µP	L	N	0.300"	IND	24	–5/15 V	1/2	1/2	1/2 LSB	5 Typ	7000
MP7228		8	8	V	2Q		DB	8, µP	L	P	0.450"	IND	28	–5/15 V	1/2	1/2	1/2 LSB	5 Typ	7000
MP7523		8	1	I	4Q		Y	8	J	N	0.300"	IND	16	5 to 16 V	1/2	1	1.8% FSR	35	150
MP7523		8	1	I	4Q		Y	8	J	S	0.300"	IND	16	5 to 16 V	1/2	1	1.8% FSR	35	150
MP7523		8	1	I	4Q		Y	8	K	N	0.300"	IND	16	5 to 16 V	1/4	1	1.8% FSR	35	150
MP7523		8	1	I	4Q		Y	8	K	S	0.300"	IND	16	5 to 16 V	1/4	1	1.8% FSR	35	150
MP7524		8	1	I	4Q	B	Y	8	A	D	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	B	D	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	C	D	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	N	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	P	0.350"	IND	20	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	R	0.150"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	J	S	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	N	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	P	0.350"	IND	20	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	R	0.150"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	K	S	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	L	N	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	L	P	0.350"	IND	20	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	L	S	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	S	D	0.300"	MIL*	16	15 V	1/2	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	T	D	0.300"	MIL*	16	15 V	1/4	1	0.6% FSR	35	100
MP7524		8	1	I	4Q	B	Y	8	U	D	0.300"	MIL*	16	15 V	1/8	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	A	N	0.300"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	A	R	0.150"	IND	16	15 V	1/2	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	B	N	0.300"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	B	R	0.150"	IND	16	15 V	1/4	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	C	N	0.300"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7524A		8	1	I	4Q	B	Y	8	C	R	0.150"	IND	16	15 V	1/8	1	0.6% FSR	35	100
MP7528		8	2	I	4Q	B	Y	8	A	D	0.300"	IND	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	B	D	0.300"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	C	D	0.300"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	J	N	0.300"	IND	20	4.5 to 15.75V	I 1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	J	P	0.350"	IND	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	J	S	0.300"	IND	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	K	N	0.300"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	K	P	0.350"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters (5 V)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits	Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed	Power (mW)	
MP7528		8	2	I	4Q	B	Y	8	K	S	0.300"	IND	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	L	N	0.300"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	L	P	0.350"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	L	S	0.300"	IND	20	4.5 to 15.75V	1/4	1	1 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	S	D	0.300"	MIL*	20	4.5 to 15.75V	1	1	5 LSB	35	200
MP7528		8	2	I	4Q	B	Y	8	T	D	0.300"	MIL*	20	4.5 to 15.75V	1/2	1	3 LSB	35	200
MP7529A		8	2	I	4Q	B	Y	8	J	N	0.300"	IND	20	10.8 to 15.75 V	1	1	5 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	J	P	0.350"	IND	20	10.8 to 15.75 V	1	1	5 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	J	S	0.300"	IND	20	10.8 to 15.75 V	1	1	5 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	K	N	0.300"	IND	20	10.8 to 15.75 V	1/2	1	3 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	K	P	0.350"	IND	20	10.8 to 15.75 V	1/2	1	3 LSB	35	200 Typ
MP7529A		8	2	I	4Q	B	Y	8	K	S	0.300"	IND	20	10.8 to 15.75 V	1/2	1	3 LSB	35	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	J	N	0.300"	IND	20	4.5 to 5.5 V	1	1	5 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	J	P	0.350"	IND	20	4.5 to 5.5 V	1	1	5 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	J	S	0.300"	IND	20	4.5 to 5.5 V	1	1	5 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	K	N	0.300"	IND	20	4.5 to 5.5 V	1/2	1	3 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	K	P	0.350"	IND	20	4.5 to 5.5 V	1/2	1	3 LSB	15	200 Typ
MP7529B		8	2	I	4Q	B	Y	8	K	S	0.300"	IND	20	4.5 to 5.5 V	1/2	1	3 LSB	15	200 Typ
MP7533		10	1	I	4Q	B	Y	10	A	D	0.300"	IND	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	B	D	0.300"	IND	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	C	D	0.300"	IND	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	J	N	0.300"	IND	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	J	S	0.300"	IND	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	K	N	0.300"	IND	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	K	S	0.300"	IND	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	L	N	0.300"	IND	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	L	S	0.300"	IND	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	S	D	0.300"	MIL*	16	4.5 to 16 V	2	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	T	D	0.300"	MIL*	16	4.5 to 16 V	1	1	1.5% FSR	2	500
MP7533		10	1	I	4Q	B	Y	10	U	D	0.300"	MIL*	16	4.5 to 16 V	1/2	1	1.5% FSR	2	500
MP7541B		12	1	I	4Q		Y	12	A	D	0.300"	IND	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	B	D	0.300"	IND	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	J	N	0.300"	IND	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	J	S	0.300"	IND	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	K	N	0.300"	IND	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	K	S	0.300"	IND	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ

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**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters (5 V)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits		Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed		Power (mW)
MP7541B		12	1	I	4Q		Y	12	S	D	0.300"	MIL*	18	4.5 to 16 V	1	1	8 LSB	2	500 Typ
MP7541B		12	1	I	4Q		Y	12	T	D	0.300"	MIL*	18	4.5 to 16 V	1/2	1/2	5 LSB	2	500 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	A	D	0.300"	IND	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	B	D	0.300"	IND	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	J	N	0.300"	IND	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	J	S	0.300"	IND	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	K	N	0.300"	IND	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	K	S	0.300"	IND	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	S	D	0.300"	MIL*	16	4.5 to 5.5 V	1	2	14.5 LSB	2	2000 Typ
MP7542		12	1	I	4Q	DB	Y	4, µP	T	D	0.300"	MIL*	16	4.5 to 5.5 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	A	D	0.300"	IND	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	B	D	0.300"	IND	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	J	N	0.300"	IND	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	J	P	0.350"	IND	20	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	J	S	0.300"	IND	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	K	N	0.300"	IND	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	K	P	0.350"	IND	20	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	K	S	0.300"	IND	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	S	D	0.300"	MIL*	16	4.75 to 5.25 V	1	2	14.5 LSB	2	2000 Typ
MP7543		12	1	I	4Q		Y	Serial, µP	T	D	0.300"	MIL*	16	4.75 to 5.25 V	1/2	1	14.5 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	A	D	0.300"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	B	D	0.300"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	C	D	0.300"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	J	N	0.300"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	J	P	0.350"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	J	S	0.300"	IND	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	K	N	0.300"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	K	P	0.350"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	K	S	0.300"	IND	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	L	N	0.300"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	L	P	0.350"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	L	S	0.300"	IND	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	S	D	0.300"	MIL*	20	5 to 15 V	2	4	25 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	T	D	0.300"	MIL*	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545		12	1	I	4Q	B	Y	12, µP	U	D	0.300"	MIL*	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	K	N	0.300"	IND	20	5 to 15 V	1	1	3 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	K	P	0.350"	IND	20	5 to 15 V	1	1	3 LSB	2	2000 Typ

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***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters (5 V)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits		Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed		Power (mW)
MP7545B		12	1	I	4Q	B	Y	12, µP	K	S	0.300"	IND	20	5 to 15 V	1	1	3 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	L	N	0.300"	IND	20	5 to 15 V	1	1	1 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	L	P	0.350"	IND	20	5 to 15 V	1	1	1 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	L	S	0.300"	IND	20	5 to 15 V	1	1	1 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	T	D	0.300"	MIL*	20	5 to 15 V	1	1	15 LSB	2	2000 Typ
MP7545B		12	1	I	4Q	B	Y	12, µP	U	D	0.300"	MIL*	20	5 to 15 V	1/2	1	10 LSB	2	2000 Typ
MP7610		14	8	V	2Q	DB		Serial, µP	A	N	0.400"	IND	28	+12/–12 V	8	4	32 LSB		50000
MP7610		14	8	V	2Q	DB		Serial, µP	A	S	0.300"	IND	28	+12/–12 V	8	4	32 LSB		50000
MP7610		14	8	V	2Q	DB		Serial, µP	B	N	0.400"	IND	28	+12/–12 V	4	3	24 LSB		50000
MP7610		14	8	V	2Q	DB		Serial, µP	B	S	0.300"	IND	28	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	A	E	0.550"	IND	44	+12/–12 V	8	4	32 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	A	G	0.600"	IND	44	+12/–12 V	8	4	32 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	A	P	0.550"	IND	44	+12/–12 V	8	4	32 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	B	E	0.550"	IND	44	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	B	G	0.600"	IND	44	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	B	P	0.550"	IND	44	+12/–12 V	4	3	24 LSB		50000
MP7611		14	8	V	2Q	DB		Parallel, µP	S	G	0.600"	MIL*	44	+12/–12 V	8	4	32 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	A	N	0.400"	IND	28	+12/–12 V	2	1	8 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	A	S	0.300"	IND	28	+12/–12 V	2	1	8 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	B	N	0.400"	IND	28	+12/–12 V	1	0.75	6 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	B	S	0.300"	IND	28	+12/–12 V	1	0.75	6 LSB		50000
MP7612		12	8	V	2Q	DB		Serial, µP	S	D	0.300"	IND	28	+12/–12 V	1	0.75	6 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	A	E	0.550"	IND	44	+12/–12 V	2	1	8 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	A	G	0.600"	IND	44	+12/–12 V	2	1	8 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	A	P	0.550"	IND	44	+12/–12 V	2	1	8 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	B	E	0.550"	IND	44	+12/–12 V	1	0.75	6 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	B	G	0.600"	IND	44	+12/–12 V	1	0.75	6 LSB		50000
MP7613		12	8	V	2Q	DB		Parallel, µP	B	P	0.550"	IND	44	+12/–12 V	1	0.75	6 LSB		50000
MP7614		14	1	I	4Q		Y	14	J	N	0.300"	IND	20	4.5 to 16 V	4	4	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	K	D	0.300"	IND	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	K	N	0.300"	IND	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	K	S	0.300"	IND	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7614		14	1	I	4Q		Y	14	T	D	0.300"	MIL*	20	4.5 to 16 V	2	2	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	J	D	0.400"	IND	22	4.5 to 16 V	14	16	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	J	N	0.400"	IND	22	4.5 to 16 V	14	16	0.8% FSR	2	2000 Typ

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**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters (5 V)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits		Track/ Hold	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed		Power (mW)
MP7616		16	1	I	4Q		Y	16	J	S	0.300"	IND	24	4.5 to 16 V	14	16	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	K	D	0.400"	IND	22	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	K	N	0.400"	IND	22	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	K	S	0.300"	IND	24	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7616		16	1	I	4Q		Y	16	T	D	0.400"	MIL*	22	4.5 to 16 V	7	8	0.8% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	J	D	0.600"	IND	24	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	J	N	0.600"	IND	24	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	J	P	0.450"	IND	28	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	K	D	0.600"	IND	24	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	K	N	0.600"	IND	24	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	K	P	0.450"	IND	28	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7626		16	1	I	4Q		Y	16	L	D	0.600"	IND	24	4.5 to 16.5 V	2	1	0.1% FSR	2	2000 Typ
MP7628		8	4	I	4Q	B	Y	8, µP	A	D	0.600"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	B	D	0.600"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	J	N	0.600"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	J	P	0.450"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	J	S	0.300"	IND	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	K	N	0.600"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	K	P	0.450"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	K	S	0.300"	IND	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	S	D	0.600"	MIL*	28	4.5 to 5.5 V	1/2	1/2	1.8% FSR	2	250
MP7628		8	4	I	4Q	B	Y	8, µP	T	D	0.600"	MIL*	28	4.5 to 5.5 V	1/4	1/4	0.9% FSR	2	250
MP7633		10	1	I	4Q	B	Y	10	A	D	0.300"	IND	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	B	D	0.300"	IND	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	C	D	0.300"	IND	16	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	J	N	0.300"	IND	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	J	P	0.350"	IND	20	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	J	S	0.300"	IND	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	K	N	0.300"	IND	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	K	P	0.350"	IND	20	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	K	S	0.300"	IND	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	L	N	0.300"	IND	16	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	L	P	0.350"	IND	20	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	L	S	0.300"	IND	16	4.5 to 16 V	1/2	1/2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	S	D	0.300"	MIL*	16	4.5 to 16 V	2	2	0.4% FSR	2	500 Typ
MP7633		10	1	I	4Q	B	Y	10	T	D	0.300"	MIL*	16	4.5 to 16 V	1	1	0.4% FSR	2	500 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	J	D	0.300"	IND	20	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q	DB	Y	8, µP	J	S	0.300"	IND	20	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ

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**Contact Factory for Non-Compliant Military Processing*

Digital-to-Analog Converters (5 V)

Part #	New	# MUXs	Res. Bits	Bus Interface Bits		Track/ Hold	Grade		Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed		Power (mW)
MP7636A		16	1	I	4Q		DB	Y	8, UP	K	D	0.300"	IND	20	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q		DB	Y	8, µP	K	S	0.300"	IND	20	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q		DB	Y	8, µP	L	D	0.300"	IND	20	4.5 to 16.5 V	2	1	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q		DB	Y	8, µP	S	D	0.300"	MIL*	20	4.5 to 16.5 V	4	4	0.1% FSR	2	2000 Typ
MP7636A		16	1	I	4Q		DB	Y	8, µP	T	D	0.300"	MIL*	20	4.5 to 16.5 V	2	2	0.1% FSR	2	2000 Typ
MP7641		8	8	V	2Q		DB	Y	Serial µP	A	N	0.300"	IND	28	–5, +5, +10 V	1	0.8	1.5% FSR		500
MP7641		8	8	V	2Q		DB	Y	Serial µP	A	S	0.335"	IND	28	–5, +5, +10 V	1	0.8	1.5% FSR		500
MP7643	New	8	4	V	2Q		DB	Y	8, µP	A	N	0.335"	IND	28	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7643	New	8	4	V	2Q		DB	Y	8, µP	A	S	0.300"	IND	28	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7645		12	1	I	4Q		B	Y	12, µP	A	D	0.300"	IND	20	4.5 to 15 V	2	2	0.4% FSR	2	2000 Typ
MP7645		12	1	I	4Q		B	Y	12, µP	B	D	0.300"	IND	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645		12	1	I	4Q		B	Y	12, µP	C	D	0.300"	IND	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7645		12	1	I	4Q		B	Y	12, µP	J	N	0.300"	IND	20	4.5 to 15 V	2	2	0.4% FSR	2	2000 Typ
MP7645		12	1	I	4Q		B	Y	12, µP	K	N	0.300"	IND	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645		12	1	I	4Q		B	Y	12, µP	L	N	0.300"	IND	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7645		12	1	I	4Q		B	Y	12, µP	S	D	0.300"	MIL*	20	4.5 to 15 V	2	2	0.4% FSR	2	2000 Typ
MP7645		12	1	I	4Q		B	Y	12, µP	T	D	0.300"	MIL*	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y	12, µP	B	D	0.300"	IND	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y	12, µP	C	D	0.300"	IND	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y	12, µP	K	N	0.300"	IND	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y	12, µP	L	N	0.300"	IND	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y	12, µP	T	D	0.300"	MIL*	20	4.5 to 15 V	1	1	0.4% FSR	2	2000 Typ
MP7645B		12	1	I	4Q		B	Y	12, µP	U	D	0.300"	MIL*	20	4.5 to 15 V	1/2	1/2	0.4% FSR	2	2000 Typ
MP7651		8	8	V	2Q			Y	Serial µP	A	N	0.300"	IND	28	–5, +5 V	1	0.8	1.5% FSR		500
MP7651		8	8	V	2Q			Y	Serial µP	A	S	0.335"	IND	28	–5, +5 V	1	0.8	1.5% FSR		500
MP7652	New	8	4	V	2Q		DB	Y	Serial	A	N	0.300"	IND	24	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7652	New	8	4	V	2Q		DB	Y	Serial	A	S	0.300"	IND	24	–5, +5, +10 V	1	1/2	1.5% FSR		150
MP7670	New	8	8	V	4Q		DB	Y	Serial	A	N	0.300"	IND	24	–5, +5 V	1	1	1/2 LSB		5 µs
MP7670	New	8	8	V	4Q		DB	Y	Serial	A	S	0.300"	IND	24	–5, +5 V	1	1	1/2 LSB		5 µs
MP7680		12	4	I	4Q		DB	Y	4/8, µP	J	D	0.600"	IND	40	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q		DB	Y	4/8, µP	J	E	0.550"	IND	44	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q		DB	Y	4/8, µP	J	N	0.600"	IND	40	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q		DB	Y	4/8, µP	K	D	0.600"	IND	40	4.5 to 5.5 V	1	2	16 LSB	2	1000 Typ

TQM™

All Ratings Max Unless Otherwise Noted

**Contact Factory for Non-Compliant Military Processing*

***PACKAGE CODES** – D = Cerdip, N = PDIP, P = PLCC, S = SOIC, L = LCC, E = Plastic Flat Pack, G = PGA, Q = SSOP, R = SOIC, W = PDIP*

***TEMP** – IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

Digital-to-Analog Converters (5 V)

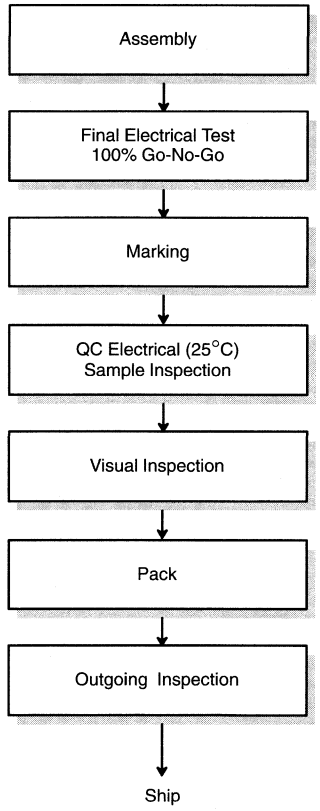
Part #	New	# MUXs	Res. Bits	Bus Interface Bits		Track/ Hold	Grade		Pkg	Pkg Width	Temp Range	# of Pins	Tested V_{REF}		V_{REF} Range	INL (± LSB)	DNL (± LSB)	Speed		Power (mW)
MP7680		12	4	I	4Q		DB	Y	4/8, µP	K	E	0.550"	IND	44	4.5 to 5.5 V	1	2	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q		DB	Y	4/8, µP	K	N	0.600"	IND	40	4.5 to 5.5 V	1	2	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q		DB	Y	4/8, µP	L	E	0.550"	IND	44	4.5 to 5.5 V	1/2	1	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q		DB	Y	4/8, µP	L	N	0.600"	IND	40	4.5 to 5.5 V	1/2	1	16 LSB	2	1000 Typ
MP7680		12	4	I	4Q		DB	Y	4/8, µP	S	D	0.600"	MIL*	40	4.5 to 5.5 V	2	4	16 LSB	2	1000 Typ
MP8840	New	8	8	V	4Q		DB	Y	Serial	A	N	0.300"	IND	24	–5, +5 V	1	1			6 µs
MP8840	New	8	8	V	4Q		DB	Y	Serial	A	S	0.300"	IND	24	–5, +5 V	1	1			6 µs

Digital-to-Analog Converters (3 V)

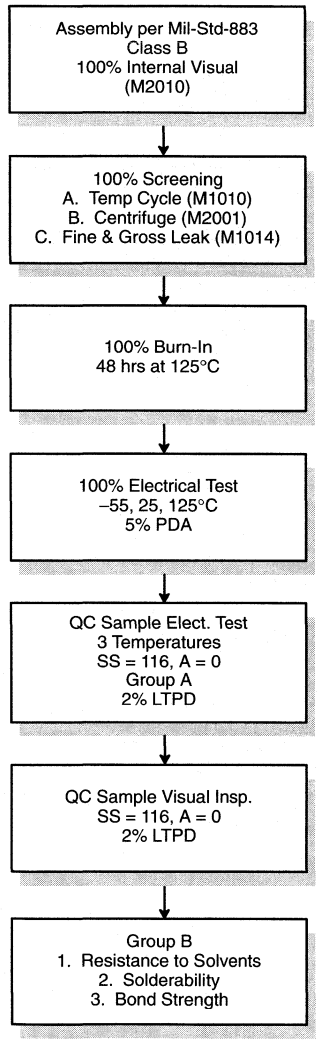
Part #	New	Res. Bits	# of DACS	I or V Out	2 or 4 Quad	Double/ Buffered	Mult.	Bus Interface Bits	Grade	Pkg	Pkg Width	Temp Range	# of Pins	Operating Voltage	INL (+/– LSB)	DNL (+/– LSB)	Gain Error (+/–)	Gain T.C.	Settling Time (ns)
MP75L24	New	8	12	I	4Q	B	Y	8	A		0.300"	IND	16	3.0 to 3.6 V	1	1	3 LSB		100
MP75L24	New	8	12	I	4Q	B	Y	8	A		0.150"	IND	16	3.0 to 3.6 V	1	1	3 LSB		100
MP75L43	New	12	1	I	4Q	B	Y	Serial, uP	J	N	0.300"	IND	16	3.0 to 3.6 V	1	1			2
MP75L43	New	12	1	I	4Q	B	Y	Serial, uP	J	S	0.300"	IND	16	3.0 to 3.6 V	1	1			2
MP75L45		12	1	I	4Q	B	Y	12, µP	K	N	0.300"	IND	20	3.0 to 3.6 V	1	1	10 LSB	2	TBD
MP75L45		12	1	I	4Q	B	Y	12, µP	K	S	0.300"	IND	20	3.0 to 3.6 V	1	1	10 LSB	2	TBD

All Ratings Max Unless Otherwise Noted
PACKAGE CODES *– D = Cerdip, N = PDIP, P = PLCC, S = SOIC, L = LCC, E = Plastic Flat Pack, G = PGA, Q = SSOP, R = SOIC, W = PDIP*
TEMP *– IND = Industrial –40 to +85°C, MIL = Military –55 to +125°C*

Commercial Products Flow



Non-Compliant Military Flow



Terms & Conditions

EXAR CORPORATION TERMS AND CONDITIONS OF SALE

1. DEFINITIONS – As used herein, the following terms shall have the meanings set forth below:
(a) "Seller" and "Buyer" shall mean, respectively, Exar Corporation and the individual or entity for whose account a Purchase Order has been placed with Seller.
(b) "Purchase Order" shall mean an oral or written offer to purchase product sold by Seller submitted to Seller by or on behalf or Buyer.
(c) "Product" shall mean the product (in die, packaged or wafer form) and service described on the face side hereof.
(d) "Standard Product" shall mean Product which are regularly inventoried by Seller and are not Custom Product or Special Order Product.
(e) "Special Order Product" shall mean Product which are not regularly inventoried by Seller and are not Custom Product.
(f) "Custom Product" shall mean Product which are customized to the specifications of Buyer, to the extent that they have little or no economic value to another customer of Seller and cannot be economically re–worked for sale to another customer.

2. PURCHASE ORDER ACCEPTANCE – These Terms and Conditions of Sale and those noted on the front hereof shall apply to all bids, quotations and orders for the sale of Product by Seller. Except as specifically set forth in a document signed by the authorized representatives of both parties, these Terms and Conditions of Sale and those noted on the front hereof shall represent the sole understanding between the Seller and Buyer with respect to the purchase and sale of Seller's Product. Any provision of Buyer's purchase order or other written communication which is in any way inconsistent with or in addition to these Terms and Conditions of Sale shall not be binding on Seller. This Order Acknowledgment constitutes a counter offer to Buyer and retention by Buyer of the Product delivered hereunder beyond the inspection period described below shall constitute acceptance of these Terms and Conditions of Sale. Seller's failure to object to provisions contained in any communication from Buyer shall not be a waiver of these Terms and Conditions of Sale nor those noted on the front of Seller's Order Acknowledgment.

3. PRICE AND PAYMENT
(a) All prices published or quoted by Seller may be changed at any time without notice. Unless otherwise specified, written quotations expire thirty (30) calendar days from the date issued.
(b) Seller will invoice Buyer on the date the Product is tendered to the carrier at Seller's shipping point (hereinafter referred to as the "delivery date"). Such invoices will be due and payable net thirty (30) days from date of invoice, subject to prior credit approval, without deduction or set off of any kind.
(c) Seller, at its option, may require that sales be entered into on the express condition that Buyer establish in favor of Seller an irrevocable letter of credit in a form acceptable to Seller confirmed by a United States bank acceptable to Seller payable to Seller in United States dollars on presentation of a sight draft, a copy of a commercial invoice, a packing list and a bill of lading indicating delivery to a carrier of a Product for delivery to Buyer or to Buyer's order. All associated costs shall be Buyer's responsibility.
(d) For sales to a Buyer having a principal place of business outside the United States of America, Seller reserves the right to bill in United States dollars or the currency of the country in which the Product is shipped. In such event the rate of exchange will be that in effect on the date the Product is tendered to the carrier at Seller's shipping point.
(e) At any time prior to the date of delivery Seller reserves the right to change any terms of credit extended to Buyer in the event Seller believes, in good faith, that there has been an adverse change in credit worthiness of Buyer or Buyer fails to comply with agreed credit terms and to require partial or full payment in advance. In such event, if Buyer refuses to accept such change in credit terms, Buyer's Purchase Order can be canceled without any liability to Seller. In the event of bankruptcy or insolvency of Buyer or in the event any proceeding is brought by or against Buyer under any bankruptcy or insolvency laws or their equivalent, Seller may cancel any purchase order then outstanding without liability to Seller and Seller shall receive reimbursement from Buyer for costs incurred and lost profit for Product so canceled.
(f) It is expressly understood by Buyer that with respect to any Product set forth on the face side hereof the purchase price(s) per unit set forth reflect volume discounts determined by reference to the total number of units of the respective Product which Buyer has agreed to purchase from Seller. Accordingly, it is expressly agreed by Buyer that if the total number of units of any Product purchased and paid for by Buyer is less than the number of units of such Product which Buyer has agreed to purchase, then Seller may immediately issue to Buyer a supplemental invoice for an amount equal, on a per unit basis, to the difference between (i) Seller's list price for such Product then in effect and (ii) the purchase price for such Product set forth on the face side hereof. Any such supplemental invoice shall be payable no later than thirty (30) days after the date thereof.
(g) Without limiting any other remedies available to Seller at law or in equity or otherwise, there shall be charged to Buyer a delinquency and service fee of one and one–half percent (1.5%) per month or the highest rate permitted by law, if less, on amounts due Seller for any period during which payment remains in arrears, and such discounts as may from time to time be offered by Seller with respect to its Product shall not be made available to Buyer while any payment owed by Buyer to Seller remain in arrears.

4. RESERVATION OF SECURITY INTEREST – Seller reserves and retains a security interest in the Product and the proceeds thereof until payment therefor in full has been made by Buyer. This Order Acknowledgment constitutes a security agreement between Buyer, as debtor, and Seller, as secured party, under the Uniform Commercial Code, and Seller shall have the rights and remedies of a secured party thereunder. Buyer authorizes Seller to file financing statements and to do any other act or thing necessary or useful in

perfecting Seller's security interest in the Product, and agrees to execute any and all documents required to be executed on its part to perfect said security interest.

5. TAXES – Unless otherwise stated on the face hereof or in the quote, the prices do not include customs duties or any sales, use, excise, or other similar taxes. Buyer shall pay, in addition to the prices indicated, the amount of any present or future customs duties or any sales, use, excise or other similar tax applicable to the sale of Product, or in lieu thereof Buyer shall supply Seller with an appropriate tax exemption certificate.

6. F.O.B. POINT – All sales are made F.O.B. point of shipment, Seller's facility. Title and risk of loss or damage shall pass to Buyer upon tender of the Product to the carrier at the shipping point. Unless written instructions from Buyer specifying the method of shipment to be used have been received and accepted by Seller, Seller will exercise its own discretion with respect to manner of shipment, insurance, and carrier to be used. Buyer shall be solely responsible for filing any claims for damage during shipment with the carrier. After the passage to Buyer of such risk of loss, the Product held by Seller, for whatever reason, shall be held for Buyer's account at Buyer's expense, irrespective of whether the Product are within the coverage of any insurance policy maintained by Seller.

7. DELIVERY
(a) Seller will manufacture in accordance with the shipment date as indicated in Seller's Order Acknowledgment. However, the shipment date is an estimate only, and Seller will be subjected to no liability for failure to perform on or by such date.
(b) Seller reserves the right to make partial shipments by line item with the consent of the Buyer, which consent shall not be unreasonably withheld, and invoices will be issued accordingly by purchase order line item. In the event of any breach as specified in Section 18, Seller may refuse to make further shipments.
(c) All Product orders hereunder must be delivered by Seller within fifteen (12) months of the date indicated on the Order Acknowledgment.

8. PRODUCT ACCEPTANCE
(a) Buyer shall have no right to reject Custom and Special Order Product on the basis of variation from the quantity ordered where such variation is within ±10% of the quantity ordered. Buyer shall pay for such Product actually received at the price indicated in Seller's Order Acknowledgment.
(b) Except as set forth in Section 8(a) above, Buyer shall give notice to Seller (and the carrier where appropriate) of discrepancies between type and quantity of Product ordered and Product delivered, or damage to the Product, within five (5)days of delivery of the Product to a common carrier or to the Buyer, whichever is earlier. Lacking such notice, Buyer shall be deemed to have accepted the Product as invoiced.
(c) Product may be returned to Seller only after prior notification and receipt of a Return Material Authorization number (hereinafter referred to as "RMA Number"). Product returned without a valid RMA number will be sent back to the Buyer at Buyer's expense and risk.
(d) No credit allowances for defective Product will be made or replacements therefore shipped until it is established to Seller's satisfaction after suitable test and inspection that the Product was in fact defective. Seller reserves the right to impose a reasonable rescreening charge if Seller determines that Product returned is found to be functional.

9. SPECIFICATIONS – All Product is subject to Seller's standard specifications. Seller reserves the right to make substitutions and modifications in the specifications of any Product without notification to or approval from Buyer, provided that such substitutions or modifications do not materially affect Product performance or purpose.

10. LIMITED WARRANTY – Seller warrants all Product against defects in materials and workmanship for a period of ninety (90) days from the date of delivery to Buyer. Seller's sole liability shall be limited to either replacing, repairing or issuing credit, at its option, for the Product if it has been paid for. Seller will not be liable under the warranty unless:
(a) Seller is promptly notified in writing upon discovery of defects by Buyer;
(b) The claimed defective Product is returned to Seller, insurance and transportation charges prepaid by Buyer;
(c) The claimed defective Product is received within ninety (90) days from the date of delivery; and
(d) Seller's examination of the Product discloses to its satisfaction that the alleged defect was not caused by misuse, neglect, improper installation, repair, alteration, accident or other hazard.
THIS WARRANTY DOES NOT COVER PRODUCT DAMAGE WHICH RESULTS FROM ACCIDENT, MISUSE, ABUSE, IMPROPER LINE VOLTAGE, FIRE, FLOOD, LIGHTNING OR OTHER ACTS OF GOD OR DAMAGE RESULTING FROM ANY MODIFICATIONS, REPAIRS OR ALTERATIONS PERFORMED OTHER THAN BY SELLER OR SELLER'S AUTHORIZED AGENT OR RESULTING FROM FAILURE TO STRICTLY COMPLY WITH SELLER'S WRITTEN OPERATING AND MAINTENANCE INSTRUCTIONS. BUYER ACKNOWLEDGES THAT THE PRODUCT ARE HIGHLY SENSITIVE ELECTRONIC PRODUCT REQUIRING SPECIAL HANDLING AND THAT THIS WARRANTY DOES NOT APPLY TO IMPROPERLY HANDLED PRODUCT. PRODUCT MANUFACTURED TO MEET BUYER'S SPECIFIC PERFORMANCE SPECIFICATIONS ACCEPTED BY SELLER ARE WARRANTED ONLY TO PERFORM IN CONFORMITY WITH SUCH SPECIFICATIONS, AND ARE WARRANTED

ONLY AGAINST DEFECTS NOT RELATED TO SUCH SPECIFICATIONS IN ACCORDANCE WITH THE TERMS AND CONDITIONS SET FORTH HEREIN ABOVE.

Seller's warranties will not be affected by rendering of technical advice in connection with the Purchase Order or Product furnished hereunder. EXCEPT AS EXPRESSLY PROVIDED ABOVE, SELLER MAKES NO WARRANTIES, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL SELLER BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES WITH RESPECT TO THE PRODUCT PURCHASED HEREUNDER. THIS WARRANTY EXTENDS ONLY TO BUYER AND NOT TO BUYER'S CUSTOMERS.

11. LIMITS OF LIABILITY AND INDEMNIFICATION

(a) THE WARRANTIES OF SELLER SET FORTH ABOVE ARE IN LIEU OF, AND BUYER HEREBY WAIVES, ALL OTHER WARRANTIES OF SELLER, EXPRESS OR IMPLIED, ARISING OUT OF OR IN CONNECTION WITH, THE SALE OF PRODUCT, OR THE USE, INSTALLATION OR PERFORMANCE THEREOF, IN THE COURSE OF DEALING OR PERFORMANCE UNDER THIS AGREEMENT, INCLUDING, BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

(b) SELLER SHALL NOT BE LIABLE TO BUYER, TO BUYER'S CUSTOMERS OR TO ANY OTHER PERSON, AND BUYER AGREES TO INDEMNIFY SELLER, WITH RESPECT TO ANY CLAIMS FOR INCIDENTAL, SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES, INCLUDING LOSS OF PROFIT, AND LOSS OF PLANT EQUIPMENT OR PRODUCTION ARISING FROM THE SALE OR SUBSEQUENT USE OF PRODUCT.

12. PATENT INFRINGEMENT – INDEMNIFICATION

(a) Seller agrees, at its own expense, to defend Buyer thereof from and against any claim, suit or proceeding, and to pay all judgments and costs finally awarded against Buyer by reason of claim, suit or proceeding insofar as it is based upon an allegation that the Product furnished by Seller infringes any United States letter patent, provided that Seller is notified promptly of such claim in writing and is given authority and full and proper information and assistance (at Seller's expense) for defense of same. In case such Product are held in such suit to constitute an infringement and the use of Product is enjoined, Seller shall at its sole discretion and at its own expense: (1) procure for Buyer the right to continue using the Product; (2) replace or modify the same so that it becomes noninfringing; or (3) remove such Product and grant Buyer a credit for the depreciated value of the same.

(b) Buyer shall have the right to employ separate counsel in any claim, suit or proceeding set forth in Section 12(a) and to participate in the defense thereof, but the fees and expenses of Buyer's counsel shall not be borne by Seller unless: (1) Seller specifically so agrees; or (2) Seller, after written request and without cause, does not assume such defense. Seller shall not be liable to indemnify Buyer for any settlement effected without Seller's consent, unless Seller failed, after notice and without cause, to defend such claim, suit or proceeding.

(c) The indemnification set forth in Section 12(a) shall not apply and Buyer shall indemnify Seller and hold it harmless from all liability or expense (including costs of suit and attorney's fees) if the infringement arises from, or is based upon Seller's compliance with particular requirements of Buyer or Buyer's customer that differ from Seller's standard specifications for the Product, or modifications or alterations of the Product, or a combination of the Product with other items not furnished or manufactured by Seller.

(d) Buyer agrees that Seller shall not be liable for any collateral, incidental or consequential damages arising out of patent infringement.

(e) The foregoing states the entire liability of Seller for patent infringement.

13. LIFE SUPPORT POLICY – Seller's Product are not authorized for use as critical components in life support devices or systems. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury or death to human life.

A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Buyer agrees to indemnify and hold Seller harmless for any cost, loss, liability, or expense (including without limitation attorneys' fees and other costs of litigation or threatened litigation) arising out of violation of the above prohibition by Buyer or any person or entity receiving Seller's Product through Buyer.

14. CANCELLATION – Buyer's rights and obligations with respect to cancellation of orders shall be governed by this Section 14.

(a) In the case of Standard Product, Seller must receive Buyer's written cancellation notice no less than thirty (30) days prior to Seller's scheduled ship date indicated in the Order Acknowledgment.

(b) In the case of Special Order Product, Seller must receive Buyer's written cancellation notice no less than ninety (90) days prior to Seller's scheduled ship date indicated in the Order Acknowledgment.

(c) In the case of Custom Product, Seller must receive Buyer's written cancellation notice no later than one hundred and twenty (120) days or the quoted lead for that specific device, which ever is longer, prior to Seller's scheduled ship date indicated in the Order Acknowledgment.

(d) Notwithstanding the provisions of Sections 14(a) through 14(c), if the Buyer cancels, at any time, Seller may, at its election, be entitled to receive from Buyer reimbursement for the costs, direct and indirect, of all work in process at the time of cancellation, NRE cancellation expenses as specified in the quote plus reasonable profit and any extra shipping or customized charges.
(e) If Buyer cancels any portion of the Product indicated on the face hereof, Buyer shall be liable for the adjustments to the purchase price on the Product actually purchased as specified in Section 3 and Seller shall be entitled to collect such adjustment in the manner specified therein.

15. RESCHEDULING OF DELIVERY – Buyer's right to reschedule deliveries shall be governed by this Section 15.
(a) In the case of Standard Product, Seller must receive Buyer's written reschedule request no less than thirty (30) days prior to Seller's scheduled ship date indicated by Seller.
(b) In the case of Special Order Product, Seller must receive Buyer's written reschedule request no less than ninety (90) days prior to Seller's scheduled ship date indicated in the Order Acknowledgment.
(c) In the case of Custom Product, Seller must receive Buyer's written reschedule request no less than one hundred twenty (120) days or the quoted lead for that specific device, which ever is longer, prior to Seller's scheduled ship date indicated in the Order Acknowledgment.
(d) With request to reschedule orders pursuant to Section 15(b) and 15(c) above, such rescheduled orders must be delivered within ninety (90) days of Seller's scheduled ship date.

16. ASSIGNMENT – Neither Buyer nor Seller may assign this Order Acknowledgment, or any interest or right herein without the prior written consent of the other. Any assignment without such consent shall be void.

17. U.S. EXPORT LAWS
Seller's obligations are subject to the export administration and control laws and regulations of the U.S. Government. Buyer shall comply fully with such laws and regulations in the export, resale or other disposition of Product.

18. BREACH – Any one of the following acts by Buyer shall constitute a breach of Buyer's obligations under the contract formed by acceptance of the quotation:
(a) Failure to make payment for any Product from Seller when due;
(b) Failure to accept conforming Product supplied hereunder;
(c) The filing of a voluntary or involuntary petition in bankruptcy against Buyer, the institution of any proceeding in insolvency or bankruptcy (including reorganization) against Buyer, the appointment of a trustee or receiver of Buyer, or an assignment for the benefit of creditors of Buyer; or
(d) Any other act by Buyer in violation of any of the provisions as stated herein. In the event that Buyer breaches any provision herein in any manner set forth above, Seller may (in addition to any other right or remedies provided herein or at law or in equity), by written notice to Buyer, terminate the contract or any part thereof, without any liability to Seller whatsoever. Buyer shall pay all costs, including reasonable attorneys' fees, incurred by Seller in any action brought by Seller to collect payments owing or otherwise enforce its rights.

19. PROPERTY RIGHTS AND TOOLING – Buyer shall retain sole title to circuit and logic diagrams, schematics, test patterns, and other relevant information provided to Seller as part of this Purchase Order. Seller shall not be obligated to return any such information to Buyer unless specifically requested to do so by Buyer in writing, detailing each item. Unless otherwise expressly agreed, circuit schematics, mask sets, design tapes, processing information, test software and hardware and any other proprietary information shall remain the sole property of Seller.

20. GENERAL
(a) This Purchase Order and the Exhibits attached, if any, hereto constitutes the entire agreement between the parties with respect to the subject matter hereof and there are no representations, warranties or commitments except as set forth herein, and supersedes all prior and contemporaneous agreements, understandings, negotiations and discussions, written or oral, of the parties, relating to the subject matter hereof.
All rights and obligations of the parties to this Purchase Order shall be governed by and construed in accordance with the laws of the State of California. The parties hereto subject themselves to the jurisdiction of and agree that venue shall be of the State courts of California in Santa Clara County with respect to any dispute, disagreement or claim arising hereunder.
(c) Failure of any party hereto to enforce any of the provisions of this Purchase Order, or any rights with respect thereto, or failure to exercise any election provided for herein, shall in no way be considered a waiver of such provisions, rights or elections, or in any way effect the validity of this Purchase Order. The failure by any party hereto to enforce any of said provisions, rights, or election shall not prejudice such party from later enforcing or exercising same or any other provisions, rights, or elections which it may have under this Purchase Order.
(d) Any notice or other communication required or permitted hereunder shall be deemed sufficient only if in writing and hand delivered or mailed, postpaid, by registered or certified mail, return receipt requested, to Seller at the following addresses:
EXAR CORPORATION, P.O. Box 49007, San Jose, California, 95161–9007

ATTN: Senior Vice President, Chief Financial Officer
or to such other address as it shall be designated by notice pursuant to this subsection. Such notice shall be deemed to have been given on the date actually received by the party to whom it is directed.

(e) No modification, amendment, waiver, consent or discharge in connection with this Purchase Order shall be binding upon either party unless in writing and signed by the party sought to be charged with the same.

(f) All covenants, stipulations and promises in this Purchase Order shall be binding upon and inure to the benefit of the parties hereto and their respective successors in interest, assignees, and legal representatives. Neither party shall have the right to assign or otherwise transfer its rights or obligations under this Purchase Order without the prior written consent of the other party; provided, however, that a successor in interest to a party by merger, by operation of law, or by assignment, purchase, or otherwise, of the entire business of either party shall acquire all the rights and be subject to all the obligations of such party hereunder, without the necessity of obtaining such prior written consent; provided, however, that nothing herein shall prevent either party from assigning all of its rights and obligations under this Purchase Order to a Subsidiary of that party upon written notice to the other party.

(g) If the performance of this Purchase Order or if any obligations hereunder, except the making of payments, is prevented, restricted, or interfered with by reason of fire or other casualty or accident; strikes or labor disputes; inability to obtain raw materials, power, or supplies, war or other violence; any law, order, proclamation, regulation, ordinance, demand, or requirement of any government agency; or any other act or condition whatsoever beyond the reasonable control of the parties hereto, the party so affected upon giving prompt written notice to the other party, will be excused from performance to the extent of the prevention, restriction, or interference, provided that the party so affected uses its best efforts to avoid or remove the causes of nonperformance and continues performance hereunder with the utmost dispatch as soon as those causes are removed.

(h) The prevailing party in any legal or arbitration action brought by one party against the other shall be entitled, in addition to any other rights and remedies it may have, to reimbursement for its expenses incurred thereby, including court costs and reasonable attorneys' fees.

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Other EXAR Products Available

Listed by Product Group

COMMUNICATIONS

PCM Transmission

XR-T5794	Quad E1 Line Interface Unit
XR-T5791	Single Channel E1 Line Interface Unit
XR-T7288	E1 Line Interface with Clock Recovery
XR-T5684	T1 Line Interface Unit with Clock Recovery
XR-T5683	E1/E2 Line Interface Unit with Clock Recovery
XR-T7295	DS3/Sonet STS1 Integrated Line Receiver
XR-T7295E	E3 Integrated Line Receiver
XR-T7296	E3/DS3/Sonet STS-1 Integrated Line Transmitter
XR-T6164	CCITT G.703 Co-directional Interface
XT-T6165	Co-directional Digital Processor
XR-T6166	Co-directional Digital Processor with Slip Buffer
XR-T56L22	Low Power PCM Repeater/Receiver
XR-T56L85	Low Power 2MBPS PCM Line Interface
XR-T5675	PCM Line Driver
XR-T5676	Low Power PCM Line Receiver

Telephony

XR-T65118A	Voice Switched Speakerphone
XR-T65119	Low Power Audio Amplifier Circuit
XR-T66100	Caller I.D. Receiver I.C.

Datacommunications

XR-T3588/ XR-T3589	V.35/Bell 306 Driver/Receive
XR-82C684	CMOS Quad Channel UART (QUART)
XR-68C681/ XR-88C681	CMOS Dual Channel UART (DUART)

Other EXAR Products Available

XR-16C550A	CMOS UART with FIFO
XR-16C450	CMOS UART
XR-16C452	DUART with Parallel Printer Port
XR-16C552	Duart with FIFO and Parallel Printer Port

CONSUMER

Audio

XR-1071	BBE" II High Definition Audio Processor
XR-1090A	Graphic Equalizer Display Filter Detector
XR-1010	Second Order Switched Capacitor Filters
XR-1091	7-Band Graphic Equalizer Display Filter
XR-1092	12-Band Graphic Equalizer Display Filter/Multiplexer
XR-1093	5-Band Graphic Equalizer Display Filter
XR-1095	7-Band Graphic Equalizer Display Filter/Driver
XR-1096	7-Band Graphic Equalizer Display Filter/Driver
XR-1097	7-Band Graphic Equalizer Display Filter/Driver

Video

XR-10823	8mm VTR Automatic Tracking Filter

MASS STORAGE

Read/Write

XR-9010	Low Power R/W Preamplifer for 3 Terminal Recording Heads, 2 or 4 channels
XR-9030	Low Power R/W Preamplifier for 2 Terminal Recording Heads
XR-9033A	5V R/W Preamplifier for 2 Terminal Recording Heads, 2 or 4 channels
XR-9035	5V R/W Preamplifier for 2 Terminal Recording Heads, 2 or 4 channels
XR-9037	5V R/W Preamplifier for 2 Terminal Recording Heads, 2 or 4 channels
XR-542	Hard Disk Pulse Detector

Other EXAR Products Available

GENERAL PURPOSE STANDARD PRODUCTS

XR-2211	FSK Tone Demodulator/Tone Decoder
XR-2206	Monolithic Function Generator
XR-215	Monolithic Phase-Lock Loop
XR-2207	Voltage Controlled Oscillator
XR-2209	Precision Oscillator
XR-2212	Precision Phase-Lock Loop
XR-8000	Microprocessor Support IC
XR-8038A	Precision Waveform Generator
XR-8073	Micropower Step-Up Switching Regulator
XR-34074	Quad High Performance Operational Amplifier

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Section 2

Quality & Reliability

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The EXAR Commitment to Continuous Quality & Reliability Improvement

Achieving improvement in quality and reliability is a continuous, unending process. EXAR is dedicated to the long-term investment toward defect reduction, performance improvement, and customer satisfaction.

We believe that understanding the requirements of the customer, and translating them into a process which can meet these requirements the first time - - every time - - is essential in enabling us to develop long-term customer partnerships.

Key elements of the EXAR Continuous Improvement Process include:

- **Quality Improvement System.**

  EXAR's quality improvement system is built on a customer-supplier model wherein every employee is both a customer and a supplier to somebody, either internally or externally. Our company quality policy reinforces this customer/supplier relationship:

  In our relentless drive to zero defects EXAR employees, using a process of continuous improvement, will accept from suppliers and deliver to customers goods and services that meet or exceed agreed requirements.

  All employees have been trained in the tools and techniques of quality improvement, and meet regularly in quality improvement meetings (QIMs). A QIM is comprised of employees in the same functional group. Each QIM works on a cycle of quality which involves identifying defects (defined as any deviation from specified requirements), monitoring to determine the extent of the defects, analyzing the data, and implementation of corrective action.

  Leadership and direction for the quality improvement system is provided by the executive quality improvement team (QIT) comprised of EXAR's president and CEO and his direct reports. This team meets weekly to review the status of the system, the results achieved, and to plan future direction.

  Corrective action teams (CATs) are cross-functional teams chartered by the QIT to address specific problems of a cross-functional nature.

  Continuous improvement goals are set annually for key business and quality metrics such as on-time delivery, cycle time reduction and outgoing product quality.

- **Supplier Management**

  EXAR uses various subcontract foundry and packaging services. These key sources of supply are managed under EXAR's Supplier Management System which encompasses the following elements:

  - EXAR's requirements are defined in a Supplier Partnerships Manual supported by a set of procurement specifications. The manual defines all the requirements that are common to all suppliers, such as a quality system, statistical process control, and quality data reporting. Procurement specifications define the requirements unique to each supplier, manufacturing process, or packaging technology.
  - Suppliers' quality systems are audited to verify that a documented system exists, that it is being followed, and to ensure that it is capable of providing reliable product.
  - Suppliers' performance is routinely measured against a defined set of criteria. Feedback to suppliers consists of a score card and individual performance reviews between employees of both companies.
  - Suppliers are required to work towards meeting a set of continuous improvement goals.
  - The criteria for supplier certification includes consistently high performance as measured by the quarterly score card.

- Continuous improvement goals are set, consistent with EXAR's goals and those of customers.

The eventual objective of the supplier management activity is to bring all suppliers up to the supplier certification criteria.

◆ **Reliability Assurance**

Reliability begins with good process controls on manufacturing operations and well-characterized processes. Also critical to reliability is the design environment. EXAR has invested in state-of-the-art design tools.

New or changed manufacturing processes are required to successfully complete qualification. New processes or proposed changes are submitted to EXAR's Qualification Review Board comprised of representatives from Design, Product, Packaging, Foundry, Reliability and Quality Engineering. The QRB determines the extent of qualification or requalification, and is also responsible for reviewing and approving qualification results.

Ongoing process reliability monitors are conducted to continuously assess the reliability of our manufacturing processes, and to provide feedback to the manufacturing operations.

The results of reliability qualifications and monitors are made available to customers through periodic reliability reports.

EXAR Management is Accessible!

R & QA, Marketing, Customer Service, Engineering and Design are available for consultation, and we pride ourselves on our prompt response time to queries!

The quality philosophy at EXAR emphasizes each employee's responsibility for building and delivering product that conforms to customer requirements, and meets specific Quality and Reliability objectives.

THE EXAR PRODUCT DEVELOPMENT ENVIRONMENT

The demonstrated reliability of EXAR's products is the result of organization goals focused on continuous quality improvement, as well as EXAR proprietary semiconductor manufacturing processes.

EXAR Mixed-Signal Technologies

EXAR products and processes are designed to achieve specific reliability objectives:

- EXAR CMOS and BiCMOS processes are designed to meet the twin product objectives of low noise and low drift – – both extremely critical characteristics in achieving high performance analog circuit functions.
- EXAR CMOS and BiCMOS processes utilize Epi in addition to various circuit design techniques to achieve latch-up free performance.
- EXAR device structures do not require planarization and reflow of intermediate dielectric layers. These unique device structures eliminate the need for reflow glasses which contain Phosphorous. This significantly reduces the potential for inducing corrosion in association with moisture.
- EXAR processes employ silicon nitride final passivation which provides excellent moisture resistance and long-term stability.
- EXAR uses a proprietary thin film technology based on SiCr compounds. The thin film resistors, coupled with barrier metallurgy and nitride passivation demonstrate excellent reliability in terms of maintaining long life and accuracy over time and temperature.

Product Emulation: Electrical and Physical

The EXAR design process is based on the premise that every characteristic of a circuit can be very nearly approximated by a combination of well understood physics, and chemical/electrical laws which can be properly applied through a computer based design procedure.

This process requires that the electrical design and specifications be captured, and then maintained on an Electronic Design Automation data base. This includes parasitic structures management. This data base is then thoroughly checked for design versus specification and physical construction versus electrical circuit with the most advanced tools available in the industry. These tools allow full mixed mode simulations, and full mixed element verification of all circuit and parasitic structures versus design rules/process specifications. This approach reduces the chance of hidden failure mechanisms.

New Design Construction

All input/output circuit and device structures are included in the design through a hierarchical approach that ensures consistent performance from one section of a circuit to another. This includes 4000 volt rated digital I/O and 2000 volt rated analog I/O pads. This process is done across product lines. The learning curve improvements applied to a specific function also are applied across the product line and are incorporated in future designs through this computer-captured know-how.

New Design Qualification

In addition to this simulated proof of design, EXAR also requires that all new products pass an LTPD of 2 for 1000 hours burn-in at 125°C, in addition to other thermal, environmental, and electrical stresses before the product is released to production. The results of this initial testing (as well as ongoing process reliability monitors) are used as feedback to the design process, and to fine tune the product emulation tools.

EXAR INNOVATIVE APPROACH TO MINIMIZE TESTER VARIABILITY

Correlation of test results between supplier and customer historically has been a significant source of frustration in the semiconductor industry. Irrespective of IC technology, brand or price of the ATE being used, test correlation remains an industry issue.

The typical industry attempt to minimize correlation problems is to use "gold standard" control devices. Used as "go-no-go samples", this approach at least tells Test Engineering that the unit tested was good before – – and

is good now. But this is only marginally better than not using "gold" devices at all. The reason is simple. A "gold" part (or any other part) that passed a tester previously could pass a bad or marginal tester later – – particularly if the typical values of the part are not near the "edge" or limit of any given test. And, if the tester were for any reason to show a part as being "better" in any way, that could translate into unknowingly shipping product which does not meet specification. This approach drives the need for quality assurance testing, with a potentially high percentage of lots requiring re-test.

EXAR has developed an innovative Statistical Process Control application to assure optimum parametric testing for its products. The first step is to determine the range of variability in test operations that takes into account testers, hardware, and environment. A minimum of five "gold standard" devices are tested and datalogged using all combinations of testers, hardware fixtures, contactors, and test sockets. This is followed by a three-way ANOVA (ANalysis Of VAriance) to determine the repeatability of the control units, the testers, the hardware, and the time tested. "Repeatability" is defined as the range of each parameter when several devices are tested over and over again. Additionally, when gold devices are repeatedly tested, they are removed from the socket or contactor assembly and reseated each time. This allows a more accurate representation of what actually happens during Production.

The three-way ANOVA between testers, hardware and environment combines the "repeatability" in a mathematically correct way to determine the "reproducibility". We can define "reproducibility" as the range that results from taking into account all of the different "repeatabilities".

Based on this statistical analysis of the test environment, Test Engineering determines Process Capability (or Cpk) limits which are programmed into the memory of each Production test system. Menu-driven software requires that control units be tested before Production is allowed access to the test program. If the control unit test results do not fall within defined upper and lower control limits, the test system is automatically locked out and can only be released to Production with a password under the control of the Engineering Department.

For the test environment, Cpk is determined by Root-Sum-Squaring the variabilities caused by different testers, different sets of hardware, different times of the day, and the interaction between these ... based on ANOVA. This is the sigma used in the Cp, Cpk calculations for the tester Cpk. This is different from a product Cpk, which is more generally understood. The tester Cpk uses the variability of everything except product variation. The goal is to achieve a tester Cpk of five for each test parameter. Once a parameter achieves that for Test Cpk, the Test Engineer will work on the hardware and software to achieve the same on as many parameters as possible.

WHAT DO CP AND CPK MEAN . . . REALLY?

Cp and Cpk represent a statistical attempt to quantify the variability of a process to allow a supplier to see if the capability of a process or product line meets its intended objective. These two indices are meaningful only if the following conditions are met:

- The process must be under "statistical control" – – which means a condition where all special causes of variation have been eliminated and only common causes remain. This can be evidenced on a control chart by the absence of points beyond the control limits and by the absence of non-random patterns or trends within the control limits.

- The people associated with the process have been statistically trained and are fully aware and capable of collecting data, constructing the control charts and interpreting the data.

- The process output is approximately normally distributed.

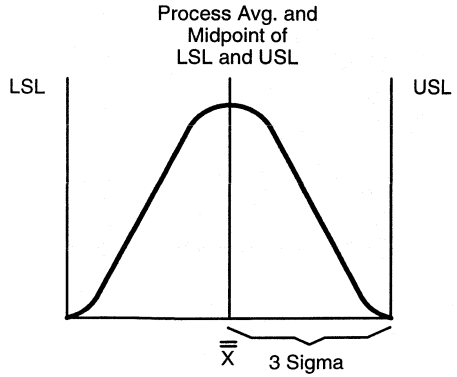


Figure 1.
The case where the Process Average and the Midpoint between Spec Limits are the same (Cp = Cpk)

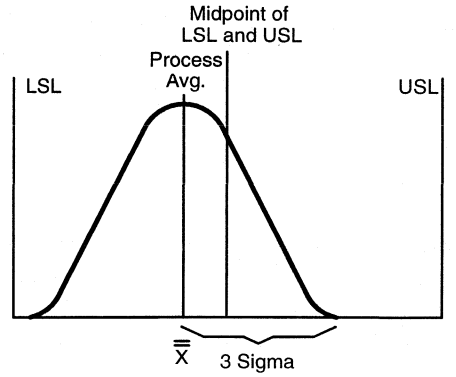


Figure 2.
The case where the Process Average and the Midpoint between spec limits are not the same (Cp ≠ Cpk)

USL = Upper Spec Limit
LSL = Lower Spec Limit
Sigma = Standard Deviation
$\overline{\overline{X}}$ = Process Average

Definition of Process Capability Indices

Cp compares the range of a process parameter distribution to the width of the specification limits.

Mathematically, Cp is equal to:

$$\frac{USL - LSL}{6\ Sigma}$$

Cpk compares both the range and location of a process parameter distribution to the width of the specification limits.

Mathematically, Cpk is equal to the smaller of:

$$\frac{USL - Process\ Average}{3\ Sigma} \quad or \quad \frac{Process\ Average - LSL}{3\ Sigma}$$

Cpk = Cp from the above relationships when the distribution is centered at the midpoint between the spec limits (*as in Figure 1.*).

A process is considered "barely capable" if the Cpk is at least equal to 1.33. However, Cpk goals of 2.0 are specified for critical parameters.

Table 1. shows the relationship between Cp and process fallout in PPM (parts per million) assuming a process in statistical control – – and normally distributed.

Cpk	PPM
0.50	133,600
0.75	24,400
1.00	2,700
1.10	966
1.20	318
1.30	96
1.40	26.6
1.50	6.8
1.60	1.6
1.80	0.06
2.00	0.0018

Table 1.
Process Fallout (PPM) versus Cpk
Assuming a Normal Process in Statistical Control

Any "capability analysis" technique, no matter how exact it appears, can give only approximate results. This is because there is always some sampling variation, no process is ever "fully" under statistical control, and no process output exactly follows the normal distribution. Final results should always be used with caution and interpreted conservatively. EXAR employs this statistical technique with the awareness that Cp and Cpk indices are only one of many tools on the journey of continuous quality improvement.

RELIABILITY CALCULATIONS

Integrated circuit reliability is defined in terms of a statistical probability that the device, which initially met its specification, continues to perform to specifications for a given time under stated usage conditions.

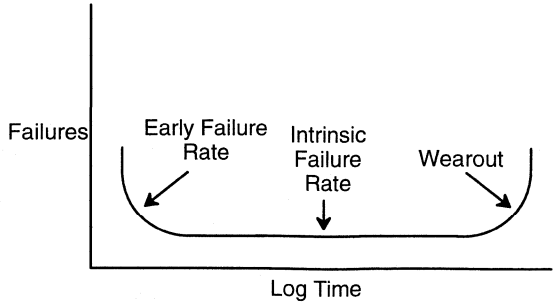


Figure 3. Bathtub-Shaped Failure Rate Curve

Device Life Cycle

The failure rate for a particular device is not uniform throughout its life of operation. Field failures occur in distinct modes that are described by the well-known "bath-tub curve". The life cycle of a device has three periods:

- *Early Failure Rate*

  Failures during this period can be attributed to latent defects from the manufacturing process. The performance level will vary depending on the complexity, the size and the technology, but a PPM better than 500 may be expected. As the latent failures occur, the failure rate decreases substantially. The early failure rate period is typically defined as the first six months of operation.

- *Intrinsic failure rate period*

  This period extends for at least the next 20-30 years. The marginal units have failed during the early period and additional failures are likely to be due to extreme or unpredictable variations in operating conditions.

- *Wear-out period*

  The onset of the wear-out period is characterized by the appearance of defects due to physical changes affecting the entire population such as wirebond thermal fatigue, irreversible chemical or metallurgical processes, and electromigration.

The most common measure of reliability for semiconductors is the failure rate and is expressed in FITs. A FIT (Failure In Time) is one failure in one billion device-hours.

Failure rate estimates are based on the relationship between the failure rate of the device under working conditions and its failure rate during high temperature life-test:

$$\lambda 1 = \frac{\lambda 2}{A}$$

where:

$\lambda 1$ = failure rate at working condition junction temperature
$\lambda 2$ = failure rate at life test junction temperature
A = acceleration factor.

Acceleration Factor

The acceleration factor is obtained from the Arrhenius equation:

$$A = \exp\left[\frac{-Ea}{k}\left(\frac{1}{Tj2} - \frac{1}{Tj1}\right)\right]$$

where:

A = Acceleration factor
Ea = Thermal activation energy (electron volts)
k = Boltzmann's constant (8.62×10^{-5} eV/°K)
Tj1 = in-use junction temperature (°K)
Tj2 = in-stress junction temperature (°K)

In order to compute the acceleration factor, the thermal activation energy of the failure mechanism and the junction temperatures must be determined. Also, an adjustment for the appropriate confidence level must be made.

Thermal Activation Energy

Table 2. gives the activation energy of some common types of failure mechanisms. They are estimates taken from published literature.

Failure Mechanism	Typical Activation Energy (eV)
Silicon Defects	0.3
Diffusion Defects	0.9
Oxide Defects	0.3
Dielectric Breakdown	0.3
Electromigration	0.5
Ionic Contamination	1.0
Bond-Metallic Interface	1.0
Metal Corrosion	0.7

Table 2.

Junction Temperature

A knowledge of junction temperature is required in order to compute the Acceleration factor. The relationship between junction temperature, ambient temperature, power dissipation and thermal resistance is given by the equation:

$$Tj = Ta + (Pd * \theta ja)$$

where:

Tj = junction temperature (°C)
Ta = ambient temperature (°C)
Pd = power dissipation (watts)
θja = thermal resistance (°C/watt)

The power dissipation (Pd) is computed using the actual supply currents and voltages used in the life test load conditions.

The thermal resistance (θja) is a function of the packaging of the device. It is also dependent on user controlled factors such as the method of mounting the package in its application, the proximity to heat sources or sinks and the presence or absence of air flow. *Table 3.* gives some typical values for common types of packages:

THERMAL RESISTANCE	
Package Type	Typical θja (°C/watt)
16 pin DIP, epoxy 300 mil	83
24 pin DIP, epoxy 300 mil	59
28 pin DIP, epoxy 600 mil	57
20 pin SO Jedec, epoxy 300 mil	108
28 pin PLCC, epoxy	75
16 pin CERDIP, 300 mil	80
24 pin CERDIP, 600 mil	68

The above values can vary by ±20 percent.

Table 3.

UPPER BOUND OF OBSERVATION AT SPECIFIED CONFIDENCE LEVEL		
Observation (Number of Failures)	60 Percent Confidence	90 Percent Confidence
0	0.92	2.3
1	2.02	3.89
2	3.11	5.32
3	4.17	6.68
4	5.14	7.99
5	6.29	9.27
6	7.34	10.53
7	8.39	11.77
8	9.43	12.99
9	10.48	14.21
10	11.51	15.41
11	12.55	16.60
12	13.59	17.78
13	14.62	18.96
14	15.66	20.13
15	16.69	21.29

Table 4.

Confidence Level of Observed Failures

When a sample is randomly selected from a population, there is always the possibility that the sample is not representative of the population at large. In particular, it is important to consider that the selected sample may have a lower failure rate than the remainder of the population.

In order to account in the reliability computations for the error sampling, confidence intervals are applied to the observed failure rate.

The confidence intervals are derived from Chi-square statistics. Only the upper bound of the intervals is of interest to us. *Table 4.* gives the upper bound of the observations at the 60 and 90 percent confidence level.

For example, if the observation is 3 failures, the upper bound for the reliability computation is 4.17 at the 60 percent confidence level.

Computation Example

A randomly selected sample of 1000 parts was subjected to a 1000-hour static life test at 125°C. The device power dissipation is 100 milliwatts and the package has a thermal resistance of 75°C/watt. The device is intended to operate in a 55°C environment.

The life test results were:

0 failure out of 1000 at 168 hours
1 failure out of 1000 at 500 hours
1 failure out of 999 at 1000 hours

The failure mode (determined by failure analysis) corresponds to an activation energy of 0.55 eV.

Total number of failures = 2
Assuming a 60 percent confidence level, the adjusted number of failures per *Table 4.* = 3.11

Total number of device-hours =
0(168) + 1(500) + 999(1000) = 999,500

Temperature rise due to power dissipation and thermal resistance:
Trise = Pd x θja = 0.1 watt x 75°C/watt = 7.5°C

Junction temperature under life test conditions:
Tj2 = 125°C + 7.5°C = 132.5°C = 405.5 °K
(Note: degrees Kelvin = degrees Celsius + 273)

Failure rate under life test conditions:

$\lambda 2$ = 3.11 failures / 999,500 device-hours
= 3,112 FITs at 132.5°C

Junction temperature under working conditions:

Tj1 = 55°C + 7.5°C = 62.5°C = 335.5 °K

Acceleration factor:

A = exp [–Ea/k (1/Tj2 – 1/Tj1)]

$$A = \exp \left[\frac{-0.55}{8.62x10^{-5}} \left(\frac{1}{405.5} - \frac{1}{335.5} \right) \right]$$

A = 27

Failure rate under working environment conditions:

$$\lambda 1 = \frac{\lambda 2}{A} = \frac{3,112}{27} =$$

116.6 FITs at 62.5°C

MP1230 12-Bit D/A Converter

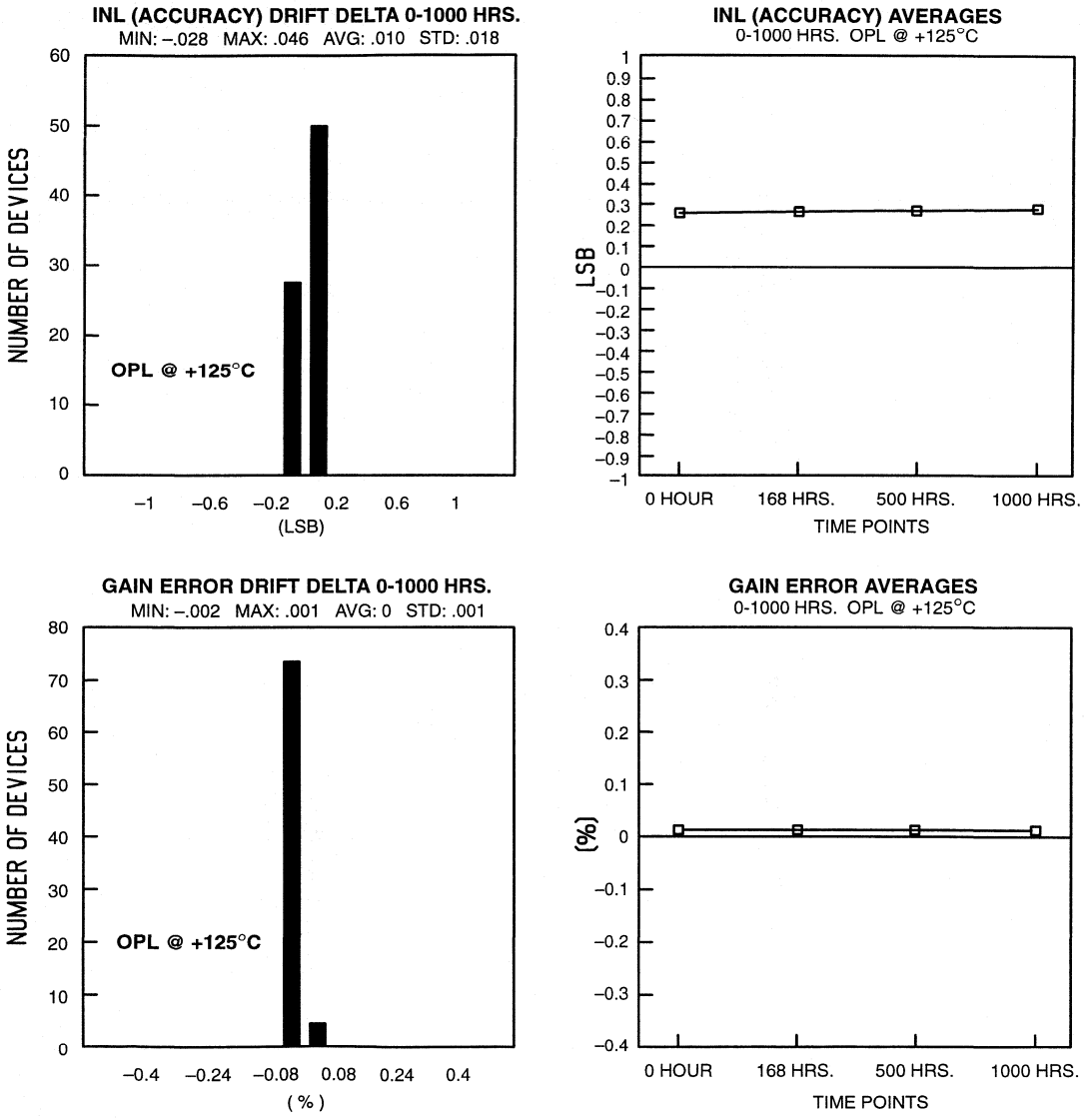


Figure 4.
MP1230 PDIP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R90-010/J1)

MP1230 12-Bit D/A Converter

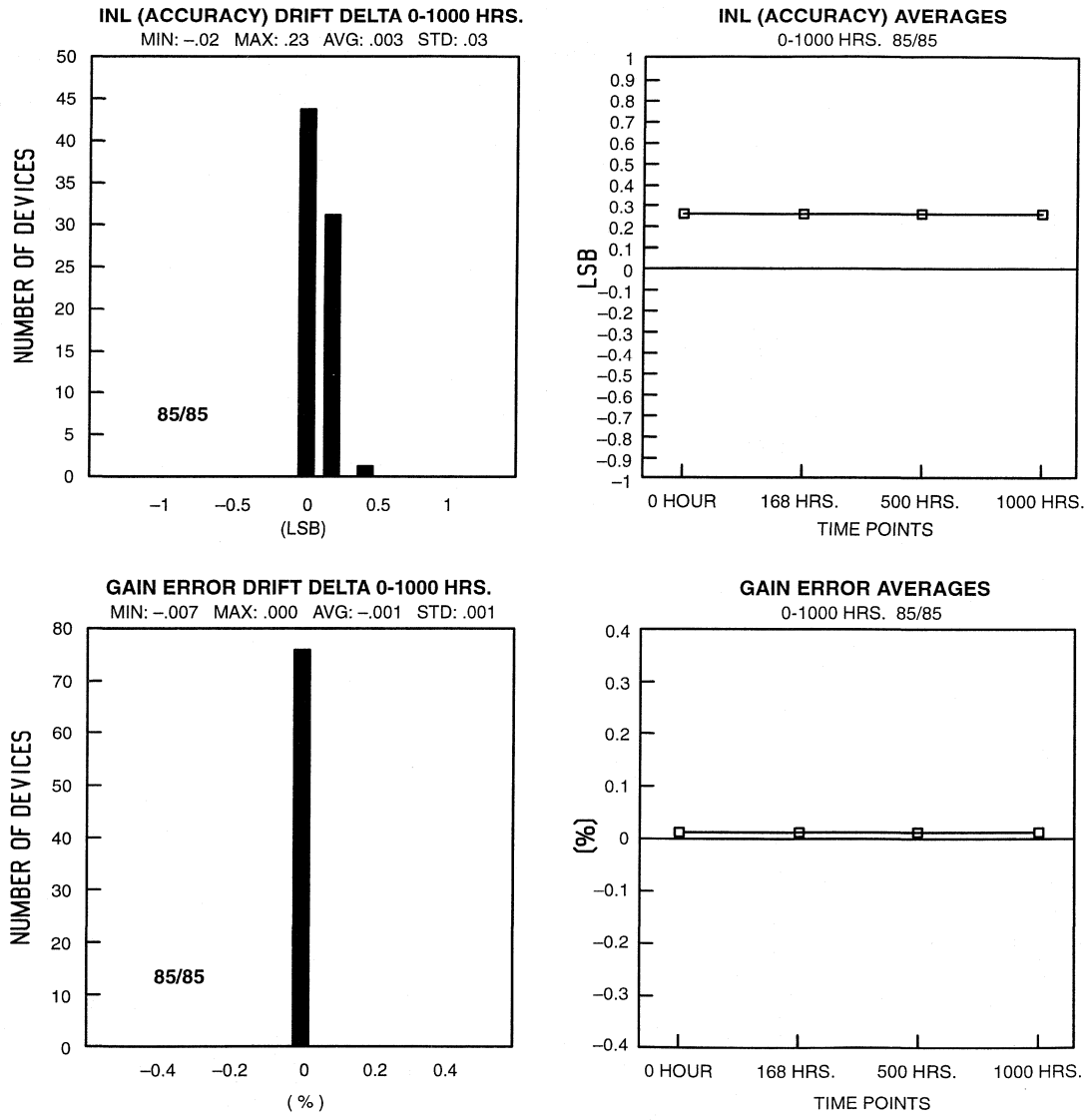


Figure 5.
MP1230 PDIP 1000 Hour 85/85
(Reference Reliability Report R90-010/D2)

MP8785 8-Bit Video A/D Converter

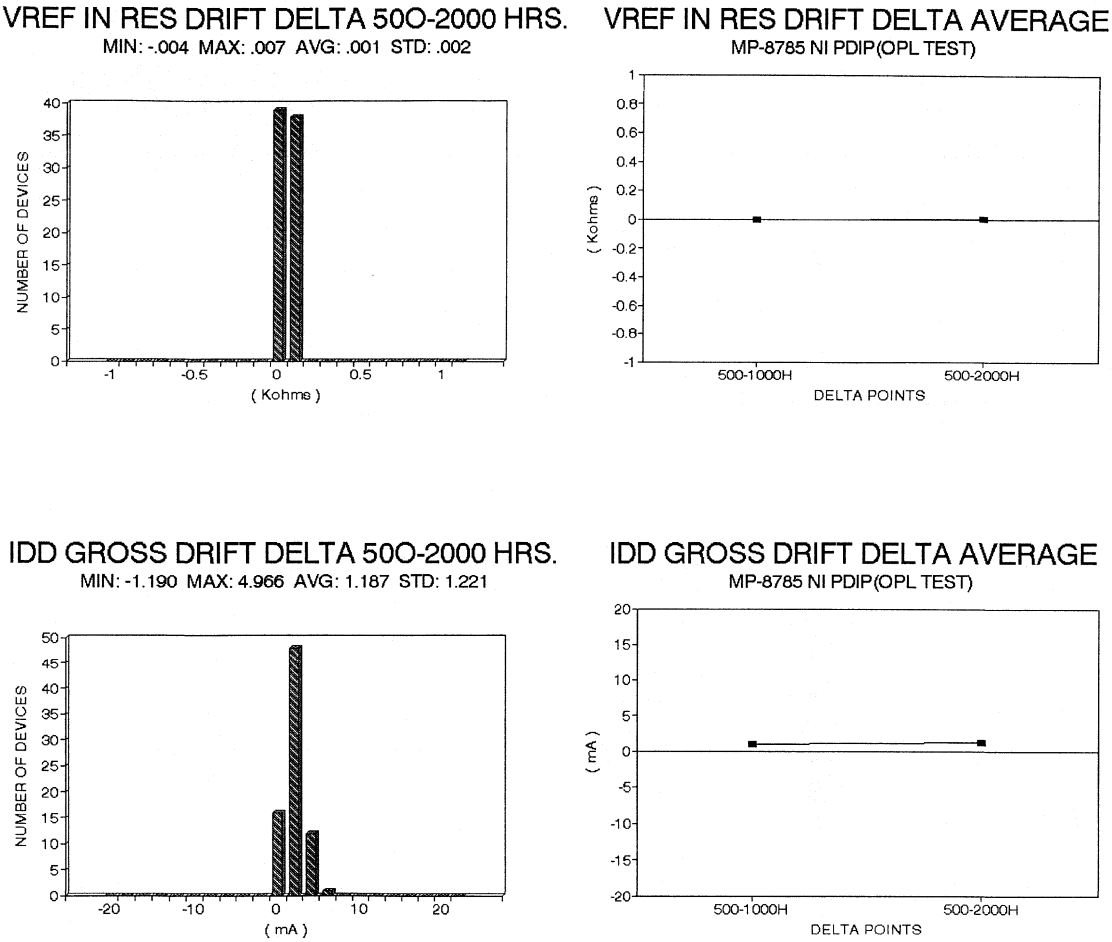
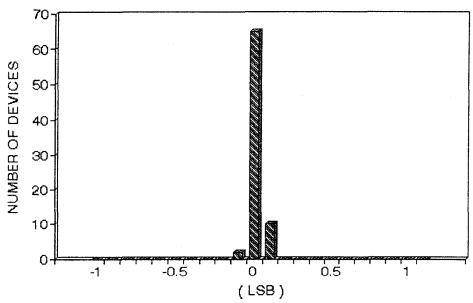


Figure 6.
MP8785 PDIP 2000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-021)

MP8785 8-Bit Video A/D Converter (Cont'd)

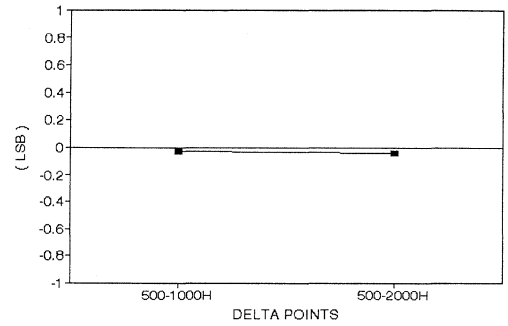
+INL DRIFT DELTA 50O-2000 HRS.

MIN: -.109 MAX: .076 AVG: -.042 STD: .037



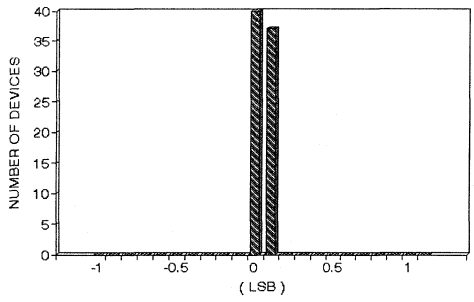
+INL DRIFT DELTA AVERAGE

MP-8785 NI PDIP(OPL TEST)



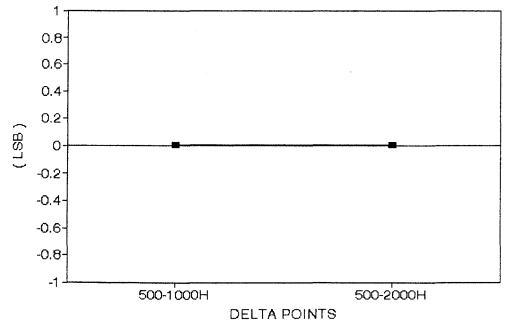
MAXIMUM DNL DRIFT DELTA 5O0-2000 HRS.

MIN: -.025 MAX: .025 AVG: .001 STD: .007



MAXIMUM DNL DRIFT DELTA AVERAGE

MP-8785 NI PDIP(OPL TEST)



MP8785 PDIP 2000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-021)

MP7626 16-Bit D/A Converter

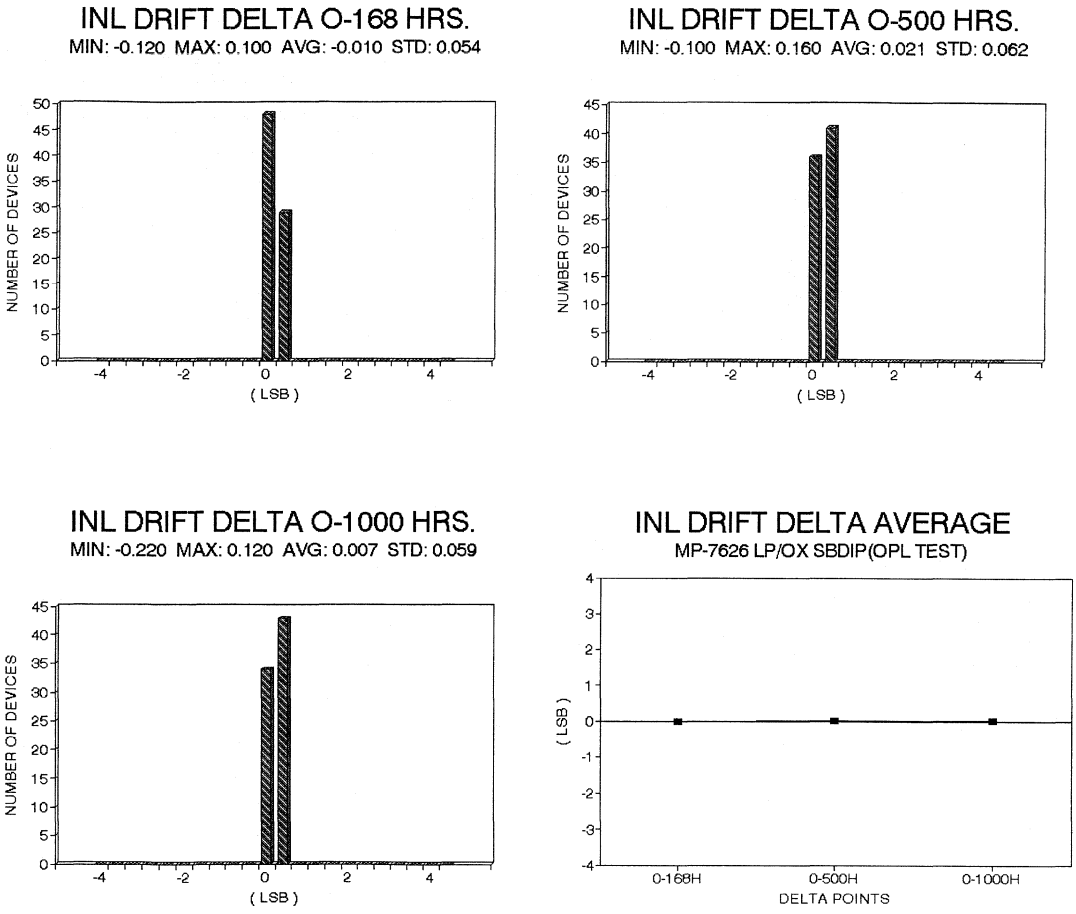
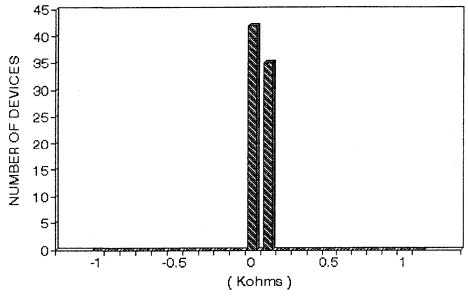


Figure 7.
MP7626 SBDIP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R91-008)

MP7626 16-Bit D/A Converter (Cont'd)

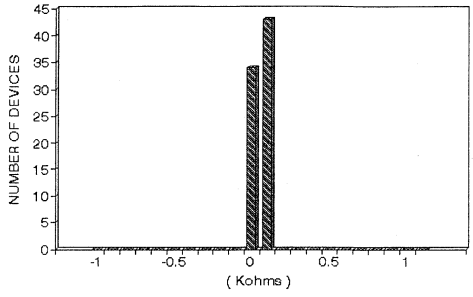
VREF IN RES DRIFT DELTA O-168 HRS.

MIN: -0.007 MAX: 0.007 AVG: -0.000 STD: 0.003



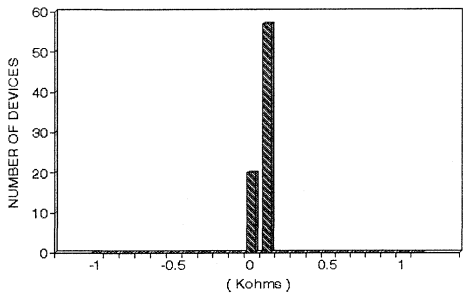
VREF IN RES DRIFT DELTA O-500 HRS.

MIN: -0.005 MAX: 0.009 AVG: 0.001 STD: 0.003



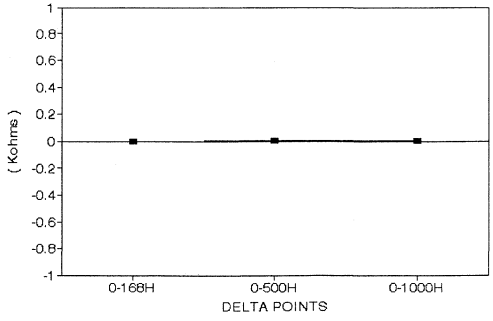
VREF IN RES DRIFT DELTA O-1000 HRS.

MIN: -0.007 MAX: 0.011 AVG: 0.003 STD: 0.004



VREF IN RES DRIFT DELTA AVERAGE

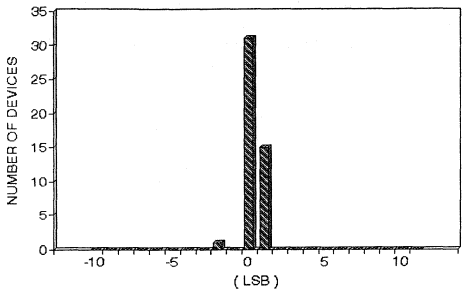
MP-7626 LP/OX SBDIP(OPL TEST)



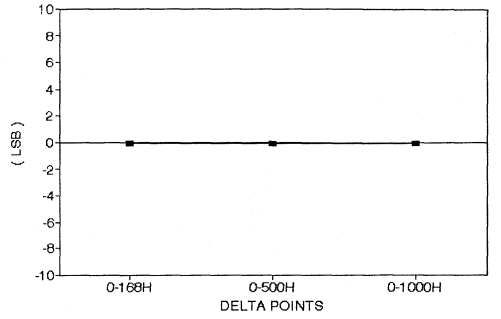
MP7626 SBDIP 1000 Hour Operating Life @ 125°C (Reference Reliability Report R91-008)

MP7613 Octal 12-Bit D/A Converter

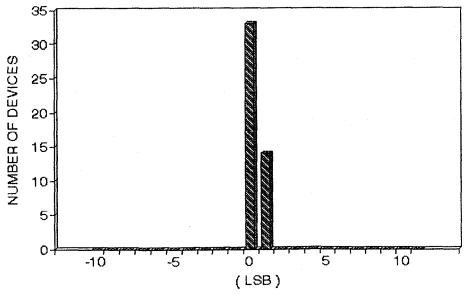
G. ERROR (D0) DRIFT DELTA O-1000 HRS.
MIN: -2.536 MAX: 0.648 AVG: -0.109 STD: 0.442



GAIN ERROR (D0) DRIFT DELTA AVERAGE
MP-7613 OX PQFP(OPL TEST)



G. ERROR (D1) DRIFT DELTA O-1000 HRS.
MIN: -0.824 MAX: 0.720 AVG: -0.040 STD: 0.277



GAIN ERROR (D1) DRIFT DELTA AVERAGE
MP-7613 OX PQFP(OPL TEST)

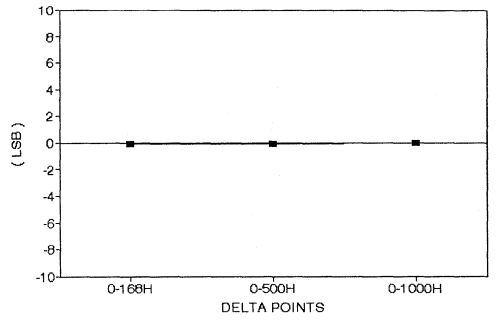
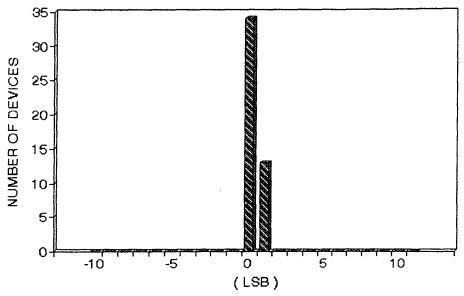


Figure 8.
MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7613 Octal 12-Bit D/A Converter (Cont'd)

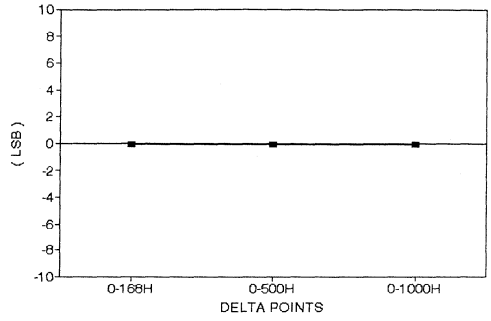
G. ERROR (D2) DRIFT DELTA O-1000 HRS.

MIN: -0.785 MAX: 0.727 AVG: -0.054 STD: 0.294



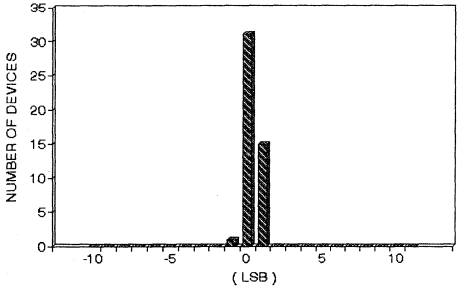
GAIN ERROR (D2) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)



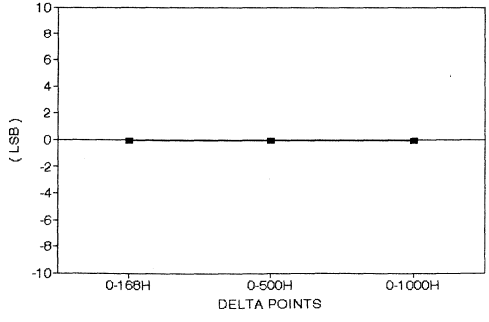
G. ERROR (D3) DRIFT DELTA O-1000 HRS.

MIN: -1.355 MAX: 0.781 AVG: -0.079 STD: 0.355



GAIN ERROR (D3) DRIFT DELTA AVERAGE

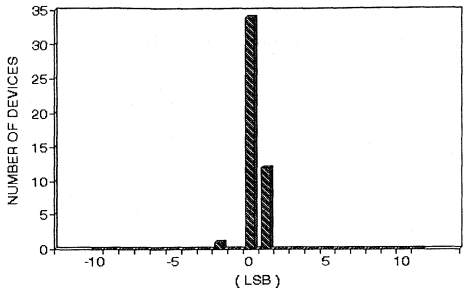
MP-7613 OX PQFP(OPL TEST)



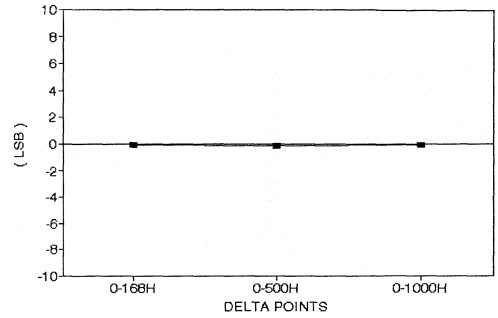
MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7613 Octal 12-Bit D/A Converter (Cont'd)

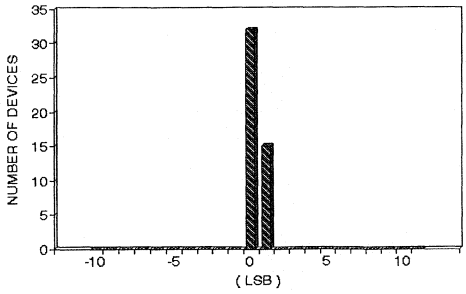
G. ERROR (D4) DRIFT DELTA O-1000 HRS.
MIN: -2.286 MAX: 0.765 AVG: -0.111 STD: 0.408



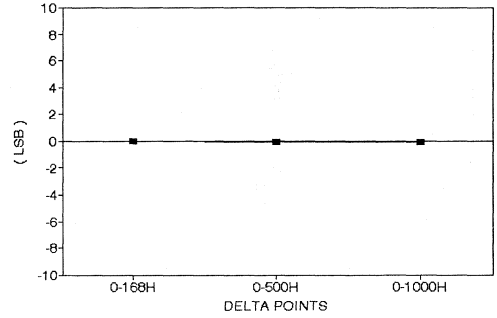
GAIN ERROR (D4) DRIFT DELTA AVERAGE
MP-7613 OX PQFP(OPL TEST)



G. ERROR (D5) DRIFT DELTA O-1000 HRS.
MIN: -0.744 MAX: 0.714 AVG: -0.062 STD: 0.264



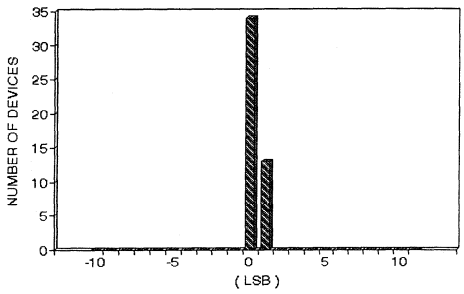
GAIN ERROR (D5) DRIFT DELTA AVERAGE
MP-7613 OX PQFP(OPL TEST)



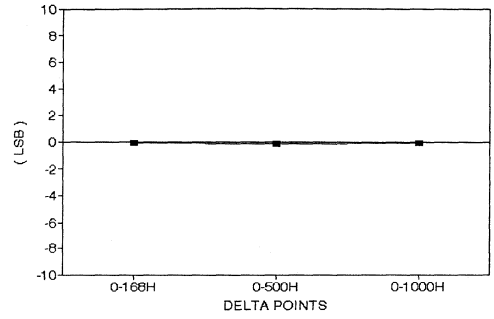
MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7613 Octal 12-Bit D/A Converter (Cont'd)

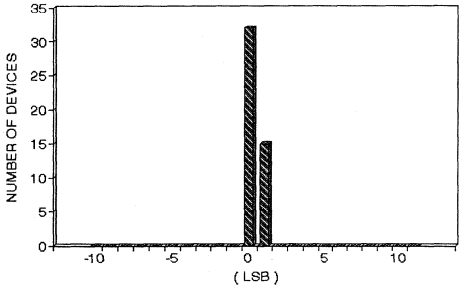
G. ERROR (D6) DRIFT DELTA O-1000 HRS.
MIN: -0.921 MAX: 0.481 AVG: -0.095 STD: 0.261



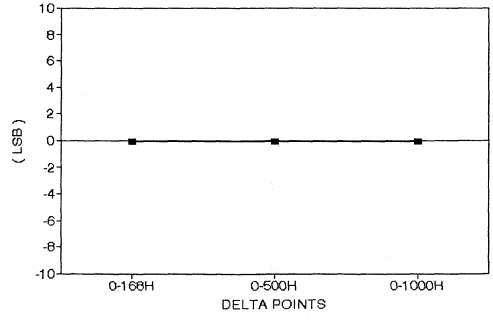
GAIN ERROR (D6) DRIFT DELTA AVERAGE
MP-7613 OX PQFP(OPL TEST)



G. ERROR (D7) DRIFT DELTA O-1000 HRS.
MIN: -0.756 MAX: 0.619 AVG: -0.076 STD: 0.275



GAIN ERROR (D7) DRIFT DELTA AVERAGE
MP-7613 OX PQFP(OPL TEST)

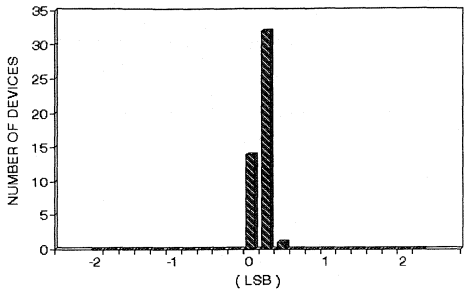


MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7613 Octal 12-Bit D/A Converter (Cont'd)

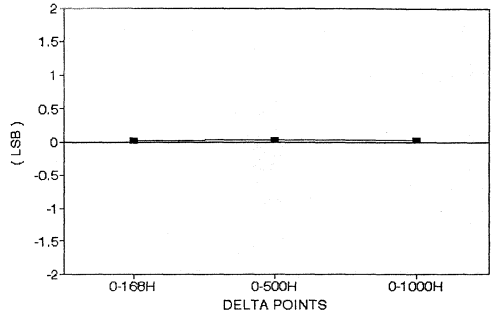
INL (D0) DRIFT DELTA O-1000 HRS.

MIN: -0.099 MAX: 0.216 AVG: 0.032 STD: 0.065



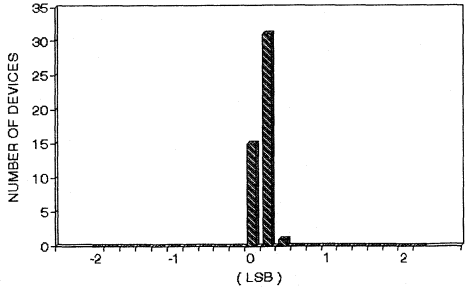
INL (D0) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)



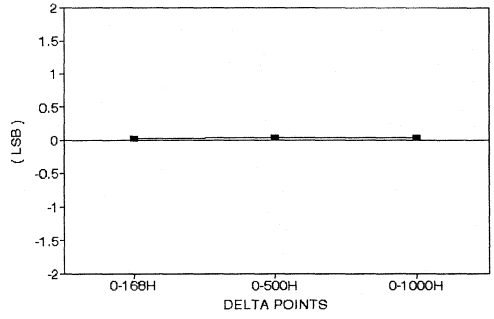
INL (D1) DRIFT DELTA O-1000 HRS.

MIN: -0.083 MAX: 0.213 AVG: 0.029 STD: 0.064



INL (D1) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)

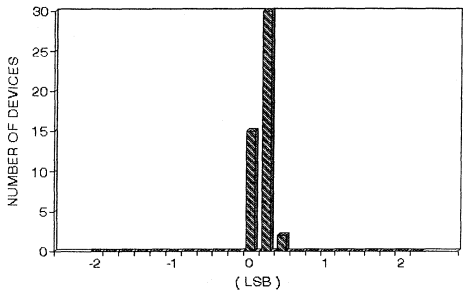


MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7613 Octal 12-Bit D/A Converter (Cont'd)

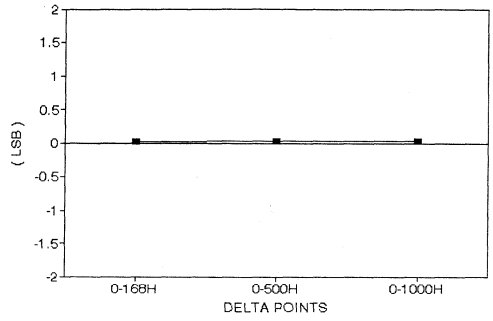
INL (D2) DRIFT DELTA O-1000 HRS.

MIN: -0.056 MAX: 0.217 AVG: 0.033 STD: 0.061



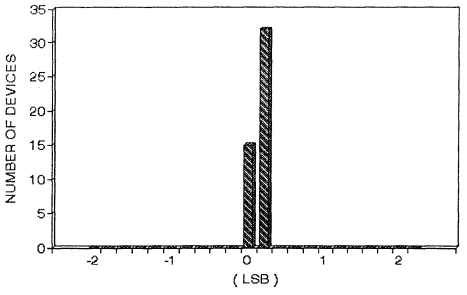
INL (D2) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)



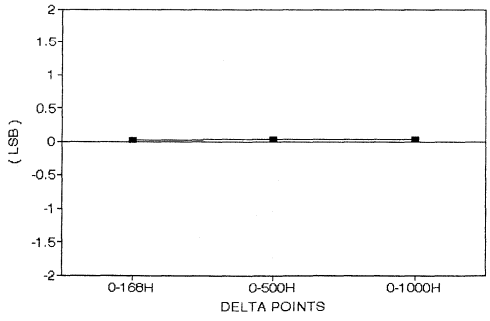
INL (D3) DRIFT DELTA O-1000 HRS.

MIN: -0.072 MAX: 0.194 AVG: 0.030 STD: 0.061



INL (D3) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)

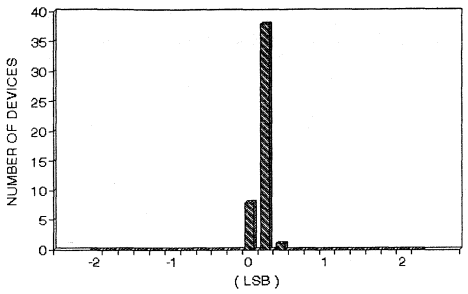


MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7613 Octal 12-Bit D/A Converter (Cont'd)

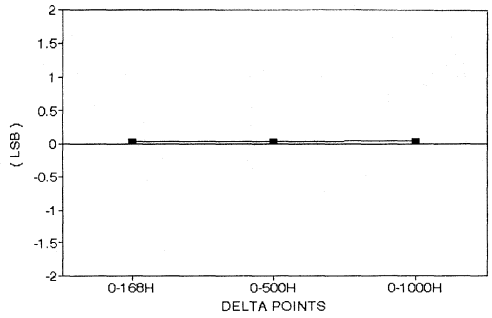
INL (D4) DRIFT DELTA O-1000 HRS.

MIN: -0.082 MAX: 0.204 AVG: 0.041 STD: 0.053



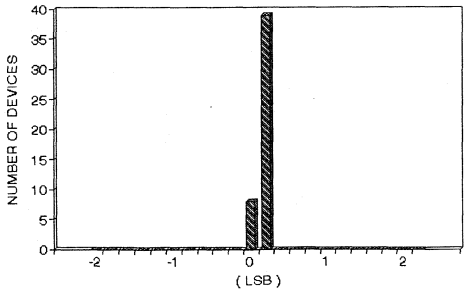
INL (D4) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)



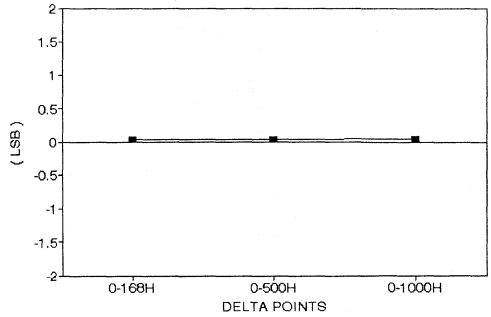
INL (D5) DRIFT DELTA O-1000 HRS.

MIN: -0.045 MAX: 0.190 AVG: 0.044 STD: 0.051



INL (D5) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)

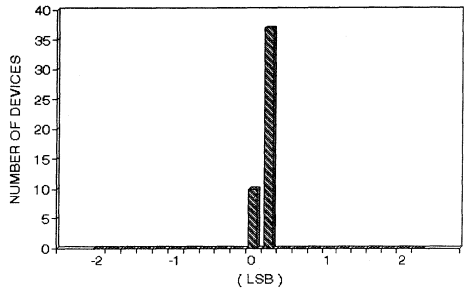


MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7613 Octal 12-Bit D/A Converter (Cont'd)

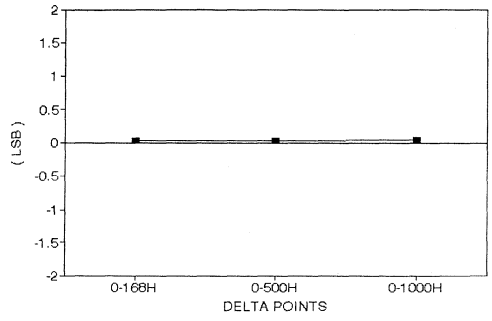
INL (D6) DRIFT DELTA O-1000 HRS.

MIN: -0.052 MAX: 0.197 AVG: 0.044 STD: 0.053



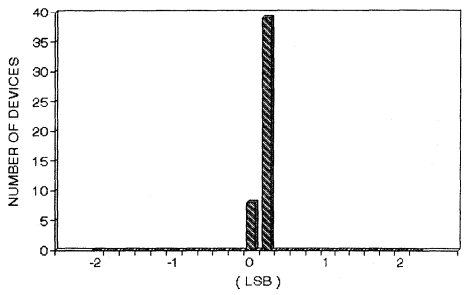
INL (D6) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)



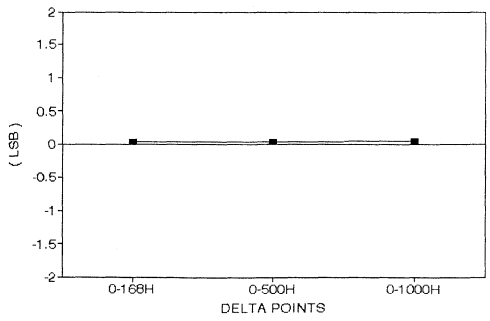
INL (D7) DRIFT DELTA O-1000 HRS.

MIN: -0.073 MAX: 0.189 AVG: 0.043 STD: 0.052



INL (D7) DRIFT DELTA AVERAGE

MP-7613 OX PQFP(OPL TEST)



MP7613 PQFP 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R92-001)

MP7695 10-Bit A/D Converter

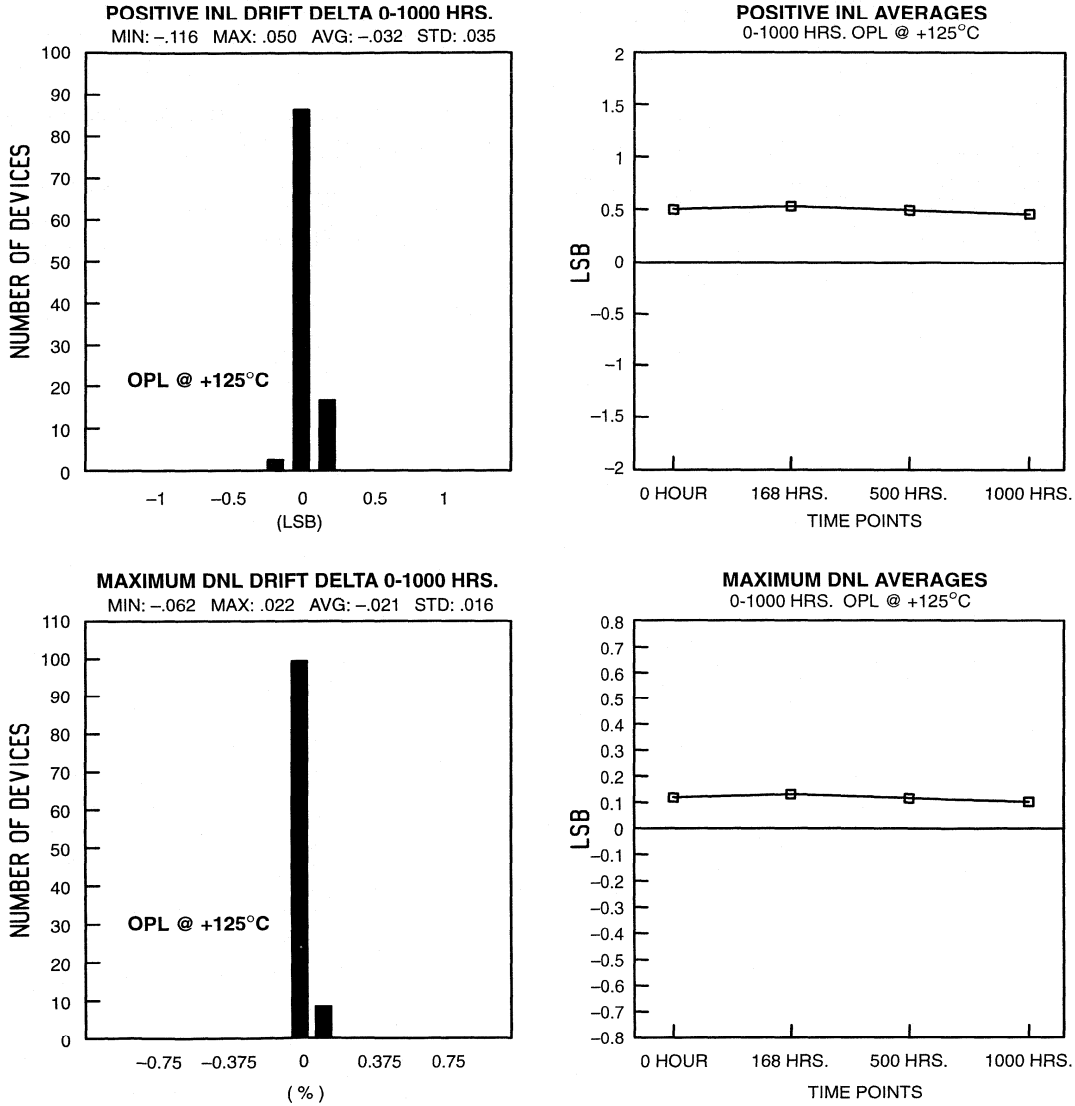


Figure 9.
MP7695 Cerdip 1000 Hour Operating Life @ 125°C
(Reference Reliability Report R90-015)

AFTERWORD

If you have questions or feedback about our process or Q & R procedures, we want to hear from you. Please call or write directly to the office of the Director of Quality.

RESOURCES AVAILABLE

- A comprehensive 25-page personnel ESD awareness and training manual has been developed by the EXAR Training Department, and is available upon request to EXAR customers (Part No. EXARAN23).
- A Quality Manual, quality data, test results, and data from reliability monitors are also available upon request.

REFERENCES

G. Box, W. Hunter, J. Hunter, "Statistics for Experimenters," John Wiley & Sons, 1978.

D. Wheeler, D. Chambers, "Understanding Statistical Process Control," Statistical Process Controls Inc., 1986.

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Section 3

Analog-to-Digital Converters

Listed Alpha-Numerically

Analog-to-Digital Converters

12-Bit Analog-to-Digital Converters

# of Channels \ MSPS	<100kHz	<1MHz	≥1MHz
1		MP87091 MP87092 MP87L92	MP87L91 MP8790 MP8791
16	MP3276 MP3275		
32	MP3274		

10-Bit Analog-to-Digital Converters

# of Channels \ MSPS	250K	750K	1M	≤2M	5M
1	MP87L95	MP87095	MP7695 MP8795 MP8796	MP87L84 MP87L82	MP8784 MP8782
4	MP87L98		MP8799 MP87198	MP8798	
8	MP87L99	MP87099	MP8799		

8-Bit Analog-to-Digital Converters

# of Channels \ MSPS	≤3	5	10	≤15	20	30
1	MP7683 MP7693 MP7783	MP76L90	MP7684 MP7690 MP87L85 MP87L75 MP87L76	MP8780 MP7690A MP7684A	MP8785 MP8775	MP8786 MP8776
8	MP8820*					

*Preliminary

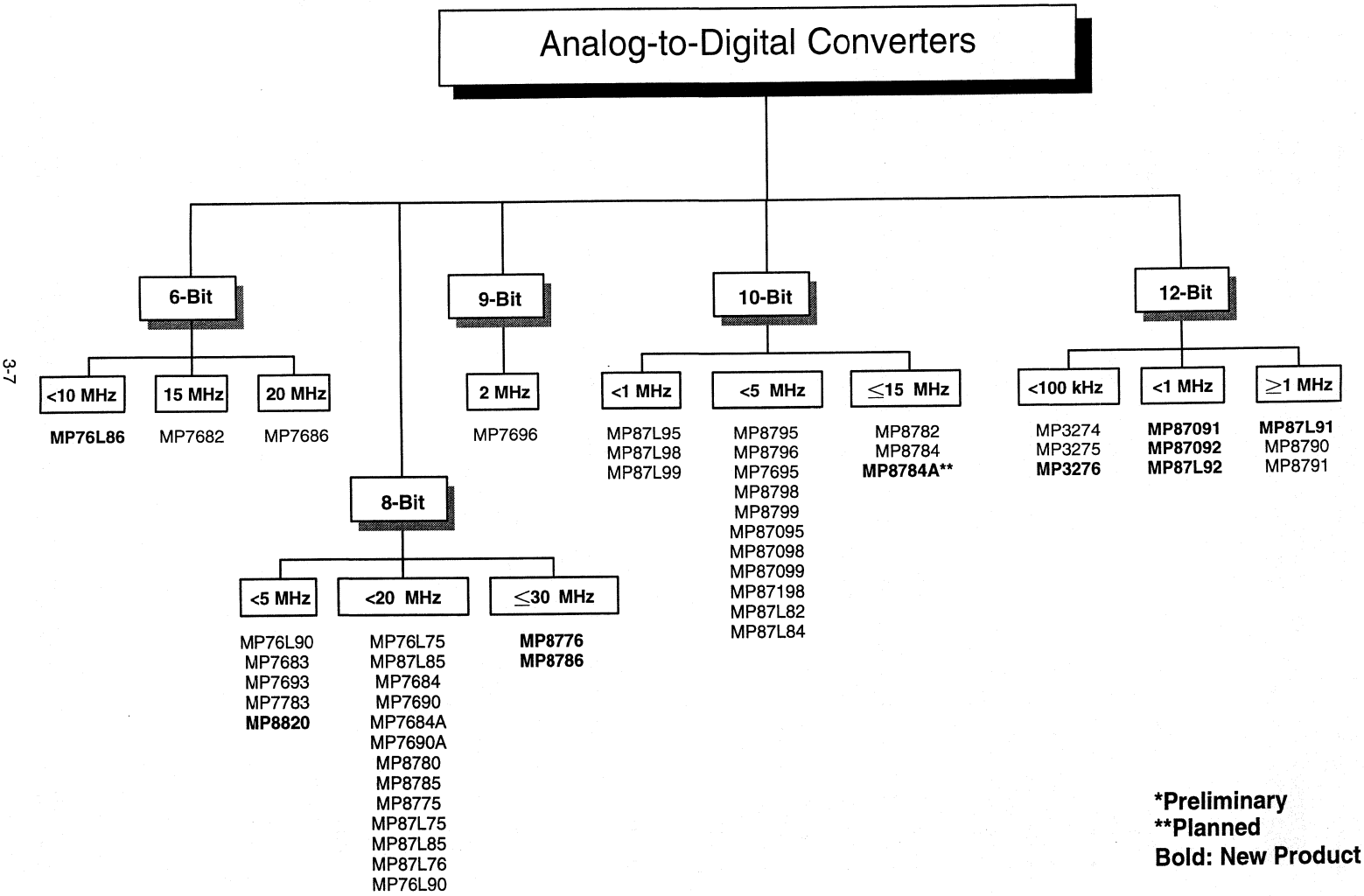
EXAR Corporation

Analog-to-Digital Converter Overview

Part No.	Resolution (Bits)	Speed	Max Power	# Chan.	Track/ Hold	V_{REF} Range	µP Bus P–Parallel S–Serial	Pkg
MP8790	12	2 MSPS	225	1	Y	1 to 5 V	12, P/S	PQFP
MP8791	12	2 MSPS	225	1	Y	1 to 5 V	12, P	PDIP, SOIC
MP3274	12	15µS	200	32	Y	4 V	8/12, µP, P/S	PGA, PLCC
MP3275	12	15µS	200	16	Y	4 V	S	PQFP
MP3276	12	15µS	200	16	Y	4 V	8/12, µP, P/S	PGA, PLCC
MP87091	12	750 KSPS	225	1	Y	1 to 5 V	12, P	PDIP, SOIC
MP87092	12	750 KSPS	225	1	Y	1 to 5 V	S	PDIP, SOIC
MP8782	10	5 MSPS	200	1	Y	1 to 5 V	10, P	PQFP
MP8784	10	5 MSPS	200	1	Y	1 to 5 V	10, P	PDIP, SOIC
**MP8784A	10	15 MSPS	200	1	Y	1 to 5 V	10, P	PDIP, SOIC
MP7695	10	1 MSPS	60	1	Y	1 to 5 V	10, P	PDIP, CDIP, SOIC
MP8795	10	1 MSPS	50	1	Y	1 to 5 V	10, P	PDIP, SOIC
MP8796	10	1 MSPS	50	1	Y	1 to 5 V	10, P	SOIC
MP8798	10	1 MSPS	50	4	Y	1 to 5 V	10, P	PDIP, SOIC, SSOP
MP8799	10	1 MSPS	50	8	Y	1 to 5 V	10, P	PQFP
MP87198	10	1 MSPS	50	4	Y	1 to 5 V	10, P	PDIP, SOIC, SSOP
MP87095	10	750 KSPS	50	1	Y	1 to 5 V	10, P	PDIP, SOIC
MP87098	10	750 KSPS	50	4	Y	1 to 5 V	10, P	PDIP, SOIC, SSOP
MP87099	10	750 KSPS	50	8	Y	1 to 5 V	10, P	PQFP
MP7696	9	2 MSPS	50	1	Y	1 to 5 V	9, P	PDIP, SOIC
MP8775	8	20 MSPS	125	1	Y	1 to 5 V	8, P	PDIP, SOIC, SSOP
MP8776	8	20 MSPS	150	1	Y	1 to 5 V	8, P	PDIP, SOIC, SSOP
MP8785	8	20 MSPS	125	1	Y	1 to 5 V	8, P	SOIC, PDIP
MP8786	8	20 MSPS	150	1	Y	1 to 5 V	8, P	SOIC, PDIP, SSOP
MP8780	8	15 MSPS	425	1	Y	1 to 5 V	8, P	PDIP, SOIC
MP7684A	8	14 MSPS	425	1	Y	1 to 5 V	8, P	PDIP, CDIP, SOIC
MP7690A	8	14 MSPS	425	1	Y	1 to 5 V	8, P	CDIP
MP7684	8	10 MSPS	450	1	Y	1 to 5 V	8, P	PDIP, CDIP, SOIC
MP7690	8	10 MSPS	450	1	Y	1 to 5 V	8, P	CDIP
MP7683	8	3 MSPS	180	1	Y	1 to 5 V	8, P	PDIP, CDIP, SOIC, SSOP
MP7693	8	3 MSPS	180	1	Y	1 to 5 V	8, P	PDIP, SOIC, PLCC
MP7783	8	2.5 MSPS	180	1	Y	1 to 5 V	8, P	PDIP, SOIC
MP8820	8	1.6 MSPS	225	8	Y	0.5 to 1.5 V	µP, P	SOIC, SSOP
MP7686	6	20 MSPS	200	1	Y	1 to 5 V	6, P	PDIP, CDIP, SOIC
MP7682	6	15 MSPS	250	1	Y	1 to 5 V	6, P	PDIP, CDIP, SOIC, LCC

Analog-to-Digital Converters with Gain and Offset Control

Part No.	Resolution (Bits)	Speed	Max Power	# Chan.	Track /Hold	Gain Control (Bits)	Offset Control (Bits)	V_{REF} Range	µP Bus P–Parallel S–Serial	Pkg
MP8830	10	1.25 MSPS	700	3***	Y	9	6	1 V	P	PQFP
**MP8831	10	1.25 MSPS	250	1	Y	9	6	1 V	P	SOIC



***Preliminary**
****Planned**
Bold: New Product

New Product Highlights

Analog-to-Digital Converters

MP3276
Fault Protected 16 Channel, 12-Bit Data Acquisition Subsystem

- Fault Protected 16-Channel 12-Bit A/D Converter with Sample & Hold, Reference, Clock and Tri-State Outputs
- Fast Conversion, less than 15µS
- 2's Complement Data Output, Parallel or Serial Data Output Modes
- Remote Analog Ground Sensing
- Overvoltage Protected Input (±50 V over the Supply Voltages)
- Guaranteed Performance at +12/–5 V, ±12 & ±15 V
- Low Power: 110 mW typ. (7 mW per Channel typ.)
- 32 Channel Version: MP3274

MP8776
30 MSPS, 8-Bit High Speed, Low Power Analog-to-Digital Converter with Power Down

- 8-Bit Resolution, DNL = ±1/4 LSB, INL = ±1/2 LSB (typ)
- Sampling Rate to 30 MHz
- Low Power: 110 mW typ. (excluding reference)
- Power Down Mode: 100µA (typ)
- Internal S/H Function
- Rail-to-Rail Input Range
- Latch-Up Free
- ESD Protection: 2000 V Minimum
- 3 State Digital Outputs

MP8786
30 MSPS, 8-Bit High Speed, Low Power Analog-to-Digital Converter with Power Down

- 8-Bit Resolution, DNL = ±1/4 LSB, INL = ±1/2 LSB (typ)
- Sampling Rate to 30 MHz
- Low Power: 110 mW typ. (excluding reference)
- Power Down Mode: 100µA (typ)
- Internal S/H Function
- Rail-to-Rail Input Range
- Latch-Up Free
- ESD Protection: 2000 V Minimum
- 3 State Digital Outputs

MP87091
750 KSPS, 12-Bit Analog-to-Digital Converter with Parallel Logic Interface Port

- 12-Bit Monotonic ADC, DNL = ±1 LSB, INL = ±2 LSB
- SNR > 66 dB
- Sampling Frequency ≤ 750 kHz
- Internal Track and Hold
- V_{REF} Range: 1.5 V to V_{DD} with Rail-to-Rail Input Range
- CMOS Low Power: 175 mW (typ)
- 1/4, 1/2 and 3/4 Scale Reference Resistor Taps
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode
- Latch-Up Free

New A/D Converter Highlights

MP87092
750 KSPS, 12-Bit Analog-to-Digital Converter with Serial Logic Interface Port

- 12-Bit Monotonic ADC with DNL = ±1 LSB, INL = ±2 LSB
- SNR > 66 dB
- Sampling Frequency ≤ 750 kHz
- Internal Track and Hold
- V_{REF} Range: 1.5 V to V_{DD} with Rail-to-Rail Input Range
- CMOS Low Power: 175 mW (typ)
- Binary and Two's Complement Digital Output Mode, Serial Port
- Underflow and Precision Aperture Outputs
- Latch-Up Free

*MP8820
7-Bit Plus Sign Analog-to-Digital Converter with an 8-Channel MUX

- Precision 7–Bit Plus Sign ADC with 8 Channel Analog Mux, DNL= ±1/2 LSB, INL=± 1 LSB
- Sampling Rate to 1.6 MHz
- Buffered Reference Input
- Unipolar to Bipolar Reference Translation
- Low Power: 75 mW (typ)
- ESD Protection: 2000 V (min)

MP8830
Triple 10-bit High Speed Analog-to-Digital Converter with Digitally Controlled References

- 3 Independent 10-bit ADCs
- Simultaneous Sampling @ 1.25 MSPS
- Independent Digitally Controlled References with 9-bit Positive Reference and 6-bit Negative Reference Adjustment per Sample
- Internal Track and Hold
- Fast Mode for OCR
- Black Level Clamp
- Latch-Up Free
- Low Power: 500mW (typ)
- ESD Protection: 2000 V Minimum

*MP8831
10-Bit High Speed Analog-to-Digital Converter with Digitally Controlled References

- 10-bit ADC with DNL < ±0.75 LSB
- 1.25 MHz Sampling Rate
- Independent Digitally Controlled References with 9-bit Positive and Negative Reference Adjustment per Sample
- Low Power CMOS: 180 mW (typical) with Power Down Mode (less than 100 µA)
- Latch-up Free
- ESD Protection: 2000V Minimum

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FEATURES

- **Complete 32-Channel 12-Bit A/D Converter with Sample & Hold, Reference, Clock and 3-State Outputs**
- **Fast Conversion, less than 15μS**
- **Microprocessor Bus Interface**
- **Parallel or Serial Data Output Modes**
- **65 ns Bus Access Time**
- **Remote Analog Ground Sensing**
- **Overvoltage Protected Input (±50 V over the Supply Voltages)**
- **Precision Reference for Long Term Stability and Low Gain T.C.**
- **Guaranteed Linearity Over Temperature**
- **Guaranteed Performance at +12/–5 V, ±12 & ±15 V**
- **Low Power (3 mW per Channel Typical)**
- **16 Channel Version: MP3276 & MP3275**

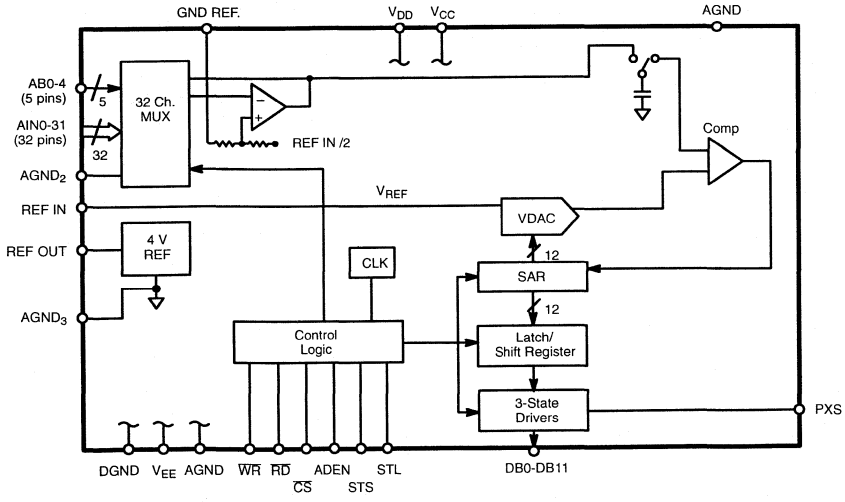
GENERAL DESCRIPTION

The MP3274 is a complete 32-channel, 12-bit Data Acquisition Subsystem with 3-state output buffers for direct interfacing to 16-bit microprocessor buses. Implemented using an advanced BiCMOS process, the converter combines a 32-channel passive overvoltage protected multiplexer instrumentation amp, a sample & hold, a SAR, a 12-bit decoded D/A, a comparator, a precision reference and the control logic to achieve an accurate, repeated conversion in less than 15μs, and a mux/instrumentation amp settling period of less than 10μs.

A unique input design provides input overvoltage protection to ±50 V over the supply voltages. Therefore, an overvoltage condition can exist on unselected channels without disrupting the measured channel or operation of the MP3274! The internal 4 V reference has sufficient output current to provide other system reference needs. Precision thin film scaling and offset resistors are laser trimmed to provide for less than 2 LSB INL for ±10 V inputs on all channels.

In addition, the MP3274 will output either full scale (0111 ....) for overrange and – full scale (1000....) for underrange conditions. This greatly simplifies microprocessor software development.

SIMPLIFIED BLOCK DIAGRAM

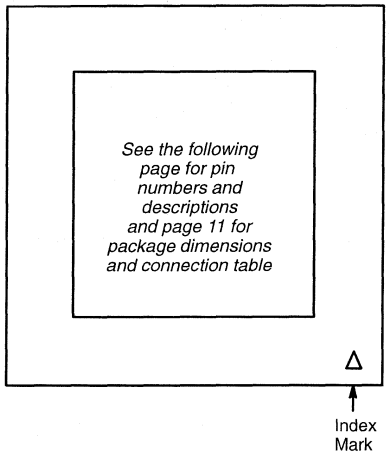


ORDERING INFORMATION

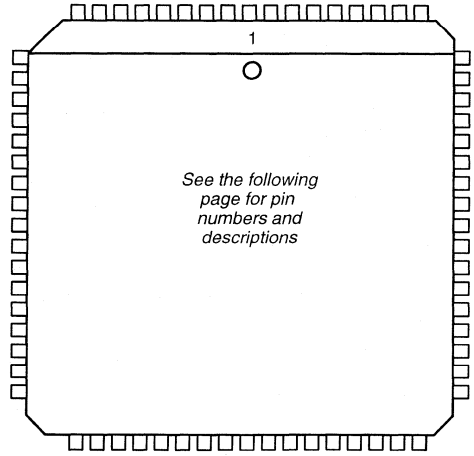
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PGA	–40 to +85°C	MP3274AG	±2	±2
PGA	–55 to +125°C	MP3274SG*	±2	±2
PLCC	–40 to +85°C	MP3274AP	±2	±2

*Contact factory for non-compliant military processing

PIN CONFIGURATIONS



68 Pin PGA
G68



68 Pin PLCC
P68

PIN OUT DEFINITIONS

PLCC PIN NO.	PGA PADS	NAME	DESCRIPTION
61	1	V_{EE}	Negative Analog Supply
62	2	$A_{IN}24$	Analog Input 24
63	3	$A_{IN}25$	Analog Input 25
64	4	$A_{IN}26$	Analog Input 26
65	5	$A_{IN}27$	Analog Input 27
66	6	$A_{IN}28$	Analog Input 28
67	7	$A_{IN}29$	Analog Input 29
68	8	$A_{IN}30$	Analog Input 30
1	9	$A_{IN}31$	Analog Input 31
2	10	GND Ref.	Input Ground Reference
3	11	AGND	ADC Analog Ground
4	12	Ref In	Reference Input
5	13	Ref Out	Reference Output
6	14	AGND3	Reference Analog Ground
7	15	DGND	Digital Ground
8	16	DB0/SDC	Data Output Bit 0/Serial Data Clock
9	17	N/C	No Connection
10	18	DB1	Data Output Bit 1
11	19	DB2	Data Output Bit 2
12	20	DB3	Data Output Bit 3
13	21	DB4	Data Output Bit 4
14	22	DB5	Data Output Bit 5
15	23	DB6	Data Output Bit 6
16	24	DB7	Data Output Bit 7
17	25	DB8	Data Output Bit 8
18	26	DB9	Data Output Bit 9
19	27	DB10	Data Output Bit 10
20	28	DB11/SDO	Data Output Bit 11/Serial Data Out
21	29	STS	Conversion Status
22	30	STL	Mux Settling Status
23	31	PXS	Parallel/XSerial
24	32	$\overline{RD}$	Read Enable
25	33	$\overline{CS}$	Chip Select
26	34	$\overline{WR}$	Write Enable

PLCC PIN NO.	PGA PADS	NAME	DESCRIPTION
27	35	ADEN	Address Enable
28	36	AB4	Channel Address 4
29	37	AB3	Channel Address 3
30	38	AB2	Channel Address 2
31	39	AB1	Channel Address 1
32	40	AB0	Channel Address 0
33	41	V_{DD}	Positive Digital Supply
34	42	V_{CC}	Positive Analog Supply
35	43	$A_{IN}0$	Analog Input 0
36	44	$A_{IN}1$	Analog Input 1
37	45	$A_{IN}2$	Analog Input 2
38	46	$A_{IN}3$	Analog Input 3
39	47	$A_{IN}4$	Analog Input 4
40	48	$A_{IN}5$	Analog Input 5
41	49	$A_{IN}6$	Analog Input 6
42	50	$A_{IN}7$	Analog Input 7
43	51	N/C	No Connection
44	52	$A_{IN}8$	Analog Input 8
45	53	$A_{IN}9$	Analog Input 9
46	54	$A_{IN}10$	Analog Input 10
47	55	$A_{IN}11$	Analog Input 11
48	56	$A_{IN}12$	Analog Input 12
49	57	$A_{IN}13$	Analog Input 13
50	58	$A_{IN}14$	Analog Input 14
51	59	$A_{IN}15$	Analog Input 15
52	60	AGND2	Analog Ground Mux Return
53	61	$A_{IN}16$	Analog Input 16
54	62	$A_{IN}17$	Analog Input 17
55	63	$A_{IN}18$	Analog Input 18
56	64	$A_{IN}19$	Analog Input 19
57	65	$A_{IN}20$	Analog Input 20
58	66	$A_{IN}21$	Analog Input 21
59	67	$A_{IN}22$	Analog Input 22
60	68	$A_{IN}23$	Analog Input 23

3

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, V_{CC} = 15 V, V_{EE} = −15 V, GNDRef = 0 V, T_A = 25°C, V_{REF}IN = Ref Out

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
Resolution (All Grades)	N	12			12			Bits
KEY FEATURES								
Resolution			12			12	Bits	
Conversion Time, Per Channel	t_{CONVR}			15		15	µs	
ACCURACY (A, S Grade)[1]								
Differential Non-Linearity	DNL		3/4	2		2	LSB	
Integral Non-Linearity	INL		1	2		2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Code Error	EZS		2	±5		±10	LSB	fff to 000 [hex] transition
Full Scale Error	EFS		0.1	±0.35		±0.5	%	V_{REF}IN = 4.000 V
POWER SUPPLY REJECTION								Max change in Full Scale Calibration
V_{CC} = 15 V ±1.5 V or 12 V ±0.6 V				±1		±1	LSB	
V_{DD} = 5 V ±0.25 V				±2		±2.5	LSB	
V_{EE} = −15 V ±1.5 V or −12 V ±0.6 V or −5 V ±0.25 V				±1		±1	LSB	
REFERENCE VOLTAGES								
Ref. Voltage Input	Ref In	3.6		4.4			V	R_{IN} ≃5KΩ; V_{DD} = 5 V
Ref. Voltage Output	Ref Out	3.975		4.025				
Ref. Source Current		3.0	4.0		3.0		mA	
Ref. Sink Current			20				µA	
ANALOG INPUT[2]								
Input Voltage Range[5]	V_{IN}	−10		10	−10	10	V	
Ground Reference	GND Ref.							
CM Range		−3		3	−3	3	V	
CM RR			TBD				LSB/V	
Input Resistance	R_{IN}	100	130		100		kΩ	
Input Capacitance	C_{IN}		5				pF	
Aperture Delay	t_{AP}		180				ns	From $\overline{WR}$ low to high after STL high to low
Channel-to-Channel Isolation[2]			−80	−70			dB	DC
DIGITAL INPUTS $\overline{CS}$, $\overline{WR}$, RD AB0-AB4, ADEN								
Logical "1" Voltage	V_{IH}	2.4		5.5	2.4	5.5	V	
Logical "0" Voltage	V_{IL}	−0.5		0.8	−0.5	0.8	V	
Leakage Currents[6]	I_{IN}	−5		5	−10	10	µA	V_{IN}=GND to V_{DD}
Input Capacitance[2]			5				pF	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL OUTPUTS (Data Format 2's Complement) DB0/SDC–DB11/SDO, STS, STL								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.0			2.4		V	I_{SOURCE} = 0.5 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{SINK} = 1.6 mA
Tristate Leakage	I_{OZ}	–5		5	–5	5	µA	V_{OUT}=GND to V_{DD}
POWER SUPPLIES								
Operating Range								
V_{DD}		+4.5		+5.5	+4.5	+5.5	V	
V_{CC}		+11.4		+16.5	+11.4	+16.5	V	
V_{EE}		–4.75		–16.5	–4.75	–16.5	V	Tested at –11.4 and –16.5 only
Operating Current								
I_{DD}			2	7		7	mA	
I_{CC}			5	8		8	mA	
I_{EE}			1.5	3		3	mA	
Power Dissipation			110	200		200	mW	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 Input bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 All channel input pins and ground reference pin have protection which becomes active above ±60 V.

6 All digital inputs have diodes to V_{DD} and AGND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{CC} to DGND ..... 0 to +16.5 V

V_{EE} to DGND ..... 0 to –16.5 V

V_{DD} to DGND ..... 0 to +7 V

AGND to DGND ..... ±1 V

Digital Inputs/Outputs to DGND ..... –0.5 V to V_{LOGIC} +0.5 V

Analog Inputs ($A_{IN}0$ – $A_{IN}31$, GND REF) to AGND ..... ±60 V

REF OUT ..... Indefinite short to DGND, Momentary short to V_{CC}

Maximum Junction Temperature ..... 150°C

Package Power Dissipation Rating to 75°C

PGA, PLCC ..... 1800 mW

Derates above 75°C ..... 25 mW/°C

Lead Temperature, Soldering ..... 300°C, 10 Sec

Storage Temperature (Ceramic) ..... –65°C to +150°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All logic inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

Basic Description

The MP3274 is a fault protected data acquisition subsystem available in monolithic form. This product contains all of the circuitry necessary to acquire 32 channels of differential or single-ended analog signals at ±10 V input range and 15kHz bandwidth. Connections to power, the analog input signals and the digital system are all that is required. The MP3274's input circuitry is protected against active input signals present with the MP3274 power off. This is also the case for any channel exceeding the MP3274 analog input dynamic range without interfering with the channel being digitized. The channel address and channel conversion can be managed in two ways: random channel conversion or same channel conversion. Circuitry on the chip adds a MUX/instrumentation amp settling delay, when a new channel is selected (ADEN = 1). Conversion start is initiated without delay for the single-channel case (ADEN = 0). Data is available in either parallel or serial format.

TIMING

Control and Timing Considerations – Parallel Mode (PXS = 1)

The MP3274 can be operated in the stand-alone mode, with one line for control and everything else hard-wired; or under microprocessor control, where changes can be made dynamically. There are 4 control lines: ADEN, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ with their functions described in *Table 1.*

PXS is the control pin for formatting data for serial or parallel control.

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	Comments
ADC Channel Select and Start Convert *(See Figure 1. and Table 2.)*							
1	X	X	X	—	0	0	No operation
0	↓	1	0	Hi-Z	0	0	No operation if ADEN = 0
0	↓	1	1	Hi-Z	↑	0	Input MUX channel selected, STL set on $\overline{WR}$ falling edge
0	0	1	X	Hi-Z	1	0	MUX select disabled
0	↑	1	X	Hi-Z	0	↑	Start convert on $\overline{WR}$ rising edge
0	1	1	X	Hi-Z	↓	↑	Start convert on STL falling edge
0	1	1	X	Hi-Z	0	↓	STS goes low at end of conversion
Read ADC Data – Parallel Output Mode (PXS = 1) *(See Figure 2. and Table 3.)*							
0	1	↓	X	—	0	0	Data outputs enabled
0	X	0	X	ADC	0	0	Data from previous conversion on data bus
0	X	↑	X	Hi-Z	0	0	Data outputs disabled
0	1	X	X	Hi-Z	0	1	Data/$\overline{RD}$ disabled while STS high
0	X	0	X	Last ADC	1	0	Data from last conversion on data bus
0	⊓	0	0	Hi-Z	0	↑	STL, MUX select disabled with ADEN = 0, data outputs disabled on STS rising edge
0	⊓	0	X	ADC	0	↓	New data appears on data bus on falling edge of STS

Note 1: If $\overline{RD}$ = 1, data outputs remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the data bus.

Table 1. Logic Truth Table for PXS = 1 (Parallel Mode)

The MP3274 is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the MP3274 control signals will provide the system designer with useful insight into the operation of the device.

Figure 1. shows a complete timing diagram for the MP3274 convert start operation.

Either $\overline{WR}$ or $\overline{CS}$ may be used to initiate a conversion. We recommend using $\overline{WR}$ as used in *Figure 1.* It is quieter and has less propagation delay than $\overline{CS}$. If $\overline{CS}$ is used to trigger the conversion the specified set-up times will be longer.

A conversion is started by taking $\overline{WR}$ low, then high again (conversion is enabled on the rising edge of $\overline{WR}$). There are two possible conditions that will affect conversion timing.

1. ADEN = 1. At the falling edge of $\overline{WR}$, the input channel is determined by the data present on the address bits. The track and hold begins to settle after which STL returns low, indicating that the multiplexer and the buffer amp have settled to less than 1/2 LSB of final value. If the rising edge of $\overline{WR}$ returns high prior to STL going low, conversion will begin on the falling edge of STL. If the rising edge of $\overline{WR}$ is delayed until after STL returns low, the input signal is sampled and the conversion is started at the rising edge of $\overline{WR}$ giving the user better control of the sampling time.
2. ADEN = 0. At the falling edge of $\overline{WR}$ the data present at the address is ignored and the channel selected during the previous conversion remains selected. In this case the track and hold settling time is omitted and STL never goes high. At the rising edge of $\overline{WR}$ the input signal is sampled, and conversion is started.

There are two possible states that the data outputs could be in during a conversion.

1. If $\overline{RD}$ is held high during a conversion the outputs would remain high impedance throughout the conversion. This is the preferred method of operation as any noise present on the data bus is rejected.
2. If $\overline{RD}$ and $\overline{CS}$ are held low during a conversion, the data present will be from the previous conversion until the present conversion is completed when STS returns low. The data from the new conversion will appear on the outputs. The state of $\overline{RD}$ or $\overline{CS}$ should not change during a conversion.

Once a conversion is started and the STL or STS line goes high, convert start commands will be ignored until the conversion cycle is completed. The output data buffers cannot be enabled during conversion. In addition, all inputs and outputs which change during conversion can introduce noise, and should be avoided when possible.

3

ADC Write Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
ADC Control Timing					
$\overline{CS}$ to $\overline{WR}$ Set-Up Time	t_1	0	0	ns min	
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2	0	0	ns min	
Address to $\overline{WR}$ Set-Up Time	t_3	0	0	ns min	
Address to $\overline{WR}$ Hold Time	t_4	0	0	ns min	
$\overline{WR}$ Pulse Width	t_5	80	80	ns min	
ADEN to $\overline{WR}$ Set-Up Time	t_6		0	ns min	
ADC Conversion Timing					
$\overline{WR}$ to STL Delay	t_7	150	150	ns max	Load ckt of Figure 5, C_L = 20 pF, ADEN = 1
STL High (mux/amp settle)	t_8	10	15	µs max	Load ckt of Figure 5, C_L = 20 pF
STL to STS Low (Converting)	t_9	15	20	µs max	Load ckt of Figure 5, C_L = 20 pF
$\overline{WR}$ to STS High (ADEN = 0)	t_{12}	200	250	ns max	STL = 0 when ADEN = 0
$\overline{WR}$ to STS Low (ADEN = 1)	t_{10}	15	20	µs max	
STS High to Bus Relinquish Time	t_{13}	150	150	ns max	Load ckt of Figure 4
STS Low to Data Valid ($\overline{RD}$ = 0)	t_{14}	50	50	ns max	Load ckt of Figure 3, C_L = 20 pF

Table 2. ADC Write Timing
(See Figure 1.)

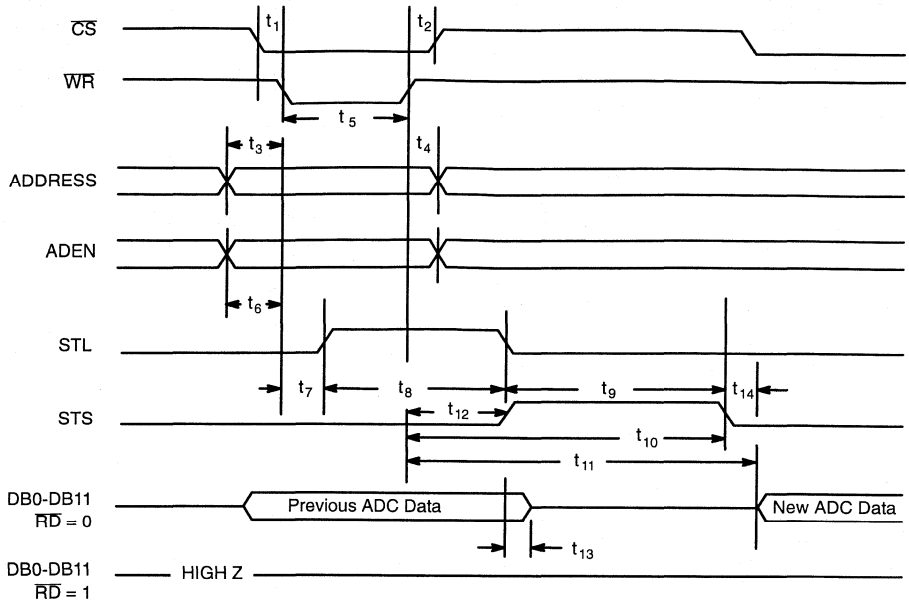


Figure 1. Timing for ADC Channel Select Start Conversion

ADC Read Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
$\overline{CS}$ to $\overline{RD}$ Set-Up Time	t_{15}	0	0	ns min	
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{16}	0	0	ns min	
$\overline{RD}$ to Data Valid Delay	t_{17}	100	150	ns max	Load ckt of *Figure 3.*, C_L = 20 pF
		150	200	ns max	Load ckt of *Figure 3.*, C_L = 100 pF
Bus Relinquish Time after $\overline{RD}$ High	t_{18}	100	150	ns max	Load ckt of *Figure 4.*
$\overline{RD}$ Pulse Width	t_{19}	100	150	ns min	

Table 3. ADC Read Timing
(*See Figure 2.*)

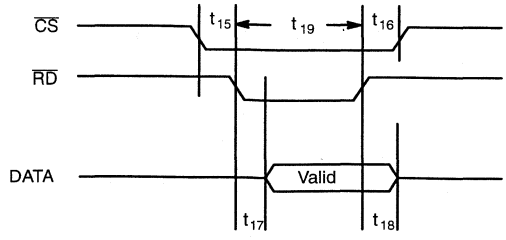


Figure 2. Timing for ADC Read

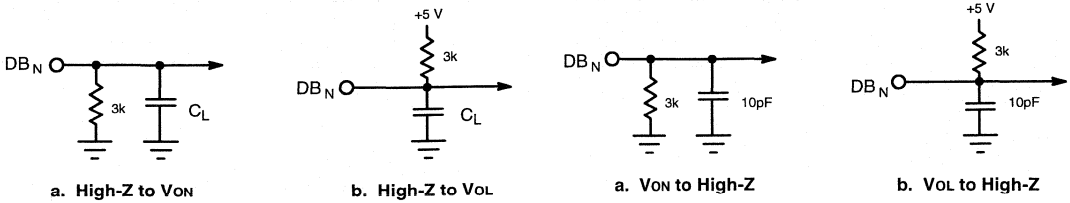


Figure 3. Load Circuit for Data Access Time Test

Figure 4. Load Circuit for Bus Relinquish Time Test

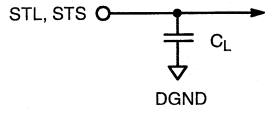


Figure 5. Load Circuit for $\overline{WR}$ to STS Delay

3

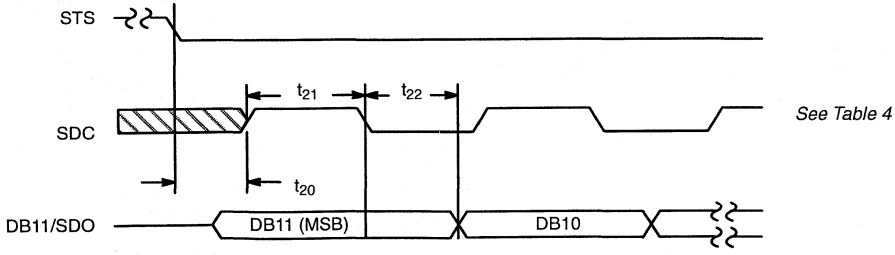
Serial Data Output Mode (PXS = 0)

The MP3274 output data is available in serial form when PXS = 0 prior to the $\overline{RD}$ high-to-low transition. When PXS = 0, the DB11/SDO pin functions as the serial data output. The DB0/SDC pin functions as the serial clock input and all other data outputs are 3-stated.

The serial data output sequence is MSB (DB11) first to LSB (DB0) last. The MSB (DB11) data bit appears at DB11/SDO when STS goes low. The second most significant bit appears at DB11/SDO on the next DB0/SDC high-to-low transition. The LSB (DB0) is present at DB11/SDO on the 11th SDC high-to-low transition.

The control pin functions (ADEN, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$) are the same as the parallel mode of operation. Further information regarding serial control and timing is shown in *Figure 6., Table 4.* and *Table 5.*

For a minimum interconnect serial environment, the channel address state can be generated in at least two ways, using an address counter, or using an address serial to parallel converter. $\overline{WR}$ can then be used as the counter clock or shift register load signal as well as the A/D converter start convert signal on the rising edge. (Note that the falling edge loads the address present at the address port.)



SDC should be in a high state during the STS high period. SDC can make the first high to low transition after t_{21}. In normal use it is assumed that PXS is hardwired low. However, if the mode of operation is changed, PXS must go low prior to $\overline{RD}$ going low.

Figure 6. Serial Data Mode Timing

Serial Data Output Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
STS low to SDO (DB11) Valid, $\overline{RD}$ = 0	t_{20}	50	50	ns max	Load Ckt 4 of *Figure 3.*
Minimum clock high pulse width	t_{21}	50	80	ns max	
SDC low to data valid delay	t_{22}	150 ns	200	ns max	Load ckt of *Figure 3.*, C_L = 20pF
		200 ns	250	ns max	Load ckt of *Figure 3.*, C_L = 100pF

Table 4. Serial Data Output Mode Timing (*See Figure 6.*)

$\overline{CS}$	PXS	$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	DB0/SDC	Comments
ADC Channel Select and Start Convert									
1	X	X	X	X	—	0	0	X	No Operation
0	↓	X	1	X	Hi-Z	0	0	X	Serial mode enabled (1)
0	0	↓	1	0	Hi-Z	0	0	X	No operation if ADEN = 0
0	0	↓	1	1	Hi-Z	↑	0	X	Input MUX channel selected, STL set on falling edge of $\overline{WR}$
0	0	0	1	X	Hi-Z	1	0	X	MUX select disabled
0	0	↑	1	X	Hi-Z	0	↑	X	Start convert on $\overline{WR}$ rising edge
0	0	1	1	X	Hi-Z	↓	↑	X	Start convert on STL falling edge
0	0	1	1	X	Hi-Z	0	↓	X	STS goes low at end of conversion
Read ADC Data (*See Table 4. and Figure 6.*)									
0	0	1	↓	X	—	0	0	1	Serial output (DB11/SDO) and serial clock input (DB0/SDC) enabled
0	0	X	X	X	MSB (DB11)	0	0	1	MSB data available at DB11/SDO
0	0	X	0	X	DB10	0	0	↓	Next significant bit shifted out to DB11/SDO
0	0	X	0	X	DB10	0	0	0	No Operation
0	0	X	0	X	DB10	0	0	↑	No Operation
0	0	X	0	X	DB9	0	0	↓	Next significant bit shifted out to DB11/SDO
0	0	X	↑	X	Hi-Z	0	0	X	Data outputs/SDC input disabled
0	X	1	X	X	Hi-Z	0	1	X	Data outputs/$\overline{RD}$ disabled when STS = 1
0	X	⊓	0	0	Hi-Z	0	↑	1	STL, MUX select disabled when ADEN = 0
0	0	⊓	0	X	MSB (DB11)	0	↓	1	New data appears at DB11/SDO on falling edge of STS

Note 1: If $\overline{RD}$ = 1, data outputs remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the data bus.

Table 5. Logic Truth Table – Serial Data Output Mode

2's Complement Output Code (Hexidecimal)						Ideal Transition Voltage
0111	1111	1110 (7fe) to	0111	1111	1111 (7ff)	+FS – 1 1/2 LSB
0000	0000	0000 (000) to	0000	0000	0001 (001)	0 V +1/2 LSB
1111	1111	1111 (fff) to	0000	0000	0000 (000)	0 V –1/2 LSB
1000	0000	0000(800) to	1000	0000	0001 (801)	–FS +1/2 LSB

Table 6. Key Output Codes vs. Input Voltage (2's Complement Code)

APPLICATION INFORMATION

The MP3274 is a complete A/D converter system, with its own built-in reference and clock. It may be used by itself ("stand-alone" operation), or it may be interfaced with a microprocessor which can control both conversion and formatting of output.

Successful application of the MP3274 requires careful attention to four main areas:

1) Physical layout.
2) Connection/Trimming according to mode of operation.
3) Conditioning of input signals.
4) Control and Timing considerations.

Physical Layout

The 12-bit accuracy of the MP3274 represents a dynamic range of 72dB. In order that this be preserved, thorough precautions must be taken to avoid any interfering signals, whether conducted or radiated.

- Avoid placing the chip and its analog signals near logic traces. In general, using a double sided printed circuit card with a good ground plane on the component side is recommended. Routing analog signals between ground traces will help isolate digital control logic. If these lines cross, do so at right angles. The GND Ref. is the positive terminal of the MUX/Instrumentation amplifier and will provide common mode noise rejection. It should be close to and shielded together with the channel inputs in order to take advantage of this feature.
- Power supplies should be quiet and well regulated. Grounds should be tied together at the package and back to the system ground with a single path. Bypass the supplies at the device with a 0.01 to 0.1μF ceramic cap and a 10-47 μF tantalum type, in parallel.

"Stand-Alone" Operation

The MP3274 can be used in "stand-alone" operation, which is useful in systems not requiring full computer bus interface capability. This operation is available for either parallel or serial mode.

For this operation, $\overline{CS}$ = 0, ADEN = 1, and conversion is controlled by $\overline{WR}$. The 3-state buffers are enabled when $\overline{RD}$ goes low. There are two possible conditions that the 3-state buffers could be in during a conversion. If $\overline{RD}$ goes low prior to $\overline{WR}$, the output buffers are enabled and the data from the previous conversion is available at the outputs during STL = 1. At the end of the present conversion which is initiated at the rising edge of $\overline{WR}$, STS returns low and the new conversion result is placed on the output data buffers.

If $\overline{WR}$ goes low prior to $\overline{RD}$ the data buffers remain in a high impedance state and conversion is initiated at the rising edge of $\overline{WR}$. Upon the end of the conversion the STS returns low and the conversion result is placed on the output data buffers.

Ground Reference

The ground reference pin can be used for remote ground sensing of a common mode input signal with a maximum 6 V p-p around AGND.

This common input can also be used to dither each input's "zero". By averaging multiple conversions digitally, higher resolution for each input conversion can be obtained. Patterns for this dither can be a ramp, a stair step, or white noise.

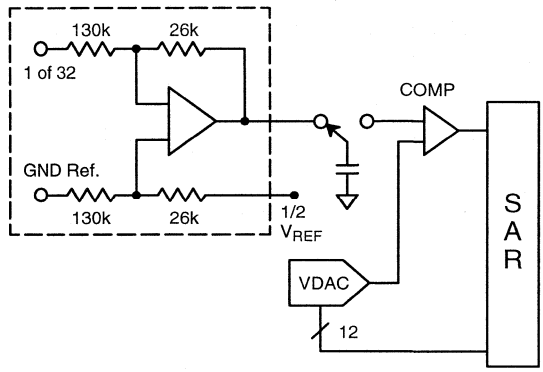


Figure 7. Equivalent Input Circuit

Quasi Differential Sampling

Method 1

For remote ground sensing where the remote ground does not change more than ±3 V from the A/D ground, connect GND Ref to the remote ground.

Method 2

Where Method 1 applies to each channel or group of channels, add a mux to allow connecting the appropriate ground to GND Ref.

Method 3

Use two parts. Tie both GND Ref pins together and connect this node to the "common" remote GND. Control the sample point by connecting each STL through an "OR" gate whose output is "NAND" connect with WR (inverted $\overline{WR}$). Use this output as $\overline{WR}$ to both $\overline{WR}$ inputs. By controlling the $\overline{WR}$, sample delay differences between the two converters is minimized. Two parts from the same date code will further minimize this difference. Treat one A/D as the (+) terminal and the other as the (–) terminal of the differential signal. Now the difference can be taken digitally.

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See MPSAN32 for MP3274 Application Hints

FEATURES

- **Fault Protected 16-Channel 12-Bit A/D Converter with Sample & Hold, Reference, Clock and 3-State Outputs**
- **Fast Conversion, less than 15μS**
- **2's Complement and Serial Data Output**
- **Remote Analog Ground Sensing**
- **Overvoltage Protected Input (±50 V over the Supply Voltages)**
- **Precision Reference for Long Term Stability and Low Gain T.C.**
- **Guaranteed Linearity Over Temperature**
- **Guaranteed Performance at +12/–5 V, ±12 & ±15 V**
- **Low Power (7 mW per Channel Typical)**
- **Parallel Version: MP3276**
- **32 Channel Version: MP3274**

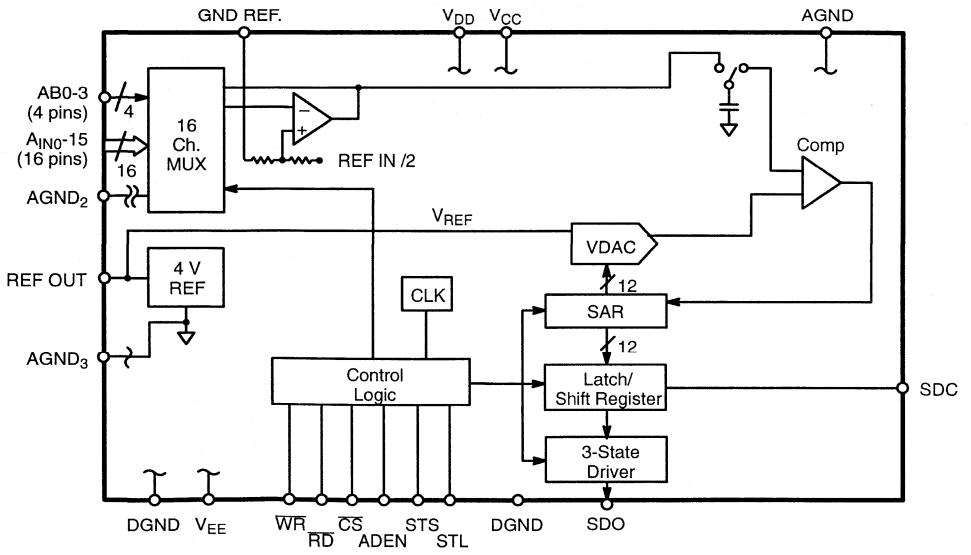
GENERAL DESCRIPTION

The MP3275 is a complete 16-channel, 12-bit Data Acquisition Subsystem with serial data port. Implemented using an advanced BiCMOS process, the converter combines a 16-channel passive overvoltage-protected multiplexer instrumentation amp, a sample & hold, a SAR, a 12-bit decoded D/A, a comparator, a precision reference and the control logic to achieve an accurate conversion in less than 15μs, and a mux/instrumentation amp settling period of less than 10μs.

A unique input design provides input overvoltage protection to ±50 V over the supply voltages. The circuit design can allow for an overvoltage condition on unselected channels without disrupting the measured channel or operation of the MP3275! The internal 4 V reference has sufficient output current to provide other system reference needs. Precision thin film scaling and offset resistors are laser trimmed to provide for less than 2 LSB INL for ±10 V inputs on all channels.

In addition, the MP3275 will output either full scale (0111 ....) for overrange and – full scale (1000....) for underrange conditions. This greatly simplifies microprocessor software development.

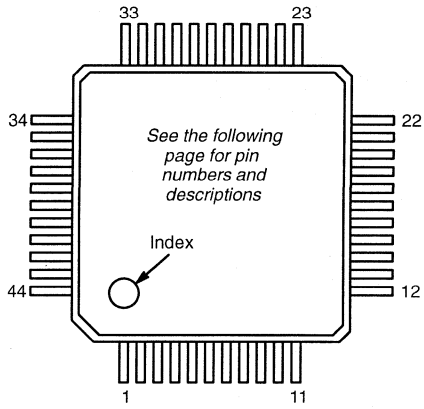
SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	−40 to +85°C	MP3275AE	±2	±2

PIN CONFIGURATIONS



44 Pin PQFP
Q44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{EE}	– Analog Supply. –4.75 To – 16.5
2	$A_{IN}12$	Channel 12 Analog Input, 1100
3	$A_{IN}13$	Channel 13 Analog Input, 1101
4	$A_{IN}14$	Channel 14 Analog Input, 1110
5	$A_{IN}15$	Channel 15 Analog Input, 1111
6	GNDREF	+ Input To Mux / Instrumentation Amp
7	AGND	A/D Section Analog Ground
8	REF	Reference Output
9	$AGND_3$	Reference Analog Ground
10	DGND	Digital Logic And Output Ground
11	SDC	Serial Data Clock
12	N/C	No Connection
13	N/C	No Connection
14	N/C	No Connection
15	N/C	No Connection
16	SDO	Serial Data Out
17	STS	Conversion Status, Converting=1
18	STL	Input Settling Period State = 1
19	DGND	Digital Gnd, Low Current
20	$\overline{RD}$	Enable Serial Data Out
21	CS	Chip Select
22	$\overline{WR}$	Input Address And Conversion Control

PIN NO.	NAME	DESCRIPTION
23	ADEN	Address Update Enable=1, Ignore=0
24	AB3	Input Address Bit 3, (MSB)
25	AB2	Input Address Bit 2
26	AB1	Input Address Bit 1
27	AB0	Input Address Bit 0, (LSB)
28	V_{DD}	Digital Logic & Output Supply, +4.75 to + 5.25 Volts
29	V_{CC}	Analog + Supply, +11.4 to + 16.5 Volts
30	$A_{IN}0$	Channel 0 Analog Input, 0000
31	$A_{IN}1$	Channel 1 Analog Input, 0001
32	$A_{IN}2$	Channel 2 Analog Input, 0010
33	$A_{IN}3$	Channel 3 Analog Input, 0011
34	N/C	No Connection
35	$A_{IN}4$	Channel 4 Analog Input, 0100
36	$A_{IN}5$	Channel 5 Analog Input, 0101
37	$A_{IN}6$	Channel 6 Analog Input, 0110
38	$A_{IN}7$	Channel 7 Analog Input, 0111
39	$AGND_2$	Agnd For Input Mux Section
40	$A_{IN}8$	Channel 7 Analog Input, 1000
41	N/C	No Connection
42	$A_{IN}9$	Channel 9 Analog Input, 1001
43	$A_{IN}10$	Channel 10 Analog Input, 1010
44	$A_{IN}11$	Channel 11 Analog Input, 1011

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, V_{CC} = 15 V, V_{EE} = –15 V, GNDRef = 0 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
Resolution (All Grades)	N	12				12		Bits
KEY FEATURES								
Resolution		12				12	Bits	
Conversion Time, Per Channel	t_{CONVR}			15		15	µs	
ACCURACY (A Grade)[1]								Refer to *Table 6.* for output coding
Differential Non-Linearity	DNL		3/4	2		2	LSB	
Integral Non-Linearity	INL		1	2		2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Code Error	EZS		2	±5		±10	LSB	fff to 000 [hex] transition
Full Scale Error	EFS		0.1	±0.35		±0.5	%	V_{REF}IN = 4.000 V
POWER SUPPLY REJECTION								Max change in Full Scale Calibration
V_{CC} = 15 V ±1.5 V or 12 V ±0.6 V				±1		±1	LSB	
V_{DD} = 5 V ±0.25 V				±2		±2.5	LSB	
V_{EE} = –15 V ±1.5 V or –12 V ±0.6 V				±1		±1	LSB	
–5 V ±0.25 V								
REFERENCE VOLTAGES								
Voltage Output	$V_{REF(+)}$	3.975	4.0	4.025	3.970	4.030	V	
Ref. Source Current		3.0	4.0		3.0		mA	
Ref. Sink Current			20				µA	
ANALOG INPUT								
Input Voltage Range[3]	V_{IN}	–10		10	–10	10	V	
Ground Reference	GND Ref.							
CM Range[2]		–3		+3	–3	3	V	
CM RR			TBD				LSB/V	
Input Resistance	R_{IN}	100	130		100		kΩ	
Input Capacitance[2]	C_{IN}		5				pF	
Aperture Delay[2]	t_{AP}		180				ns	From $\overline{WR}$ low to high after STL high to low
Channel-to-Channel Isolation[2]			–80	–70			dB	DC
DIGITAL INPUTS $\overline{WR}$, RD AB0-AB4, ADEN, SDC								
Logical "1" Voltage	V_{IH}	2.4		5.5	2.4	5.5	V	
Logical "0" Voltage	V_{IL}	–0.5		0.8	–0.5	0.8	V	
Leakage Currents[4]	I_{IN}	–5		5	–10	10	µA	V_{IN}=GND to V_{DD}
Input Capacitance[2]			5				pF	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL OUTPUTS (Data Format 2's Complement) SDO, STS, STL								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.0			2.4		V	I_{SOURCE} = 0.5 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{SINK} = 1.6 mA
Tristate Leakage	I_{OZ}	–5		5	–5	5	µA	V_{OUT}=GND to V_{DD}
POWER SUPPLIES								
Operating Range								
V_{DD}		+4.5		+5.5	+4.5	+5.5	V	
V_{CC}		+11.4		+16.5	+11.4	+16.5	V	
V_{EE}		–4.75		–16.5	–4.75	–16.5	V	Tested at –11.4 and –16.5 only
Operating Current								
I_{DD}			2	7		7	mA	
I_{CC}			5	8		8	mA	
I_{EE}			1.5	3		3	mA	
Power Dissipation			110	200		200	mW	

NOTES
1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage
2. Guaranteed. Not tested.
3. All channel input pins and ground reference pin have protection which becomes active above ±60 V.
4. All digital inputs have diodes to V_{DD} and AGND. Input DC currents will not exceed specified limits for any input voltage between AGND and V_{DD}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... 0 to +16.5 V
V_{EE} to AGND ..... 0 to –16.5 V
V_{DD} to AGND ..... 0 to +7 V
AGND to DGND ..... ±1 V
Digital Inputs or Outputs ($\overline{WR}$, $\overline{RD}$, $\overline{CS}$, AB0-AB4, ADEN, SDC) to DGND ..... –0.5 V to V_{DD} +0.5 V
Analog Inputs ($A_{IN}0$ – $A_{IN}15$, GND REF) to AGND ..... ±60 V

REF OUT ..... Indefinite short to DGND, Momentary short to V_{CC}
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Rating to 75°C
PQFP ..... 750 mW
Derates above 75°C ..... 10 mW/°C
Lead Temperature, Soldering ..... 300°C, 10 Sec
Storage Temperature (Ceramic) ..... –65°C to +150°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All logic inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

Basic Description

The MP3275 is a fault protected data acquisition subsystem available in monolithic form. This product contains all of the circuitry necessary to acquire 16 channels of quasi differential or single-ended analog signals at ±10 V input range and 15kHz bandwidth. Connections to power, the analog input signals and the digital system are all that is required. The MP3275's input circuitry is protected against active input signals present with the MP3275 power off. This is also the case for any channel exceeding the MP3275 analog input dynamic range without interfering with the channel being digitized. The channel address and channel conversion can be managed in two ways: random channel conversion or same channel conversion. Circuitry on the chip adds a MUX/instrumentation amp settling delay of 10µs max, when a new channel is selected (ADEN = 1). Conversion start is initiated without delay for the single-channel case (ADEN = 0). Data is available in serial format.

TIMING

Control and Timing Considerations

The MP3275 can be operated in the stand-alone mode, with one line for control and everything else hard-wired; or under microprocessor control, where changes can be made dynamically. There are 4 control lines: ADEN, $\overline{WR}$, $\overline{CS}$ and $\overline{RD}$ with their functions described in *Table 1.*

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	Comments
ADC Channel Select and Start Convert *(See Figure 1. and Table 2.)*							
1	X	X	X	—	0	0	No operation
0	↓	1	0	Hi-Z	0	0	No operation if ADEN = 0
0	↓	1	1	Hi-Z	↑	0	Input MUX channel selected, STL set on $\overline{WR}$ falling edge
0	0	1	X	Hi-Z	1	0	MUX select disabled
0	↑	1	X	Hi-Z	0	↑	Start convert on $\overline{WR}$ rising edge
0	1	1	X	Hi-Z	↓	↑	Start convert on STL falling edge
0	1	1	X	Hi-Z	0	↓	STS goes low at end of conversion
Read ADC Data *(See Figure 2. and Table 3.)*							
0	1	↓	X	—	0	0	SDO enabled
0	X	0	X	ADC	0	0	Data from previous conversion on SDO
0	X	↑	X	Hi-Z	0	0	SDO disabled
0	1	X	X	Hi-Z	0	1	SDO/$\overline{RD}$ disabled while STS high
0	X	0	X	Last ADC	1	0	Data from last conversion on SDO
0	⊓	0	0	Hi-Z	0	↑	STL, MUX select disabled with ADEN = 0, SDO disabled on STS rising edge
0	⊓	0	X	ADC	0	↓	New data appears on SDO on falling edge of STS

Note 1: If $\overline{RD}$ = 1, SDO remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the SDO.

Table 1. Logic Truth Table

The MP3275 is easily interfaced to a wide variety of digital systems. Discussion of the timing requirements of the MP3275 control signals follows.

Figure 1. shows a complete timing diagram for the MP3275 convert start operation.

$\overline{WR}$ is used to initiate a conversion.

A conversion is started by taking $\overline{WR}$ low, then high again (conversion is enabled on the rising edge of $\overline{WR}$). There are two possible conditions that will affect conversion timing.

1. ADEN = 1. At the falling edge of $\overline{WR}$, the input channel is determined by the data present on the address bits. The track and hold begins to settle after which STL returns low, indicating that the multiplexer, buffer amp, and sample/hold have settled to less than 1/2 LSB of final value. If the rising edge of $\overline{WR}$ returns high prior to STL going low, conversion will begin on the falling edge of STL. If the rising edge of $\overline{WR}$ is delayed until after STL returns low, the input signal is sampled and the conversion is started at the rising edge of $\overline{WR}$ giving the user better control of the sampling time.
2. ADEN = 0. At the falling edge of $\overline{WR}$ the data present at the address is ignored and the channel selected during the previous conversion remains selected. In this case the track and hold settling time is omitted and STL never goes high. At the rising edge of $\overline{WR}$ the input signal is sampled, and conversion is started.

There are two possible states that the data output could be in during a conversion.

1. If $\overline{RD}$ is held high during a conversion the output would remain high impedance throughout the conversion. This is the preferred method of operation as any noise present on SDO is rejected.
2. If $\overline{RD}$ is held low during a conversion, the data present SDO will be from the previous conversion until the present conversion is completed, when STS returns low. The data from the new conversion will be available through SDO. The state of $\overline{RD}$ should not change during a conversion.

Once a conversion is started and the STL or STS line goes high, convert start commands will be ignored until the conversion cycle is completed. The SDO output buffer cannot be enabled during conversion. In addition, all input and output changes during conversion can introduce noise, and should be avoided when possible.

3

ADC Write Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
ADC Control Timing					
Address to $\overline{WR}$ Set-Up Time	t_3	0	0	ns min	
Address to $\overline{WR}$ Hold Time	t_4	0	0	ns min	
$\overline{WR}$ Pulse Width	t_5	80	80	ns min	
ADEN to $\overline{WR}$ Set-Up Time	t_6		0	ns min	
ADC Conversion Timing					
$\overline{WR}$ to STL ↑ Delay	t_7	150	150	ns max	Load ckt of Figure 5, C_L = 20 pF, ADEN = 1
STL High (Settling Period)	t_8	10	15	µs max	Load ckt of Figure 5, C_L = 20 pF
STL to STS Low (Converting)	t_9	15	20	µs max	Load ckt of Figure 5, C_L = 20 pF
$\overline{WR}$ to STS High (ADEN = 0)	t_{12}	200	250	ns max	STL = 0 when ADEN = 0
$\overline{WR}$ to STS Low (ADEN = 1)	t_{10}	15	20	µs max	
STS High to SDO Relinquish Time	t_{13}	150	150	ns max	Load ckt of Figure 4
STS Low to Data Valid ($\overline{RD}$ = 0)	t_{14}	50	50	ns max	Load ckt of Figure 3, C_L = 20 pF

Table 2. ADC Write Timing
(See Figure 1.)

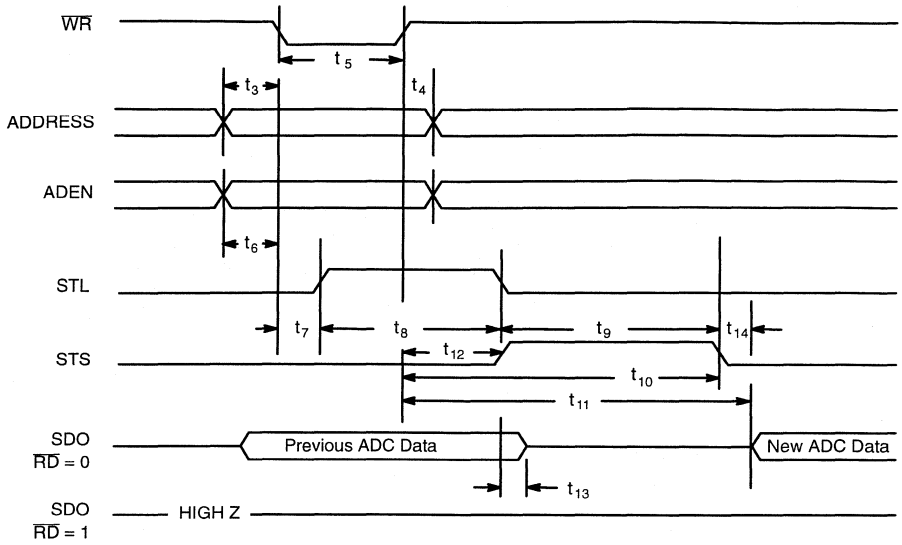


Figure 1. Timing for ADC Channel Select Start Conversion

ADC Read Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
$\overline{RD}$ to Data Valid Delay	t_{17}	100	150	ns max	Load ckt of *Figure 3.*, C_L = 20 pF
		150	200	ns max	Load ckt of *Figure 3.*, C_L = 100 pF
SDO Relinquish Time after $\overline{RD}$ High	t_{18}	100	150	ns max	Load ckt of *Figure 4.*
$\overline{RD}$ Pulse Width	t_{19}	100	150	ns min	

Table 3. ADC Read Timing
(*See Figure 2.*)

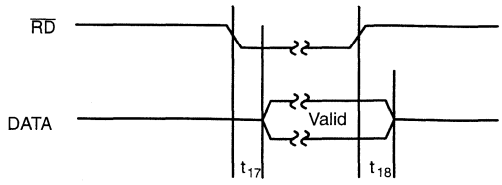
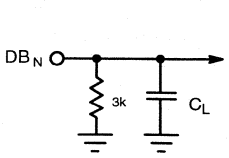
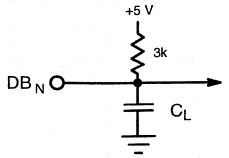


Figure 2. Timing for ADC Read

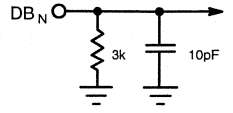


a. High-Z to VON

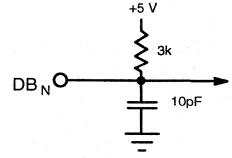


b. High-Z to VOL

Figure 3. Load Circuit for Data Access Time Test



a. VON to High-Z



b. VOL to High-Z

Figure 4. Load Circuit for Bus Relinquish Time Test

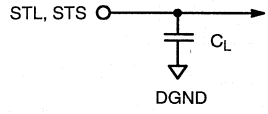


Figure 5. Load Circuit for $\overline{WR}$ to STS Delay

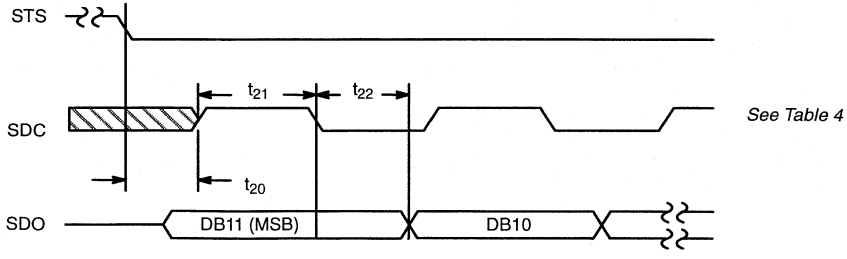
3

Serial Data Output

The serial data output sequence is MSB (DB11) first to LSB (DB0) last. The MSB (DB11) data bit appears at SDO when STS goes low. The second most significant bit appears at SDO on the SDC high-to-low transition next. The LSB (DB0) is present at SDO on the 11th SDC high-to-low transition.

Further information regarding serial control and timing is shown in *Figure 6., Table 4.* and *Table 5.*

For a minimum interconnect serial environment, the channel address state can be generated in at least two ways, using an address counter, or using an address serial to parallel converter. $\overline{WR}$ can then be used as the counter clock or shift register load signal as well as the A/D converter start convert signal on the rising edge. (Note that the falling edge loads the address present at the address port.)



SDC should be in a high state during the STS high period. SDC can make the first high to low transition after t_{21}.

Figure 6. Serial Data Mode Timing

Serial Data Output Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
STS low to SDO Valid, $\overline{RD}$ = 0	t_{20}	50	50	ns max	Load Ckt 4 of *Figure 3.*
Minimum clock high pulse width	t_{21}	50	80	ns max	
SDC low to data valid delay	t_{22}	150	200	ns max	Load ckt of *Figure 3.*, C_L = 20pF
		200	250	ns max	Load ckt of *Figure 3.*, C_L = 100pF

Table 4. Serial Data Output Mode Timing
(*See Figure 6.*)

$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	DB0/SDC	Comments
ADC Channel Select and Start Convert							
↓	1	0	Hi-Z	0	0	X	No operation if ADEN = 0
↓	1	1	Hi-Z	↑	0	X	Input MUX channel selected, STL set on falling edge of $\overline{WR}$
0	1	X	Hi-Z	1	0	X	MUX select disabled
↑	1	X	Hi-Z	0	↑	X	Start convert on $\overline{WR}$ rising edge
1	1	X	Hi-Z	↓	↑	X	Start convert on STL falling edge
1	1	X	Hi-Z	0	↓	X	STS goes low at end of conversion
Read ADC Data (*See Figure 6. and Table 4.*)							
1	↓	X	—	0	0	1	Serial output (SDO) and serial clock input (SDC) enabled
X	X	X	MSB (DB11)	0	0	1	MSB data available at SDO
X	0	X	DB10	0	0	↓	Next significant bit shifted out to SDO
X	0	X	DB10	0	0	0	No Operation
X	0	X	DB10	0	0	↑	No Operation
X	0	X	DB9	0	0	↓	Next significant bit shifted out to SDO
X	↑	X	Hi-Z	0	0	X	Data outputs/SDC input disabled
1	X	X	Hi-Z	0	1	X	Data outputs/$\overline{RD}$ disabled when STS = 1
⊓	0	0	Hi-Z	0	↑	1	STL, MUX select disabled when ADEN = 0
⊓	0	X	MSB (DB11)	0	↓	1	New data appears at SDO on falling edge of STS

Note 1: If $\overline{RD}$ = 1, data outputs remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the data bus.

Table 5. Logic Truth Table – Serial Data Output

2's Complement Output Code (Hexidecimal)						Ideal Transition Voltage
0111	1111	1110 (7fe) to	0111	1111	1111 (7ff)	+FS – 1 1/2 LSB
0000	0000	0000 (000) to	0000	0000	0001 (001)	0 V +1/2 LSB
1111	1111	1111 (fff) to	0000	0000	0000 (000)	0 V –1/2 LSB
1000	0000	0000(800) to	1000	0000	0001 (801)	–FS +1/2 LSB

Table 6. Key Output Codes vs. Input Voltage (2's Complement Code)

APPLICATION INFORMATION

The MP3275 is a complete A/D converter system, with its own built-in reference and clock. It may be used by itself ("stand-alone" operation), or it may be interfaced with a microprocessor.

Successful application of the MP3275 requires careful attention to four main areas:

1) Physical layout.
2) Connection/Trimming according to mode of operation.
3) Conditioning of input signals.
4) Control and Timing considerations.

Physical Layout

The 12-bit accuracy of the MP3275 represents a dynamic range of 72dB. Precautions must be taken to avoid any interfering signals, whether conducted or radiated, to assure that this is not degraded.

- Avoid placing the chip and its analog signals near logic traces. In general, using a double sided printed circuit card with a good ground plane on the component side is recommended. Routing analog signals between ground traces will help isolate digital control logic. If these lines cross, do so at right angles. The GND Ref. is the positive terminal of the MUX/Instrumentation amplifier and will provide common mode noise rejection. It should be close to and shielded together with the channel inputs in order to take advantage of this feature.
- Power supplies should be quiet and well regulated. Grounds should be tied together at the package and back to the system ground with a single path. Bypass the supplies at the device with a 0.01 to 0.1µF ceramic cap and a 10-47 µF tantalum type, in parallel.

"Stand-Alone" Operation

The MP3275 can be used in "stand-alone" operation, which is useful in systems not requiring full computer bus interface capability.

For this operation, $\overline{CS}$ = 0, ADEN = 1, and conversion is controlled by $\overline{WR}$. The 3-state buffer SDO is enabled when $\overline{RD}$ goes low. There are two possible conditions that the 3-state buffer could be in during a conversion. If $\overline{RD}$ goes low prior to $\overline{WR}$ the output buffer is enabled and the data from the previous conversion is available at the outputs during STL = 1. At the end of the present conversion which is initiated at the rising edge of $\overline{WR}$, STS returns low and the new conversion result is placed on the output data buffer.

If $\overline{WR}$ goes low prior to $\overline{RD}$, the data buffer remains in a high impedance state and conversion is initiated at the rising edge of $\overline{WR}$. Upon the end of the conversion the STS returns low and the conversion result is placed on the output data buffers.

Ground Reference

The ground reference pin can be used for remote ground sensing of a common mode input signal with a maximum 6 V p-p around AGND.

This common input can also be used to dither each input's "zero". By averaging multiple conversions digitally, higher resolution for each input conversion can be obtained. Patterns for this dither can be a ramp, a stair step, or white noise.

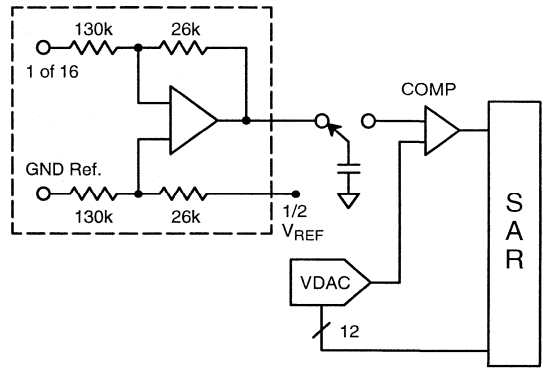


Figure 7. Equivalent Input Circuit

Quasi Differential Sampling

Method 1

For remote ground sensing where the remote ground does not change more than ±3 V from the A/D ground, connect GND Ref to the remote ground.

Method 2

Where Method 1 applies to each channel or group of channels, add a mux to allow connecting the appropriate ground to GND Ref.

Method 3

Use two parts. Tie both GND Ref pins together and connect this node to the "common" remote GND. Control the sample point by connecting each STL through an "OR" gate whose output is "NAND" connect with WR (inverted $\overline{WR}$). Use this output as $\overline{WR}$ to both $\overline{WR}$ inputs. By controlling the $\overline{WR}$, sample delay differences between the two converters is minimized. Two parts from the same date code will further minimize this difference. Treat one A/D as the (+) terminal and the other as the (–) terminal of the differential signal. Now the difference can be taken digitally.

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MP3276

Fault Protected 16 Channel, 12-Bit Data Acquisition Subsystem

FEATURES

- **Fault Protected 16-Channel 12-Bit A/D Converter with Sample & Hold, Reference, Clock and 3-state Outputs**
- **Fast Conversion, less than 15μS**
- **Microprocessor Bus Interface**
- **2's Complement Data Output**
- **Parallel or Serial Data Output Modes**
- **65 ns Bus Access Time**
- **Remote Analog Ground Sensing**
- **Overvoltage Protected Input (±50 V over the Supply Voltages)**
- **Precision Reference for Long Term Stability and Low Gain T.C.**
- **Guaranteed Linearity Over Temperature**
- **Guaranteed Performance at +12/–5 V, ±12 & ±15 V**
- **Low Power: 110 mW typ. (7 mW per Channel typ.)**
- **32 Channel Version: MP3274**

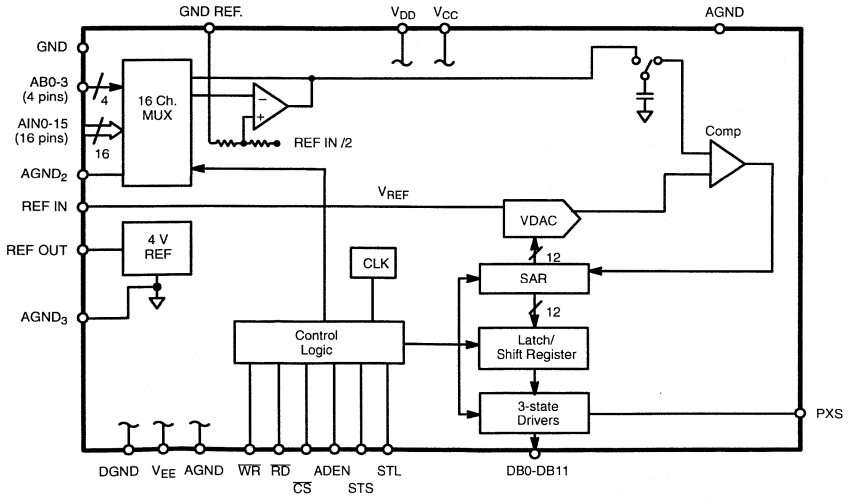
GENERAL DESCRIPTION

The MP3276 is a complete 16-channel, 12-bit Data Acquisition Subsystem with 3-state output buffers for direct interfacing to 16-bit microprocessor buses. Implemented using an advanced BiCMOS process, the converter combines a 16-channel passive overvoltage protected multiplexer instrumentation amp, a sample & hold, a SAR, a 12-bit decoded D/A, a comparator, a precision reference and the control logic to achieve an accurate repeated conversion in less than 15μs, and a mux/instrumentation amp settling period of less than 10μs.

A unique input design provides input overvoltage protection to ±50 V over the supply voltages. The circuit design can allow for an overvoltage condition on unselected channels without disrupting the measured channel or operation of the MP3276! The internal 4 V reference has sufficient output current to provide other system reference needs. Precision thin film scaling and offset resistors are laser trimmed to provide for less than 2 LSB INL for ±10 V inputs on all channels.

In addition, the MP3276 will output either full scale (0111 ....) for overrange and – full scale (1000....) for underrange conditions. This greatly simplifies microprocessor software development.

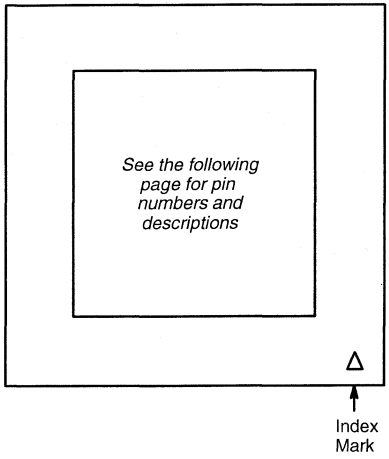
SIMPLIFIED BLOCK DIAGRAM



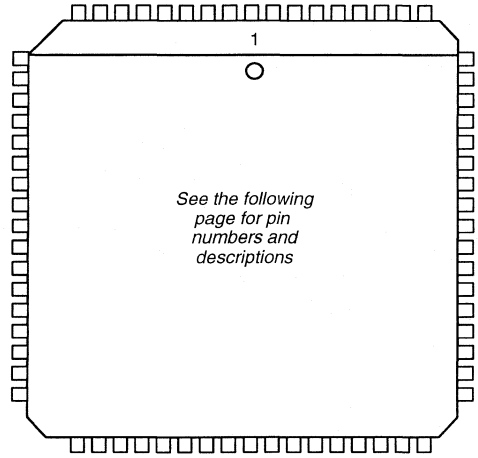
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PGA	–40 to +85°C	MP3276AG	±2	±2
PLCC	–40 to +85°C	MP3276AP	±2	±2

PIN CONFIGURATIONS



68 Pin PGA
G68



68 Pin PLCC
P68

PIN OUT DEFINITIONS

PLCC PIN NO.	PGA PADS	NAME	DESCRIPTION
61	1	V_{EE}	Negative Analog Supply
62	2	$A_{IN}12$	Analog Input 12, AB3-AB0 = 1100
63	3		N/C or GND
64	4	$A_{IN}13$	Analog Input 13, AB3-AB0 = 1101
65	5		N/C or GND
66	6	$A_{IN}14$	Analog Input 14, AB3-AB0 = 1110
67	7		N/C or GND
68	8	$A_{IN}15$	Analog Input 15, AB3-AB0 = 1111
1	9		N/C or GND
2	10	GND Ref.	Input Ground Reference
3	11	AGND	ADC Analog Ground
4	12	Ref In	Reference Input
5	13	Ref Out	Reference Output
6	14	AGND3	Reference Analog Ground
7	15	DGND	Digital Ground
8	16	DB0/SDC	Data Output Bit 0/Serial Data Clock
9	17	N/C	No Connection
10	18	DB1	Data Output Bit 1
11	19	DB2	Data Output Bit 2
12	20	DB3	Data Output Bit 3
13	21	DB4	Data Output Bit 4
14	22	DB5	Data Output Bit 5
15	23	DB6	Data Output Bit 6
16	24	DB7	Data Output Bit 7
17	25	DB8	Data Output Bit 8
18	26	DB9	Data Output Bit 9
19	27	DB10	Data Output Bit 10
20	28	DB11/SDO	Data Output Bit 11/Serial Data Out
21	29	STS	Conversion Status
22	30	STL	Mux Settling Status
23	31	PXS	Parallel/XSerial
24	32	$\overline{RD}$	Read Enable
25	33	$\overline{CS}$	Chip Select
26	34	$\overline{WR}$	Write Enable

PLCC PIN NO.	PGA PADS	NAME	DESCRIPTION
27	35	ADEN	Address Enable
28	36	AB3	Channel Address 3
29	37	AB2	Channel Address 2
30	38	AB1	Channel Address 1
31	39	AB0	Channel Address 0
32	40	GND	GND
33	41	V_{DD}	Positive Digital Supply
34	42	V_{CC}	Positive Analog Supply
35	43	$A_{IN}0$	Analog Input 0, AB3-AB0 = 0000
36	44		N/C or GND
37	45	$A_{IN}1$	Analog Input 1, AB3-AB0 = 0001
38	46		N/C or GND
39	47	$A_{IN}2$	Analog Input 2, AB3-AB0 = 0010
40	48		N/C or GND
41	49	$A_{IN}3$	Analog Input 3, AB3-AB0 = 0011
42	50		N/C or GND
43	51	N/C	No Connection
44	52	$A_{IN}4$	Analog Input 4, AB3-AB0 = 0100
45	53		N/C or GND
46	54	$A_{IN}5$	Analog Input 5, AB3-AB0 = 0101
47	55		N/C or GND
48	56	$A_{IN}6$	Analog Input 6, AB3-AB0 = 0110
49	57		N/C or GND
50	58	$A_{IN}7$	Analog Input 7, AB3-AB0 = 0111
51	59		N/C or GND
52	60	AGND2	Analog Ground Mux Return
53	61	$A_{IN}8$	Analog Input 8, AB3-AB0 = 1000
54	62		N/C or GND
55	63	$A_{IN}9$	Analog Input 9, AB3-AB0 = 1001
56	64		N/C or GND
57	65	$A_{IN}10$	Analog Input 10, AB3-AB0 = 1010
58	66		N/C or GND
59	67	$A_{IN}11$	Analog Input 11, AB3-AB0 = 1011
60	68		N/C or GND

3

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, V_{CC} = 15 V, V_{EE} = –15 V, GNDRef = 0 V, T_A = 25°C, V_{REF}IN = ReOut

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
Resolution (All Grades)	N	12			12			Bits
KEY FEATURES								
Resolution			12			12	Bits	
Conversion Time, Per Channel	t_{CONVR}			15		15	µs	
ACCURACY (A Grade)[1]								Refer to *Table 6.* for output coding
Differential Non-Linearity	DNL		3/4	2		2	LSB	
Integral Non-Linearity	INL		1	2		2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Code Error	EZS		2	±5		±10	LSB	fff to 000 [hex] transition
Full Scale Error	EFS		0.1	±0.35		±0.5	%	V_{REF}IN = 4.000 V
POWER SUPPLY REJECTION								Max change in Full Scale Calibration
V_{CC} = 15 V ±1.5 V or 12 V ±0.6 V				±1		±1	LSB	
V_{DD} = 5 V ±0.25 V				±2		±2.5	LSB	
V_{EE} = –15 V ±1.5 V or –12 V ±0.6 V or –5 V ±0.25 V				±1		±1	LSB	
REFERENCE VOLTAGES[5]								
Ref. Voltage Input	Ref In	3.6		4.4			V	R_{IN} ≃5 KΩ, V_{DD} = 5 V
Ref. Voltage Output	Ref Out	3.975		4.025			V	
Ref. Source Current		3.0	4.0		3.0		mA	
Ref. Sink Current			20				µA	
ANALOG INPUT								
Input Voltage Range[3]	V_{IN}	–10		10	–10	10	V	
Ground Reference	GND Ref.							
CM Range[2]		–3		3	–3	3	V	
CM RR			TBD				LSB/V	
Input Resistance	R_{IN}	100	130		100		kΩ	
Input Capacitance[2]	C_{IN}		5				pF	
Aperture Delay[2]	t_{AP}		180				ns	From $\overline{WR}$ low to high after STL high to low
Channel-to-Channel Isolation[2]			–80	–70			dB	DC
DIGITAL INPUTS $\overline{CS}$, $\overline{WR}$, RD AB0-AB4, ADEN, SDC								
Logical "1" Voltage	V_{IH}	2.4		5.5	2.4	5.5	V	
Logical "0" Voltage	V_{IL}	–0.5		0.8	–0.5	0.8	V	
Leakage Currents[4]	I_{IN}	–5		5	–10	10	µA	V_{IN}=GND to V_{DD}
Input Capacitance[2]			5				pF	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL OUTPUTS (Data Format 2's Complement) DB0/SDC–DB11/SDO, STL, STS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.0			2.4		V	I_{SOURCE} = 0.5 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{SINK} = 1.6 mA
Tristate Leakage	I_{OZ}	–5		5	–5	5	µA	V_{OUT}=GND to V_{DD}
POWER SUPPLIES								
Operating Range								
V_{DD}		+4.5		+5.5	+4.5	+5.5	V	
V_{CC}		+11.4		+16.5	+11.4	+16.5	V	
V_{EE}		–4.75		–16.5	–4.75	–16.5	V	Tested at –11.4 and –16.5 only
Operating Current								
I_{DD}			2	7		7	mA	
I_{CC}			5	8		8	mA	
I_{EE}			1.5	3		3	mA	
Power Dissipation			110	200		200	mW	

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage
2. Guaranteed. Not tested.
3. All channel input pins and ground reference pin have protection which becomes active above ±60 V.
4. All digital inputs have diodes to V_{DD} and AGND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.
5. Refin should not vary from Refout by more than ±10% of the nominal value of Refout.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{CC} to DGND ..... 0 to +16.5 V
V_{EE} to DGND ..... 0 to –16.5 V
V_{DD} to DGND ..... 0 to +7 V
AGND to DGND ..... ±1 V
Digital Inputs/Outputs to DGND ..... –0.5 V to V_{LOGIC} +0.5 V
Analog Inputs ($A_{IN}0$ – $A_{IN}31$, GND REF) to AGND ..... ±60 V
REF OUT ..... Indefinite short to DGND, Momentary short to V_{CC}
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Rating to 75°C
PGA, PLCC ..... 1800 mW
Derates above 75°C ..... 25 mW/°C
Lead Temperature, Soldering ..... 300°C, 10 Sec
Storage Temperature (Ceramic) ..... –65°C to +150°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All logic inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

Basic Description

The MP3276 is a fault protected data acquisition subsystem available in monolithic form. This product contains all of the circuitry necessary to acquire 16 channels of quasi differential or single-ended analog signals at ±10 V input range and 15kHz bandwidth. Connections to power, the analog input signals and the digital system are all that is required. The MP3276's input circuitry is protected against active input signals present with the MP3276 power off. This is also the case for any channel exceeding the MP3276 analog input dynamic range without interfering with the channel being digitized. The channel address and channel conversion can be managed in two ways: random channel conversion or same channel conversion. Circuitry on the chip adds a MUX/instrumentation amp settling (STL) delay of 10μs max, when a new channel is selected (ADEN = 1). Conversion start is initiated without delay for the single-channel case (ADEN = 0). Data is available in either parallel or serial format.

TIMING

Control and Timing Considerations – Parallel Mode (PXS = 1)

The MP3276 can be operated in the stand-alone mode, with one line for control and everything else hard-wired; or under microprocessor control, where changes can be made dynamically. There are 4 control lines: ADEN, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ with their functions described in *Table 1.*

PXS is the control pin for formatting data for serial or parallel control.

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	Comments
ADC Channel Select and Start Convert *(See Figure 1. and Table 2.)*							
1	X	X	X	—	0	0	No operation
0	↓	1	0	Hi-Z	0	0	No operation if ADEN = 0
0	↓	1	1	Hi-Z	↑	0	Input MUX channel selected, STL set on $\overline{WR}$ falling edge
0	0	1	X	Hi-Z	1	0	MUX select disabled
0	↑	1	X	Hi-Z	0	↑	Start convert on $\overline{WR}$ rising edge
0	1	1	X	Hi-Z	↓	↑	Start convert on STL falling edge
0	1	1	X	Hi-Z	0	↓	STS goes low at end of conversion
Read ADC Data – Parallel Output Mode (PXS = 1) *(See Figure 2. and Table 3.)*							
0	1	↓	X	—	0	0	Data outputs enabled
0	X	0	X	ADC	0	0	Data from previous conversion on data bus
0	X	↑	X	Hi-Z	0	0	Data outputs disabled
0	1	X	X	Hi-Z	0	1	Data/$\overline{RD}$ disabled while STS high
0	X	0	X	Last ADC	1	0	Data from last conversion on data bus
0	⊓	0	0	Hi-Z	0	↑	STL, MUX select disabled with ADEN = 0, data outputs disabled on STS rising edge
0	⊓	0	X	ADC	0	↓	New data appears on data bus on falling edge of STS

Note 1: If $\overline{RD}$ = 1, data outputs remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the data bus.

Table 1. Logic Truth Table for PXS = 1 (Parallel Mode)

The MP3276 is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the MP3276 control signals follows.

Figure 1. shows a complete timing diagram for the MP3276 convert start operation.

Either $\overline{WR}$ or $\overline{CS}$ may be used to initiate a conversion. We recommend using $\overline{WR}$ as used in *Figure 1.* It is quieter and has less propagation delay than $\overline{CS}$. If $\overline{CS}$ is used to trigger the conversion the specified set-up times will be longer.

A conversion is started by taking $\overline{WR}$ low, then high again (conversion is enabled on the rising edge of $\overline{WR}$). There are two possible conditions that will affect conversion timing.

1. ADEN = 1. At the falling edge of $\overline{WR}$, the input channel is determined by the data present on the address bits. The track and hold begins to settle after which STL returns low, indicating that the multiplexer and the buffer amp have settled to less than 1/2 LSB of final value. If the rising edge of $\overline{WR}$ returns high prior to STL going low, conversion will begin on the falling edge of STL. If the rising edge of $\overline{WR}$ is delayed until after STL returns low, the input signal is sampled and the conversion is started at the rising edge of $\overline{WR}$ giving the user better control of the sampling time.
2. ADEN = 0. At the falling edge of $\overline{WR}$ the data present at the address is ignored and the channel selected during the previous conversion remains selected. In this case the track and hold settling time is omitted and STL never goes high. At the rising edge of $\overline{WR}$ the input signal is sampled, and conversion is started.

There are two possible states that the data outputs could be in during a conversion.

1. If $\overline{RD}$ is held high during a conversion the outputs would remain high impedance throughout the conversion. This is the preferred method of operation as any noise present on the data bus is rejected.
2. If $\overline{RD}$ and $\overline{CS}$ are held low during a conversion, the data present will be from the previous conversion until the present conversion is completed when STS returns low. The data from the new conversion will appear on the outputs. The state of $\overline{RD}$ or $\overline{CS}$ should not change during a conversion.

Once a conversion is started and the STL or STS line goes high, convert start commands will be ignored until the conversion cycle is completed. The output data buffers cannot be enabled during conversion. In addition, all inputs and outputs which change during conversion can introduce noise, and should be avoided when possible.

3

ADC Write Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
ADC Control Timing					
$\overline{CS}$ to $\overline{WR}$ Set-Up Time	t_1	0	0	ns min	
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2	0	0	ns min	
Address to $\overline{WR}$ Set-Up Time	t_3	0	0	ns min	
Address to $\overline{WR}$ Hold Time	t_4	0	0	ns min	
$\overline{WR}$ Pulse Width	t_5	80	80	ns min	
ADEN to $\overline{WR}$ Set-Up Time	t_6		0	ns min	
ADC Conversion Timing					
$\overline{WR}$ to STL Delay	t_7	150	150	ns max	Load ckt of Figure 5, C_L = 20 pF, ADEN = 1
STL High (mux/amp settle)	t_8	10	15	µs max	Load ckt of Figure 5, C_L = 20 pF
STL to STS Low (Converting)	t_9	15	20	µs max	Load ckt of Figure 5, C_L = 20 pF
$\overline{WR}$ to STS High (ADEN = 0)	t_{12}	200	250	ns max	STL = 0 when ADEN = 0
$\overline{WR}$ to STS Low (ADEN = 1)	t_{10}	15	20	µs max	
STS High to Bus Relinquish Time	t_{13}	150	150	ns max	Load ckt of Figure 4
STS Low to Data Valid ($\overline{RD}$ = 0)	t_{14}	50	50	ns max	Load ckt of Figure 3, C_L = 20 pF

Table 2. ADC Write Timing
(See Figure 1.)

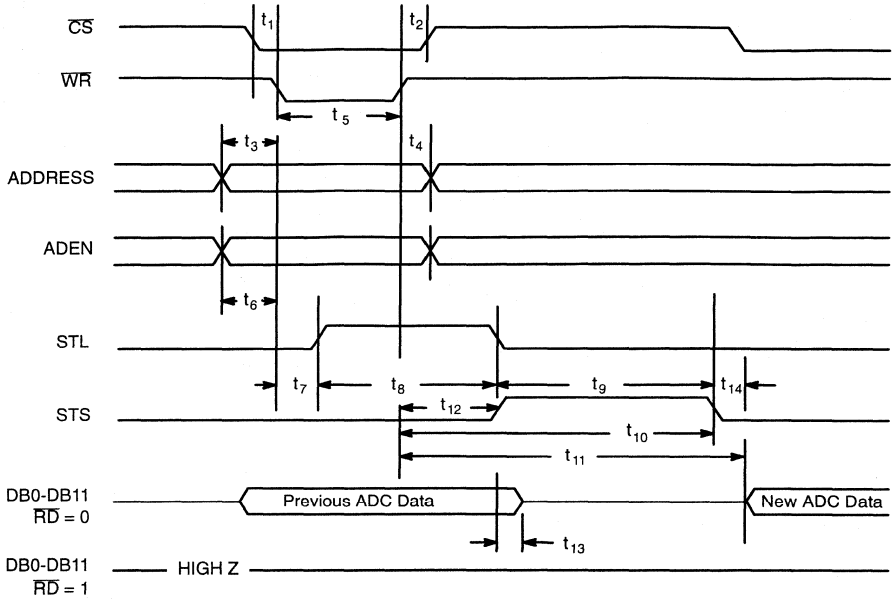


Figure 1. Timing for ADC Channel Select Start Conversion

ADC Read Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
$\overline{CS}$ to $\overline{RD}$ Set-Up Time	t_{15}	0	0	ns min	
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{16}	0	0	ns min	
$\overline{RD}$ to Data Valid Delay	t_{17}	100	150	ns max	Load ckt of *Figure 3.*, C_L = 20 pF
		150	200	ns max	Load ckt of *Figure 3.*, C_L = 100 pF
Bus Relinquish Time after $\overline{RD}$ High	t_{18}	100	150	ns max	Load ckt of *Figure 4.*
$\overline{RD}$ Pulse Width	t_{19}	100	150	ns min	Load ckt 4

Table 3. ADC Read Timing
(See Figure 2.)

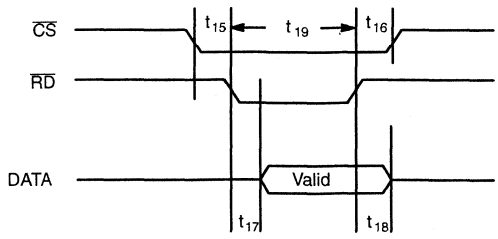
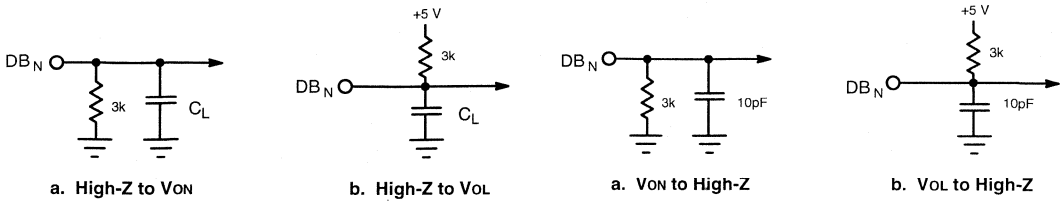


Figure 2. Timing for ADC Read



a. High-Z to VON b. High-Z to VOL a. VON to High-Z b. VOL to High-Z

Figure 3. Load Circuit for Data Access Time Test

Figure 4. Load Circuit for Bus Relinquish Time Test

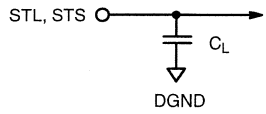


Figure 5. Load Circuit for $\overline{WR}$ to STS Delay

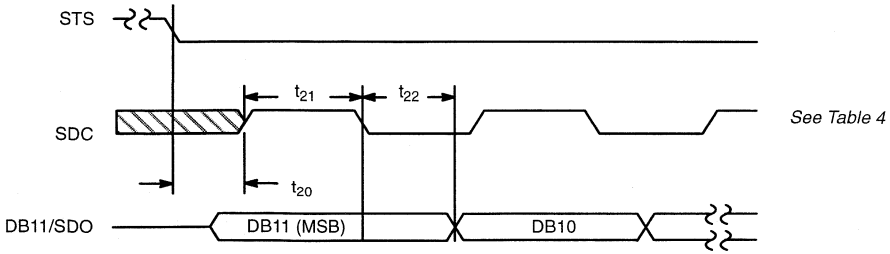
Serial Data Output Mode (PXS = 0)

The MP3276 output data is available in serial form when PXS = 0 prior to the $\overline{RD}$ high-to-low transition. When PXS = 0, the DB11/SDO pin functions as the serial data output. The DB0/SDC pin functions as the serial clock input and all other data outputs are 3-stated.

The serial data output sequence is MSB (DB11) first to LSB (DB0) last. The MSB (DB11) data bit appears at DB11/SDO when STS goes low. The second most significant bit appears at DB11/SDO on the next DB0/SDC high-to-low transition. The LSB (DB0) is present at DB11/SDO on the 11th SDC high-to-low transition.

The control pin functions (ADEN, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$) are the same as the parallel mode of operation. Further information regarding serial control and timing is shown in *Figure 6., Table 4.* and *Table 5.*

For a minimum interconnect serial environment, the channel address state can be generated in at least two ways, using an address counter, or using an address serial to parallel converter. $\overline{WR}$ can then be used as the counter clock or shift register load signal as well as the A/D converter start convert signal on the rising edge. (Note that the falling edge loads the address present at the address port.)



SDC should be in a high state during the STS high period. SDC can make the first high to low transition after t_{21}. In normal use it is assumed that PXS is hardwired low. However, if the mode of operation is changed, PXS must go low prior to $\overline{RD}$ going low.

Figure 6. Serial Data Mode Timing

Serial Data Output Timing	Time Interval	25°C	Tmin to Tmax	Limits	Comments/Test Conditions
STS low to SDO (DB11) Valid, $\overline{RD}$ = 0	t_{20}	50	50	ns max	Load Ckt 4 of *Figure 3.*
Minimum clock high pulse width	t_{21}	50	80	ns max	
SDC low to data valid delay	t_{22}	150	200	ns max	Load ckt of *Figure 3.*, C_L = 20pF
		200	250	ns max	Load ckt of *Figure 3.*, C_L = 100pF

Table 4. Serial Data Output Mode Timing (*See Figure 6.*)

$\overline{CS}$	PXS	$\overline{WR}$	$\overline{RD}$	ADEN	Data	STL	STS	DB0/SDC	Comments
ADC Channel Select and Start Convert									
1	X	X	X	X	—	0	0	X	No Operation
0	↓	X	1	X	Hi-Z	0	0	X	Serial mode enabled (1)
0	0	↓	1	0	Hi-Z	0	0	X	No operation if ADEN = 0
0	0	↓	1	1	Hi-Z	↑	0	X	Input MUX channel selected, STL set on falling edge of $\overline{WR}$
0	0	0	1	X	Hi-Z	1	0	X	MUX select disabled
0	0	↑	1	X	Hi-Z	0	↑	X	Start convert on $\overline{WR}$ rising edge
0	0	1	1	X	Hi-Z	↓	↑	X	Start convert on STL falling edge
0	0	1	1	X	Hi-Z	0	↓	X	STS goes low at end of conversion
Read ADC Data (*See Table 4. and Figure 6.*)									
0	0	1	↓	X	—	0	0	1	Serial output (DB11/SDO) and serial clock input (DB0/SDC) enabled
0	0	X	X	X	MSB (DB11)	0	0	1	MSB data available at DB11/SDO
0	0	X	0	X	DB10	0	0	↓	Next significant bit shifted out to DB11/SDO
0	0	X	0	X	DB10	0	0	0	No Operation
0	0	X	0	X	DB10	0	0	↑	No Operation
0	0	X	0	X	DB9	0	0	↓	Next significant bit shifted out to DB11/SDO
0	0	X	↑	X	Hi-Z	0	0	X	Data outputs/SDC input disabled
0	X	1	X	X	Hi-Z	0	1	X	Data outputs/$\overline{RD}$ disabled when STS = 1
0	X	⊓	0	0	Hi-Z	0	↑	1	STL, MUX select disabled when ADEN = 0
0	0	⊓	0	X	MSB (DB11)	0	↓	1	New data appears at DB11/SDO on falling edge of STS

Note 1: If $\overline{RD}$ = 1, data outputs remain high impedance. It is recommended that $\overline{RD}$ will not change during a conversion in order to reduce noise. It is further recommended that $\overline{RD}$ = 1 during conversion to reject any noise present on the data bus.

Table 5. Logic Truth Table – Serial Data Output Mode

2's Complement Output Code (Hexidecimal)						Ideal Transition Voltage
0111	1111	1110 (7fe) to	0111	1111	1111 (7ff)	+FS – 1 1/2 LSB
0000	0000	0000 (000) to	0000	0000	0001 (001)	0 V +1/2 LSB
1111	1111	1111 (fff) to	0000	0000	0000 (000)	0 V –1/2 LSB
1000	0000	0000(800) to	1000	0000	0001 (801)	–FS +1/2 LSB

Table 6. Key Output Codes vs. Input Voltage (2's Complement Code)

APPLICATION INFORMATION

The MP3276 is a complete A/D converter system, with its own built-in reference and clock. It may be used by itself ("stand-alone" operation), or it may be interfaced with a microprocessor which can control both conversion and formatting of output.

Successful application of the MP3276 requires careful attention to four main areas:

1) Physical layout.
2) Connection/Trimming according to mode of operation.
3) Conditioning of input signals.
4) Control and Timing considerations.

Physical Layout

The 12-bit accuracy of the MP3276 represents a dynamic range of 72dB. Precautions must be taken to avoid any interfering signals, whether conducted or radiated, to assure that this is not degraded.

- Avoid placing the chip and its analog signals near logic traces. In general, using a double sided printed circuit card with a good ground plane on the component side is recommended. Routing analog signals between ground traces will help isolate digital control logic. If these lines cross, do so at right angles. The GND Ref. is the positive terminal of the MUX/Instrumentation amplifier and will provide common mode noise rejection. It should be close to and shielded together with the channel inputs in order to take advantage of this feature.
- Power supplies should be quiet and well regulated. Grounds should be tied together at the package and back to the system ground with a single path. Bypass the supplies at the device with a 0.01 to 0.1μF ceramic cap and a 10-47 μF tantalum type, in parallel.

"Stand-Alone" Operation

The MP3276 can be used in "stand-alone" operation, which is useful in systems not requiring full computer bus interface capability. This operation is available for either parallel or serial mode.

For this operation, $\overline{CS}$ = 0, ADEN = 1, and conversion is controlled by $\overline{WR}$. The 3-state buffers are enabled when $\overline{RD}$ goes low. There are two possible conditions that the 3-state buffers could be in during a conversion. If $\overline{RD}$ goes low prior to $\overline{WR}$, the output buffers are enabled and the data from the previous conversion is available at the outputs during STL = 1. At the end of the present conversion which is initiated at the rising edge of $\overline{WR}$, STS returns low and the new conversion result is placed on the output data buffers.

If $\overline{WR}$ goes low prior to $\overline{RD}$, the data buffers remain in a high impedance state and conversion is initiated at the rising edge of $\overline{WR}$. Upon the end of the conversion the STS returns low and the conversion result is placed on the output data buffers. It is imperative that $\overline{RD}$ or $\overline{WR}$ not change during a conversion to insure that errors will not occur.

Ground Reference

The ground reference pin can be used for remote ground sensing of a common mode input signal with a maximum 6 V p-p around AGND.

This common input can also be used to dither each input's "zero". By averaging multiple conversions digitally, higher resolution for each input conversion can be obtained. Patterns for this dither can be a ramp, a stair step, or white noise.

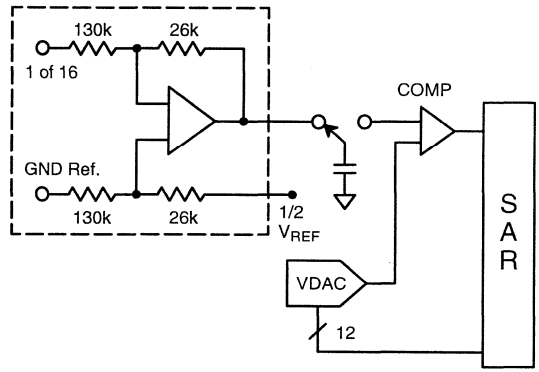


Figure 7. Equivalent Input Circuit

Quasi Differential Sampling

Method 1

For remote ground sensing where the remote ground does not change more than ±3 V from the A/D ground, connect GND Ref to the remote ground.

Method 2

Where Method 1 applies to each channel or group of channels, add a mux to allow connecting the appropriate ground to GND Ref.

Method 3

Use two parts. Tie both GND Ref pins together and connect this node to the "common" remote GND. Control the sample point by connecting each STL through an "OR" gate whose output is "NAND" connect with WR (inverted $\overline{WR}$). Use this output as $\overline{WR}$ to both $\overline{WR}$ inputs. By controlling the $\overline{WR}$, sample delay differences between the two converters is minimized. Two parts from the same date code will further minimize this difference. Treat one A/D as the (+) terminal and the other as the (–) terminal of the differential signal. Now the difference can be taken digitally.

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FEATURES

- **Sampling Rates from 0.001 to 15 MHz (MSPS)**
- **Interface to any Analog Input Range between GND and V_{DD}**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 Volt)**
- **Low Power CMOS (150 mW typ.)**
- **ESD Protection: 2000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

- **High Conversion Speed at Low Power**
- **Most Flexible Input Range of any A/D Available**
- **No Sample/Hold Needed**
- **Easy Ping-Ponging for 30 MSPS System**

3

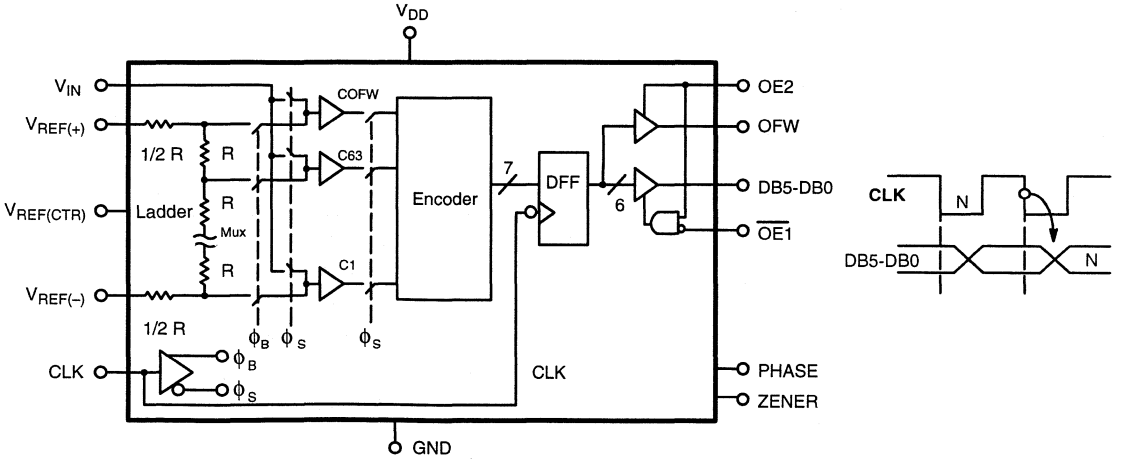
GENERAL DESCRIPTION

The MP7682 is a 6-bit monolithic CMOS single step flash Analog-to-Digital Converter designed for precision 6-bit applications in video, scanning and data acquisition requiring conversion rates to 15 MHz. Differential Linearity error is less than 1/2 LSB at 10 MHz, and power consumption is 150 mW, typical.

The MP7682 has a unique input architecture which eliminates the need for an input track and hold and allows full scale input ranges from about 1 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets $V_{REF(-)}$ and $V_{REF(+)}$ to encompass the desired input range.

MP7682 includes 64 auto-balanced clocked comparators, an encoder, 3-state output buffers, a reference resistor ladder, and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 7-bit resolution by connecting two devices in parallel. In normal operation this flag has no effect on the data bits.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

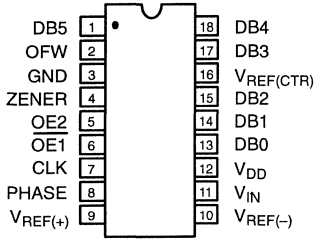


ORDERING INFORMATION

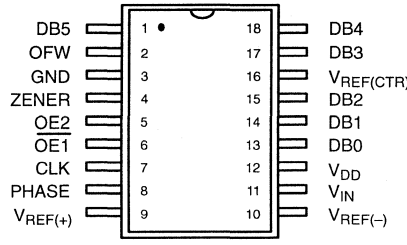
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7682JN	±2	±2
Plastic Dip	–40 to +85°C	MP7682KN	±1	±1
SOIC	–40 to +85°C	MP7682JS	±2	±2
SOIC	–40 to +85°C	MP7682KS	±1	±1
Ceramic Dip	–55 to +125°C	MP7682SD	±2	±2
Ceramic Dip	–55 to +125°C	MP7682TD	±1	±1

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin CDIP, PDIP (0.300")
D18, N18



18 Pin SOIC (0.300", Jedec)
S18

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB5	Data Output Bit 5 Output (MSB)
2	OFW	Digital Output Overflow
3	GND	Ground
4	ZENER	On Chip Zener Output
5	OE2	Output Enable Control
6	$\overline{OE1}$	Output Enable Control
7	CLK	Clock Input
8	PHASE	Sampling Clock Phase Control
9	$V_{REF(+)}$	Reference Voltage (+) Input

PIN NO.	NAME	DESCRIPTION
10	$V_{REF(-)}$	Reference Voltage (–) Input
11	V_{IN}	Analog Input
12	V_{DD}	Power Supply
13	DB0	Data Output Bit 0 Output (LSB)
14	DB1	Data Output Bit 1 Output
15	DB2	Data Output Bit 2 Output
16	$V_{REF(CTR)}$	R Ladder Mid Point
17	DB3	Data Output Bit 3 Output
18	DB4	Data Output Bit 4 Output

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, F_S = 15 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		6			6		Bits	
Sampling Rate	F_S	0.001		15	0.001	15	MHz	
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±1		±2	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			±1		±2	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		±1.7				LSB	
Full Scale Error	EFS		±1.7				LSB	
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±1	LSB	
Integral Non-Linearity	INL			±1/2		±1	LSB	Best Fit Line
Zero Scale Error	EZS		±1.7				LSB	
Full Scale Error	EFS		±1.7				LSB	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			5			V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Differential Ref. Voltage[3]	V_{REF}	1.0	V_{DD}-GND			V_{DD}-GND	V	
Ladder Resistance	R_L	175		500	150	600	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[2]								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		3				MΩ	
Input Capacitance Sample[5]	C_{INA}		30				pF	
Aperture Delay	t_{AP}		20				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		220				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			0.4		0.4	V	
Leakage Currents								V_{IN}=GND to V_{DD}
CLK	I_{IN}			±1		±30	µA	
OE2				±1		±30	µA	
$\overline{OE1}$				±1		±30	µA	
Phase				±1		±30	µA	
Input Capacitance[2]	C_{IND}		5				pF	
Clock Timing (*See NO TAG*)								
Clock Period	t_S	66					ns	
"High" Time	t_H	33					ns	
"Low" Time	t_L	33					ns	
Duty Cycle			50				%	

3

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								
Logical "1" Voltage	V_{OH}	4.3			4.3		V	I_{LOAD} = –1.0 mA
Logical "0" Voltage	V_{OL}			0.6		0.6	V	I_{LOAD} = 2.0 mA
3-state Leakage	I_{OZ}	±1			±20		µA	V_{OUT} = GND to V_{DD}
Data Valid Delay[2]	t_{DL}		66				ns	
Data Enable Delay[2]	t_{DEN}		20				ns	
Data 3-state Delay[2]	t_{DHZ}		26				ns	
Output Capacitance[2]	C_O		5				pF	
POWER SUPPLIES								
Operating Voltage	V_{DD}	4		6	4	6	V	
Current	I_{DD}		20	30		50	mA	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/64) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

Digital Inputs ..... GND –0.5 to V_{DD} +0.5 V

Digital Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

CDIP, PDIP, SOIC 850mW

Derates above 75°C ..... 11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

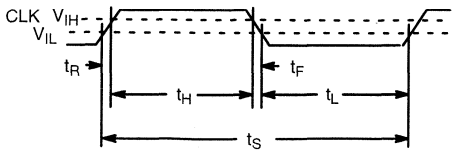


Figure 1. Clock Timing Specification ($t_R = t_F = 10$ ns typical)

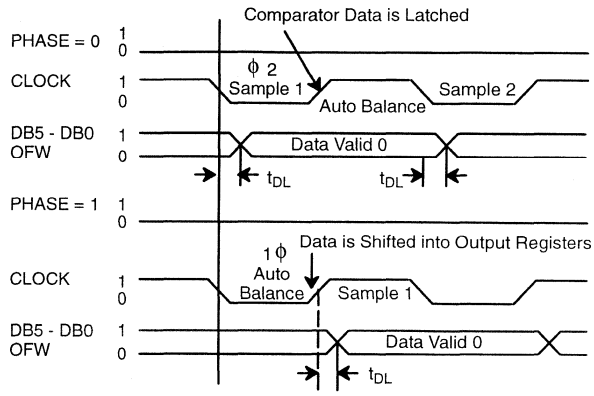


Figure 2. Data Line Enable Delay

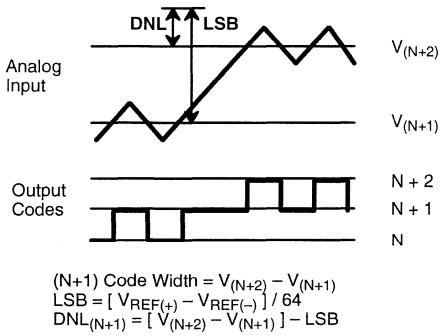


Figure 3. DNL Measurement

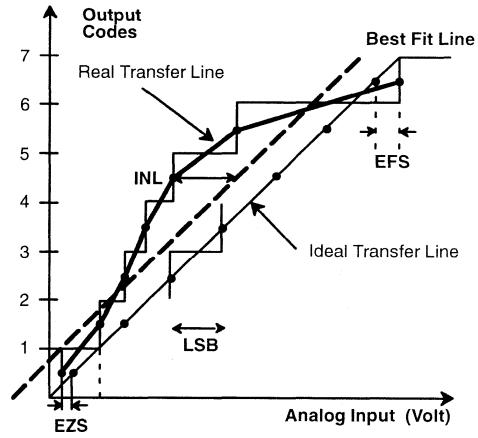


Figure 4. INL Error Calculation

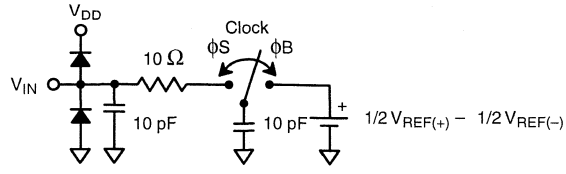


Figure 5. Analog Input Equivalent Circuit

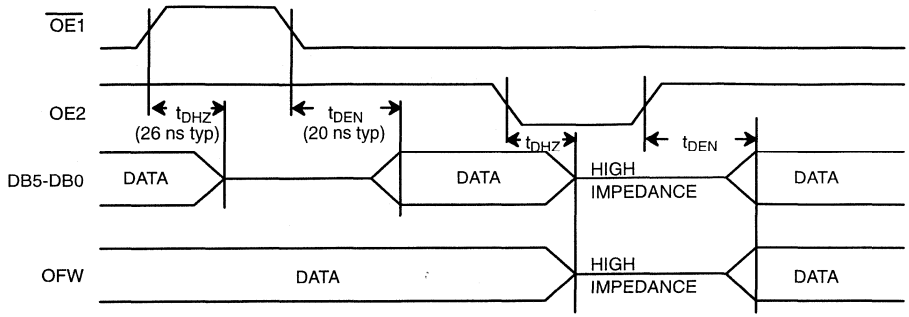


Figure 6. Output Enable and Disable Timing Diagram

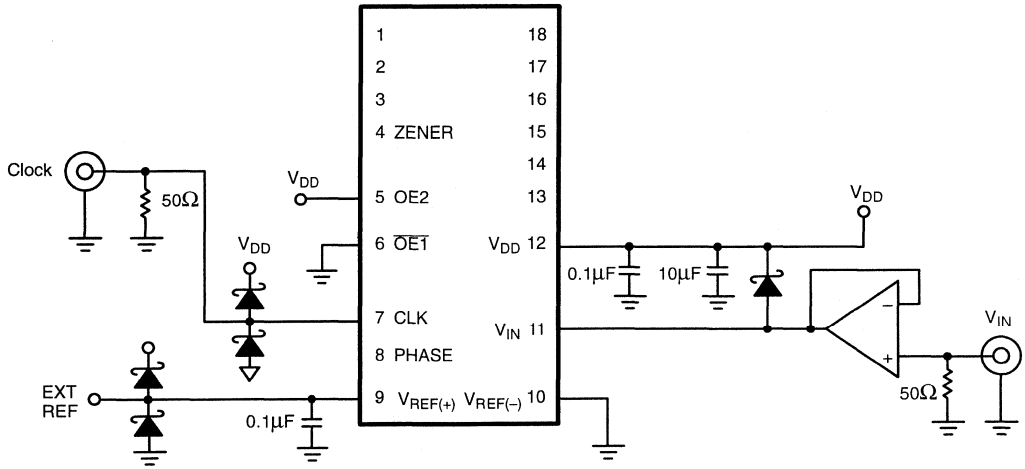
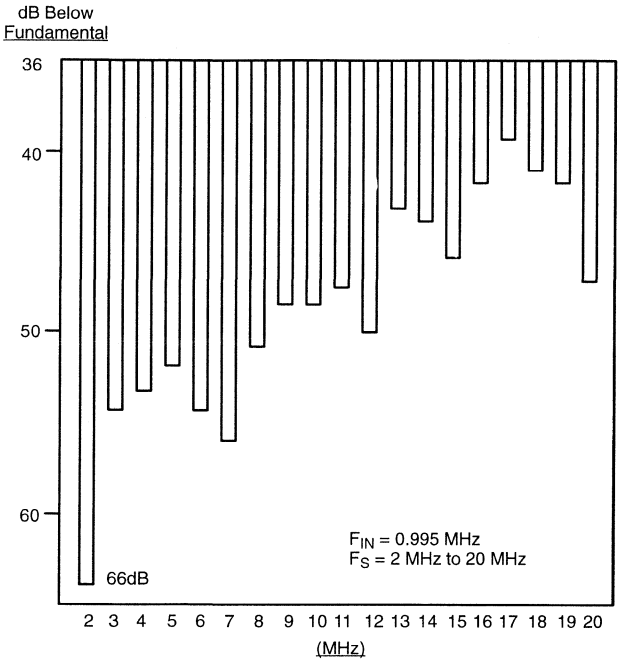


Figure 7. Typical Connections

$\overline{OE1}$	OE2	DB0 - DB5	OFW
0	1	Valid	Valid
1	1	3-State	Valid
X	0	3-State	3-State

Table 1. Truth Table



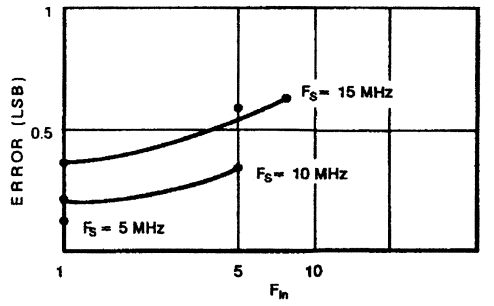


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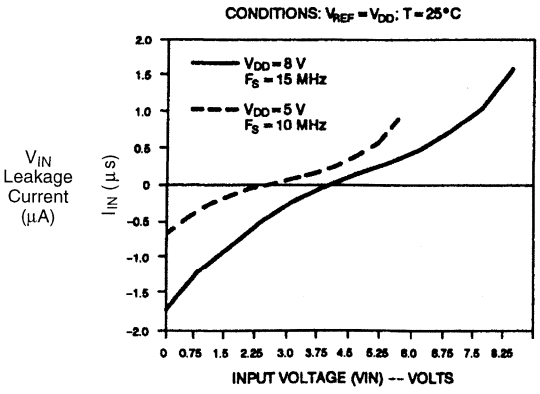
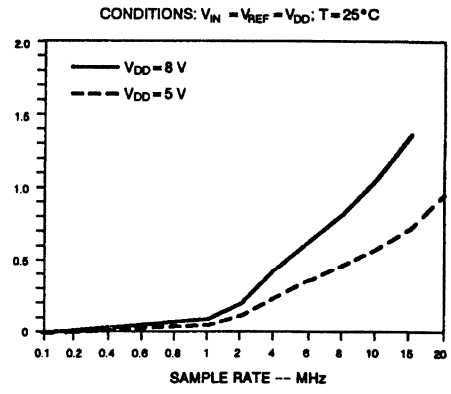
Figure 8. MP7682 Second Harmonic as a Function of Sample Rate



Graph 1. Analog Input Current vs. Input Voltage



Graph 2. Analog Input Current vs. Sample Rate

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MP7683

CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **3 MHz Sampling Rate**
- **Non-Linearity +1/4 LSB (typ) with S/H**
- **Low Power CMOS - 100mW (typ)**
- **Requires NO SAMPLE AND HOLD for signals less than 100 kHz**
- **Single Supply Voltage (+4 V to +6 V)**
- **Latch-Up Free**

APPLICATIONS

- **High Speed Low Power A/D Conversion**
- **Satellite Operations**
- **High Energy Physics Research**
- **Portable Products**
- **Radar Pulse Analysis**
- **µP Data Acquisition Systems**

3

GENERAL DESCRIPTION

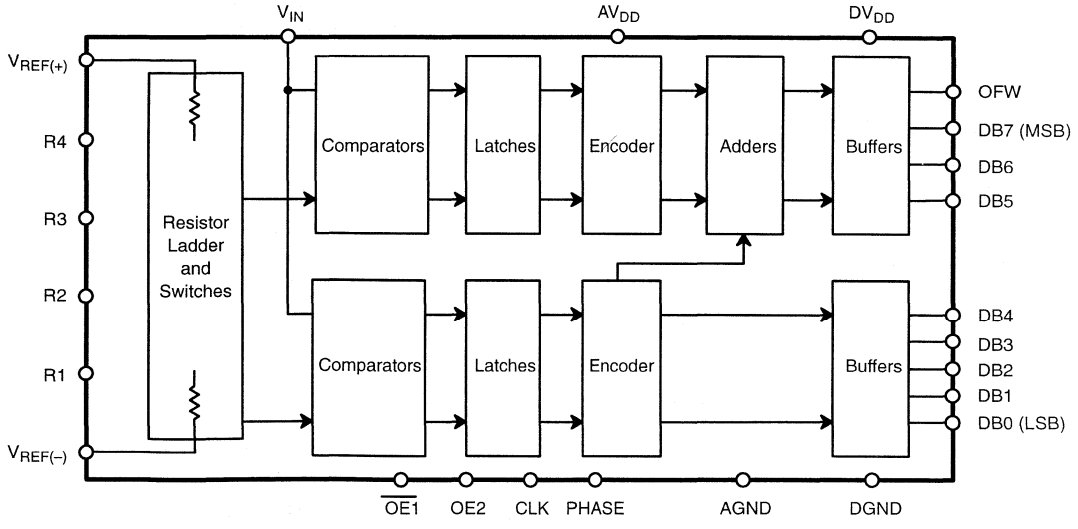
The MP7683 is a monolithic CMOS 8-bit two step flash Analog-to-Digital Converter designed for applications which demand Low Power Consumption and High Speed digitization (2 MHz sampling rate, 100mW power dissipation). The linearity error is 1/4 LSB (typical), with clock frequency of 2 MHz at a supply voltage of 5 volts.

The MP7683 conversion is done in two segments. The first segment converts the 3 MSBs and consists of eight (8) auto–balanced comparators, latches, an encoder, and four buffer storage registers. The second segment converts the five (5) LSBs and consists of 32 auto-balanced comparators, latches, an encoder, and five buffer storage registers. The MP7683 operates over a wide, full-scale input voltage range from 4.0 volts up to 6.5 volts, full-scale.

The overflow bit makes it possible to achieve 9-bit resolution by connecting two MP7683's in series. See *Figure 3.*

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7683 is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line, Shrunk Small Outline (SSOP) and Surface Mount (SOIC) packages.

SIMPLIFIED BLOCK DIAGRAM

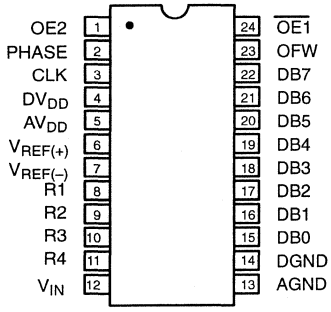


ORDERING INFORMATION

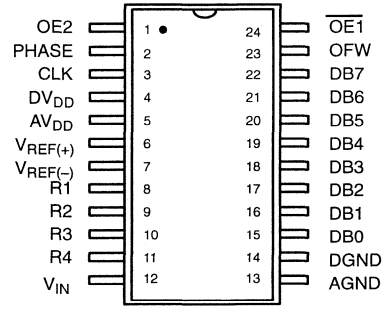
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7683JN	±1 1/4	1 1/4
Plastic Dip	–40 to +85°C	MP7683KN	±3/4	3/4
SOIC	–40 to +85°C	MP7683JS	±1 1/4	1 1/4
SOIC	–40 to +85°C	MP7683KS	±3/4	3/4
SSOP	–40 to +85°C	MP7683JQ	±1 1/4	1 1/4
SSOP	–40 to +85°C	MP7683KQ	±3/4	3/4
Ceramic Dip	–55 to +125°C	MP7683SD*	±1 1/4	1 1/4
Ceramic Dip	–55 to +125°C	MP7683TD*	±3/4	3/4

*Contact factory for non-compliant military processing

PIN CONFIGURATIONS



24 Pin CDIP, PDIP (0.600")
D24, N24



24 Pin SOIC (EIAJ, 0.335") - R24
24 Pin SSOP - A24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	OE2	Output Enable Control 2
2	PHASE	Sampling Clock Phase Control
3	CLK	Clock Input
4	DV_{DD}	Power Supply
5	AV_{DD}	Power Supply for Analog Circuit
6	$V_{REF(+)}$	Reference Voltage (+) Input
7	$V_{REF(-)}$	Reference Voltage (–) Input
8	R1	1/16th Point of Ladder R Matrix
9	R2	5/16th Point of Ladder R Matrix
10	R3	9/16th Point of Ladder R Matrix
11	R4	13/16th Point of Ladder R Matrix
12	V_{IN}	Analog Input

PIN NO.	NAME	DESCRIPTION
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DB0	Data Output Bit 0 (LSB)
16	DB1	Data Output Bit 1
17	DB2	Data Output Bit 2
18	DB3	Data Output Bit 3
19	DB4	Data Output Bit 4
20	DB5	Data Output Bit 5
21	DB6	Data Output Bit 6
22	DB7	Data Output Bit 7 (MSB)
23	OFW	Digital Output Overflow
24	$\overline{OE1}$	Output Enable Control 1

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 3 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	F_S	0.001		3	0.001	3	MHz	For specified accuracy
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±1		±1 1/4	LSB	
Integral Non-Linearity	INL			1		1 1/4	LSB	Best Fit Line (Max INL – Min INL) / 2
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±3/4	LSB	
Integral Non-Linearity	INL			1/2		3/4	LSB	Best Fit Line
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$	2	4.1	AV_{DD}	2	AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			AGND		V	
Differential Ref. Voltage[2]	V_{REF}	4.1		AV_{DD}-AGND	4.1	AV_{DD}-AGND	V	For specified accuracy
Ladder Resistance	R_L	500		1500	300	1950	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					2000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance[2]	Z_{IN}		10				MΩ	
Input Capacitance[4]	C_{INA}		50				pF	
Aperture Delay[2]	t_{AP}		55				ns	
Aperture Uncertainty (Jitter)[2]	t_{AJ}		200				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents[5]								V_{IN} = DGND to DV_{DD}
CLK	I_{IN}			±50		±50	µA	
Input Capacitance[2]	C_{IND}		5				pF	
Clock Timing (*See Figure 1.*)								
Clock Period	t_S	333					ns	
"High" Time	t_h	166.5					ns	
"Low" Time	t_l	166.5					ns	
Duty Cycle			50				%	

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.6			4.6		V	I_{LOAD} = –1.0 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 2.0 mA
Tristate Leakage	I_{OZ}			±50		±50	µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		55				ns	*(See Figure 1.)*
Data Enable Delay[2]	t_{DEN}		20				ns	*(See Figure 2.)*
Data Tristate Delay[2]	t_{DHZ}		26				ns	*(See Figure 2.)*
Output Capacitance[2]	C_O		5				pF	
POWER SUPPLIES								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}[6]	4		6.5	4	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			20		36	mA	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error. The INL error is the maximum distance (in LSB) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (F_S).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 See V_{IN} input equivalent circuit (*Figure 4*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to DV_{DD} and DGND.

6 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply loop.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +6.5 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
Digital Inputs ..... GND –0.5 to V_{DD} +0.5 V
Digital Outputs ..... GND –0.5 to V_{DD} +0.5 V
Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 1000mW
Derates above 75°C ..... 14mW/°C
SSOP 750mW
Derates above 75°C ..... 10mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

DEVICE OPERATION

Figure 1. shows the timing diagram of the MP7683 8-bit Flash Converter. A reference voltage is applied between the $V_{REF(+)}$ and $V_{REF(-)}$ which drives 256 resistors and switches with 4 voltage taps. These taps drive the inverting inputs of comparators. There are four control lines: Clock, $\overline{OE1}$, OE2, and Phase. The phase line determines the polarity of the clock.

Figure 2. shows waveforms with the phase line high and low. With 0 = 1, the "sample" occurs during the high period of the clock cycle and the "auto-balance" occurs during the low period of the clock. The "sample" is queued and pipelined through a series of registers and latches. It appears at the output after 2 clock periods and time delay (Td). After the sample is acquired the data is valid for every clock period. The $\overline{OE1}$ will independently disable DB0 through DB7 when it is in a high state. CE2 will independently disable DB0 through DB7 and the OFW buffers when it is in a low state. The Truth Table (*Table 1.*) summarizes this effect.

$\overline{OE1}$	OE2	DB7-DB0	OFW
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

Table 1. Truth Table

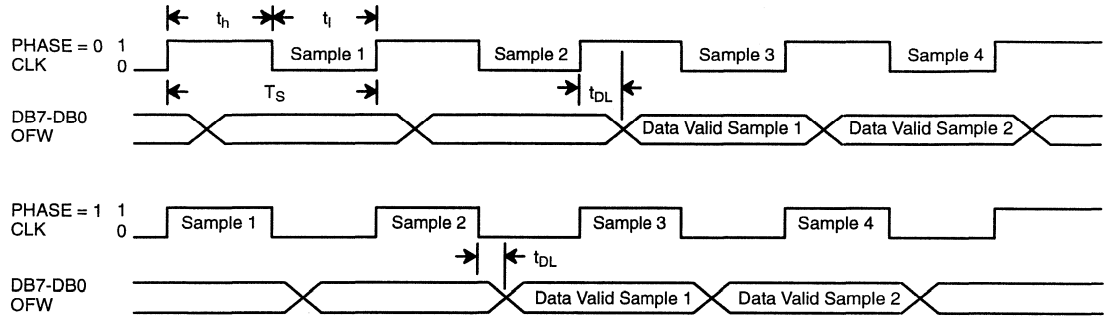


Figure 1. Timing Diagram

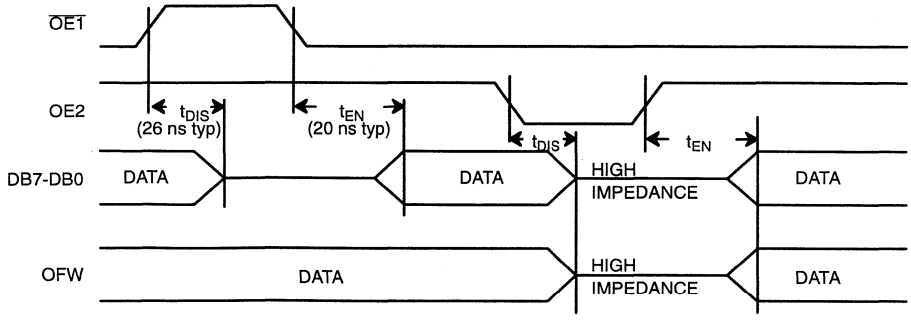


Figure 2. Output Enable and Disable Timing Diagram

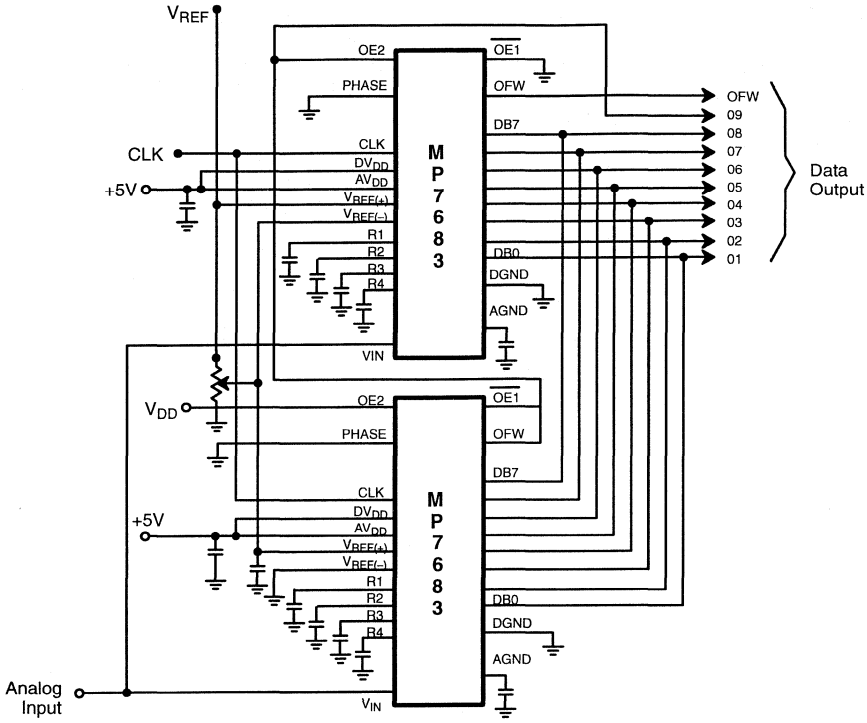


Figure 3. MP7683 9-Bit Resolution Configuration

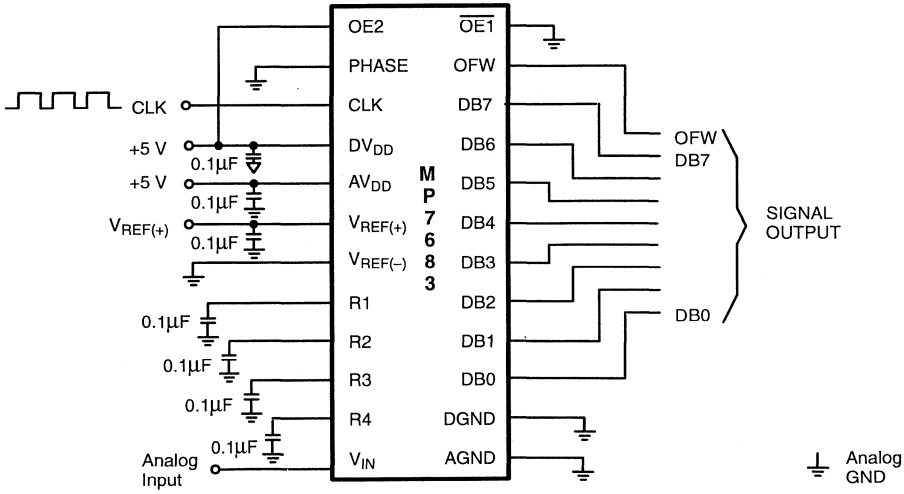
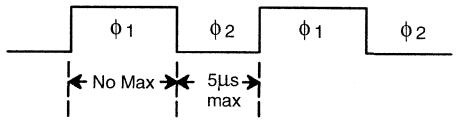


Figure 4. MP7683 Typical Connections

APPLICATION NOTES:

The following information will be useful in maximizing the performance of the MP7683.

1. This device may be susceptible to latch-up. All signals must not exceed AV_{DD} or AGND, or DV_{DD} or DGND at any time. Digital Supply (DV_{DD} & AV_{DD}) must be applied before all other signals to avoid a latch-up condition.
2. The design of a PC layout and assembly will seriously affect the accuracy of the MP7683. Use of wire wrap is not recommended.
3. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
4. The analog input should be driven with a buffer op amp ($Z_{OUT} \leq 50\ \Omega$).
5. The use of a large shield plane is highly recommended, connected only at one point and connected to virtual ground. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
6. The power supplies and reference voltages should be decoupled with ceramic (0.01 to 0.1µF) and tantalum (10µF) capacitors as close to the device as possible.
7. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.



   a. When at 50% Duty Cycle, the minimum clock rate is 100 kHz.
   b. When at non-50% Duty Cycle, the minimum clock rate may be DC as long as 2 is kept to less than 5 µs.
8. To avoid a possible latch-up condition, power should be applied before any input signal is connected.

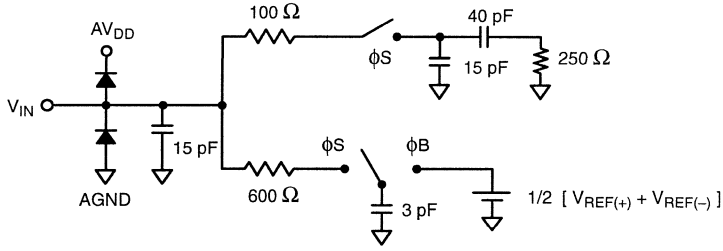
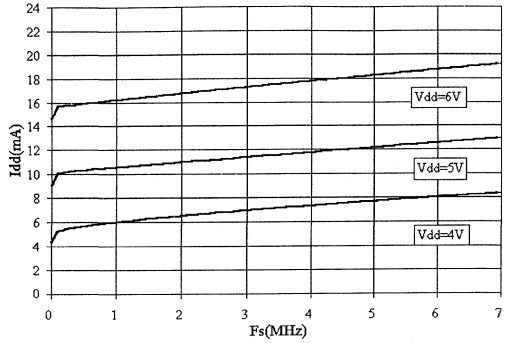
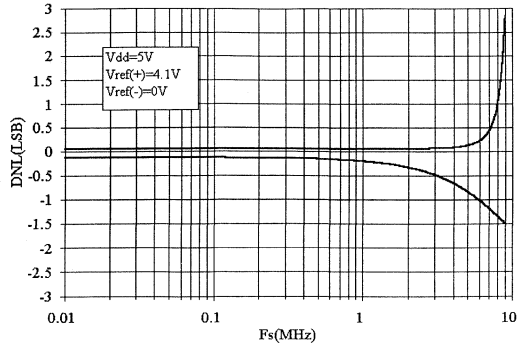


Figure 5. Analog Input Equivalent Circuit

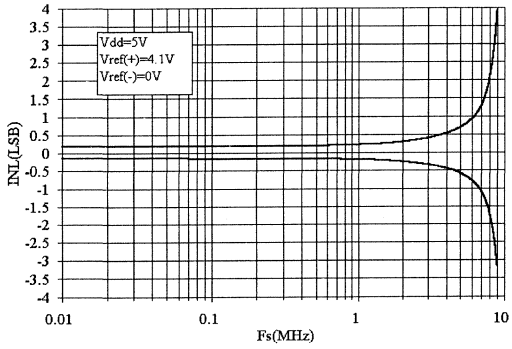
PERFORMANCE CHARACTERISTICS



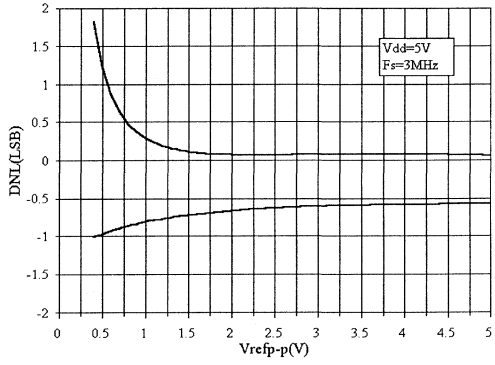
Graph 1. Supply Current vs. Sampling Frequency



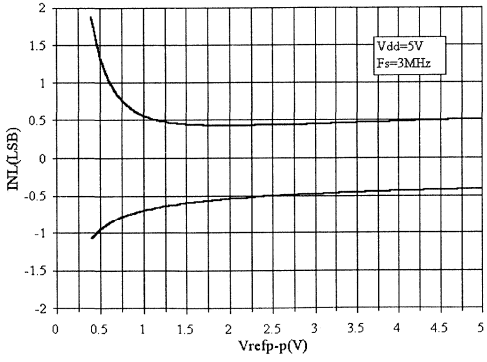
Graph 2. DNL vs. Sampling Frequency



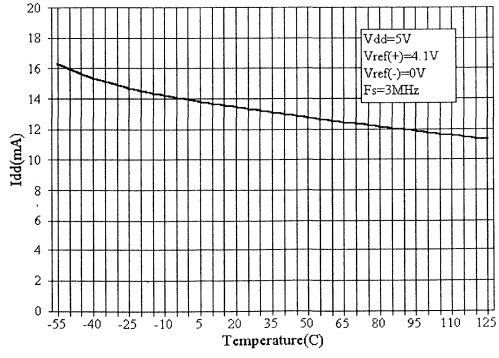
Graph 3. INL vs. Sampling Frequency



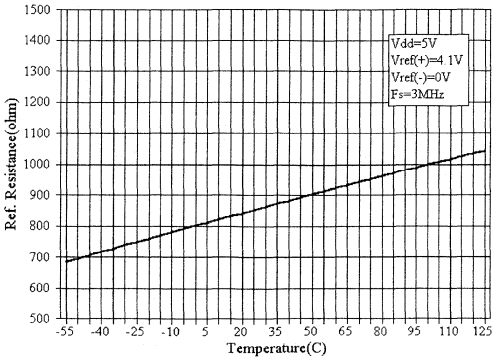
Graph 4. DNL vs. Reference Voltage



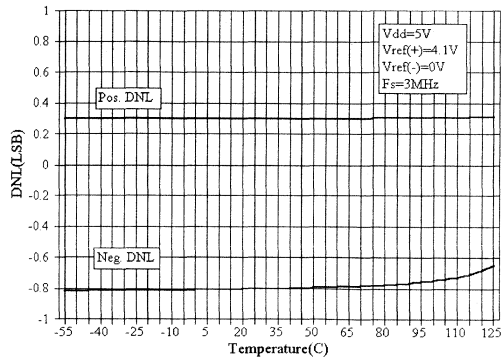
Graph 5. INL vs. Reference Voltage



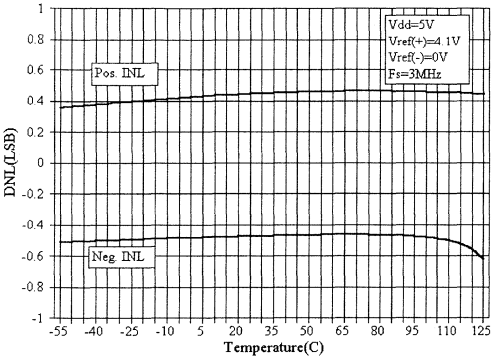
Graph 6. Supply Current vs. Temperature



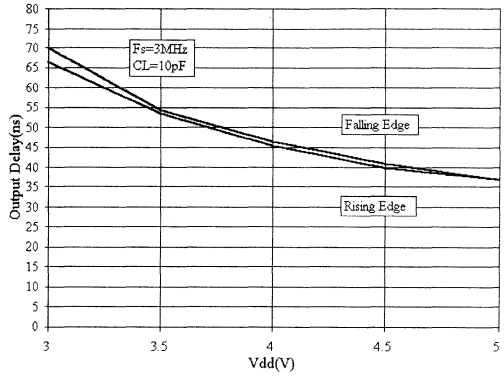
Graph 7. Reference Resistance vs. Temperature



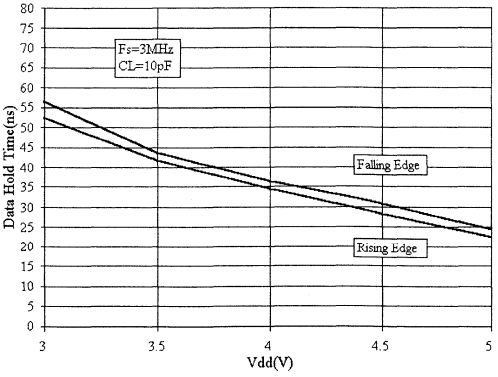
Graph 8. DNL vs. Temperature



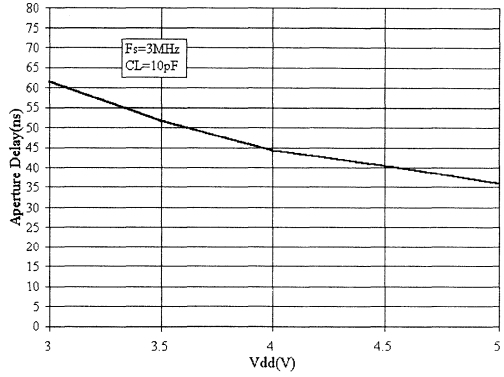
Graph 9. INL vs. Temperature



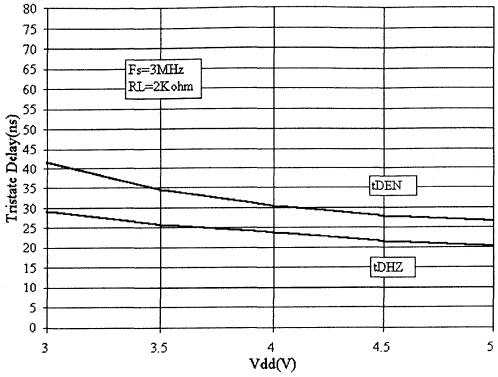
Graph 10. Output Delay vs. Supply Voltage



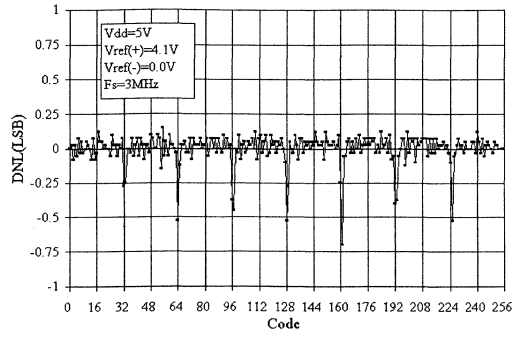
Graph 11. Data Hold Time vs. Supply Voltage



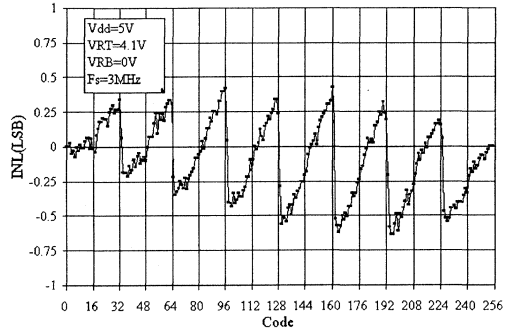
Graph 12. Aperture Delay vs. Supply Voltage



Graph 13. Tristate Enable Delay vs. Supply Voltage



Graph 14. DNL Error Plot



Graph 15. INL Error Plot

MP7684

CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 0.001 to 15 MHz (MSPS)**
- **1/2 LSB (K Grade) DNL to 6 MHz**
- **Interface to any Input Range between GND and V_{DD}**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 volt)**
- **Low Power CMOS (300 mW)**
- **2000 Volts ESD Protection**
- **Latch-Up Free**

BENEFITS

- **Low Power for Lower System Noise**
- **Most Flexible Input Range of any A/D Available**
- **No Sample/Hold Needed**
- **Use MP7684A for New Designs**

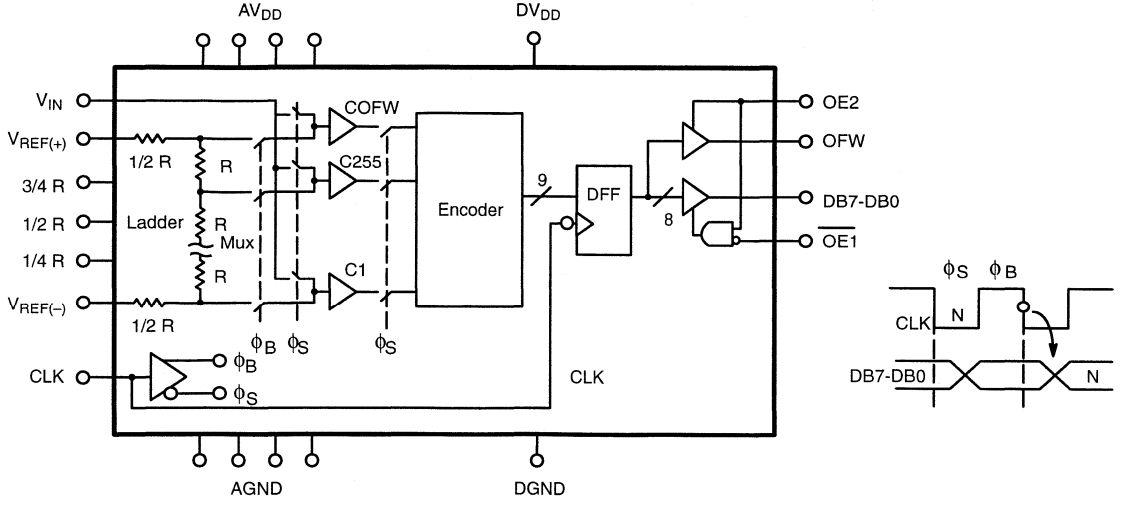
3

GENERAL DESCRIPTION

The MP7684 is an 8-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 10 MHz with differential linearity error less than 1/2 LSB and low power consumption. A unique feature of this converter is its input architecture which eliminates the need for an input track and hold and allows full scale input ranges from 1.2 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets $V_{REF(-)}$ and $V_{REF(+)}$ to encompass the desired input range.

The MP7684 includes 256 clocked comparators, encoders, 3-state output buffers, a reference resistor ladder and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 9-bit resolution by connecting two devices in parallel. In normal operation this flag has no effect on the data bits.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



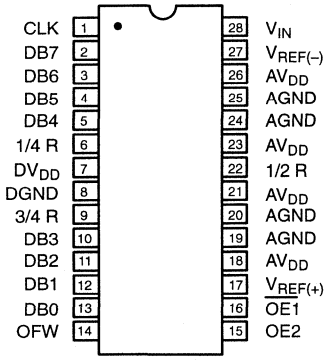
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7684JN	±1 1/2	2
Plastic Dip	–40 to +85°C	MP7684KN	±1	1 1/2
SOIC	–40 to +85°C	MP7684JS	±1 1/2	2
SOIC	–40 to +85°C	MP7684KS	±1	1 1/2
Ceramic Dip	–40 to +85°C	MP7684JD	±1 1/2	2
Ceramic Dip	–40 to +85°C	MP7684KD	±1	1 1/2
Ceramic Dip	–55 to +125°C	MP7684SD*	±1 1/2	2
Ceramic Dip	–55 to +125°C	MP7684TD*	±1	1 1/2

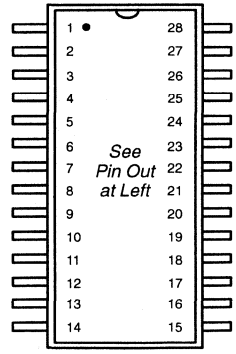
*Contact factory for availability

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP, CDIP (0.600")
N28, D28



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	CLK	Clock Input Pin
2	DB7	Data Output Bit 7 (MSB)
3	DB6	Data Output Bit 6
4	DB5	Data Output Bit 5
5	DB4	Data Output Bit 4
6	1/4R	1/4 of Resistance Ladder
7	DV_{DD}	Power Supply of Digital Circuit
8	DGND	Digital Ground
9	3/4R	3/4 of Resistance Ladder
10	DB3	Data Output Bit 3
11	DB2	Data Output Bit 2
12	DB1	Data Output Bit 1
13	DB0	Data Output Bit 0 (LSB)
14	OFW	Digital Output Overflow Pin
15	OE2	Output Enable Control Pin
16	$\overline{OE1}$	Output Enable Control Pin
17	$V_{REF(+)}$	Positive Reference Voltage Pin
18	AV_{DD}	Power Supply of Analog Circuit
19	AGND	Analog Circuit Ground
20	AGND	Analog Circuit Ground
21	AV_{DD}	Power Supply of Analog Circuit
22	1/2R	Center of Resistance Ladder
23	AV_{DD}	Power Supply of Analog Circuit
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Power Supply of Analog Circuit
27	$V_{REF(-)}$	Negative Reference Voltage Pin
28	V_{IN}	Analog Input

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 10 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)}$ = +4.1 V, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	F_S	0.1		6	0.1	6	MHz	For Specified Accuracy
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±3/4		±1 1/2	LSB	
Integral Non-Linearity	INL			1 1/2		2	LSB	Best Fit Line
(Relative Accuracy)								(Max INL – Min INL) / 2
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±1	LSB	
Integral Non-Linearity	INL			1		1 1/2	LSB	Best Fit Line
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
DYNAMIC ACCURACY[2]								Histogram Test
Differential Non-Linearity	DNL		±0.3				LSB	F_{IN} = 390 kHz
REFERENCE VOLTAGES								
Positive Ref. Voltage[3]	$V_{REF(+)}$			AV_{DD}		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			AGND		V	
Ladder Resistance	R_L	120		400	90	430	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[2]								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Capacitance Sample[4]	C_{IN}		50				pF	
Input Impedance	Z_{IN}		10				MΩ	
Aperture Delay	t_{AP}		25				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		60				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents[5]	I_{IN}							V_{IN}=DGND to DV_{DD}
CLK		–100		100		±100	µA	
$\overline{OE1}$[7]		–1		50	–1	75	µA	
OE2[6]		–60		1	–100	1	µA	
Input Capacitance[2]			5				pF	
Clock Timing (*See Figure 1.*)								
Duty Cycle			50				%	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.3			4.3		V	I_{LOAD} = –1.0 mA
Logical "0" Voltage	V_{OL}			0.6		0.6	V	I_{LOAD} = 2.0 mA
Off Current	I_{OFF}		±1	10		±1.5 (typ)	µA	
Output Capacitance[2]	C_O		5				pF	
3-state Leakage	I_{OZ}		1	10		10	µA	V_{OUT}=DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[2]	t_{HLD}		50				ns	
Data Valid Delay[2]	t_{DL}		55				ns	
Data Enable Delay[2]	t_{DEN}		40				ns	
Data 3-state Delay[2]	t_{DHZ}		40				ns	
POWER SUPPLIES[9] (Tmin to Tmax)								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4		6	4	6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			75		90	mA	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE1}$ has internal pull down. Input OE2 has internal pull up. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

6 Internal resistor to DV_{DD} biases unconnected input to active high logical level.

7 Internal resistor to GND biases unconnected input to active low logical level.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, LCC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

(3) V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

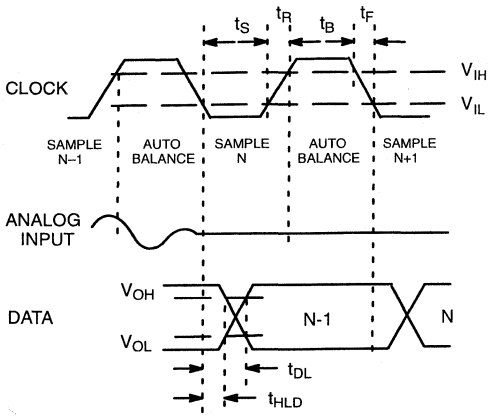


Figure 1. MP7684 Timing Diagram

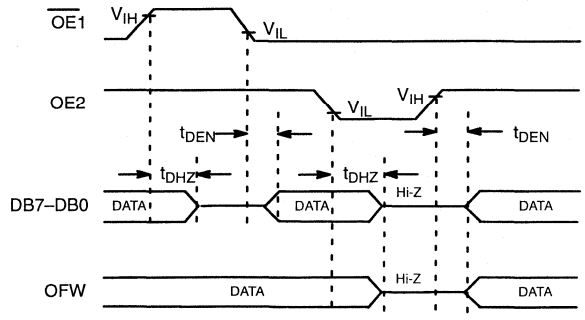
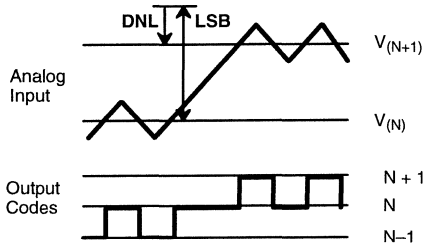


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$

Figure 3. DNL Measurement

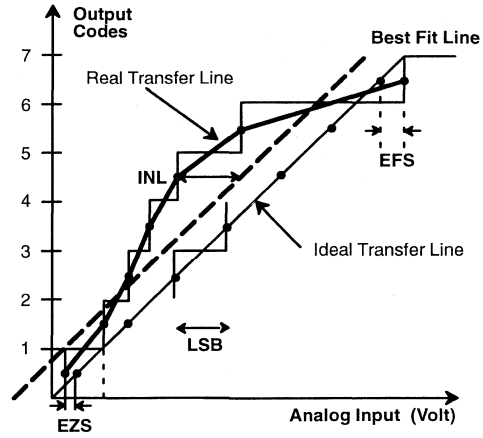


Figure 4. INL Error Calculation

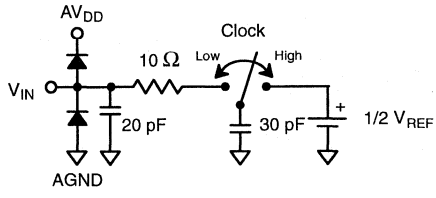


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7684 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $\quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

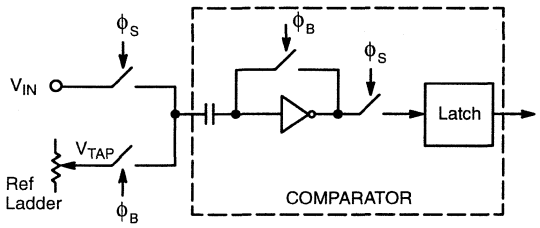


Figure 6. MP7684 Comparator

The MP7684 comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propagates the digital level to the encode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is if $(dv/dt) * t_{AJ} \approx V_{REF}/256$, an internal error of 1 LSB results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

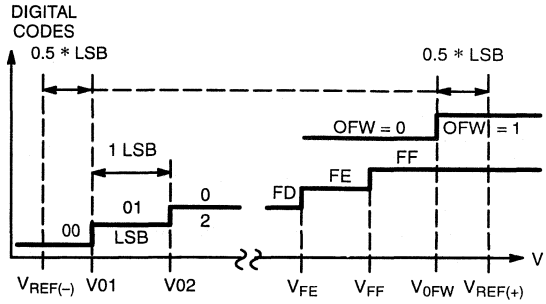


Figure 7. Ideal A/D Transfer Function

The overflow transition (V0FW) takes place at:

$V_{IN} = V_{0FW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V01 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(-)} - 1.5 * LSB$

$LSB = (V_{REF(+)} - V_{REF(-)} / 256 = (V_{FF} - V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

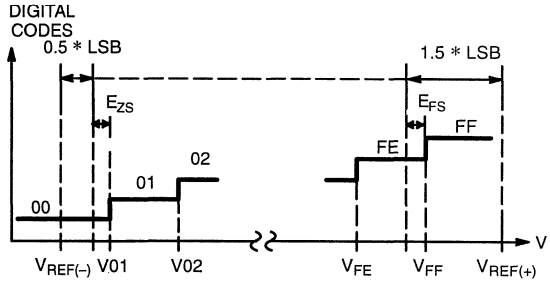


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every ($V_{REF(+)} - V_{REF(-)}$) / 256 volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 and 1.5

LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

EZS (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

Figure 4. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP7684, such adjustments have little impact at frequencies lower than 10 MHz. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. This may change an INL of –1 to +2 LSB's relative to the Ideal Line into a ±1.5 relative to the Best Fit Line.

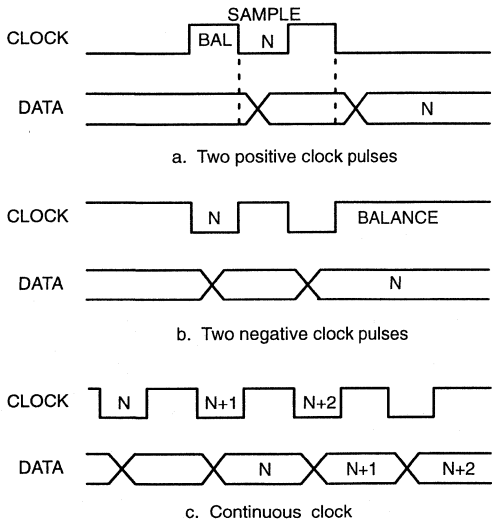


Figure 9. Relationship of Data to Clock

Clock Timing

A system will clock the MP7684 continuously (*Figure 9a.*) or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b.* keeps the MP7684 comparators in balance and ready to sample the analog input. This mode draws the most current from V_{DD}. The timing of *Figure 9c.* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

The MP7684 has very flexible input range characteristics. The user sets $V_{REF(+)}$ and $V_{REF(-)}$ to fixed voltages and then varies the input DC and AC levels to match the V_{REF} range.

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7684's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

Reference Voltages

If the input bandwidth is limited to the Nyquist region ($F_{IN} < F_S/2$) then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $F_S/2$, then it is recommended that VREF be lower than $V_{DD}/2$.

At V_{REF} = 1.5 V, the LSB is reduced to 6mV. Further reductions show an increased error in terms of LSB (which is getting smaller) even if the error in terms of mV remains constant.

The input/output relationship as a function of V_{REF}:

$$A_{IN} = (V_{IN} - V_{REF(-)})$$
$$DATA = 256 * (A_{IN}/V_{REF})$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range.** A system can increase dynamic range by using DAC's to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner), a first digitization would point to the input range in which most of the output codes fall. The system then would adjust the DACs to generate $V_{REF(+)}$ and $V_{REF(-)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution**. Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merging of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

$\overline{OE1}$	OE2	OFW	DB7 – DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If another DFF is to follow the ADC, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge, then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

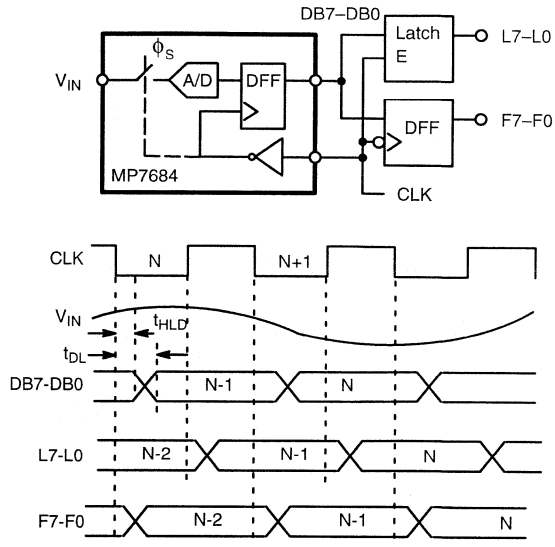


Figure 10. MP7684 Functional Equivalent Circuit and Interface Timing

3

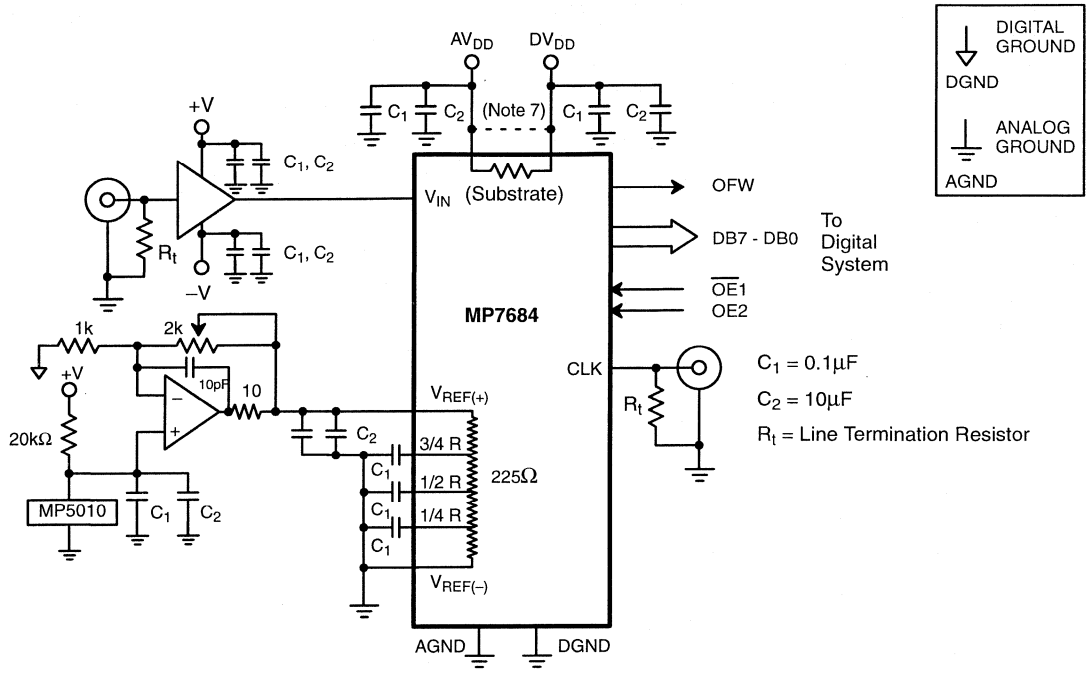
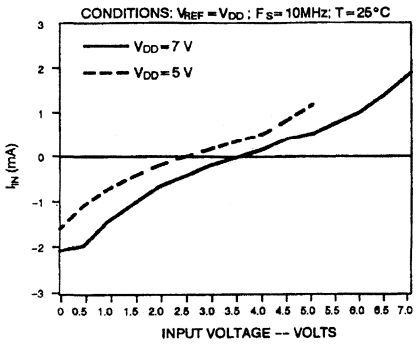


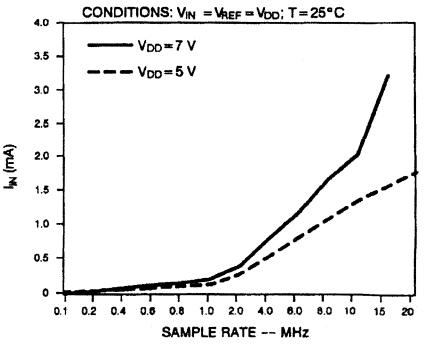
Figure 11. Typical Circuit Connections

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7684. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs to minimize cross coupling and noise pickup.
5. The analog input should be driven by a buffer op amp with as low output impedance as possible. The impedance should be less than 50Ω for clock frequencies above 10 MHz.
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
7. DV_{DD} should not be shared with other digital circuitry. DV_{DD} for the MP7684 should be connected to AV_{DD} next to the MP7684.
8. DV_{DD} and AV_{DD} are connected inside the MP7684 through the N – doped silicon substrate. DC voltage differences between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. The power supplies and reference voltages should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

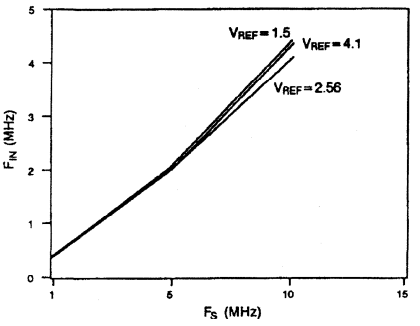
INPUT CURRENT vs. INPUT VOLTAGE



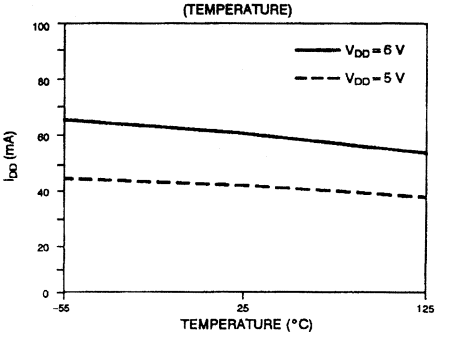
INPUT CURRENT vs. SAMPLE RATE



SMALL SIGNAL BANDWIDTH

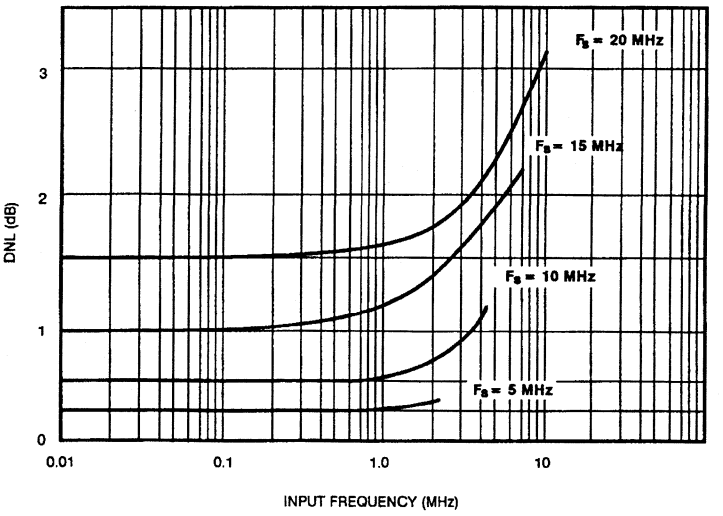


IDD (TEMPERATURE)

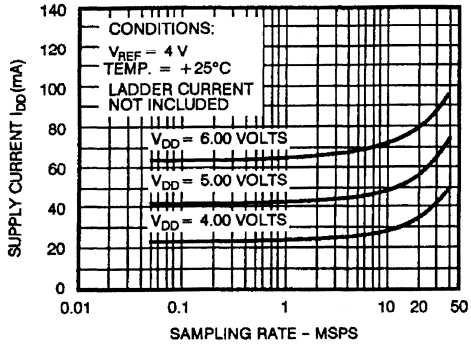


DNL VS. INPUT BANDWIDTH AS A FUNCTION OF SAMPLE RATE

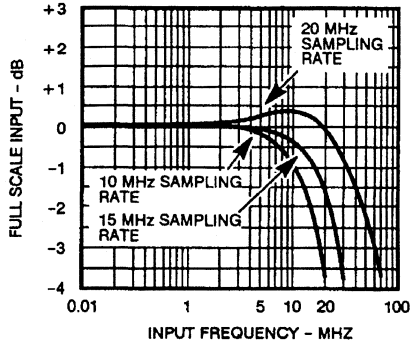
(DNL IS THE LARGEST ERROR APPEARING ON THE HISTOGRAM)



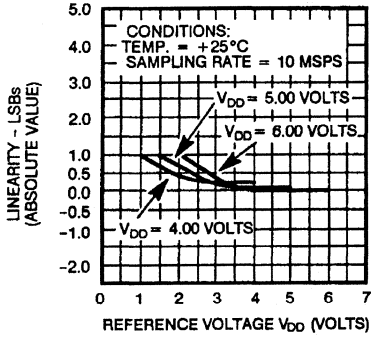
POWER CONSUMPTION
VS. SAMPLING RATE



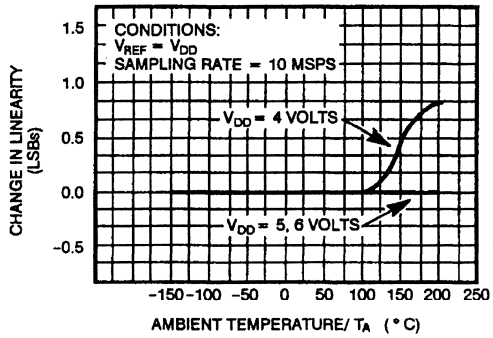
FULL SCALE INPUT VS. INPUT FREQUENCY
AS A FUNCTION OF SAMPLING RATE



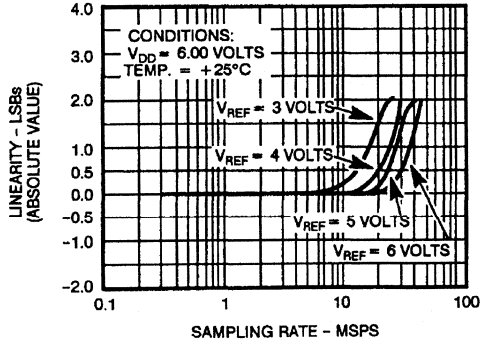
REFERENCE VOLTAGE
VS. LINEARITY



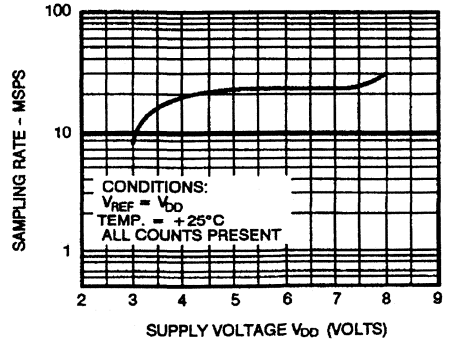
LINEARITY VS. TEMPERATURE
AS A FUNCTION OF V_{DD}



LINEARITY VS. SAMPLING RATE
AS A FUNCTION OF REFERENCE VOLTAGE



SAMPLING RATE
VS. SUPPLY VOLTAGE



MP7684A

CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 0.001 to 20 MHz (MSPS)**
- **1/4 LSB DNL from 0.001 to 10 MHz**
- **1/2 LSB DNL to 14 MHz**
- **Interface to any Input Range between GND and V_{DD}**
- **Pin Compatible Upgrade of MP7684**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 volt)**
- **Low Power CMOS (300 mW)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

- **Low Power for Lower System Noise**
- **Most Flexible Input Range of any A/D Available**
- **No Sample/Hold Needed**

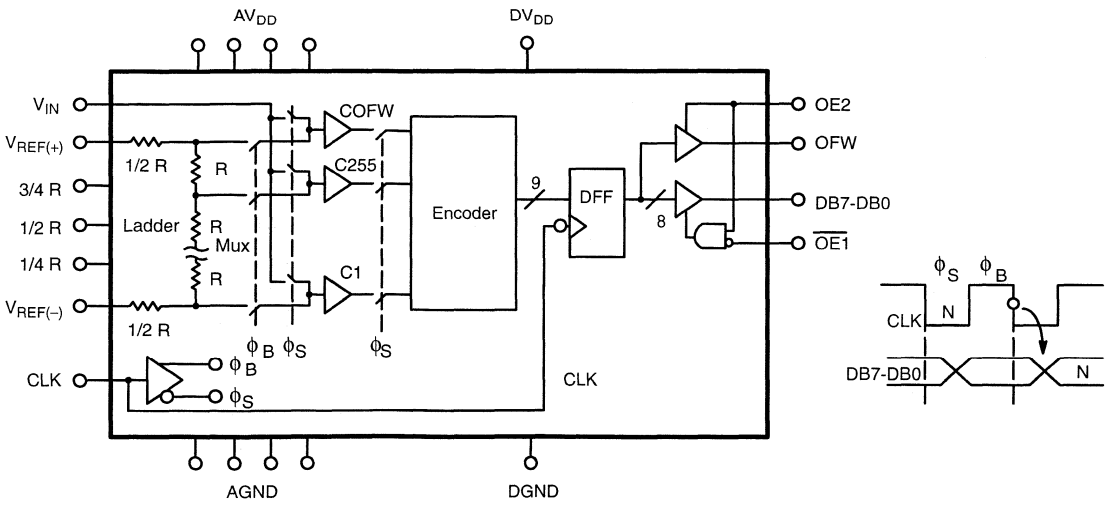
3

GENERAL DESCRIPTION

The MP7684A is an 8-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 14 MHz with differential linearity error less than 1/2 LSB and low power consumption. A unique feature of this converter is its input architecture which eliminates the need for an input track and hold and allows full scale input ranges from 1.2 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets $V_{REF(-)}$ and $V_{REF(+)}$ to encompass the desired input range.

The MP7684A includes 256 clocked comparators, encoders, 3-state output buffers, a reference resistor ladder and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 9-bit resolution by connecting two devices in parallel. In normal operation this flag has no effect on the data bits.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

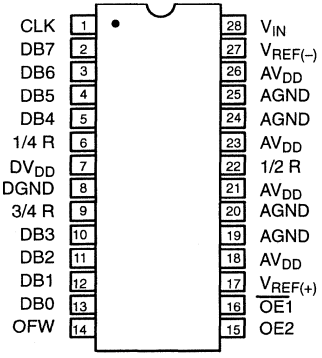


ORDERING INFORMATION

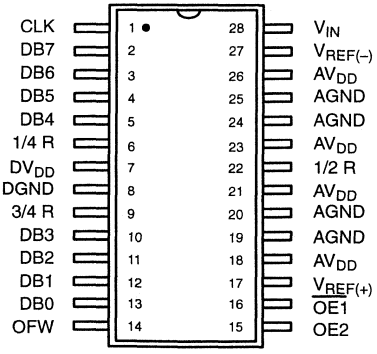
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7684AJN	±1	2
Plastic Dip	–40 to +85°C	MP7684AKN	±3/4	1 1/2
SOIC	–40 to +85°C	MP7684AJS	±1	2
SOIC	–40 to +85°C	MP7684AKS	±3/4	1 1/2
Ceramic Dip	–40 to +85°C	MP7684AJD	±1	2
Ceramic Dip	–40 to +85°C	MP7684AKD	±3/4	1 1/2
Ceramic Dip	–55 to +125°C	MP7684ASD	±1	2
Ceramic Dip	–55 to +125°C	MP7684ATD	±3/4	1 3/4

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP, CDIP (0.600")
N28, D28



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	CLK	Clock Input Pin
2	DB7	Output Data Bit 7 (MSB)
3	DB6	Output Data Bit 6
4	DB5	Output Data Bit 5
5	DB4	Output Data Bit 4
6	1/4R	1/4 Point of Resistance Ladder
7	DV_{DD}	Power Supply of Digital Circuit
8	DGND	Digital Ground
9	3/4R	3/4 Point of Resistance Ladder
10	DB3	Output Data Bit 3
11	DB2	Output Data Bit 2
12	DB1	Output Data Bit 1
13	DB0	Output Data Bit 0 (LSB)
14	OFW	Digital Output Overflow
15	OE2	Output Enable Control 2
16	$\overline{OE1}$	Output Enable Control 1
17	$V_{REF(+)}$	Positive Reference Voltage Pin
18	AV_{DD}	Power Supply of Analog Circuit
19	AGND	Analog Circuit Ground
20	AGND	Analog Circuit Ground
21	AV_{DD}	Power Supply of Analog Circuit
22	1/2R	Center of Resistance Ladder
23	AV_{DD}	Power Supply of Analog Circuit
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Power Supply of Analog Circuit
27	$V_{REF(-)}$	Negative Reference Voltage Pin
28	V_{IN}	Analog Input

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 14 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)}$ = 4.1 V, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8		Bits	
Sampling Rate	F_S	0.001		14	0.001	14	MHz	For Specified Accuracy
ACCURACY (J Grade)								
Differential Non-Linearity	DNL			±3/4		±1	LSB	
Integral Non-Linearity	INL			1 1/2		2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		30				mV	
Full Scale Error	EFS		15				mV	
ACCURACY (K Grade)								
Differential Non-Linearity	DNL		1/3	±1/2		±3/4	LSB	
Integral Non-Linearity	INL		4/5	1		1 1/2	LSB	Best Fit Line
Zero Scale Error	EZS		30				mV	
Full Scale Error	EFS		15				mV	
ACCURACY (S Grade)								
Differential Non-Linearity	DNL			±3/4		±1	LSB	
Integral Non-Linearity	INL			±1 1/2		±2	LSB	Best Fit Line
Zero Scale Error	EZS		30				mV	
Full Scale Error	EFS		15				mV	
ACCURACY (T Grade)								
Differential Non-Linearity	DNL		1/3	±1/2		±3/4	LSB	
Integral Non-Linearity	INL		4/5	±1		±1 3/4	LSB	Best Fit Line
Zero Scale Error	EZS		30				mV	
Full Scale Error	EFS		15				mV	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			AGND		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}-AGND	1.0	AV_{DD}-AGND	V	
Ladder Resistance	R_L	170	225	300	130	330	Ω	
Res. Temp. Coefficient[2] (Tmin to Tmax)	R_{TCO}					3000	ppm/°C	
ANALOG INPUT								
Input Voltage Range[12]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Capacitance[4]	C_{IN}		50				pF	
Aperture Delay[2]	t_{AP}		15				ns	
Aperture Uncertainty (Jitter)[2]	t_{AJ}		45				ps	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2			2		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Leakage Currents[5]	I_{IN}							V_{IN}=DGND to DV_{DD}
CLK		–10		10	–10	10	µA	
OE2[6]		–50		5	–50	5	µA	
$\overline{OE1}$[7]		–5		50	–5	50	µA	
Input Capacitance			5				pF	
Clock Timing (*See Figure 9.*)								
Clock Period[2]	t_S	50			50		ns	
Rise & Fall Time[8]	t_R, t_F			5		5	ns	
"High" Time (Auto-balance)	t_B	35					ns	No max limit
"Low" Time (Sampling)	t_S	35		500,000		500,000	ns	
DIGITAL OUTPUTS								(*See Fig. 1 & 2*) C_{OUT}=50 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			DV_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}	–10		10	–15	15	µA	V_{OUT}=DGND to DV_{DD}
Data Hold Time[2]	t_{HLD}	13	17		11		ns	
Data Valid Delay[2]	t_{DL}		25	33		35	ns	
Data Enable Delay[2]	t_{DEN}			20		25	ns	
Data 3-state Delay[2]	t_{DHZ}			20		25	ns	
POWER SUPPLIES								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4		6	4	6	V	(9)
Current (AV_{DD} + DV_{DD})	I_{DD}		50	80		85	mA	
AC PARAMETERS[2]								RMS/RMS Meas.
Signal Noise Ratio[10]	SNR		46				dB	F_S = 3X NTSC
	SNR		45				dB	F_S = 4X NTSC
Differential Gain Error	d_G		2				%	F_S = 3X NTSC
Differential Phase Error	d_{PH}		1				Degree	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 Guaranteed; Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE1}$ has internal pull down. Input OE2 has internal pull up. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

6 Internal resistor to DV_{DD} biases unconnected input to active high logical level.

7 Internal resistor to DGND biases unconnected input to active low logical level.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 DV_{DD} and AV_{DD} are connected through the silicon substrate. DC voltages differences will cause undesirable internal currents.

10 SNR: Ratio of fundamental over noise.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

CDIP, PDIP, SOIC, LCC 1050mW

Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

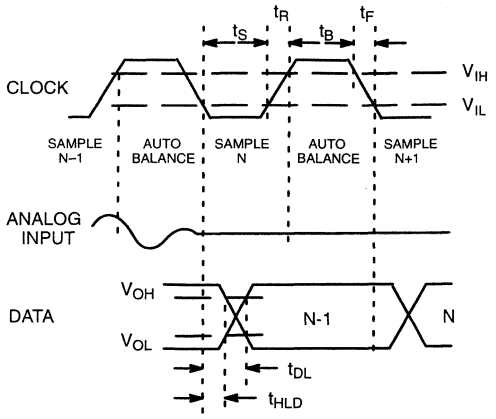


Figure 1. MP7684 Timing Diagram

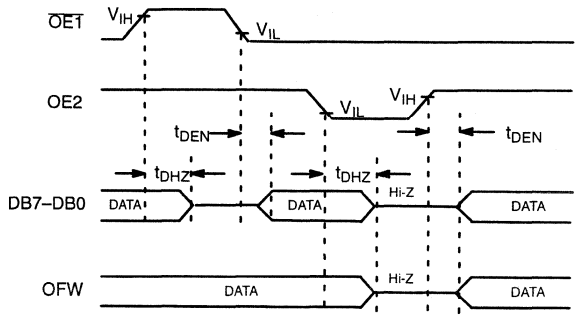
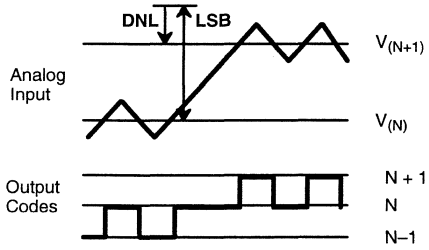


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

$$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$$

Figure 3. DNL Measurement

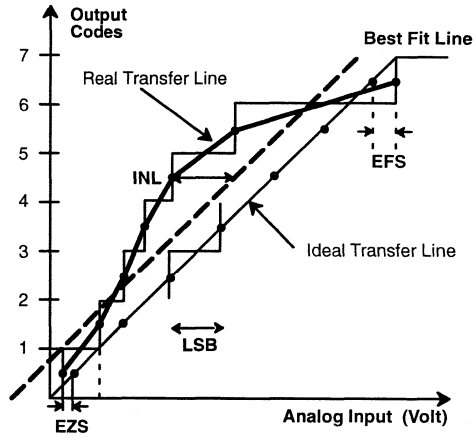


Figure 4. INL Error Calculation

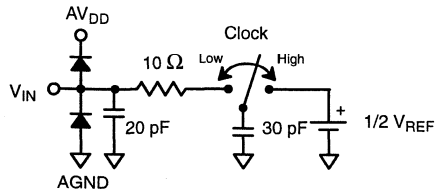


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7684A converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period at the same time the input is sampled.

The clock signal generates the two internal phases, ϕB (CLK high = balance) and ϕS (CLK low = sample). ϕB connects the comparators to the reference tap points. ϕS connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $\quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

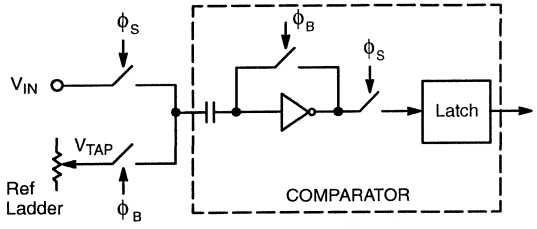


Figure 6. MP7684A Comparator

The MP7684A comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propogates the digital level to the encode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if $(dv/dt) * t_{AJ} \approx V_{REF}/256$, an internal error of 1 LSB of error results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

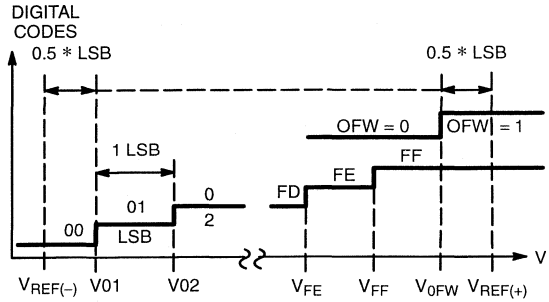


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{0FW}) takes place at:

$V_{IN} = V_{0FW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{REF} = (V_{REF(+)} - V_{REF(-)})$

$V_{IN} = V01 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 256 = (V_{FF} - V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

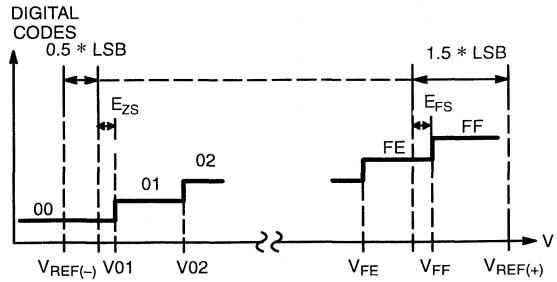


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every $V_{REF}/256$ volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are between the stated value. A specification of

Max DNL = ± 0.5 LSB means that all codes are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is between 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

EZS (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

Figure 4. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP7684A, such adjustments have little impact at frequencies lower than 10 MHz. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. This may change an INL of –1 to +2 LSB's relative to the Ideal Line into a ±1.5 relative to the Best Fit Line.

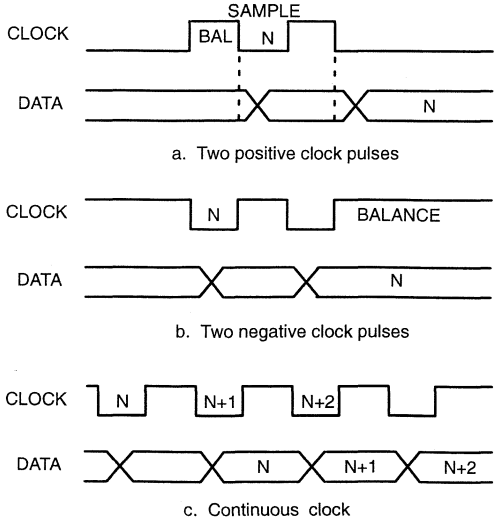


Figure 9. Relationship of Data to Clock

Clock Timing

A system will clock the MP7684A continuously *(Figure 9a.)* or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b.* keeps the MP7684A comparators in balance and ready to sample the analog input. This mode draws the most current from V_{DD}. The timing of *Figure 9c.* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

The MP7684A has very flexible input range characteristics. The user sets $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then varies the input DC and AC levels to match the V_{REF} range.

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7684's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

Reference Voltages

If the input bandwidth is limited to the Nyquist region ($F_{IN} < F_S/2$) then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $F_S/2$, then it is recommended that VREF be lower than $V_{DD}/2$.

At V_{REF} = 1.5 V, the LSB is reduced to 6mV. Further reductions show an increased error in terms of LSB (which is getting smaller) even if the error in terms of mV remains constant.

The input/output relationship as a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$DATA = 256 * (A_{IN}/V_{REF})$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range.** A system can increase dynamic range by using DACs to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner), the first digitization would point to the input range in which most of the output codes fall. The system then would adjust the DACs to generate $V_{REF(+)}$ and $V_{REF(-)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution**. Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merging of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

$\overline{OE1}$	OE2	OFW	DB7–DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If another DFF follows the ADC, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge, then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

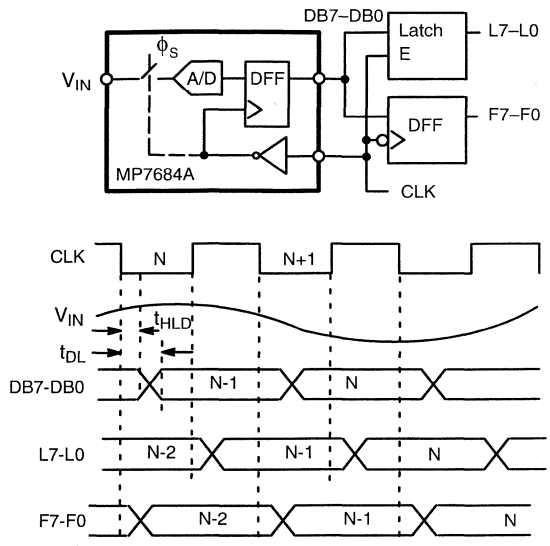


Figure 10. MP7684A Functional Equivalent Circuit and Interface Timing

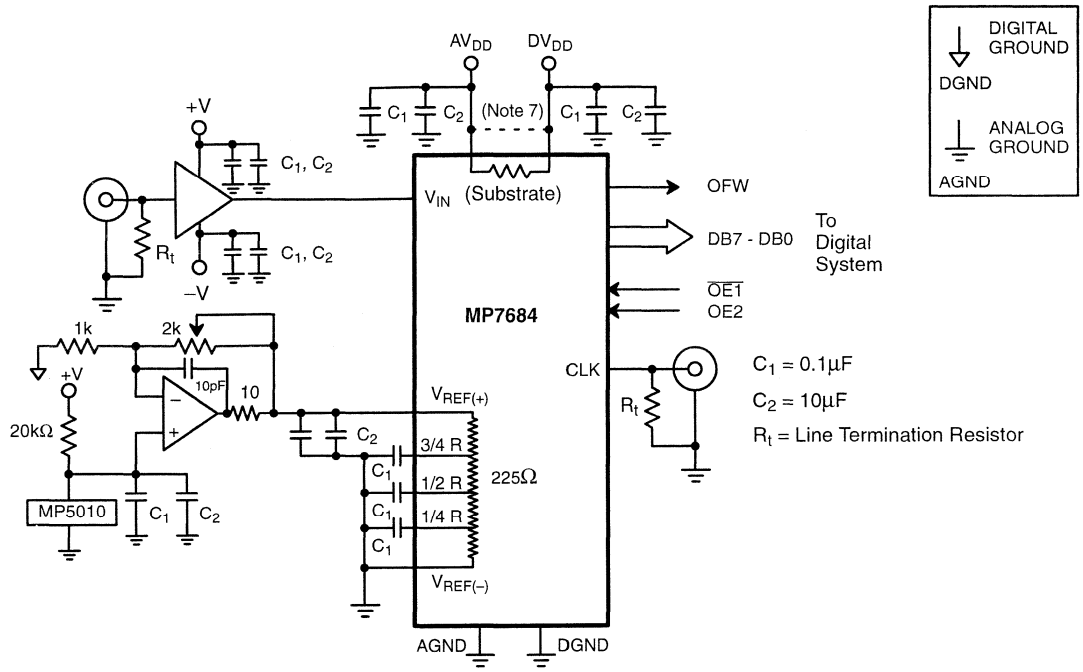
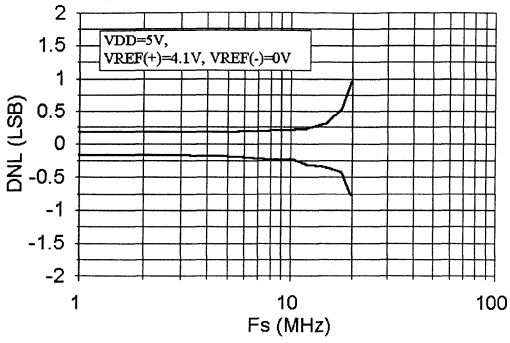


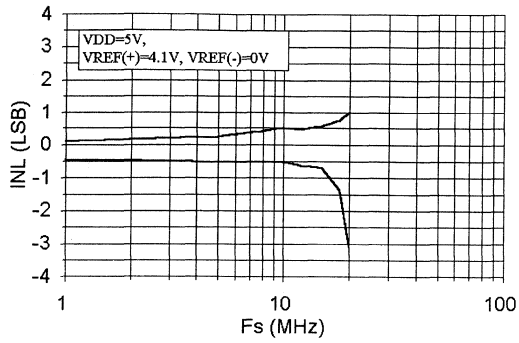
Figure 11. Typical Circuit Connections

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7684A. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs to minimize cross coupling and noise pickup.
5. The analog input should be driven by a buffer op amp with as low output impedance as possible. The impedance should be less than 50Ω for clock frequencies above 10 MHz.
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
7. DV_{DD} should not be shared with other digital circuitry. DV_{DD} should be connected to AV_{DD} next to the MP7684A.
8. DV_{DD} and AV_{DD} are connected inside the MP7684A through the N – doped silicon substrate. DC voltage differences between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. The power supplies and reference voltages should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitative coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

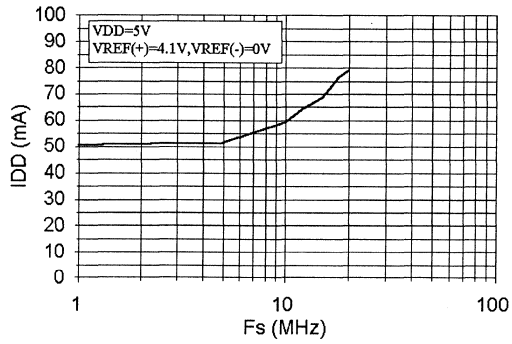
PERFORMANCE CHARACTERISTICS



Graph 1. DNL vs. Sampling Frequency



Graph 2. INL vs. Sampling Frequency



Graph 3. I_{DD} vs. Sampling Frequency

MP7686

CMOS
6-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 0.001 to 25 MHz (MSPS)**
- **Interface to any Input Range between GND and V_{DD}**
- **Pipeline Mode (Pin Compatible Upgrade of MP7682)**
- **One Shot Mode**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 volt)**
- **Low Power CMOS (135 mW typ.)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**
- **3 V Version: MP76L86**

BENEFITS

- **Highest Conversion Speed at Low Power**
- **Most Flexible Input Range of any A/D Available**
- **No Sample/Hold Needed**
- **Easy Ping-Ponging for 40 MSPS System**

3

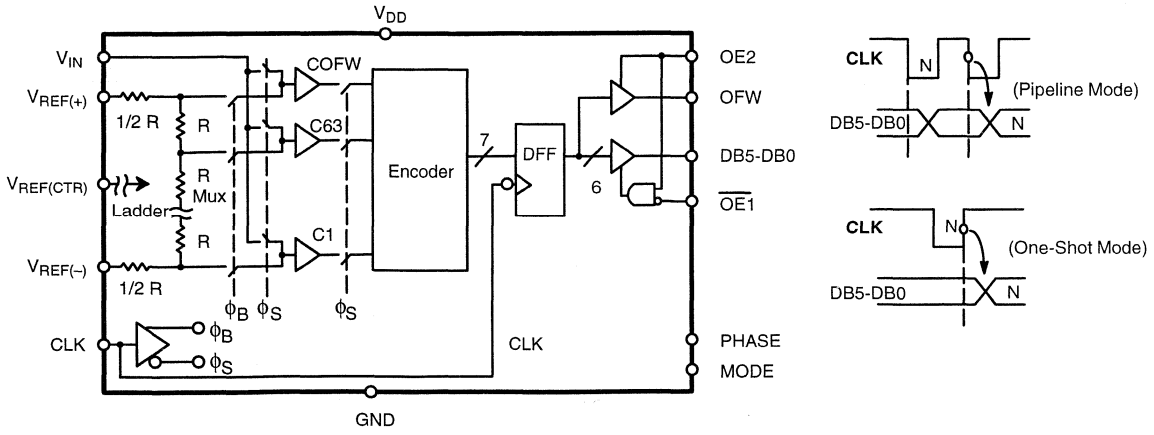
GENERAL DESCRIPTION

The MP7686 is a 6-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision 6-bit applications in video, scanning and data acquisition requiring conversion rates to 25 MHz. Differential Linearity error is less than 1/2 LSB at 20 MHz, and power consumption is 135 mW typical. A unique feature of this converter is its ability to do a complete conversion with just two clock edges (one clock pulse), by setting MODE low. When MODE is set high, the device behaves like a standard pipelined converter, requiring 3 clock edges (two clock pulses) to complete the conversion, compatible with the MP7682.

Another feature of MP7686 is its unique input architecture which eliminates the need for an input track and hold and allows full scale input ranges from about 1 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets $V_{REF(-)}$ and $V_{REF(+)}$ to encompass the desired input range.

MP7686 includes 64 auto-balanced clocked comparators, an encoder, 3-state output buffers, a reference resistor ladder, and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 7-bit resolution by connecting two devices in parallel. In normal operation, this flag has no effect on the data bits.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

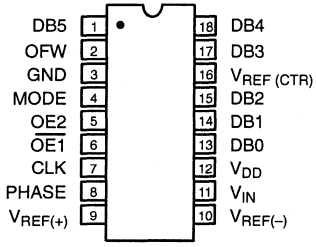


ORDERING INFORMATION

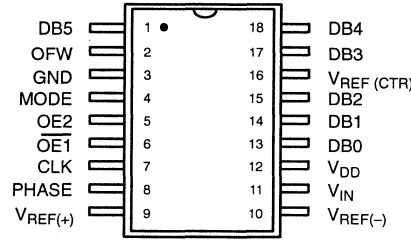
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7686JN	±1 1/4	2
Plastic Dip	–40 to +85°C	MP7686KN	±1	1 1/4
SOIC	–40 to +85°C	MP7686JS	±1 1/4	2
SOIC	–40 to +85°C	MP7686KS	±1	1 1/4
Ceramic Dip	–40 to +85°C	MP7686JD	±1 1/4	2
Ceramic Dip	–40 to +85°C	MP7686KD	±1	1 1/4

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin CDIP, PDIP (0.300")
D18, N18



18 Pin SOIC (Jedec, 0.300")
S18

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB5	Data Output Bit 5 (MSB)
2	OFW	Digital Output Overflow
3	GND	Ground
4	MODE	Mode Select
5	OE2	Output Enable Control
6	$\overline{OE1}$	Output Enable Control
7	CLK	Clock Input
8	PHASE	Sampling Clock Phase Control
9	$V_{REF(+)}$	Positive Reference Voltage Pin

PIN NO.	NAME	DESCRIPTION
10	$V_{REF(-)}$	Negative Reference Voltage Pin
11	V_{IN}	Analog Input
12	V_{DD}	Power Supply
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1
15	DB2	Data Output Bit 2
16	$V_{REF\ (CTR)}$	R Ladder Mid Point
17	DB3	Data Output Bit 3
18	DB4	Data Output Bit 4

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, F_S = 20 MHz (Duty Cycle: 1/3 Sample, 2/3 Balance), $V_{REF(+)}$ = 4.6, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		6			6		Bits	
Sampling Rate	F_S	0.001		20	0.001	15	MHz	For specified accuracy
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±3/4		±1 1/4	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			1 1/2		2	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		±2				LSB	
Full Scale Error	EFS		±2				LSB	
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±1	LSB	
Integral Non-Linearity	INL			1		1 1/4	LSB	Best Fit Line
Zero Scale Error	EZS		±2				LSB	
Full Scale Error	EFS		±2				LSB	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			V_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		V_{DD}-GND	1.0	V_{DD}-GND	V	
Ladder Resistance	R_L	175	230	270	160	300	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[2]								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Capacitance[5]	C_{IN}		20				pF	
Aperture Delay	t_{AP}		15				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		50				ps	
Clock Kickback Pulse			10				pAs	*See NO TAG*
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2			2		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Leakage Currents[6]	I_{IN}							V_{IN}=GND to V_{DD}
CLK		–1		1	–1	1	µA	
OE2		–20		1	–20	1	µA	
Phase		–20		1	–20	1	µA	
Mode		–20		1	–20	1	µA	
$\overline{OET}$		–1		20	–1	20	µA	
Input Capacitance[2]	C_{IND}		5				pF	
Clock Timing (*See NO TAG*)								
Clock Period	t_S	50			66		ns	
Rise & Fall Time	t_R, t_F			5		5		
"High" Time (Auto-Balance)	t_H	25			33		ns	Phase=0, Mode=1
"Low" Time (Sampling)	t_L	25		500,000	33	500,000	ns	Phase=0, Mode=1

3

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								
Logical "1" Voltage	V_{OH}	V_{DD}-0.5			V_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 2.0 mA
3-state Leakage	I_{OZ}	–10		10	–15	15	µA	V_{OUT} = GND to V_{DD}
Data Enable Delay	t_{DEN}		18	22		25	ns	
Data 3-state Delay	t_{DHZ}		18	22		25	ns	
Pipeline Mode (*See NO TAG*)								Phase=0, Mode=1
Data Hold Time[2]	t_{HLD}	15	22		15		ns	
Data Valid Delay[2]	t_{DL}		30	40		40	ns	
One-Shot Mode (*See NO TAG*)								Phase=0, Mode=0
Data Hold Time[2]	t_{HLD}	13	19		10		ns	
Data Valid Delay[2]	t_{DL}		30	37		40	ns	
POWER SUPPLIES								
Operating Voltage	V_{DD}	4		6	4	6	V	
Current	I_{DD}		27	35		40	mA	
AC PARAMETERS[2]								RMS/RMS Measures
Signal Noise Ratio[10]	SNR		36				dB	F_{IN} = 5 MHz
Harmonic Distortion								
Second Harmonic	2nd HD		35				–dB	F_{IN} = 1 MHz
Third Harmonic	3rd HD		35				–dB	F_{IN} = 5 MHz
Total Harmonic Distortion[12]	THD		29				–dB	F_{IN} = 5 MHz
Total Dynamic Error[11]	TDE		30				dB	F_{IN} = 5 MHz
Differential Gain Error	d_G		2				%	F_S = 3 x NTSC
Differential Phase Error	d_{PH}		1				Degree	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/64) is the DNL error (*NO TAG*). The INL error is the maximum distance (in LSBs) from the Best Fit Line to any transition voltage (*NO TAG*). Accuracy is a function of the sampling rate (F_S).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 Input bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
BW calculation: $BW = V_{OUT} / V_{IN}$
$V_{OUT} = V_{REF} * (CODE_{MAX} - CODE_{MIN}) / 64$

5 See V_{IN} input equivalent circuit (*NO TAG*) for high sampling rates. Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to V_{DD} and GND. Inputs OE2, Phase, Mode have internal pull ups. Input OE1 has internal pull down. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

7 Internal resistor to V_{DD} biases unconnected input to active high logical level.

8 Internal resistor to GND biases unconnected input to active low logical level.

9 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

10 SNR: Ratio of fundamental over noise.

11 TDE: Ratio of fundamental over noise + harmonics (2nd to 9th).

12 THD: Ratio of harmonics (2nd to 9th) over fundamental.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND	+7 V
$V_{REF(+)}$ & $V_{REF(-)}$	GND –0.5 to V_{DD} +0.5 V
V_{IN}	GND –0.5 to V_{DD} +0.5 V
Digital Inputs	GND –0.5 to V_{DD} +0.5 V
Digital Outputs	GND –0.5 to V_{DD} +0.5 V
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering 10 seconds)	+300°C
Package Power Dissipation Rating to 75°C	
CDIP, PDIP, SOIC	850mW
Derates above 75°C	11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

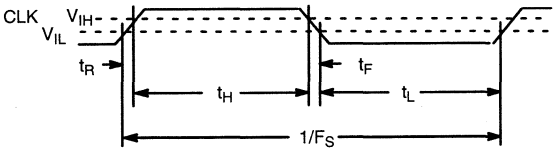


Figure 1. Clock Timing Specification

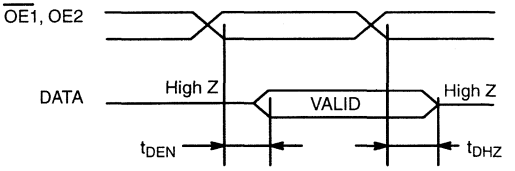


Figure 2. Data Line Enable Delay

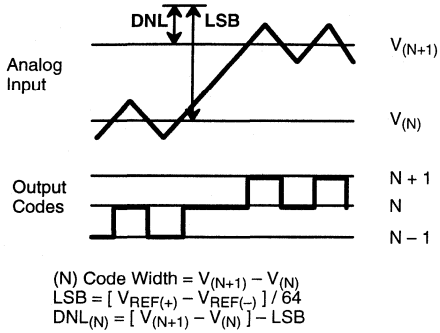


Figure 3. DNL Measurement

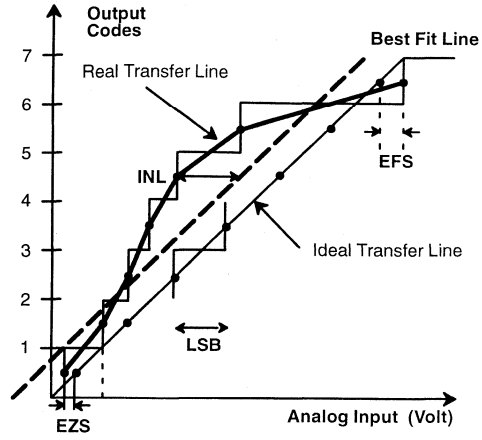


Figure 4. INL Error Calculation

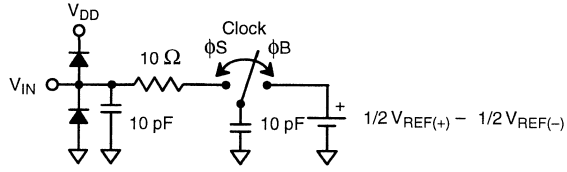


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

The MP7686 has three operating modes. It has two pipelined modes (MP7682 compatible), and a one shot mode. The voltages applied to the Phase and Mode pins determine the operating mode. *Figures 1 through 7* show the timing specifications. Timing parameters are measured to and from valid logic levels (i.e. t_{DH} is the time from CLK = 0.8 V to DATA = 0.4 or 2.4V).

Pipeline Modes (Mode = High)

In this configuration, the MP7686 works in a continuous fashion (MP7682 compatible). *NO TAG* shows the timing with the Phase pin high and low. When Phase is low, "sampling" occurs during the low period of the clock, and "balancing" during the high period. When Phase is high, operation is reversed (see *NO TAG*), "sampling" occurs during the high period and "balancing" during the low period. The actual time when the internal comparators are connected to V_{IN} is called the Acquisition Time. This time is equal to the sample phase of the external clock delayed by t_{AD} and t_{AP}.

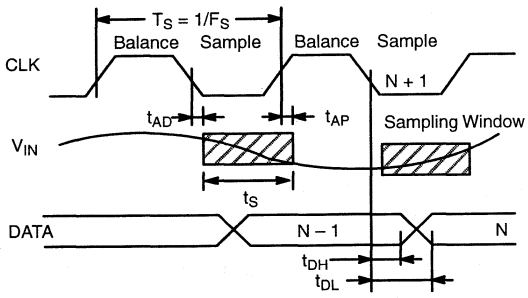


Figure 6. Pipeline Mode Timing (7682 compatible)
(Phase = 0, Mode = 1)

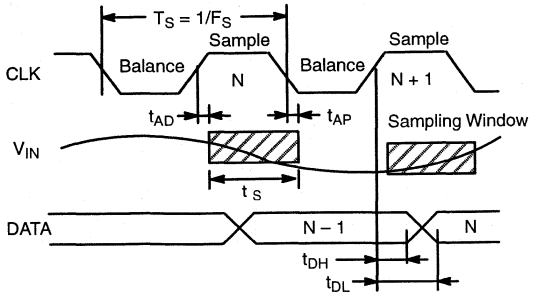


Figure 7. Pipeline Mode Timing (MP7682 compatible)
(Phase = 1, Mode = 1)

The MP7686 converts analog voltages into 64 digital codes by encoding the outputs of comparators. A comparator is used to generate the overflow bit. The conversion is synchronous with the sample clock. A complete conversion cycle is accomplished in 1.5 cycles. Data is transferred from the comparator latches to the output register each cycle and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕB (CLK high = balance) and ϕS (CLK low = sample). Phase B connects the comparators to the reference tap points. Phase S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 65 resistors. The first and the last resistors of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = R * 64 \qquad V_{REF} = V_{REF(+)} - V_{REF(-)} = 64 * LSB$

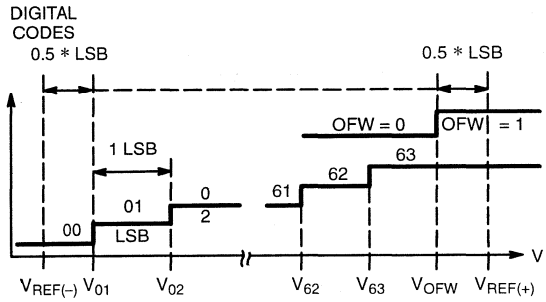


Figure 8. Ideal A/D Transfer Function

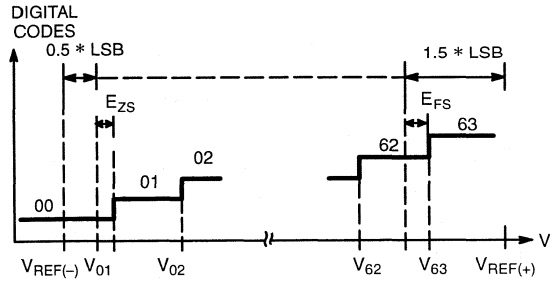


Figure 9. Real A/D Transfer Curve

For MP7686 the overflow flag is ideally set at

$V_{OFW} = V_{REF(+)} - 0.5 * LSB$

Thus the first and last transition of the data bits take place at

$V_{IN} = V_{01} = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{63} = V_{REF(+)} - 1.5 * LSB$

$LSB = (V_{63} - V_{01}) / 62$

MP7686 also has zero scale and full scale errors which indicate the deviations from the ideal initial and final transitions, thus

the various error relationships for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and the zero and full scale errors (EZS and EFS) can be described as follows:

DNL (01) = $V_{02} - V_{01} - LSB$

: : :

DNL (62) = $V_{63} - V_{62} - LSB$

E_{FS} (full scale error) = $V_{63} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

INL (i) = Σ DNL (i)

Systems that adjust the V_{REF} voltages only increase the DNL accuracy at the two extreme points. In the MP7686, such adjustments have little impact at frequencies lower than 15 MHz.

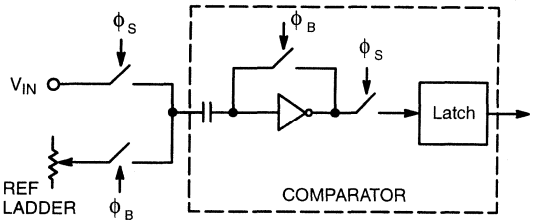


Figure 10. MP7686 Comparator

The MP7686 uses the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point and the other to the inverter/comparator trigger point (*NO TAG*). During the sample phase (ϕ_S), one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if (dv/dt) * $t_{AJ} \approx V_{REF}/64$, an internal 1 LSB of error results.

The logic encodes the 64 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

$\overline{OE1}$	OE2	OFW	DB5 - DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

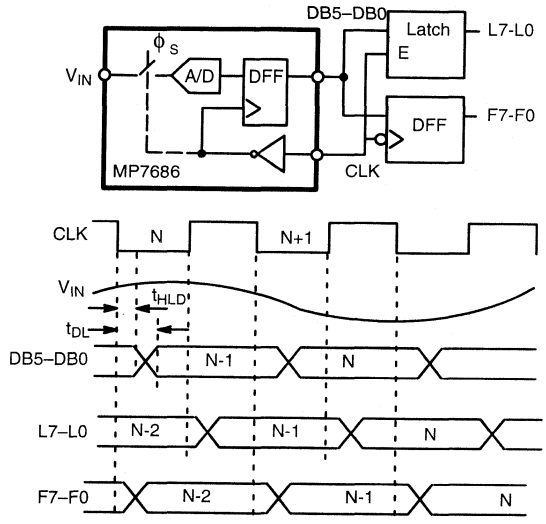


Figure 11. MP7686 Functional Equivalent Circuit and Interface Timing (Pipeline Mode)

The MP7686 functional equivalent circuit is shown to help the designer to correctly design the timing of his system. The MP7686 is equivalent to an A/D converter followed by a D-type flip-flop (DFF) with the hold and delay times specified in the electrical characteristics.

If another DFF is to follow the ADC, we recommend that the system latches the data at the negative going edge of the clock. If a latch follows the ADC, the positive half of the clock used as enable signal should guarantee stable output at the end of the enable pulse. At high sampling frequencies (F_S > 20 MHz) the user should verify in his system that the MP7686 digital outputs do not change when the digital logic is trying to latch the data. If this problem occurs it may be necessary to invert the logic state

of the input PHASE or to change the edge that latches the data into the external circuitry.

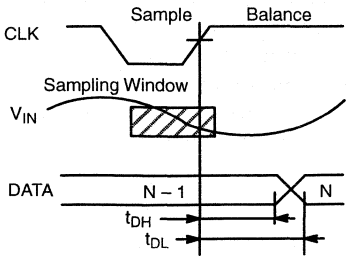


Figure 12. One Shot Mode Timing
(Phase = 0, Mode = 0)

One Shot Mode (Mode = Low, Phase = Low)

While the pipeline mode requires three clock edges (two clock pulses) to accomplish one A/D conversion, the One Shot mode (see *NO TAG*) requires only two edges (one clock pulse) to complete a conversion.

Reserved (Mode = Low, Phase = High)

This mode is not a valid operational mode.

Reference Voltages

If the input bandwidth is limited to the Nyquist region (F_{IN} < FS/2) then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds FS/2, then it is recommended that V_{REF} be lower than $V_{DD}/2$.

3

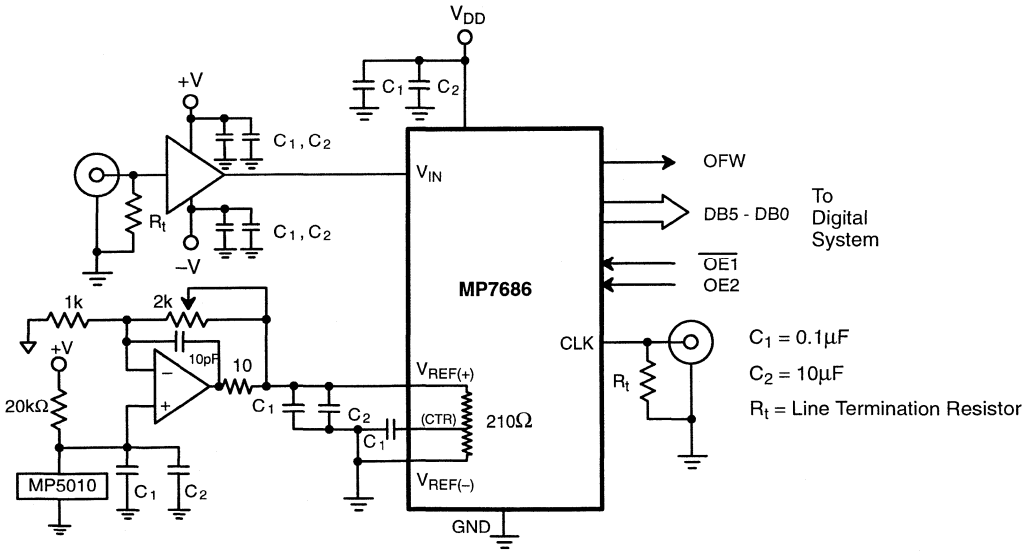


Figure 13. Typical Circuit Connections

1. All signals should not exceed V_{DD} +0.5 V or GND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (V_{DD} +0.5 V or GND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7686 inputs have input protection diodes which will protect the device from short transients outside the supplies range.

3. The PC board design will affect the MP7686 accuracy. Use of wire wrap is not recommended.

4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.

5. The analog input should be driven by a buffer op amp with as low an output impedance as possible. The impedance should be less than 25Ω for clock frequencies above 15 MHz

6. Ground plane should be substantial. The ground plane should act as a shield for parasitics and not a return path for signals. Separate low impedance ground paths will reduce noise levels.

7. The power supplies and reference voltages should be decoupled with a ceramic (0.1μF) and a tantalum (10μF) capacitor as close to the device as possible.

8. The digital output should not be driving long wires as the capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

MP7690

CMOS
Programmable Input Range 8-Bit
High Speed Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 1 kHz to 15 MHz (MSPS)**
- **DNL better than 1/2 LSB from 1 kHz to 10 MHz**
- **Interface to any Input Range between GND and V_{DD}**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 volt)**
- **Low Power CMOS (300 mW)**
- **Latch-Up Free**
- **2000 Volt ESD Protection**

BENEFITS

- **Reduced Board Space (small package)**
- **Excellent Accuracy Without High System Power**
- **Reduced External Parts, No Sample/Hold Needed**
- **Designer Can Adapt Input Range and Scaling**
- **Use MP7690A for New Designs**

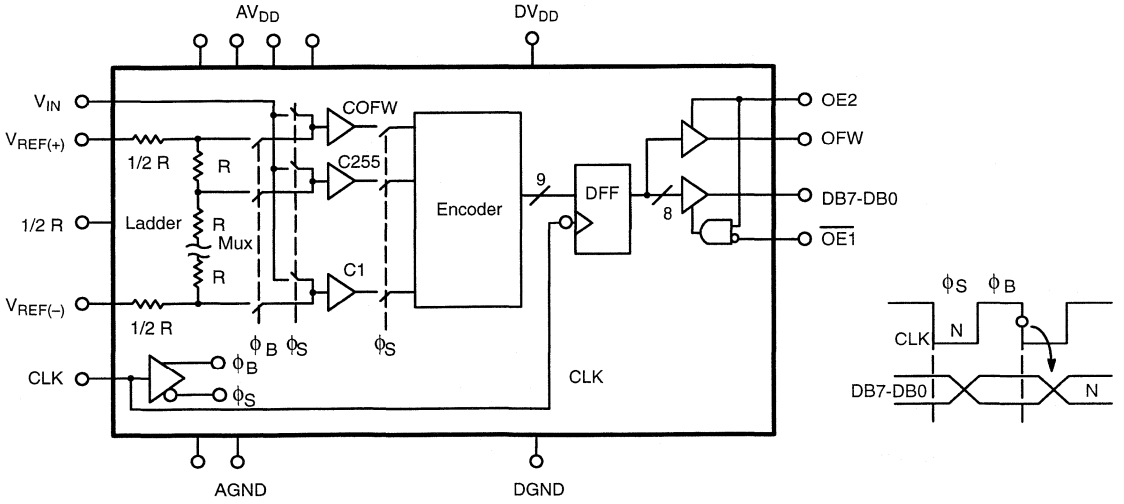
3

GENERAL DESCRIPTION

The MP7690 is an 8-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 10 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP7690 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP7690 includes 256 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

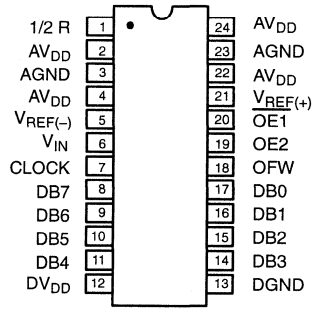


ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Ceramic Dip	–40 to +85°C	MP7690JD	±1 1/2	2
Ceramic Dip	–40 to +85°C	MP7690KD	±1	1 1/2
Ceramic Dip	–55 to +125°C	MP7690SD	±1 1/2	2
Ceramic Dip	–55 to +125°C	MP7690TD	±1	1 1/2

PIN CONFIGURATION

See Packaging Section for Package Dimensions



24 Pin CDIP (0.300")
DN24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	Center of Reference Resistance Ladder
2	AV_{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground Return
4	AV_{DD}	Analog Power Supply Voltage
5	$V_{REF(-)}$	Lower Reference Voltage Input
6	V_{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV_{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground Return
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow flag
19	OE2	Output Enable Control Pin
20	$\overline{OE1}$	Output Enable Control Pin
21	$V_{REF(+)}$	Upper Reference Voltage Input
22	AV_{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground Return
24	AV_{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S =$ 10.0 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)} = 4.1$, $V_{REF(-)} = GND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	F_S	0.001		10	0.001	10	MHz	For Specified Accuracy
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±3/4		±1 1/2	LSB	
Integral Non-Linearity	INL			±1 1/2		±2	LSB	Best Fit Line
(Relative Accuracy)								(Max INL – Min INL) / 2
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±1	LSB	
Integral Non-Linearity	INL			±1		±1 1/2	LSB	Best Fit Line
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
REFERENCE VOLTAGES								
Positive Ref. Voltage[2]	$V_{REF(+)}$			V_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Ladder Resistance	R_L	120		400	90	430	Ω	
Ladder Temp. Coefficient[3]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance Sample[4]	C_{INA}		50				pF	
Aperture Delay	t_{AP}		25				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		60				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents[5]								V_{IN}=GND to V_{DD}
CLK	I_{IN}	–100		100	–150	150	µA	
OE2 (Internal Res to V_{DD})[6]		–60		1	–100	1	µA	
$\overline{OE1}$ (Internal Res to GND)[7]		–1		50	–1	75	µA	
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.3			4.3		V	I_{LOAD} = –1.0 mA
Logical "0" Voltage	V_{OL}			0.6		0.6	V	I_{LOAD} = 2.0 mA
Tristate Leakage	I_{OZ}		±0.6	±1	±0.8	±1.5	µA	V_{OUT}=GND to V_{DD}
Data Valid Delay[3]	t_{DL}		50				ns	
Data Enable Delay[3]	t_{DEN}		40				ns	
Data Tristate Delay[3]	t_{DHZ}		40				ns	

3

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLIES[9]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6			V	
Current (AV_{DD} + DV_{DD})	I_{DD}		52	75		90	mA	

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).
2. For best results it is recommended that the reference voltage be limited to (V_{DD} –0.5 V) maximum.
3. Guaranteed. Not tested.
4. See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.
5. All inputs have diodes to V_{DD} and GND. Input $\overline{OE1}$ has an internal pull down. Input OE2 has an internal pull up. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.
6. Internal resistor to V_{DD} biases unconnected input to active high logical level.
7. Internal resistor to GND biases unconnected input to active low logical level.
8. Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
9. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP 1100mW
Derates above 75°C ..... 15mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

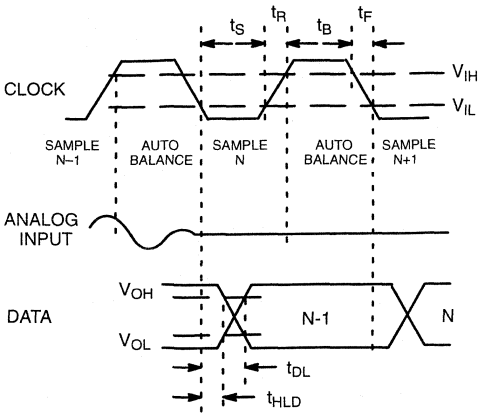


Figure 1. MP7690 Timing Diagram

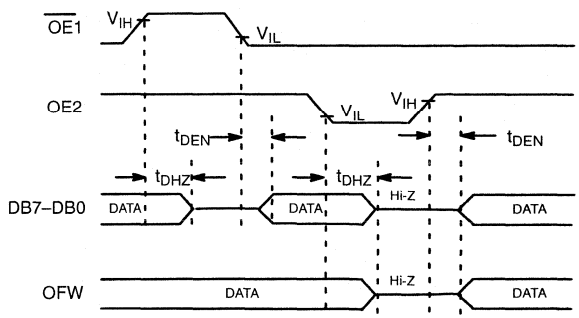
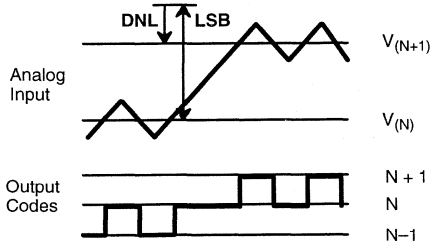


Figure 2. Output Enable/Disable Timing Diagram

3



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

DNL(N) = [$V_{(N+1)} - V_{(N)}$] – LSB

Figure 3. DNL Measurement

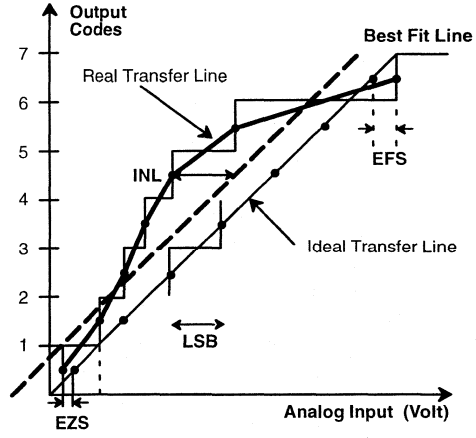


Figure 4. INL Error Calculation

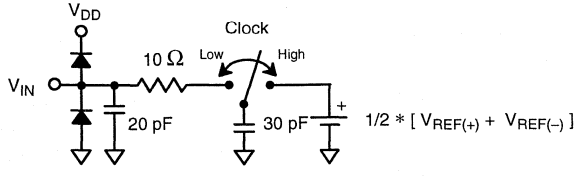


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7690 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $\quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

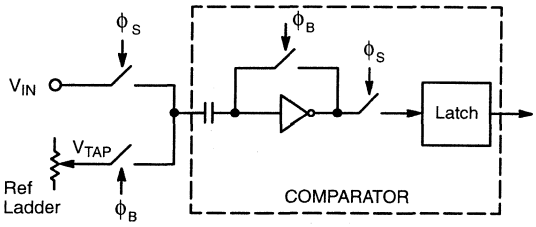


Figure 6. MP7690 Comparator

The MP7690 comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitors and forces the inverters into one of the two possible logic states. Latches (connected to the comparators during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The aperture delay may vary from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is in the same order of magnitude of the LSB. That is, if $(dv/dt) * t_{AJ} \approx V_{REF}/256$, an internal error of 1 LSB results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

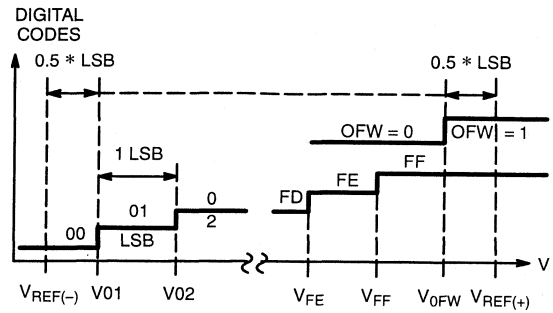


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{0FW}) takes place at:

$V_{IN} = V_{0FW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V01 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = (V_{REF(+)} - V_{REF(-)}) / 256 = (V_{FF} - V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

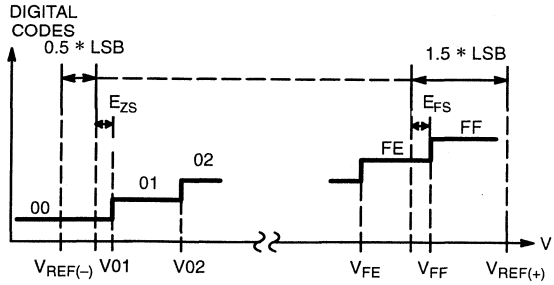


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every $(V_{REF(+)} - V_{REF(-)}) / 256$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than or less than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

EZS (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

Figure 8. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP7690, such adjustments have little impact at frequencies lower than 10 MHz and generally are not required. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

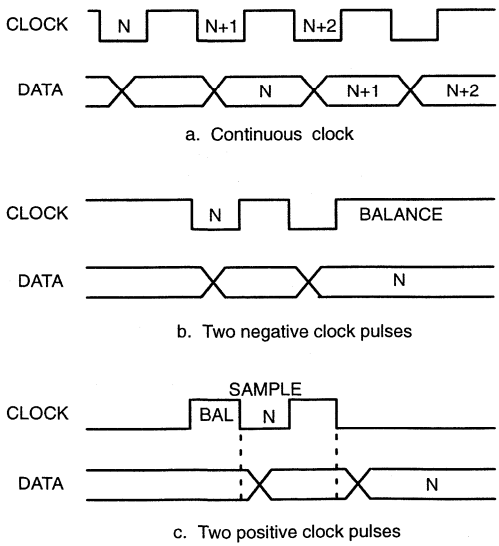


Figure 9. Relationship of Data to Clock

Clock and Conversion Timing

A system will clock the MP7690 continuously (*Figure 9a.*) or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b.* keeps the MP7690 comparators in balance and ready to sample the analog input. This mode draws the most current from V_{DD}. The timing of *Figure 9c.* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

The MP7690 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7690's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input.

Reference Voltages

If the input bandwidth is limited to the Nyquist region (F_{IN}) < (F_S) /2 then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds (F_S) /2, then it is recommended that V_{REF} be lower than $V_{DD}/2$.

At V_{REF} = 1.5 V the LSB is reduced to 6mV. Further reductions show an increased error in terms of LSB (which is getting smaller) even if the error in terms of mV is about constant.

The input/output relationship as a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 256 * (A_{IN}/V_{REF})$$
$$0 \le V_{IN} \le V_{REF} - 1\ LSB,\ DATA = 255\ if\ V_{IN} = V_{REF}$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range**. A system can increase dynamic range by using DAC's to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner), a first digitization would point to the input range in which most of the output codes fall. The system then would adjust the DAC's to generate $V_{REF(+)}$ and $V_{REF(-)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution**. Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merging of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

The functional equivalent of the MP7690 (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An A/D which tracks and converts V_{IN} with no delay.
3) A DFF with specified hold (t_{HLD}) and delay (t_{DL}) times. t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

$\overline{OE1}$	OE2	DB0 – DB7	OFW
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If an external DFF is to follow the MP7690, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

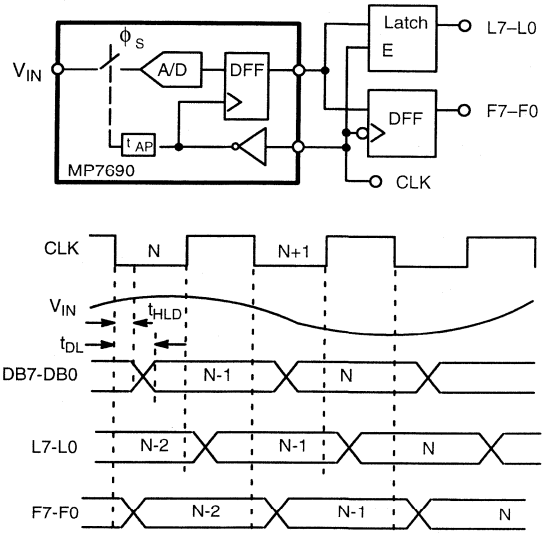


Figure 10. MP7690 Functional Equivalent Circuit and Interface Timing

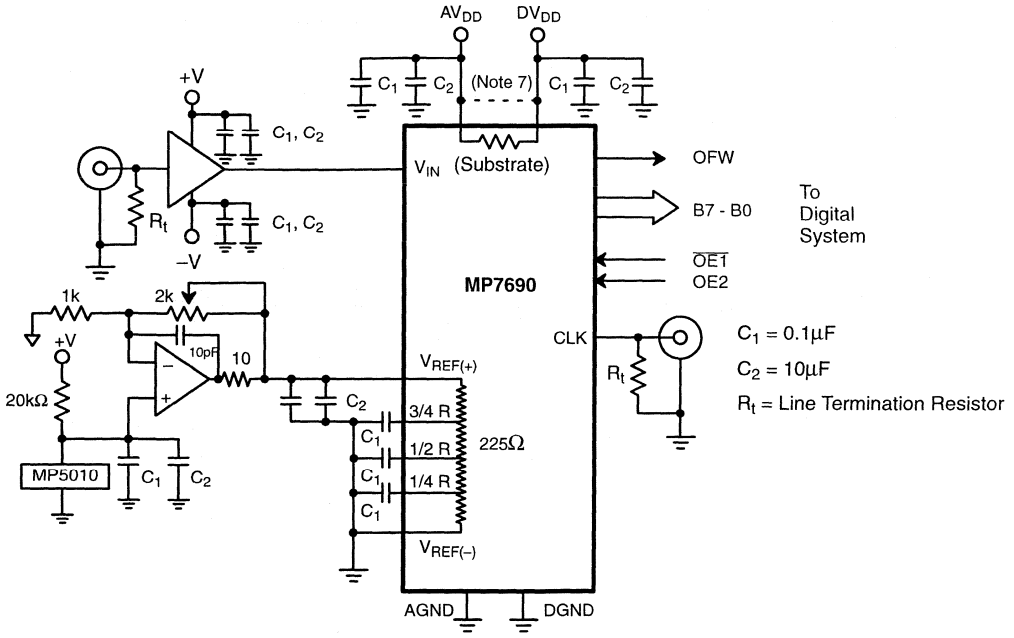


Figure 11. Typical Circuit Connections

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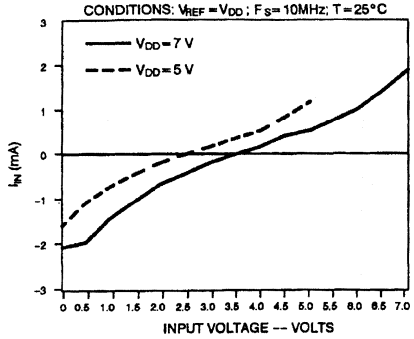
The following information will be useful in maximizing the performance of the MP7690.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7690. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
7. DV_{DD} should not be shared with other digital circuitry to avoid conversion errors caused by digital supply transients. DV_{DD} should be connected to AV_{DD} next to the MP7690.
8. DV_{DD} and AV_{DD} are connected inside the MP7690 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

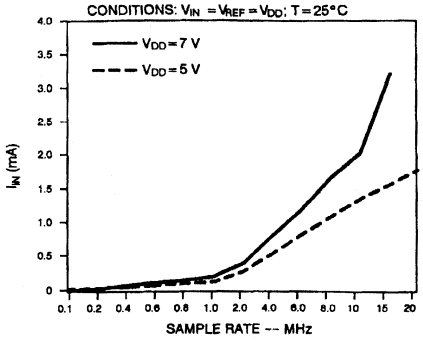
INPUT CURRENT vs. INPUT VOLTAGE

CONDITIONS: $V_{REF} = V_{DD}$; F_S = 10MHz; T = 25°C

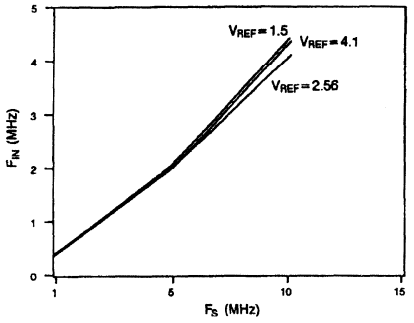


INPUT CURRENT vs. SAMPLE RATE

CONDITIONS: $V_{IN} = V_{REF} = V_{DD}$; T = 25°C

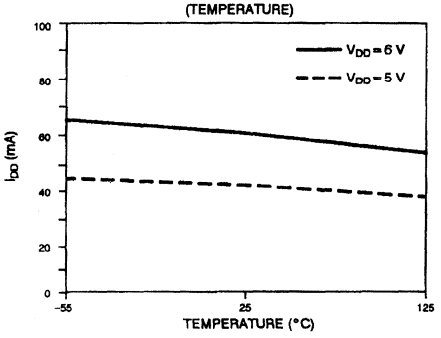


SMALL SIGNAL BANDWIDTH



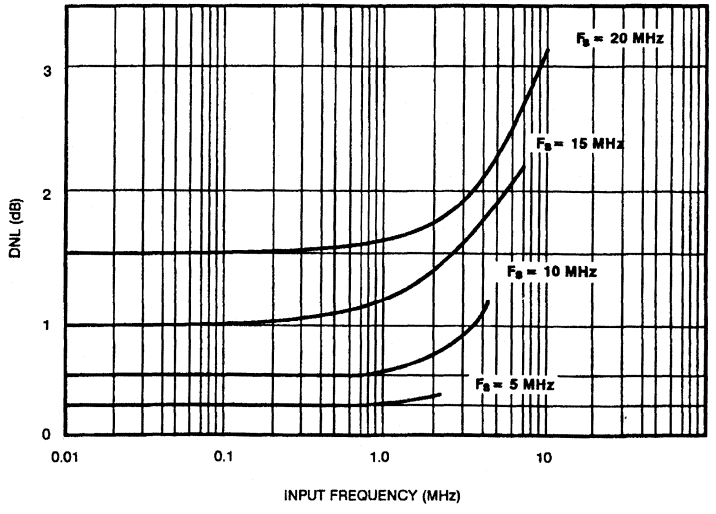
IDD

(TEMPERATURE)

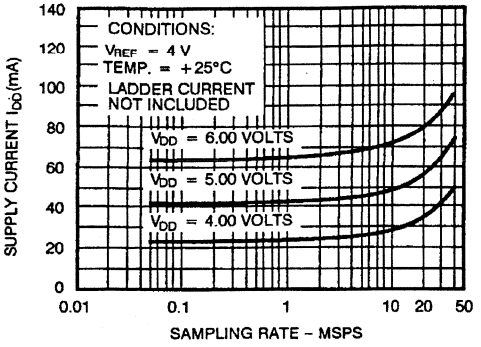


DNL VS. INPUT BANDWIDTH AS A FUNCTION OF SAMPLE RATE

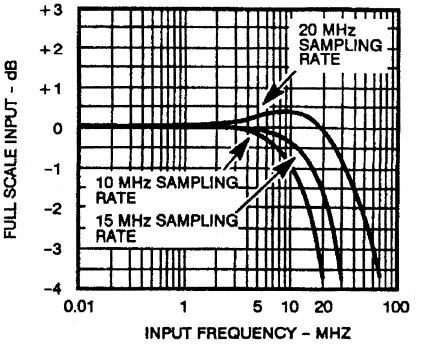
(DNL IS THE LARGEST ERROR APPEARING ON THE HISTOGRAM)



POWER CONSUMPTION
VS. SAMPLING RATE



FULL SCALE INPUT VS. INPUT FREQUENCY
AS A FUNCTION OF SAMPLING RATE



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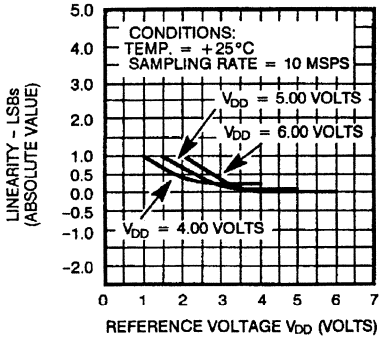
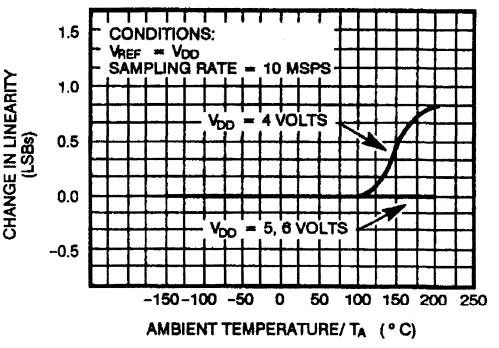
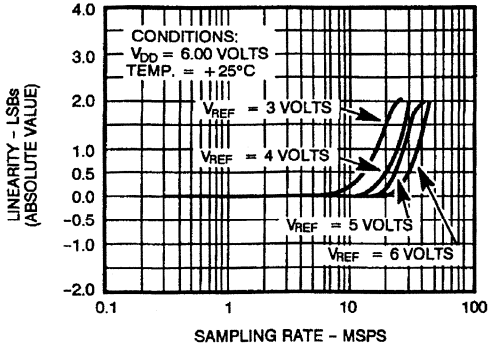
REFERENCE VOLTAGE
VS. LINEARITY



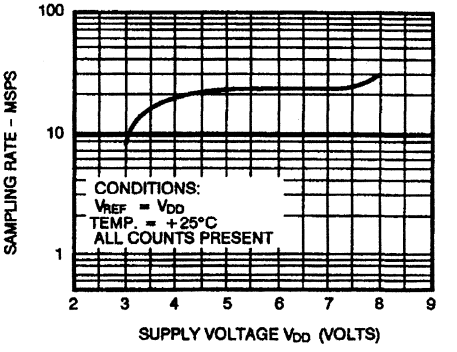
LINEARITY VS. TEMPERATURE
AS A FUNCTION OF V_{DD}



LINEARITY VS. SAMPLING RATE
AS A FUNCTION OF REFERENCE VOLTAGE



SAMPLING RATE
VS. SUPPLY VOLTAGE



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MP7690A

CMOS
Programmable Input Range 8-Bit
High Speed Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 1 kHz to 20 MHz (MSPS)**
- **DNL better than 1/4 LSB from 1 kHz to 10 MHz**
- **DNL better than 1/2 LSB to 14 MHz**
- **Adjustable Input Range between GND and V_{DD}**
- **Pin Compatible Upgrade of MP7690A**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 volt)**
- **Low Power CMOS (300 mW)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

- **Reduced Board Space (Small Package) and Reduced External Parts**
- **No External Sample/Hold Needed, Reducing System Cost and Improving Ease of Design**
- **Adjustable Input Range and Scaling**

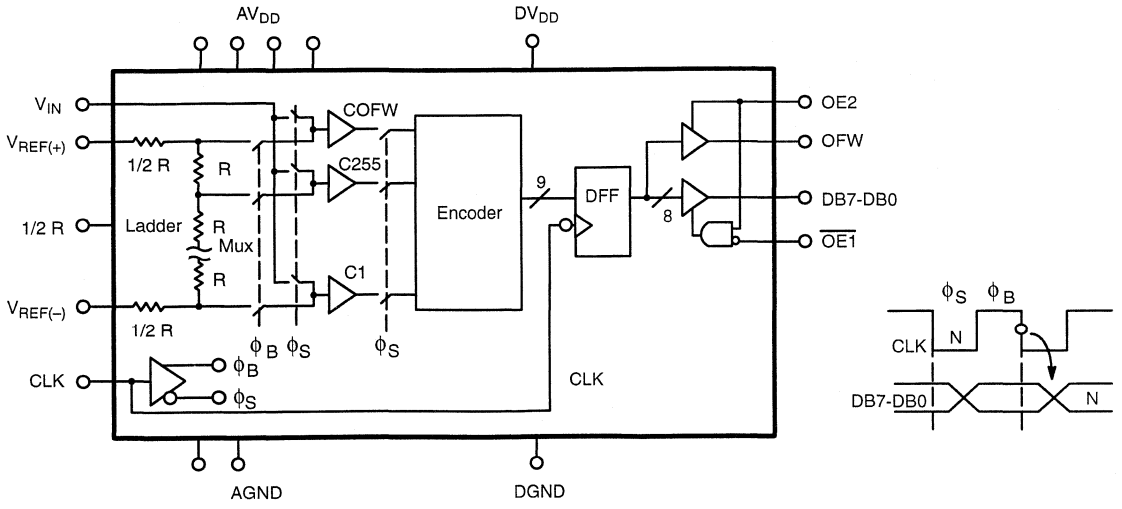
3

GENERAL DESCRIPTION

The MP7690A is an 8-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 14 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP7690A allows direct interface to any analog input range between AGND and DV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP7690A includes 256 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

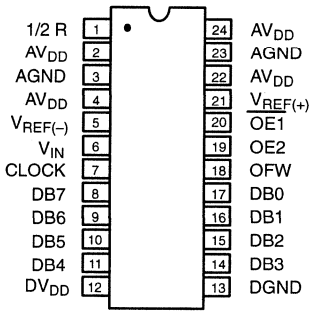


ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Ceramic Dip	–40 to +85°C	MP7690AAD	±1	±2
Ceramic Dip	–40 to +85°C	MP7690ABD	±3/4	±1 3/4
Ceramic Dip	–55 to +125°C	MP7690ASD	±1	±2
Ceramic Dip	–55 to +125°C	MP7690ATD	±3/4	±1 3/4

PIN CONFIGURATION

See Packaging Section for Package Dimensions



24 Pin CDIP (0.300")
DN24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	Center Point of Reference Ladder
2	AV_{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground
4	AV_{DD}	Analog Power Supply Voltage
5	$V_{REF(-)}$	Lower Reference Voltage Input
6	V_{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Output Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV_{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow Bit Output
19	OE2	Output Enable Control Pin
20	$\overline{OE1}$	Output Enable Control Pin
21	$V_{REF(+)}$	Upper Reference Voltage Input
22	AV_{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground Return
24	AV_{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 14.0 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	FS	0.001		14	0.001	14	MHz	For Specified Accuracy
ACCURACY (A, S Grades)[1]								
Differential Non-Linearity	DNL			±3/4		±1	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			±1 1/2		±2	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
ACCURACY (B, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±3/4	LSB	
Integral Non-Linearity	INL			±1		±1 3/4	LSB	Best Fit Line
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
DYNAMIC ACCURACY								Histogram Test
Differential Non-Linearity	DNL		±0.30				LSB	F_{IN} = 1 MHz
	DNL		±0.65				LSB	F_{IN} = 5 MHz
REFERENCE VOLTAGES								
Positive Ref. Voltage[2]	$V_{REF(+)}$			V_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Ladder Resistance	R_L	170	225	300	130	330	Ω	
Ladder Temp. Coefficient[3]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance Sample[4]	C_{INA}		50				pF	
Aperture Delay	t_{AP}		15				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		45				ps	
Clock Kickback Pulse			20				pAs	V_{REF} = 4 V
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2.0			2.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Leakage Currents[5]								V_{IN}=GND to V_{DD}
CLK	I_{IN}	–10		10	–10	10	µA	
OE2 (Internal Res to V_{DD})[6]		–50		5	–50	5	µA	
$\overline{OE1}$ (Internal Res to GND)[7]		–5		50	–5	50	µA	

3

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	V_{DD}-0.5			V_{DD}-0.5		V	I_{LOAD} = –4.0 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 4.0 mA
Tristate Leakage	I_{OZ}			±10		±20	µA	V_{OUT}=GND to V_{DD}
Data Valid Delay[3]	t_{DL}		23	33	23	35	ns	
Data Enable Delay[3]	t_{DEN}			20		25	ns	
Data Tristate Delay[3]	t_{DHZ}			20		25	ns	
POWER SUPPLIES[9]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6	4	6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			80		85	mA	
AC PARAMETERS[3]								RMS/RMS Measures
Signal Noise Ratio[10]	SNR		47				dB	FS = 3X NTSC
	SNR		46				dB	FS = 4X NTSC
Differential Gain Error	dG		2				%	FS = 3X NTSC
Differential Phase Error	dPh		1				Degree	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 For best results it is recommended that the reference voltage be limited to (V_{DD} –0.5 V) maximum.

3 Guaranteed. Not tested.

4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to V_{DD} and GND. Input $\overline{OE1}$ has an internal pull down. Input OE2 has an internal pull up. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

6 Internal resistor to V_{DD} biases unconnected input to active high logical level.

7 Internal resistor to GND biases unconnected input to active low logical level.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply loop.

10 SNR: Ratio of RMS signal to RMS noise up to 1/2 F_S in dB.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Digital Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Digital Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP 1100mW
Derates above 75°C ..... 15mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

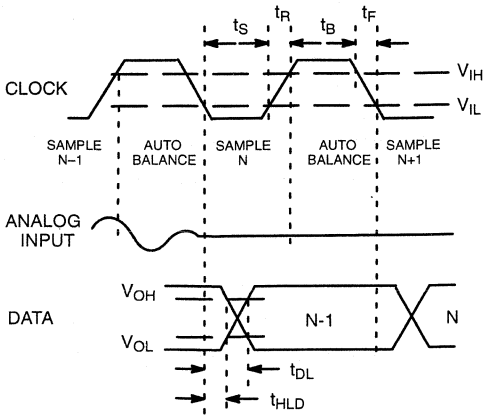


Figure 1. MP7690A Timing Diagram

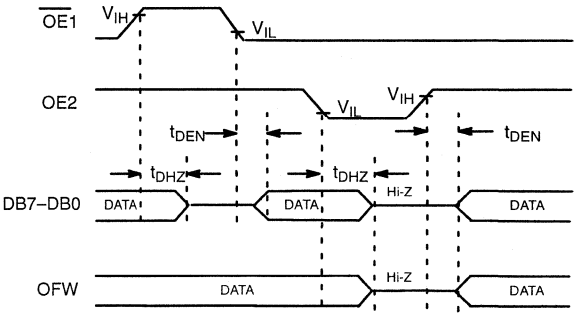
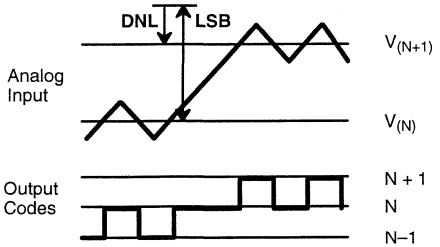


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

DNL(N) = [$V_{(N+1)} - V_{(N)}$] – LSB

Figure 3. DNL Measurement

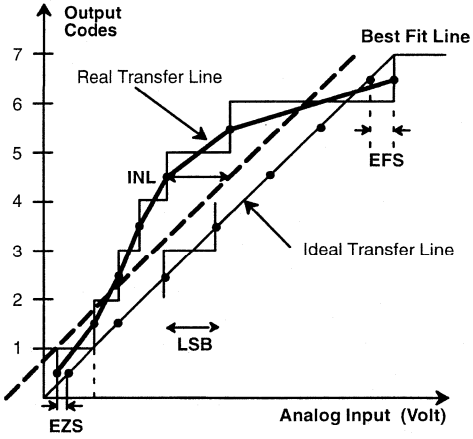


Figure 4. INL Error Calculation

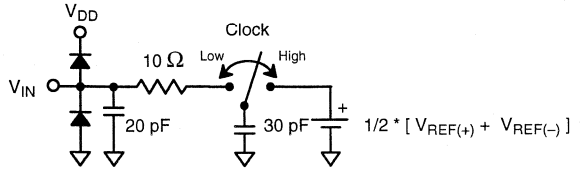


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7690A converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $\quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

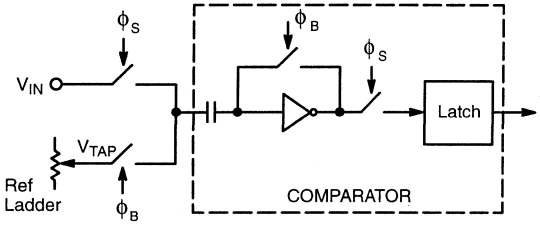


Figure 6. MP7690A Comparator

The MP7690A comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitors and forces the inverters into one of the two possible logic states. Latches (connected to the comparators during ϕ_S) restore and propagate the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The aperture delay may vary from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if $(dv/dt) * t_{AJ} \approx V_{REF}/256$ then one LSB of error results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

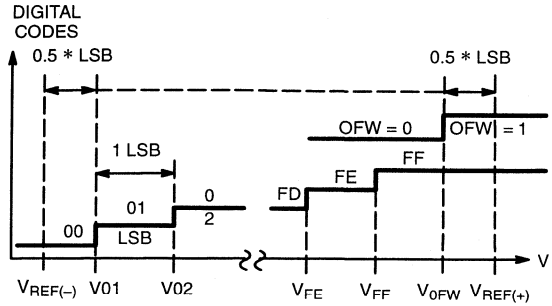


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{0FW}) takes place at:

$V_{IN} = V_{0FW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V_{01} = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(-)} - 1.5 * LSB$

$LSB = V_{REF} / 256 = (V_{FF} - V_{01}) / 254$

Note that the overflow bit has no impact on the data bits.

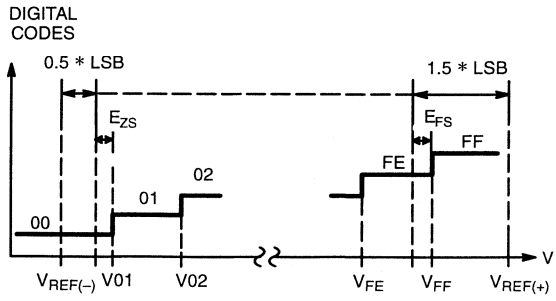


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions are not always exactly every $V_{REF}/256$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated values. A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is between 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

EZS (zero scale error) = V01 – $[V_{REF(-)} + 0.5 * LSB]$

Figure 8. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP7690A, such adjustments have little impact at frequencies lower than 10 MHz and generally are not required. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from an ideal one.

INL is specified in terms of best fit line. Best fit line makes the INL+ and INL– errors equal by using the algebraic sum divided by 2. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

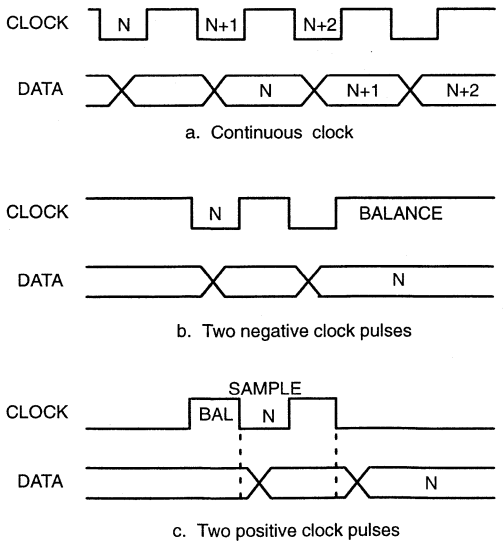


Figure 9. Relationship of Data to Clock

Clock and Conversion Timing

A system will clock the MP7690A (*Figure 9b.)* continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b.* keeps the MP7690A comparators in balance and ready to sample the analog input. This mode draws the most current from V_{DD}. The timing of *Figure 9c.* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

The MP7690A has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7690A's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input.

Reference Voltages

If the input bandwidth is limited to the Nyquist region ($F_{IN} < F_S/2$) then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $F_S/2$, then it is recommended that VREF be lower than $V_{DD}/2$.

If V_{REF} is reduced below 1.5 V, accuracy will be degraded due to the decreased signal-to-noise ratio.

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 255 * (A_{IN}/V_{REF}) \text{ (Full Scale)}$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range**. A system can increase dynamic range by using DACs to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner) a first digitization would point to the input range in which most of the output codes fall. The system can then adjust the DACs to generate $VR_{EF(+)}$ and $V_{REF(-)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution**. Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merg-

ing of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 input bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

The functional equivalent of the MP7690A (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An A/D which tracks and converts V_{IN} with no delay.
3) A DFF (D type flip-flop) with specified hold (t_{HLD}) and de lay (t_{DL}) times. t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

$\overline{OE1}$	OE2	OFW	DB7–DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If an external DFF is to follow the MP7690A, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as an enable signal for the latch guarantees stable output at the end of the enable pulse.

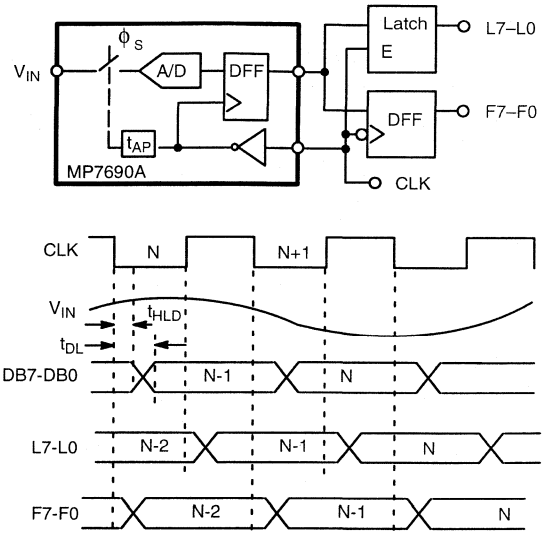


Figure 10. MP7690A Functional Equivalent Circuit and Interface Timing

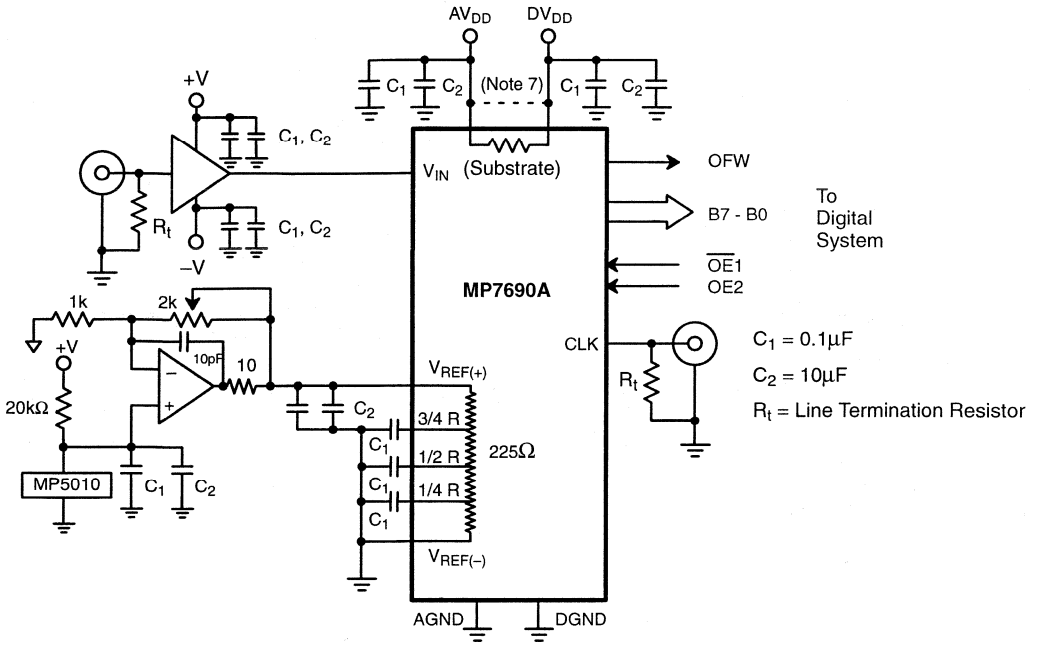
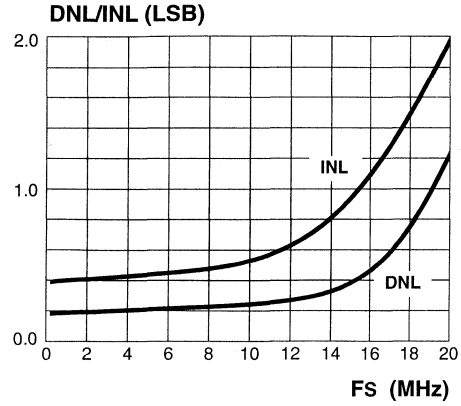


Figure 11. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP7690A.

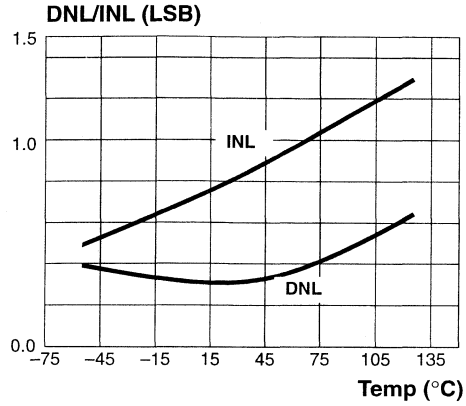
1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7690A. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
7. DV_{DD} should not be shared with other digital circuitry to avoid conversion errors caused by digital supply transients. DV_{DD} should be connected to AV_{DD} next to the MP7690A.
8. DV_{DD} and AV_{DD} are connected inside the MP7690A through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

CHARACTERIZATION CHARTS (Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S = 14$ MHz (50% Duty Cycle), $V_{REF(+)} = 4.1$ V, $V_{REF(-)} = GND$, $T_A = 25°C$



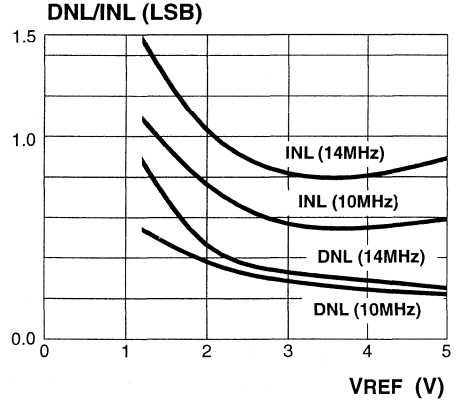
Accuracy (DNL/INL)
vs. Sampling Rate (FS)

Graph 1.



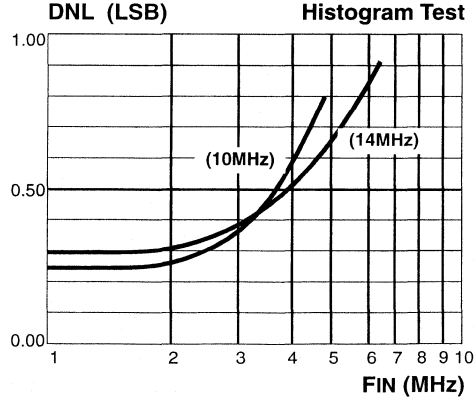
Accuracy (DNL/INL)
vs. Ambient Temperature (T)

Graph 2.



Accuracy (DNL/INL)
vs. Reference Voltage (VREF)
vs. Sampling Rate (FS = 10, 14 MHz)
(VIN p-p = VREF)

Graph 3.



Dynamic (DNL/INL)
vs. Input Sinewave (FIN)
vs. Sampling Rate (FS = 10, 14 MHz)

Graph 4.

MP7693

CMOS
Low Power 8-Bit
Analog-to-Digital Converter

FEATURES

- Sampling Rates from 1 kHz to 2.5 MHz
- DNL better than 1/2 LSB (typ) up to 3 MHz
- Low Power CMOS - 75 mW at 5 V
- Monotonic; No Missing Codes
- Interface to any Analog Input Range between GND and V_{DD}
- No S/H needed for CCD Outputs or Input Signals less than100 kHz
- Single Power Supply
- ESD Protection to 2000 Volts
- Latch-Up Free

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer can Adapt Input Range & Scaling

APPLICATIONS

- Low Power A/D Applications
- High Resolution Imaging
- Multiplexed Data Acquisition
- Radar Pulse Analysis

3

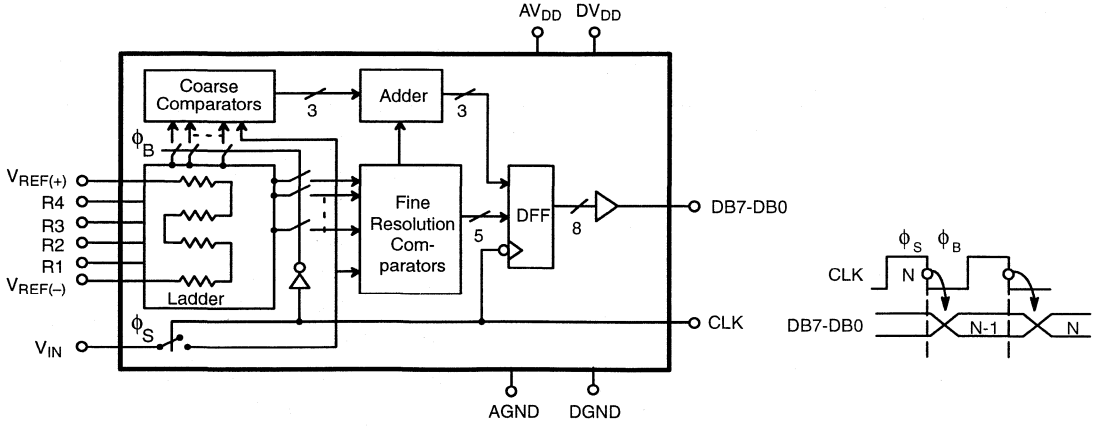
GENERAL DESCRIPTION

The MP7693 is an 8-bit monolithic CMOS Analog-to-Digital Converter designed for precision applications demanding low power consumption and fast conversion. The input architecture of the MP7693 allows direct interface to any analog input range between AGND and AVDD (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets VREF(+) and VREF(–) to encompass the desired input range.

The MP7693 uses a two-step flash technique. The first segment converts the 3 MSBs and consists of 7 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 5 LSBs.

With 75 mW typical and 100 mW maximum power dissipation, the MP7693 achieves its excellent performance due to the inherent high speed of a proprietary CMOS Process.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

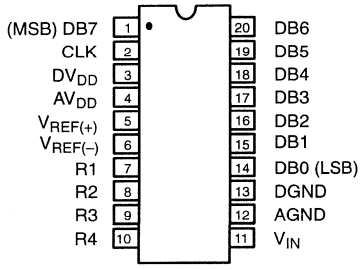


ORDERING INFORMATION

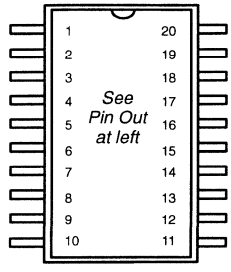
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7693BN	±3/4	3/4
PLCC	–40 to +85°C	MP7693BP	±3/4	3/4
SOIC	–40 to +85°C	MP7693BS	±3/4	3/4

PIN CONFIGURATIONS

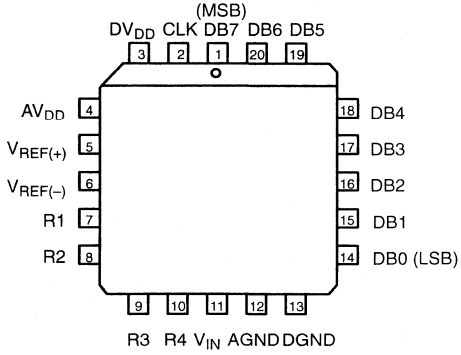
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB7	Data Output Bit 7 (MSB)
2	CLK	Clock Input
3	DV_{DD}	Power Supply
4	AV_{DD}	Analog Power Supply
5	$V_{REF(+)}$	Upper Ref. Voltage
6	$V_{REF(-)}$	Lower Ref. Voltage
7	R1	Ref. Ladder Tap
8	R2	Ref. Ladder Tap
9	R3	Ref. Ladder Tap
10	R4	Ref. Ladder Tap

PIN NO.	NAME	DESCRIPTION
11	V_{IN}	Analog Signal Input
12	AGND	Analog Ground
13	DGND	Digital Ground
14	DB0	Data Output Bit 0 (LSB)
15	DB1	Data Output Bit 1
16	DB2	Data Output Bit 2
17	DB3	Data Output Bit 3
18	DB4	Data Output Bit 4
19	DB5	Data Output Bit 5
20	DB6	Data Output Bit 6

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 2.5 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	T_A = 25°C Min	Typ	Max	Tmin to Tmax Min	Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate[1]	F_S	.001		3	.001	3	MHz	
ACCURACY[2]								
Differential Non-Linearity	DNL			±3/4		±3/4	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			±3/4		±3/4	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		10				mV	
Full Scale Error	EFS		10				mV	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			V_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Differential Ref. Voltage[5]	V_{REF}	2.0		V_{DD}	2.0	V_{DD}	V	
Ladder Resistance	R_L	500		1500	300	1950	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[1]								
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		50				pF	
Aperture Delay[1]	t_{AP}		55				ns	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents	I_{IN}							V_{IN}=GND to V_{DD}
CLK		–10		10	–10	10	µA	
Input Capacitance			5				pF	
Clock Timing (*See Figure 1.*)[1]								
Clock Period	t_S	333			333		ns	
Rise & Fall Time[4]	t_R, t_F			10		10	ns	
"High" Time[6]	t_S	166		500,000	250	500,000	ns	
"Low" Time[6]	t_B	166		500,000	250	500,000	ns	
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	V_{DD}-0.5			V_{DD}-0.5		V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 2 mA
Data Hold Time	t_{HLD}	10			10		ns	(*See Figure 1.*) (1)
Data Valid Delay[1]	t_{DL}			55			ns	
POWER SUPPLIES[8]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6	4	6	V	(1)
Current (AV_{DD} + DV_{DD})	I_{DD}		15	20		35	mA	V_{IN} = 2 V

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

NOTES

1 Guaranteed by Design. Not production tested.

2 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/256) is the DNL error (*Figure 2.*). The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage (*Figure 3.*).

3 See V_{IN} input equivalent circuit (*Figure 4.*).

4 Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.

5 Specified values guarantee functionality. Refer to other parameters for accuracy.

6 System can clock MP7693 with any duty cycle as long as all timing conditions are met.

7 Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.

8 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} (to GND) ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, PLCC, SOIC 900mW

Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

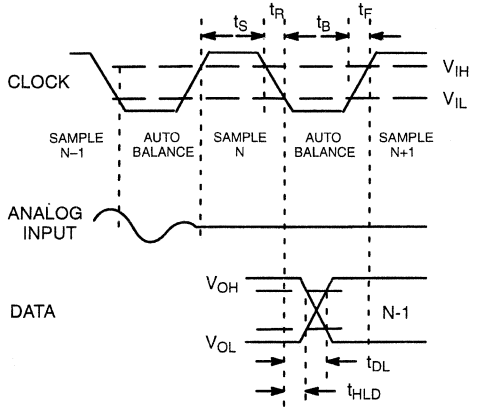


Figure 1. MP7693 Timing Diagram

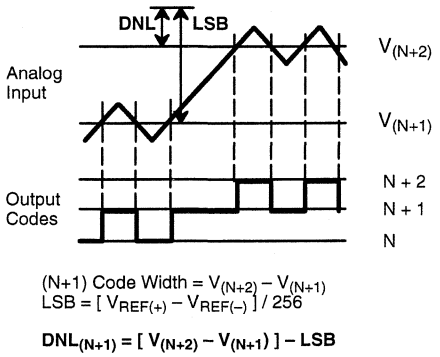


Figure 2. DNL Measurement On Production Tester

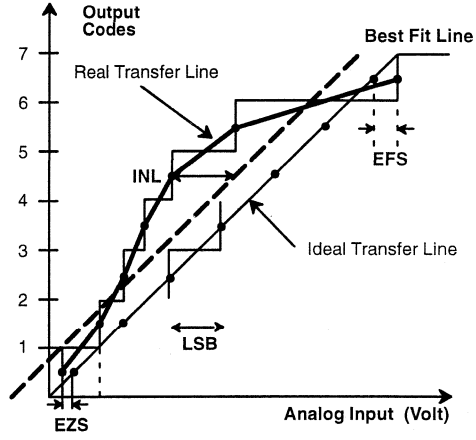


Figure 3. INL Error Calculation

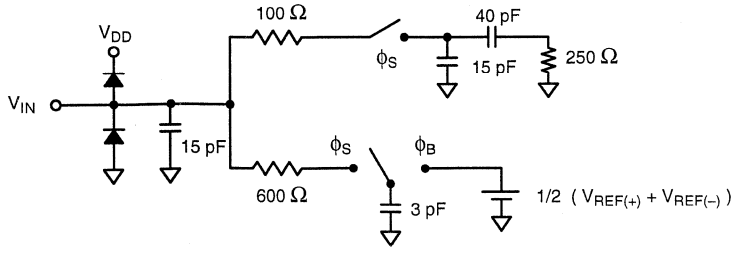


Figure 4. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7693 converts analog voltages into 256 digital codes by encoding the outputs of 7 coarse and 33 fine comparators. The conversion is synchronous with the clock and is accomplished in 2 clock periods.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

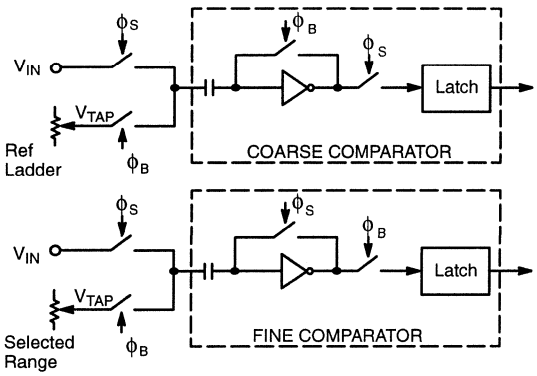


Figure 5. MP7693 Comparators

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 5.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 6.*

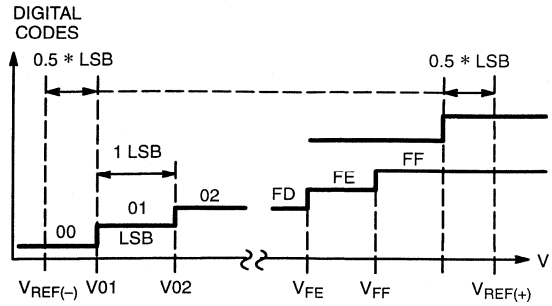


Figure 6. Ideal A/D Transfer Function

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 256 = (V_{FF} - V01) / 254$

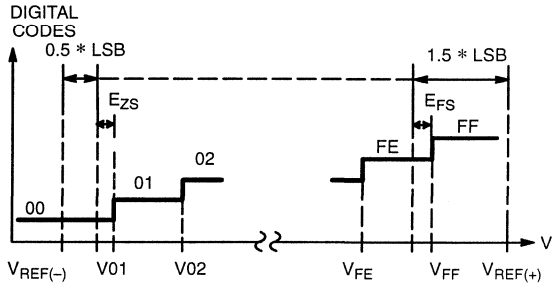


Figure 7. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every $V_{REF}/256$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ±0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16.0 mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

E_{FS} (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

Figure 7. shows the zero scale and full scale error terms.

Figure 3. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated

DNL errors to show the deviation of the real transfer curve from the ideal one.

After all transition voltages are measured, a best straight line is drawn (*see Figure 3.*) so that the positive INL error equals the negative INL error in magnitude., i.e. best fit line INL = (maximum positive – maximum negative) / 2.

Clock and Conversion Timing

A system will clock the MP7693 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP7693 in balance and ready to sample the analog input.

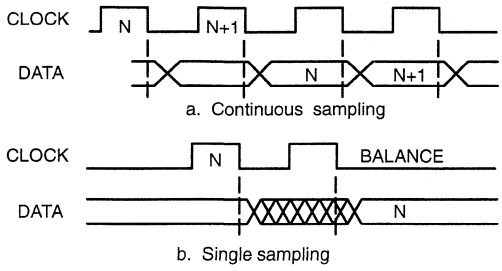


Figure 8. Relationship of Data to Clock

Analog Input

The MP7693 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7693's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 255 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP7693 (*Figure 9.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

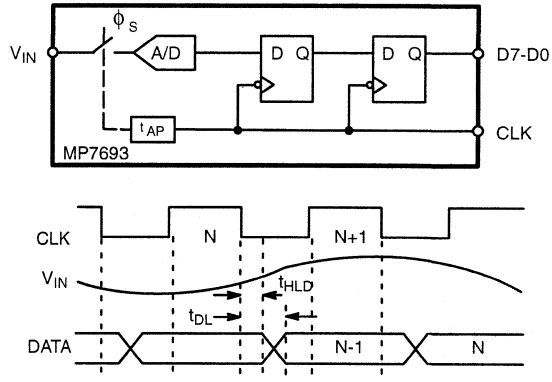


Figure 9. MP7693 Functional Equivalent Circuit and Interface Timing

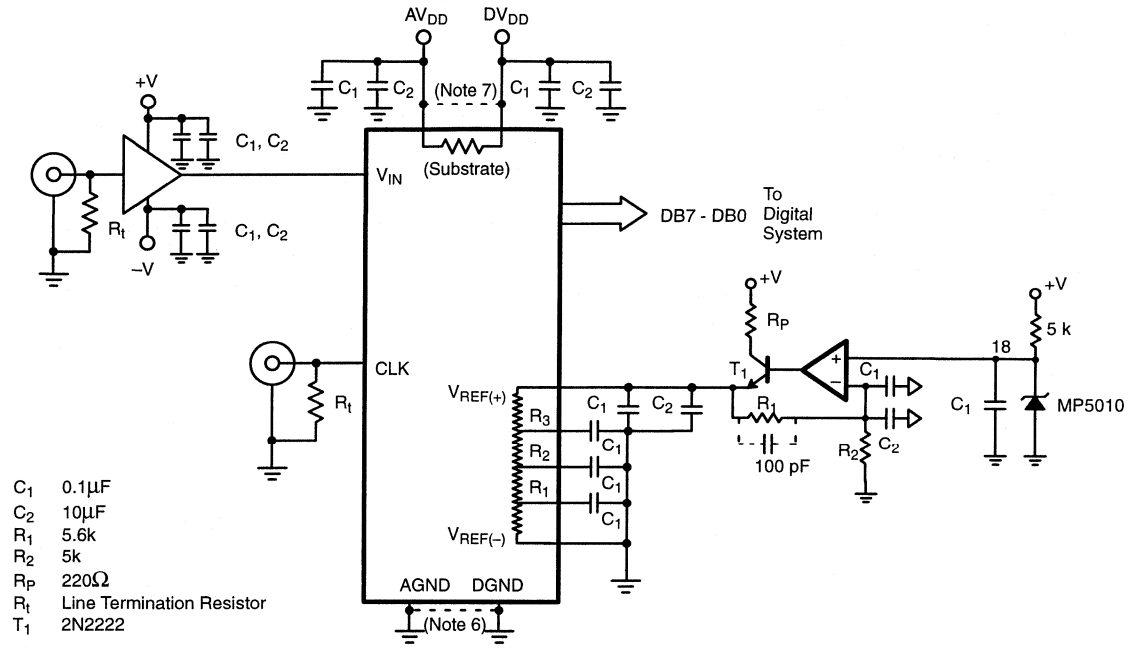
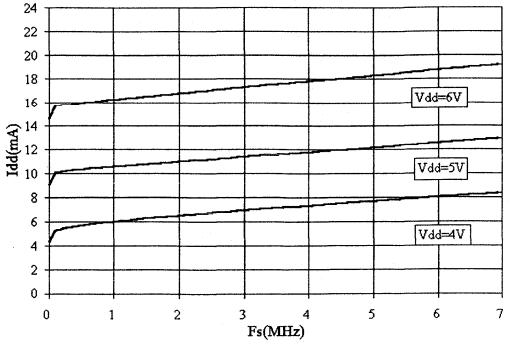


Figure 10. Typical Circuit Connections

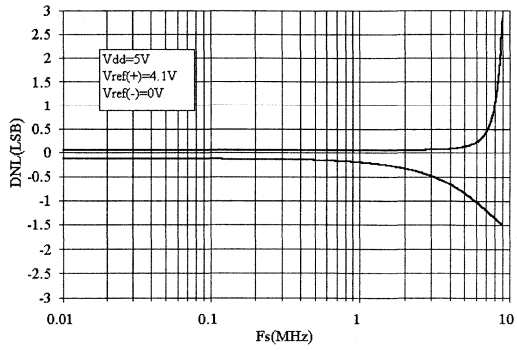
The following information will be useful in maximizing the performance of the MP7693.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7693. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. Separate low impedance ground paths will reduce noise levels. *DGND should not be shared with other digital circuitry.* DGND should be connected to AGND next to the MP7693.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} should be connected to AV_{DD} next to the MP7693.
8. DV_{DD} and AV_{DD} are connected inside the MP7693 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not be driving long wires as the capacitative coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

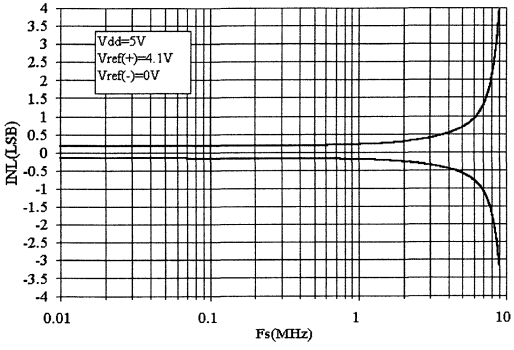
PERFORMANCE CHARACTERISTICS



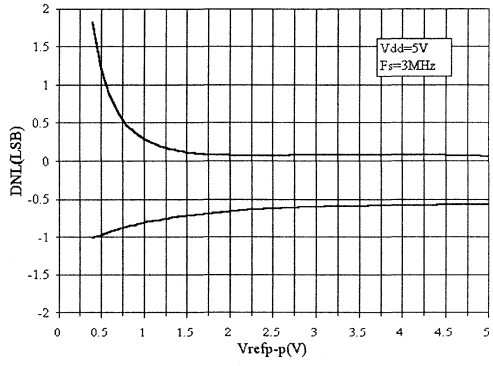
Graph 1. Supply Current vs. Sampling Frequency



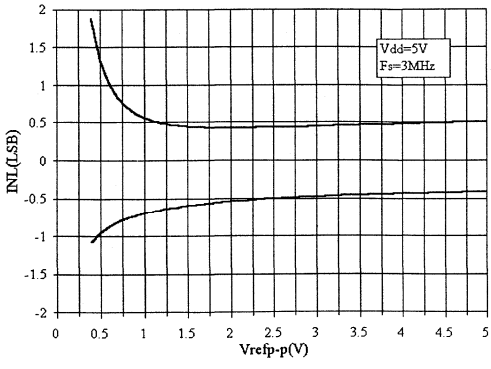
Graph 2. DNL vs. Sampling Frequency



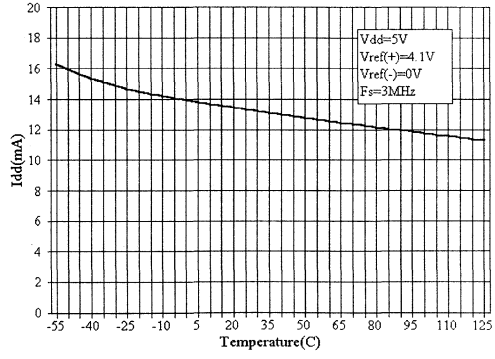
Graph 3. INL vs. Sampling Frequency



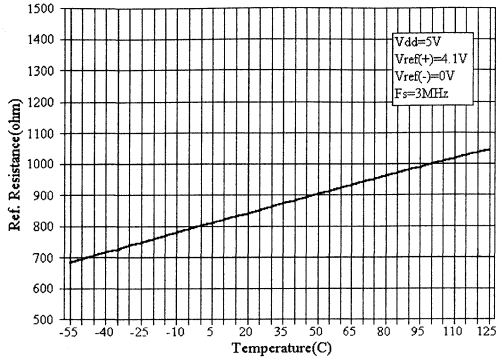
Graph 4. DNL vs. Reference Voltage



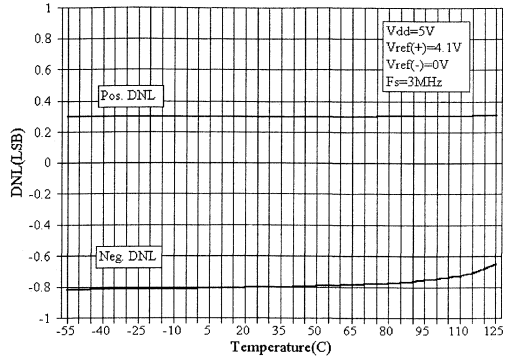
Graph 5. INL vs. Reference Voltage



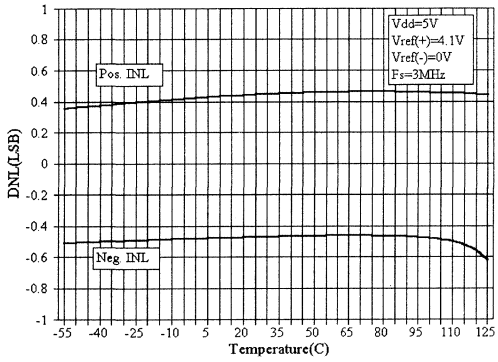
Graph 6. Supply Current vs. Temperature



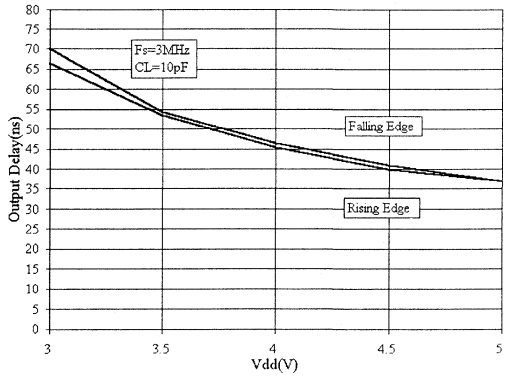
Graph 7. Reference Resistance vs. Temperature



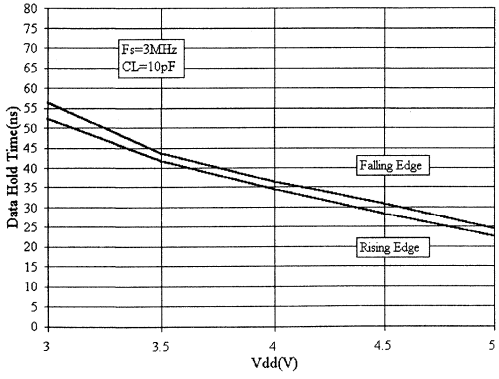
Graph 8. DNL vs. Temperature



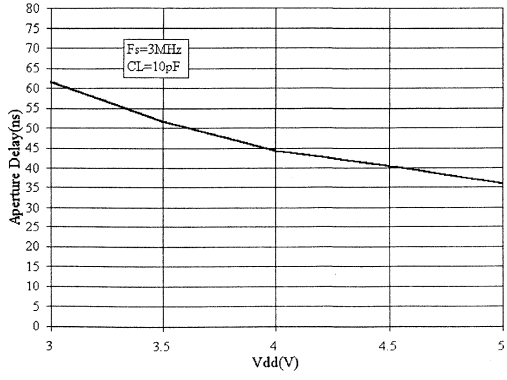
Graph 9. INL vs. Temperature



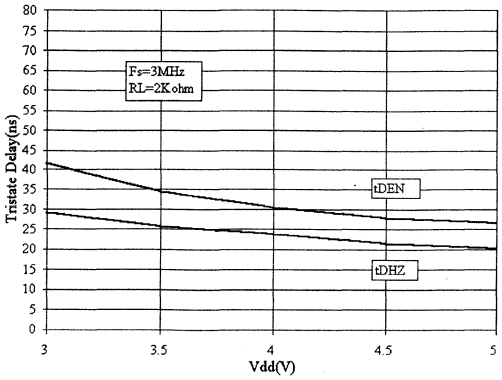
Graph 10. Output Delay vs. Supply Voltage



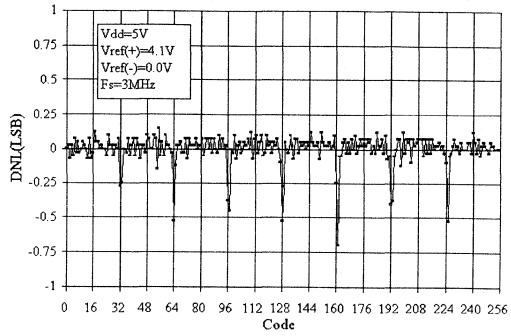
Graph 11. Data Hold Time vs. Supply Voltage



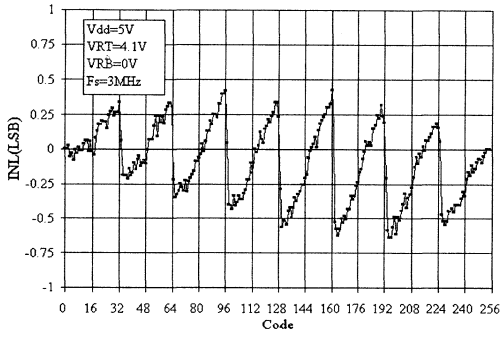
Graph 12. Aperture Delay vs. Supply Voltage



Graph 13. Tristate Enable Delay vs. Supply Voltage



Graph 14. DNL Error Plot



Graph 15. INL Error Plot

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MP7695

1 MSPS, CMOS
Very Low Power 10-Bit
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from <1 kHz to 2 MHz**
- **DNL better than 1/2 LSB (typ) up to 1 MHz**
- **Very Low Power CMOS - 30 mW (typ)**
- **Monotonic; No Missing Codes**
- **Interface to any Input Range between GND and V_{DD}**
- **No S/H Required for CCD or most Muxed Input Applications**
- **Single Power Supply (4 to 6 volts)**
- **Latch-Up Free**
- **High ESD Protection: 4000 Volts Minimum**
- **Use MP8795 For New Designs**
- **No S/H Required for Signals <25kHz**

BENEFITS

- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer Can Adapt Input Range & Scaling**

APPLICATIONS

- **µP/DSP Interface and Control Applications**
- **High Resolution Imaging – Scanners, Copiers, Facsimile**
- **Multiplexed Data Acquisition**
- **Radar Pulse Analysis**
- **Low Power A/D Applications**

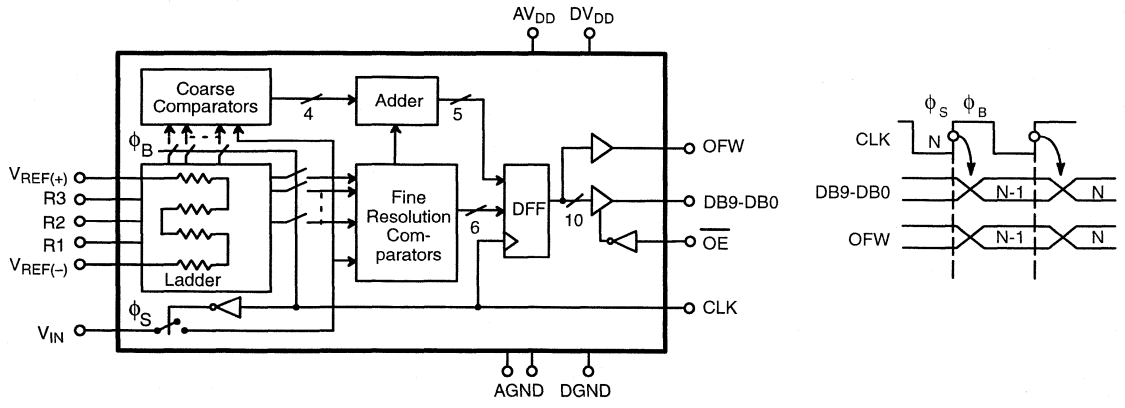
3

GENERAL DESCRIPTION

The MP7695 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter that operates over a wide range of input and sampling conditions. The MP7695 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 2 MHz. The elimination of S/H, operation of 5 V supply and small board space offer the designer a low cost solution, while also offering very low power consumption (30mW typ.) even at high speed (1 MHz) operation. No sample and hold is required for CCD applications, up to 2 MHz, or multiplexed input applications when the signal source bandwidth is limited to 25 kHz. The input architecture of the MP7695 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP7695 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



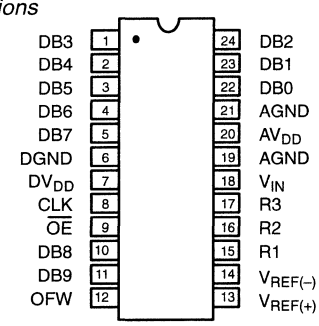
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7695AN	±1	1 1/4
SOIC	–40 to +85°C	MP7695AS	±1	1 1/4
Ceramic Dip	–40 to +85°C	MP7695AD	±1	1 1/4
Ceramic Dip	–55 to +125°C	MP7695SD*	±1	1 1/4

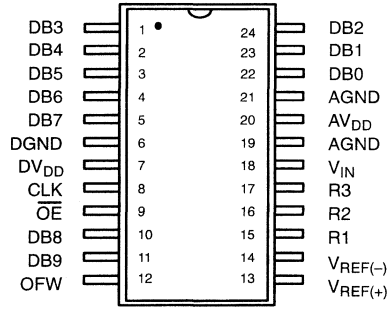
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin CDIP, PDIP (0.300")
DN24, NN24



24 Pin SOIC (EIAJ, 0.335")
R24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(-)}$	Lower Reference Voltage
15	R1	Reference Ladder Tap
16	R2	Reference Ladder Tap
17	R3	Reference Ladder Tap
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	AGND	Analog Ground
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 1 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.6, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		10			10		Bits	
Sampling Rate	F_S	.001		1	.001	1	MHz	For Rated Performance
ACCURACY[2]								
Differential Non-Linearity	DNL							
AN, AS, AD				±3/4		±3/4	LSB	99.2% of Codes
				±1 1/4		±1 1/4	LSB	100% of Codes
Integral Non-Linearity	INL							
AN, AS, AD			±3/4	2		2	LSB	Best Fit Line
Zero Scale Error	EZS		±2				mV	
Full Scale Error	EFS		±10				mV	
DYNAMIC ACCURACY[1]								Histogram Test
Differential Non-Linearity	DNL		±1/2				LSB	F_{IN} = 7 kHz
	DNL		±1				LSB	F_{IN} = 10 kHz
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			AGND		V	
Differential Ref. Voltage[5]	V_{REF}	2.0		V_{DD}	3.0	V_{DD}	V	
Ladder Resistance	R_L	525	675	900	475	1200	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[1]								
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60				pF	
Aperture Delay	t_{AP}		35				ns	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2.0			2.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Leakage Currents	I_{IN}							V_{IN}=DGND to DV_{DD}
CLK				±100		±100	µA	
$\overline{OE}$ (Internal Res to GND)		–5		30	–5	30	µA	
Input Capacitance			5				pF	
Clock Timing (*See Figure 1.*)[1]								
Clock Period	t_S	1000			1000		ns	
Rise & Fall Time[4]	t_R, t_F			10		10	ns	
"High" Time[6]	t_B	500		500,000	500	500,000	ns	
"Low" Time[6]	t_S	500		500,000	500	500,000	ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			DV_{DD}-0.5		V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5		±10	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30		20		ns	
Data Valid Delay[1]	t_{DL}		70			90	ns	
Data Enable Delay[1]	t_{DEN}		25			50	ns	
Data Tristate Delay[1]	t_{DHZ}		15			35	ns	
POWER SUPPLIES[8]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	4	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10		12	mA	V_{IN} = 2 V

NOTES:

1 Guaranteed. Not tested.

2 Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 4.*).

3 See V_{IN} input equivalent circuit (*see Figure 5.*).

4 Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.

5 Specified values guarantee functional device. Refer to other parameters for accuracy.

6 System can clock MP7695 with any duty cycle as long as all timing conditions are met.

7 Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.

8 AV_{DD} & DV_{DD} are connected through silicon substrate. Connect together at package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

CDIP, PDIP, SOIC 1000mW

Derates above 75°C ..... 13mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

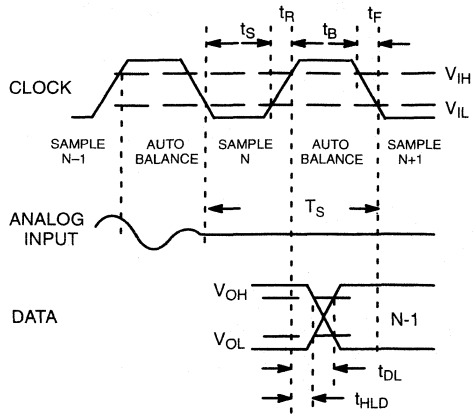


Figure 1. MP7695 Timing Diagram

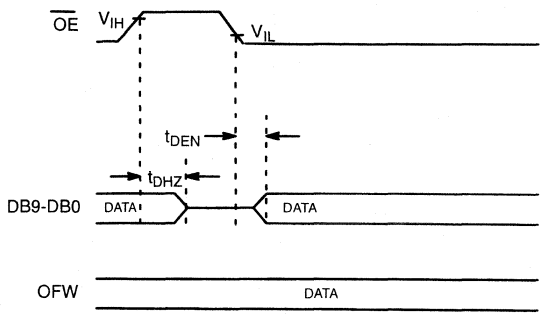
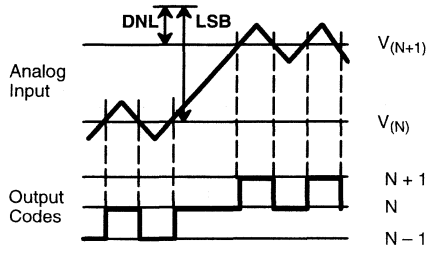


Figure 2. Output Enable/Disable Timing Diagram



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 3. DNL Measurement On Production Tester

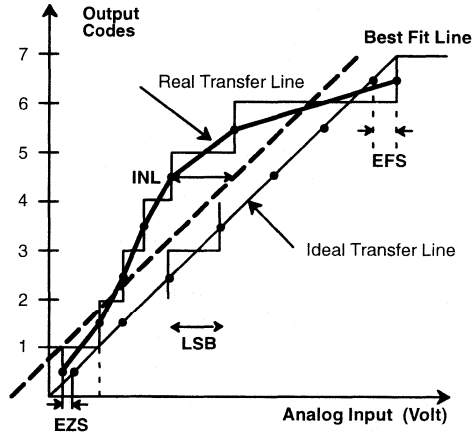


Figure 4. INL Error Calculation

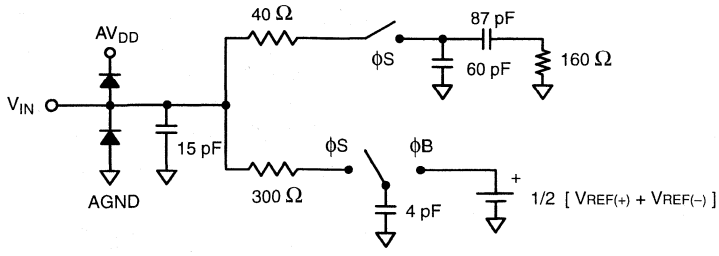


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7695 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

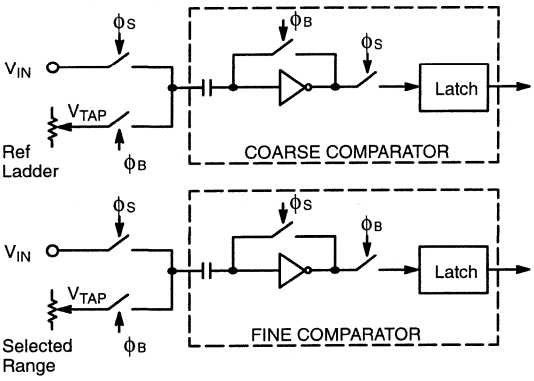


Figure 6. MP7695 Comparators

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 6.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

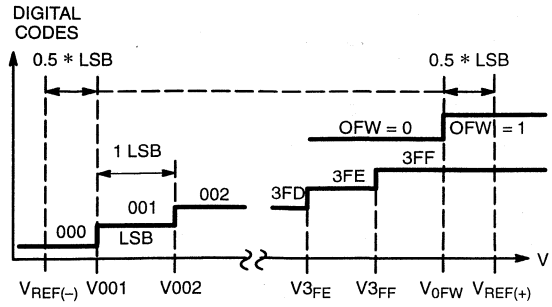


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V3_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 1024 = (V3_{FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

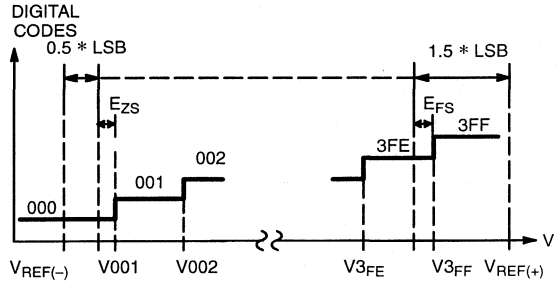


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

$DNL\ (001) = V002 - V001 - LSB$

: : :

$DNL\ (3FE) = V3_{FF} - V3_{FE} - LSB$

E_{FS} (full scale error) = $V3_{FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

Figure 8. shows the zero scale and full scale error terms.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

Clock and Conversion Timing

A system will clock the MP7695 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9a* shows normal operation, while the timing of *Figure 9b* keeps the MP7695 in balance and ready to sample the analog input.

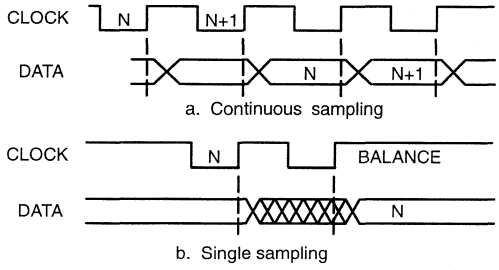


Figure 9. Relationship of Data to Clock

Analog Input

The MP7695 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7695's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE}$ controls the output buffers in an asynchronous mode.

$\overline{OE}$	OFW	DB9 – DB0
1	Valid	High Z
0	Valid	Valid

Table 1. Output Enable Logic

The functional equivalent of the MP7695 (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

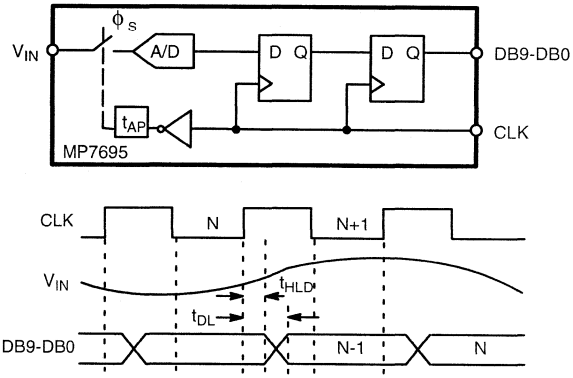
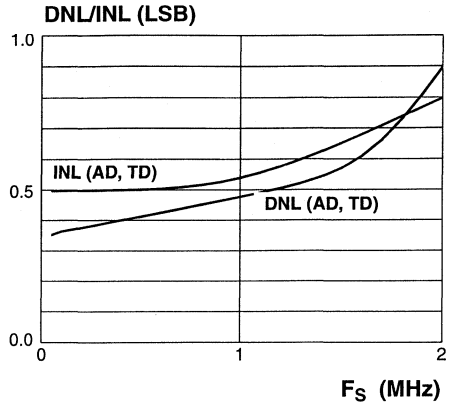


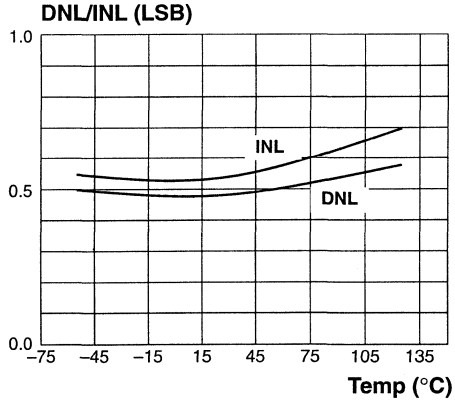
Figure 10. MP7695 Functional Equivalent Circuit and Interface Timing

CHARACTERIZATION CHARTS

(Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S =$ 1 MHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)} = AGND$, $T_A = 25°C$



Accuracy (DNL/INL)
vs. Sampling Rate (F_S)



Accuracy (DNL/INL)
vs. Ambient Temperature (T)

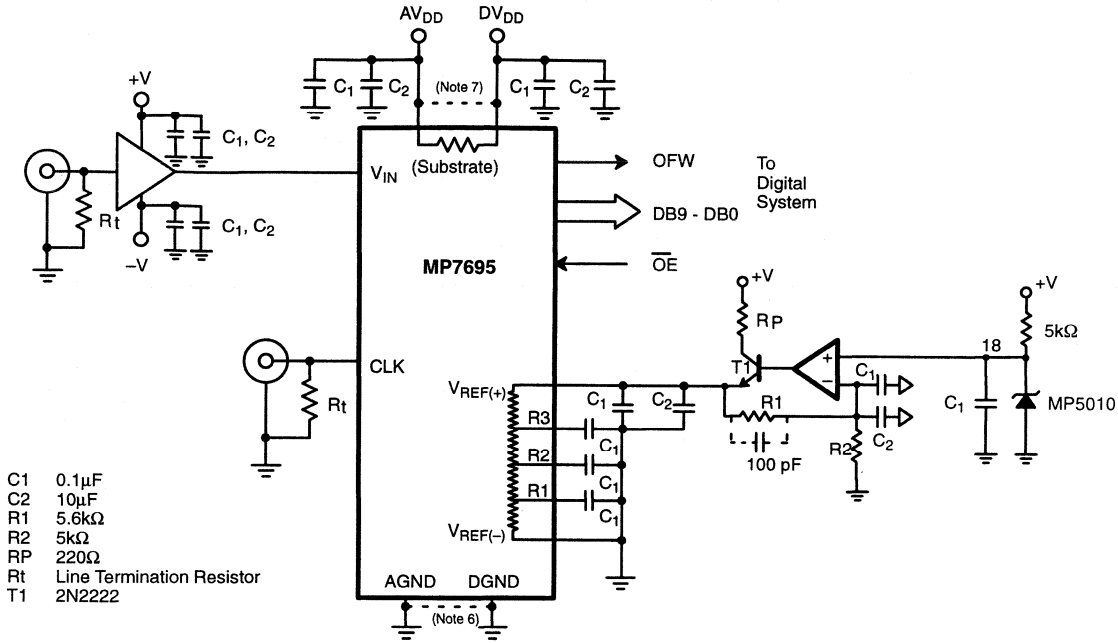


Figure 11. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP7695.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7695. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP7695.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP7695 should be connected to AV_{DD} next to the MP7695.
8. DV_{DD} and AV_{DD} are connected inside the MP7695 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

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MP7696

CMOS
Very Low Power, 9-Bit
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 1 kHz to 2 MHz**
- **DNL better than 1/2 LSB (typ) up to 1 MHz**
- **Very Low Power CMOS - 30 mW (typ)**
- **Monotonic; No Missing Codes**
- **Interface to any Input Range between GND and V_{DD}**
- **No S/H needed for Input Signals Less Than 10 kHz**
- **Single Power Supply (4 to 6.5 Volts)**
- **Latch-Up Free**
- **High ESD Protection: 4000 Volts Minimum**
- **For New Designs use MP8784 or MP8795**

BENEFITS

- **Reduced Board Space (Small Package)**
- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer Can Adapt Input Range & Scaling**

APPLICATIONS

- **Low Power A/D Applications**
- **High Resolution Imaging**
- **Multiplexed Data Acquisition**
- **Radar Pulse Analysis**

3

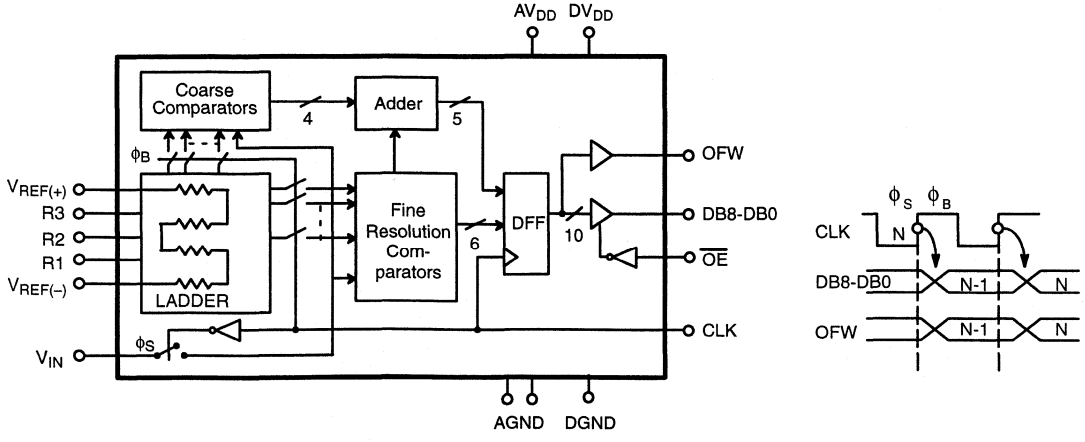
GENERAL DESCRIPTION

The MP7696 is a 9-bit CMOS Analog-to-Digital Converter designed for precision applications demanding *Low Power Consumption*. The input architecture of the MP7696 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP7696 uses a two-step flash technique. The first segment converts the 3 MSBs and consists of 8 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

With 30 mW power dissipation, the MP7696 achieves its excellent performance due to the inherent high speed of our proprietary 2µ Refractory Molybdenum CMOS Process.

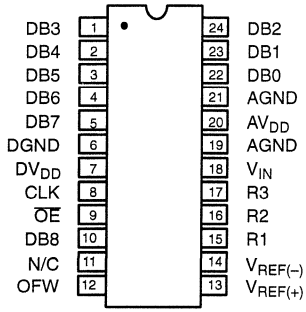
SIMPLIFIED BLOCK AND TIMING DIAGRAM



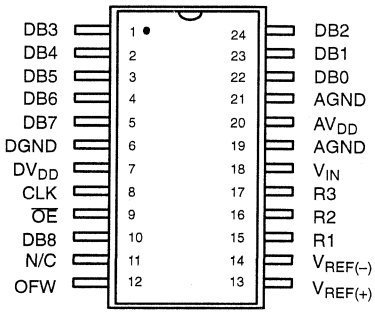
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7696AN	±1	1
SOIC	–40 to +85°C	MP7696AS	±1	1

PIN CONFIGURATIONS



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (EIAJ, 0.335")
R24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8 (MSB)
11	N/C	No Connection
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(-)}$	Lower Reference Voltage
15	R1	Reference Ladder Tap
16	R2	Reference Ladder Tap
17	R3	Reference Ladder Tap
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	AGND	Analog Ground
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

MP7783

CMOS
Low Power 8-Bit
Analog-to-Digital Converter

FEATURES

- **Sampling Rates up to 3 MHz**
- **Requires NO SAMPLE AND HOLD for CCD Outputs or for Signals less than 100 kHz**
- **Single Supply Voltage**
- **Low Power Consumption (100 mW typ)**
- **Latch-Up Free**

APPLICATIONS

- **Data Acquisition Systems**
- **Computer Peripherals**
- **Scanners**
- **Process Control**

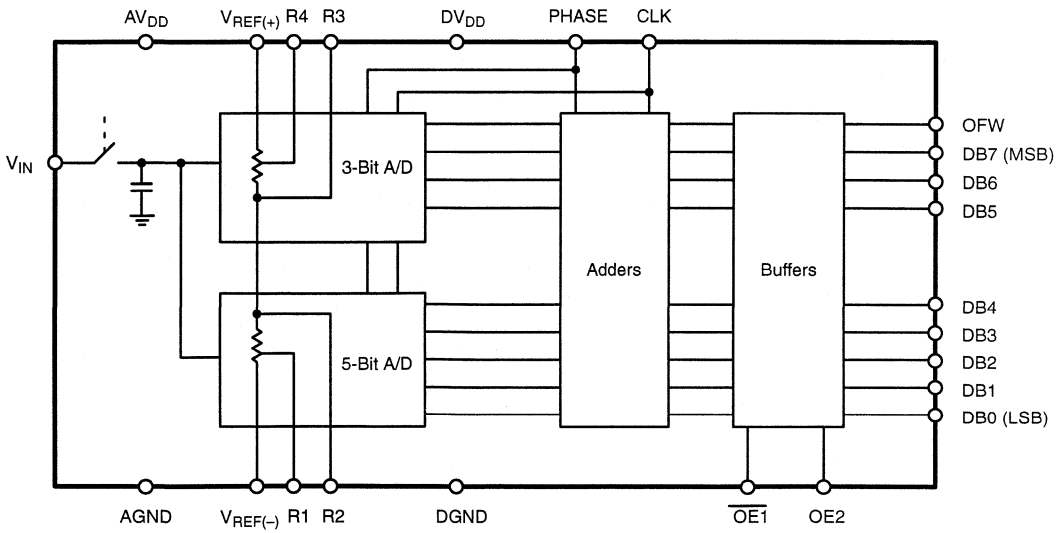
3

GENERAL DESCRIPTION

The MP7783 is a CMOS 8-Bit two step Analog-to-Digital Converter designed for precision applications requiring conversion times under a micro-second. Featuring a built in Track and Hold function, input signals to 100 kHz can be digitized with confidence. Integral and differential non-linearities are typically less than 1/4 LSB, with a clock frequency of 2 MHz and a supply of 5 volts.

Built on EXAR's proprietary CMOS technology, the conversion is done in two segments. The first segment converts the 3 MSBs while the second segment converts the five LSBs. An overflow bit is provided for applications requiring 9-bit resolution by using two devices in cascade.

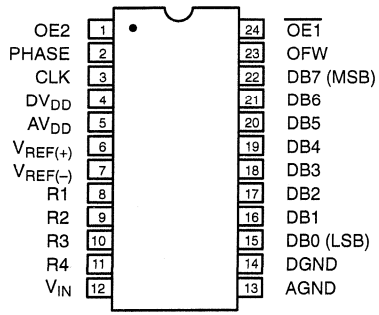
SIMPLIFIED BLOCK DIAGRAM



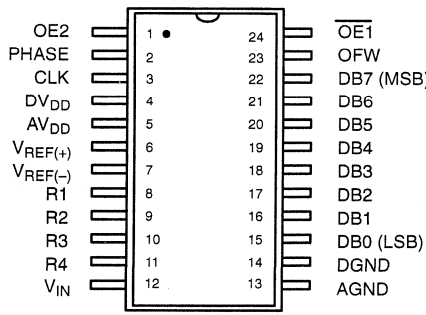
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7783JN	±3/4	±3/4
SOIC	–40 to +85°C	MP7783JS	±3/4	±3/4

PIN CONFIGURATIONS



24 Pin PDIP (0.600")
N24



24 Pin SOIC (EIAJ, 0.335")
R24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	OE2	Output Enable Control 2
2	PHASE	Sampling Clock Phase Control
3	CLK	Clock Input
4	DV_{DD}	Power Supply for Digital Circuits
5	AV_{DD}	Power Supply for Analog Circuits
6	$V_{REF(+)}$	Reference Voltage (+) Input
7	$V_{REF(-)}$	Reference Voltage (–) Input
8	R1	1/16th Point of Ladder R Matrix
9	R2	5/16th Point of Ladder R Matrix
10	R3	9/16th Point of Ladder R Matrix
11	R4	13/16th Point of Ladder R Matrix
12	V_{IN}	Analog Input

PIN NO.	NAME	DESCRIPTION
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DB0	Data Output Bit 0 (LSB)
16	DB1	Data Output Bit 1
17	DB2	Data Output Bit 2
18	DB3	Data Output Bit 3
19	DB4	Data Output Bit 4
20	DB5	Data Output Bit 5
21	DB6	Data Output Bit 6
22	DB7	Data Output Bit 7 (MSB)
23	OFW	Digital Output Overflow
24	$\overline{OE1}$	Output Enable Control 1

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 2.5 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate[1]	F_S	0.001		3.0	0.001	3.0	MHz	
ACCURACY (J Grade)[2]								
Differential Non-Linearity	DNL			±3/4		±3/4	LSB	
Integral Non-Linearity	INL			±3/4		±3/4	LSB	Best Fit Line
REFERENCE VOLTAGES								
Positive Ref. Voltage[3]	$V_{REF(+)}$			AV_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			AGND		V	
Differential Ref. Voltage	V_{REF}	AV_{DD}-AGND			AV_{DD}-AGND		V	
Ladder Resistance	R_L	500		1500	300	1950	Ω	
Ladder Temp. Coefficient[4]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[4]								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance Sample[6]	C_{IN}		50				pF	
Aperture Delay[7]	t_{AP}		55				ns	
Aperture Uncertainty (Jitter)[7]	t_{AJ}		200				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			0.4		0.4	V	
Leakage Currents[8]								V_{IN}=DGND to DV_{DD}
$\overline{CLK}$	I_{IN}			±50		±50	µA	
Input Capacitance[4]	C_{IN}		5				pF	
Clock Timing (*See Figure 1.*)								
Clock Period	t_S	400			400		ns	
"High" Time	t_H	200			200		ns	
"Low" Time	t_L	200			200		ns	
Duty Cycle			50				%	
DIGITAL OUTPUTS								C_{OUT}=5 pF
Logical "1" Voltage	V_{OH}	4.6			4.6		V	I_{LOAD} = −1.0 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 2.0 mA
3-state Leakage	I_{OZ}			±50		±60	µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[4]	t_{DL}		55				ns	
Data Enable Delay[4]	t_{DEN}		20				ns	
Data 3-state Delay[4]	t_{DHZ}		26				ns	
Digital Output Delay[4]	t_D			55			ns	
Output Capacitance[4]	C_{OL}		5				ns	

3

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLIES[9]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4.0	5.0	6.0		6.0	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			20.0		36.0	mA	

NOTES

1 Maximum sampling frequency is the frequency which will still meet the non-linearity specification. However, the device is capable of higher frequency operation.

2 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

3 For best results, it is recommended that the reference voltage be limited to AV_{DD} –0.5 V.

4 Guaranteed. Not tested.

5 Specified values guarantee functionality. Refer to other parameters for accuracy.

6 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

7 All inputs have diodes to DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply. DGND should be tied to AGND at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +6.5 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... V_{DD} to GND

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

Digital Inputs ..... GND –0.5 to V_{DD} +0.5 V

Digital Outputs ..... GND –0.5 to V_{DD} +0.5 V

Operating Temperature ..... 0 to +70°C

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering 10 secs) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC 1000mW

Derates above 75°C ..... 13mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

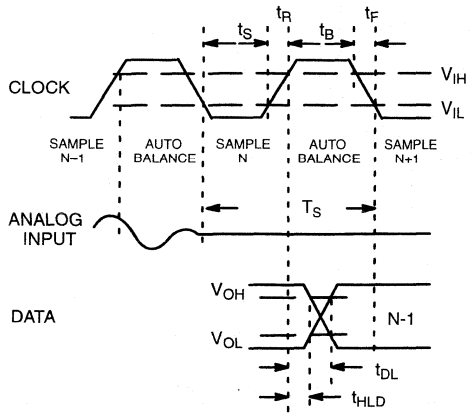


Figure 1. MP7783 Timing Diagram

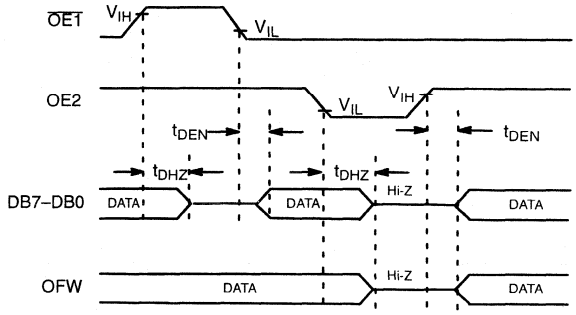
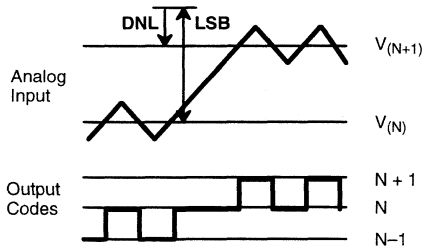


Figure 2. Output Enable/Disable Timing Diagram

3



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

DNL(N) = [$V_{(N+1)} - V_{(N)}$] – LSB

Figure 3. DNL Measurement

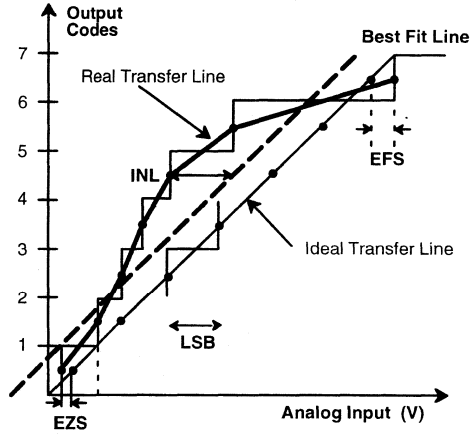


Figure 4. INL Error Calculation

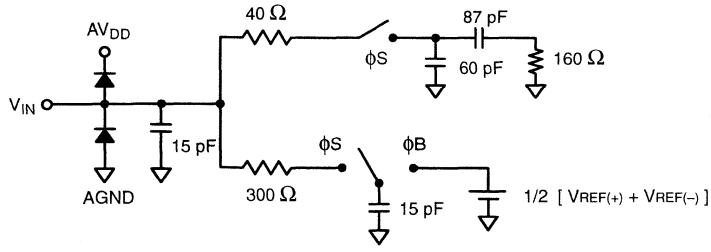


Figure 5. Analog Input Equivalent Circuit

DEVICE OPERATION

Figure 1. shows the timing information for the MP7783. A reference voltage is applied between the $V_{REF(+)}$ and $V_{REF(-)}$ which drives 256 resistors and switches with 4 voltage taps. These taps drive the inverting inputs of comparators. There are four control lines: Clock, $\overline{OE1}$, OE2 and phase. The phase line determines the polarity of the clock.

Figure 6. shows waveforms with the phase line high and low. With phase = 1, the "sample" occurs during the high period of the clock cycle, and the "auto-balance" occurs during the low period of the clock. The "sample" is queued and pipelined through a series of registers and latches. It appears at the output after 2 clock periods and time delay (Td). After the sample is acquired the data is valid for every clock period. The $\overline{OE1}$ will independently disable the 8 data bit buffers when it is in a high state. The truth table (*Table 1.*) summarizes this effect.

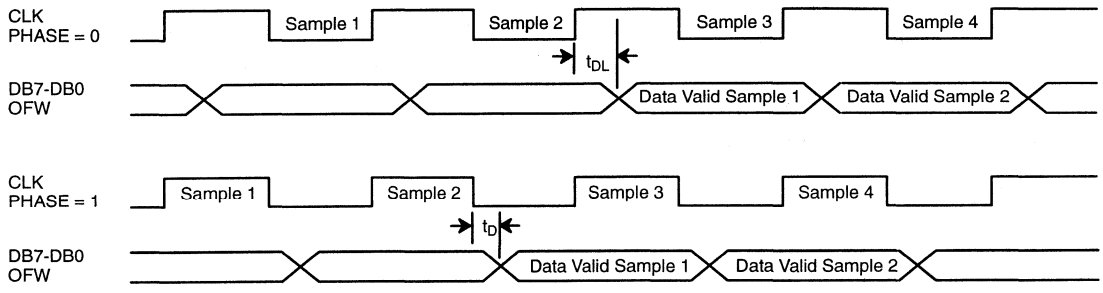


Figure 6. Timing Diagram

$\overline{OE1}$	OE2	DB7 - DB0	OFW
0	1	Valid	Valid
1	1	3-state	Valid
X	0	3-state	3-state

Table 1. Truth Table

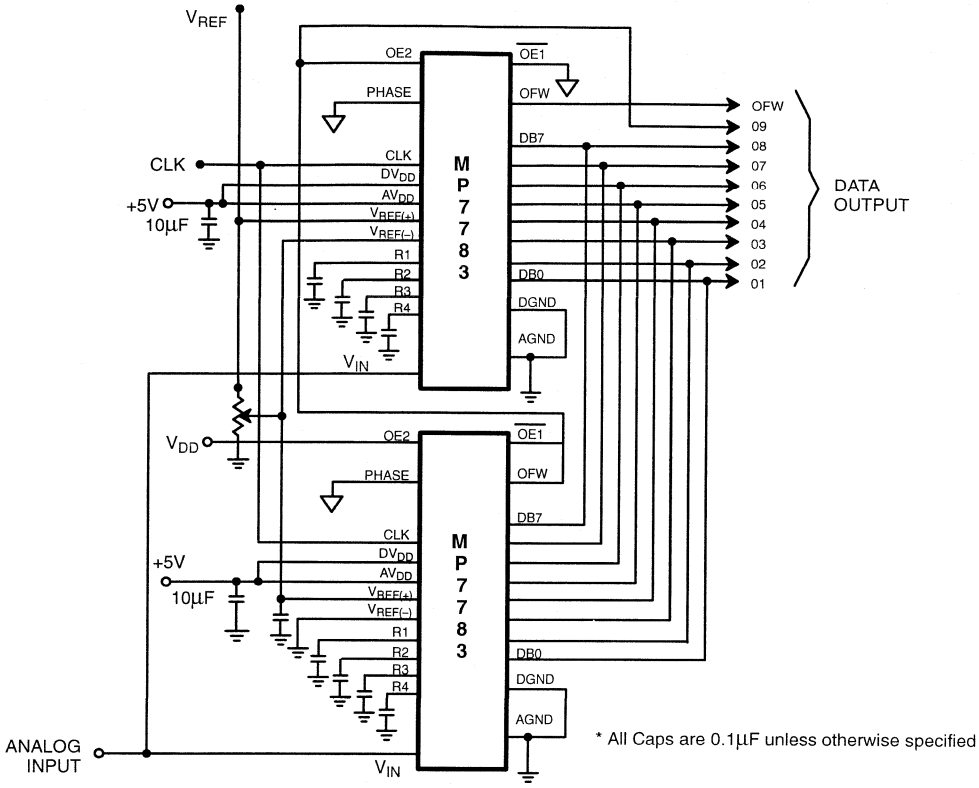


Figure 7. MP7783 9-Bit Resolution Configuration

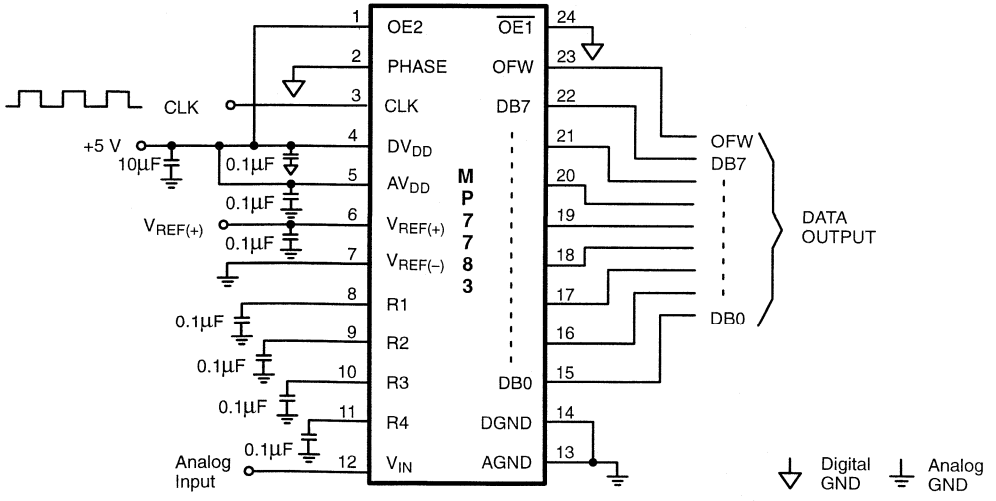


Figure 8. MP7783 Typical Connections

LINEARITY ADJUSTMENT

As noted in the specifications, integral non-linearity can be adjusted externally to enhance performance. While the setup may seem a little awkward, we have found that it can prove beneficial for high speed applications requiring 1/4 LSB at room temperature and 1/2 LSB over temperature.

Referring to *Figure 9.*, the reference resistor taps for 1/16th, 5/16ths, 9/16ths and 13/16ths of V_{REF} are brought out separately. In normal applications the user simply ties a 0.1 µF capacitor to ground at each of these nodes to provide a measure of filtering when the comparators are "zeroed" to their respective reference voltage points along the continuous ladder network. To compensate for comparator loading and other subtle errors associated with the distributed resistance of the ladder, the user can connect a "true" voltage source at each node and trim for optimized performance. As shown in *Figure 10.*, a series of op amps is used to set the proper voltage at each node. The value is best determined empirically by setting the nominal value for the node (e.g. 1/16th of V_{REF} at R1) and then fine tuning to significantly reduce the integral error.

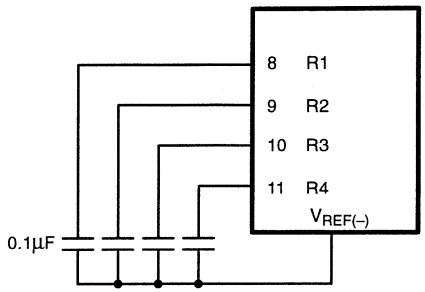


Figure 9.

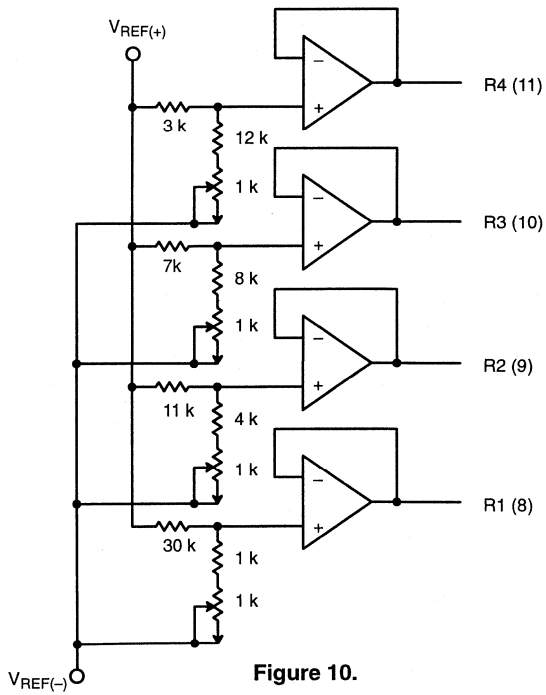
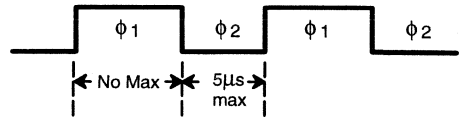


Figure 10.

APPLICATION NOTES:

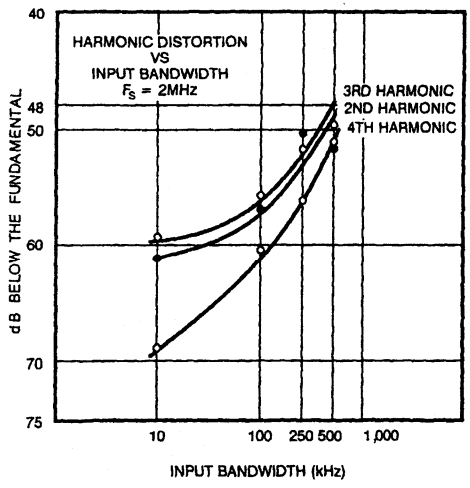
The following information will be useful in maximizing the performance of the MP7783.

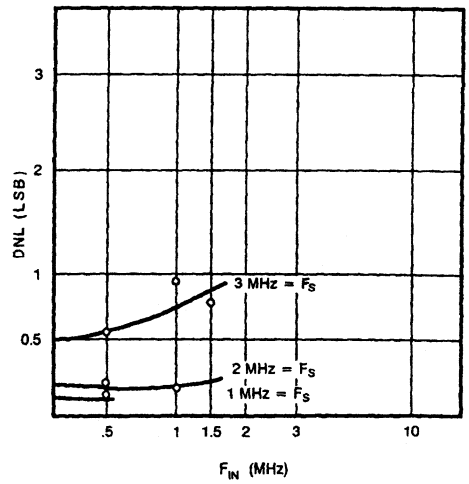
1. This device may be susceptible to latch-up. All signals must not exceed DV_{DD} or DGND, or AV_{DD} or AGND at any time. Power should always be applied before any input signal is connected to avoid a latch-up condition.
2. The design of the PC layout and assembly will seriously affect the accuracy of the MP7783. Use of wire wrap is not recommended.
3. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
4. The analog input should be driven with a buffer Op Amp ($Z_{OUT} \leq 50\ \Omega$).
5. The use of a large shield plane is highly recommended, connected only at one point and connected to virtual ground.
6. The power supplies and reference voltages should be decoupled with ceramic (0.01 to 0.1µF) and tantalum (10µF) capacitors as close to the device as possible.
7. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.



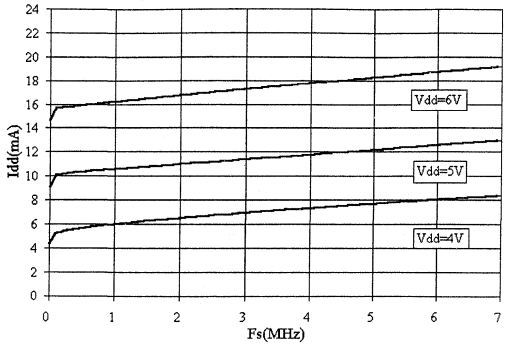
a. The minimum clock rate at 50% Duty Cycle is 10 kHz.
b. The minimum clock rate at non-50% Duty cycle may be DC as long as ϕ2 is kept to less than 5 µs.

3

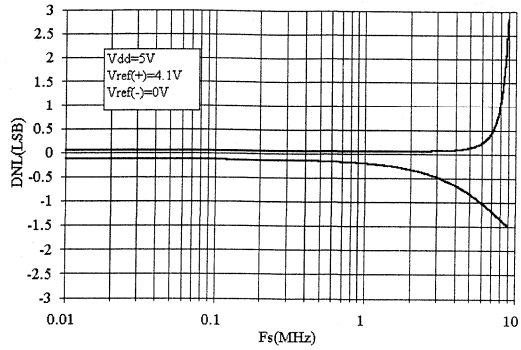




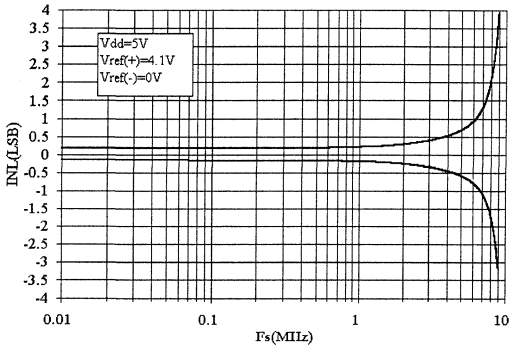
PERFORMANCE CHARACTERISTICS



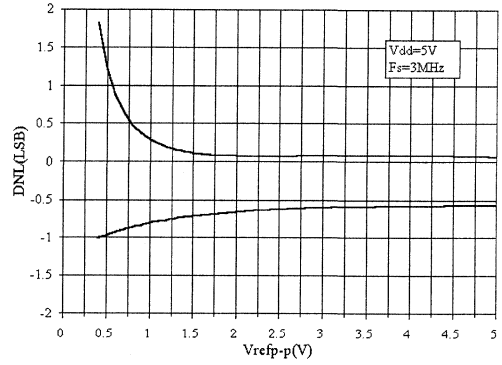
Graph 1. Supply Current vs. Sampling Frequency



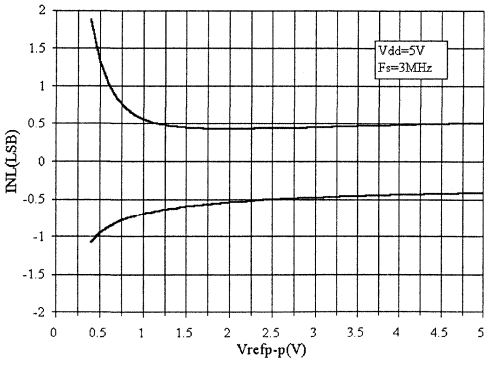
Graph 2. DNL vs. Sampling Frequency



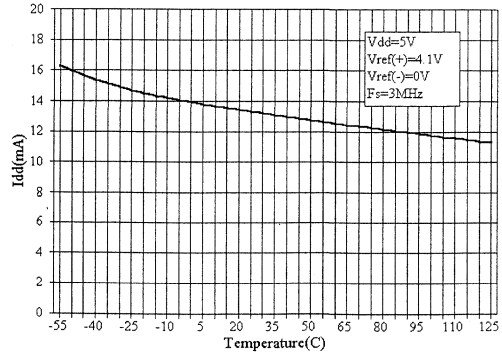
Graph 3. INL vs. Sampling Frequency



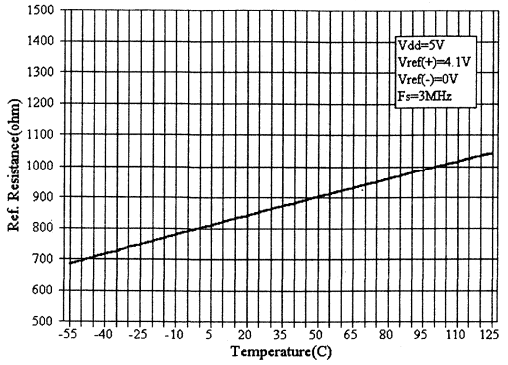
Graph 4. DNL vs. Reference Voltage



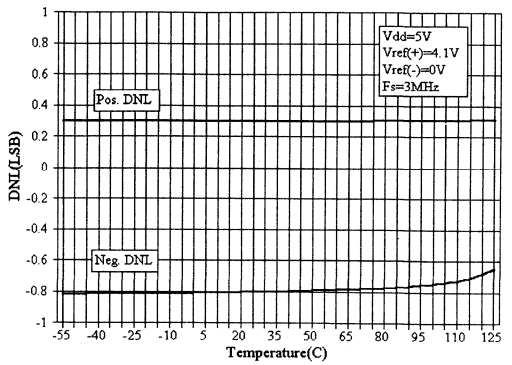
Graph 5. INL vs. Reference Voltage



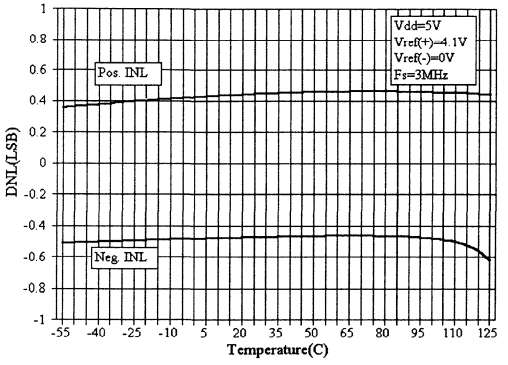
Graph 6. Supply Current vs. Temperature



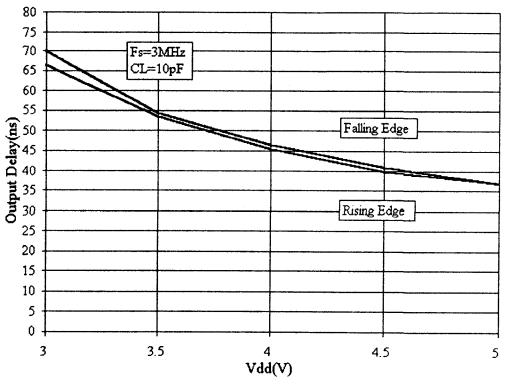
Graph 7. Reference Resistance vs. Temperature



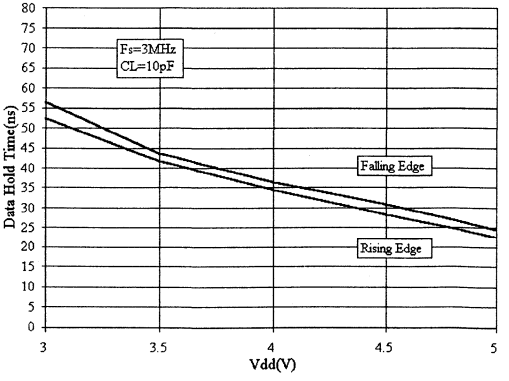
Graph 8. DNL vs. Temperature



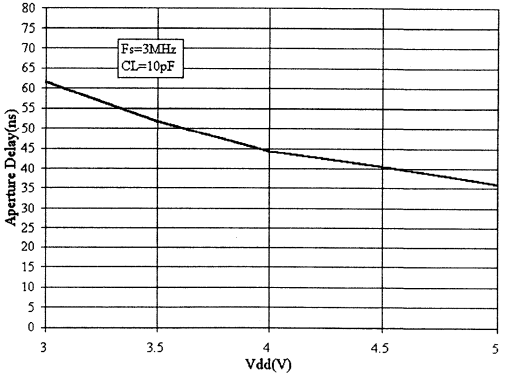
Graph 9. INL vs. Temperature



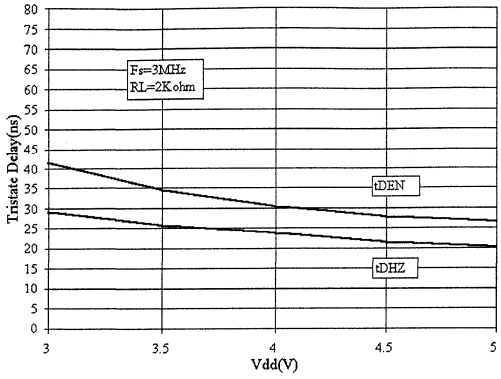
Graph 10. Output Delay vs. Supply Voltage



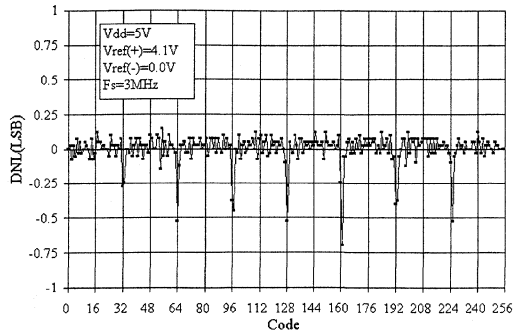
Graph 11. Data Hold Time vs. Supply Voltage



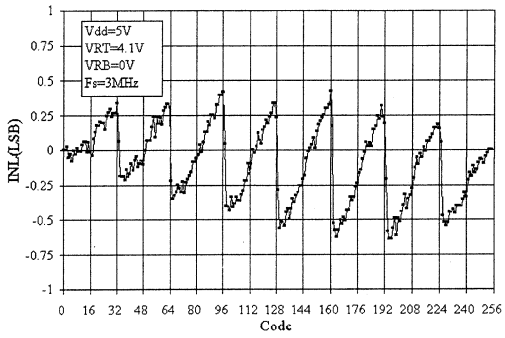
Graph 12. Aperture Delay vs. Supply Voltage



Graph 13. 3-state Enable Delay vs. Supply Voltage



Graph 14. DNL Error Plot



Graph 15. INL Error Plot

MP8775

CMOS
20 MSPS, 8-Bit, High Speed
Analog-to-Digital Converter

FEATURES

- **8-Bit Resolution**
- **20 MHz Sampling Rate**
- **DNL = ±1/2 LSB, INL = ±1 LSB (typ)**
- **Internal S/H Function**
- **Single Supply: 5 V**
- **V_{IN} DC Range: 0 V to V_{DD}**
- **V_{REF} DC Range: 1 V to V_{DD}**
- **Low Power: 85 mW typ. (excluding reference)**
- **Latch-Up Free**
- **ESD Protection: 1500 V Minimum**
- **Power Down Available: MP8776**
- **3 V Version: MP87L75**
- **Small 20 Pin SOIC Package**

APPLICATIONS

- **Digital Color Copiers**
- **Cellular Telephones**
- **CCD's and Scanners**
- **Video Capture Boards**

3

GENERAL DESCRIPTION

The MP8775 is an 8-bit Analog-to-Digital Converter in a small 20 pin SOIC package. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

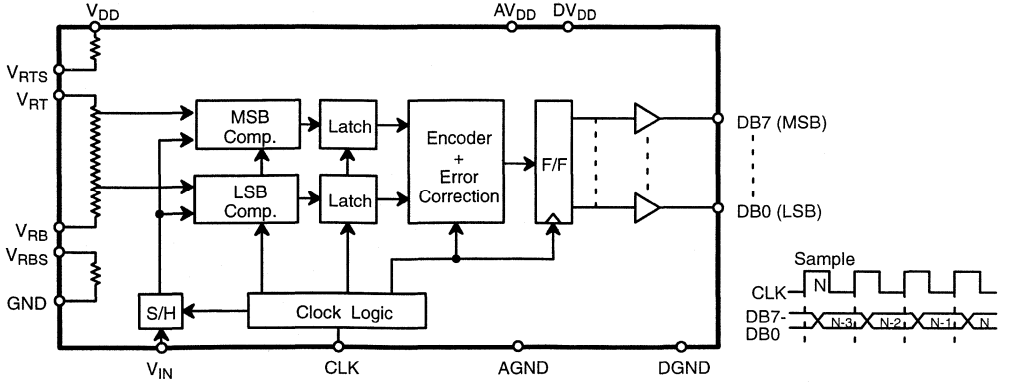
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8775 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP8775.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 V supply. Power consumption is 85 mW at FS = 20 MHz.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP8775 is available in Surface Mount (SOIC), Shrunk Small Outline (SSOP) and Plastic dual-in-line (PDIP) packages.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

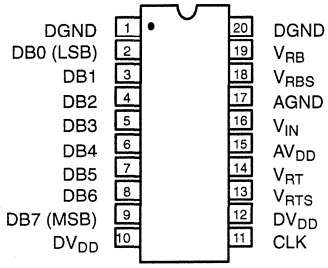


ORDERING INFORMATION

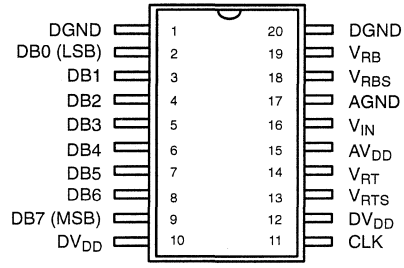
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP8775AS	±3/4	±1 1/2
PDIP	–40 to +85°C	MP8775AN	±3/4	±1 1/2
SSOP	–40 to +85°C	MP8775AQ	±3/4	±1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV_{DD}	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV_{DD}	Digital Power Supply
13	V_{RTS}	Generates 2.6 V if tied to V_{RT}
14	V_{RT}	Top Reference
15	AV_{DD}	Analog Power Supply
16	V_{IN}	Analog Input
17	AGND	Analog Ground
18	V_{RBS}	Generates 0.6 V if tied to V_{RB}
19	V_{RB}	Bottom Reference
20	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 15 MHz (50% Duty Cycle), V_{RT} = 2.6 V, V_{RB} = 0.6 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS			20	MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±3/4	LSB	@ 15 MHz
Differential Non-Linearity	DNL			±1/2	LSB	@ 10 MHz
Integral Non-Linearity	INL			1 1/2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±1 1/4		LSB	
Full Scale Error	EFS		±1 1/4		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	455	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.6		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		2		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		2.3		V	
ANALOG INPUT						
Input Bandwidth (–1 dB)[4]	BW		14		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance[5]	C_{IN}		16		pF	
Aperture Delay	t_{AP}		20		ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	4.0			V	
Logical "0" Voltage	V_{IL}			1.0	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[7]						
Clock Period	1/FS	50			ns	
High Pulse Width	t_{PWH}	25			ns	
Low Pulse Width	t_{PWL}	25			ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Data Valid Delay[2, 8]	t_{DL}		20	25	ns	
Data Hold Line	t_{HL}		12	15	ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
AC PARAMETERS						
Differential Gain Error	d_G		2		%	FS = 4 x NTSC
Differential Phase Error	d_{PH}		1		°	FS = 4 x NTSC
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		17	25	mA	Does not include ref. current

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 2.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 3.*). Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} input equivalent circuit (*Figure 4.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 t_R, t_F should be limited to >5 ns for best results.

8 Depends on the RC load connected to the output pin.

9 AGND and DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
SOIC, SSOP, PDIP ..... 700 mW
Derates above 75°C ..... 9 mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

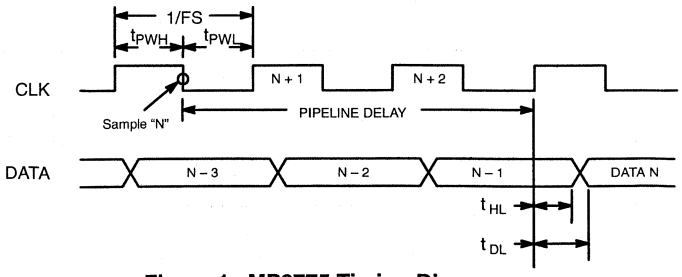
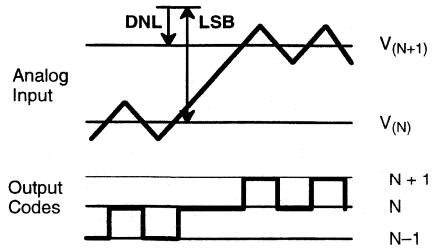


Figure 1. MP8775 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 256

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 2. DNL Measurement

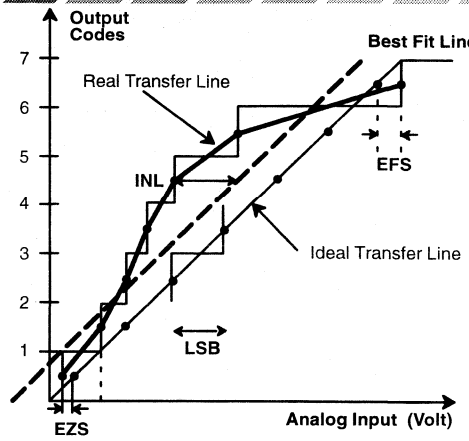


Figure 3. INL Error Calculation

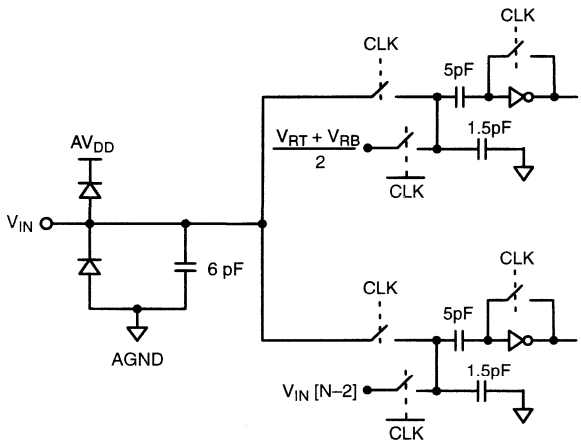


Figure 4. Equivalent Input Circuit

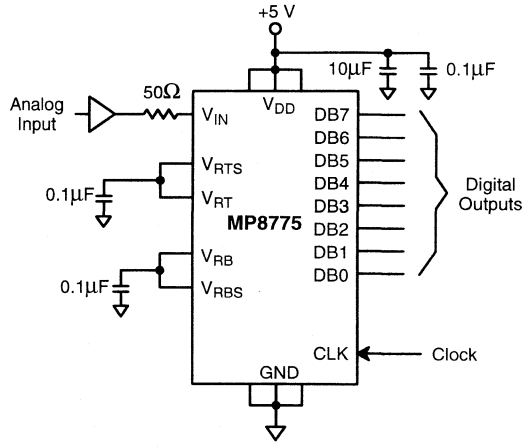


Figure 5. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V or DV_{DD} +0.5 V or DGND –0.5 V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

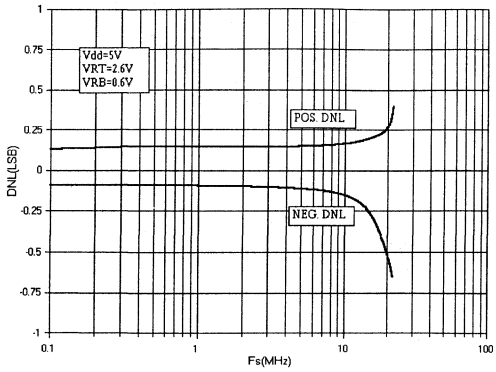
The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

It is possible for the data valid delay (t_{DL}) to be equal to or greater than the high pulse width of the sampling clock (t_{PWH}), See *Figure 1.* This can cause timing related errors. For sample rates above 14 MSPS use only the rising edge of the sample clock (CLK) to latch data from the MP8775 to other parts of the system.

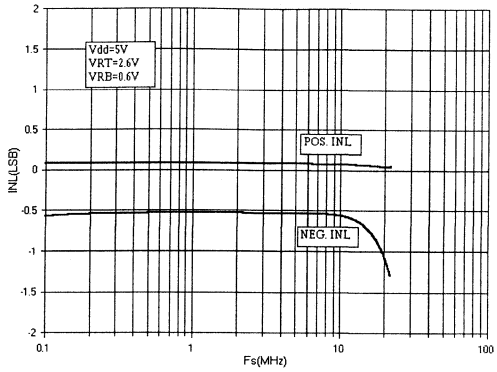
The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.6 V at V_{RB} and 2.6 V at V_{RT} (see *Figure 5.).*

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

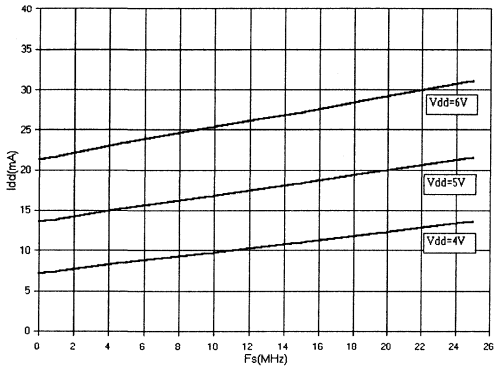
PERFORMANCE CHARACTERISTICS



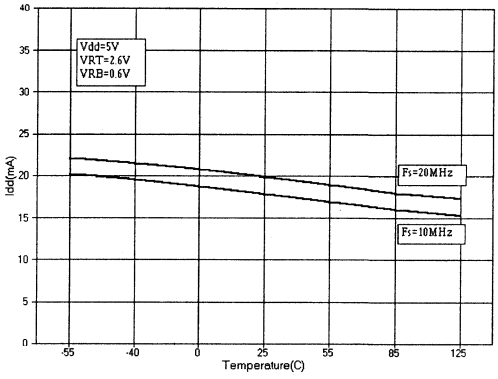
Graph 1. DNL vs. Sampling Frequency



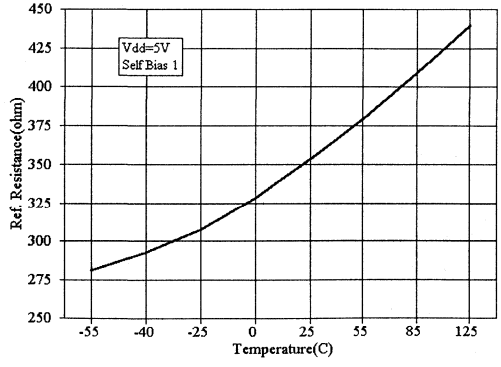
Graph 2. INL vs. Sampling Frequency



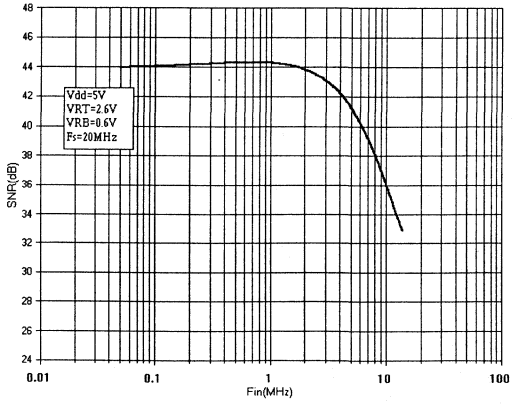
Graph 3. Supply Current vs. Sampling Frequency



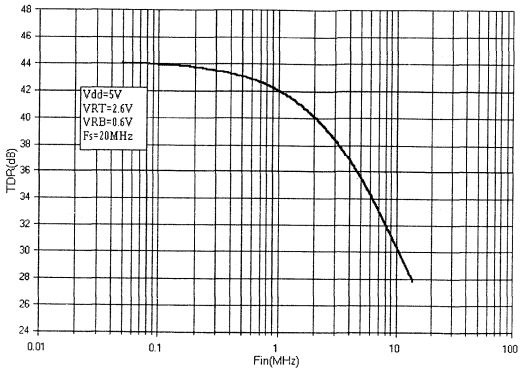
Graph 4. Supply Current vs. Temperature



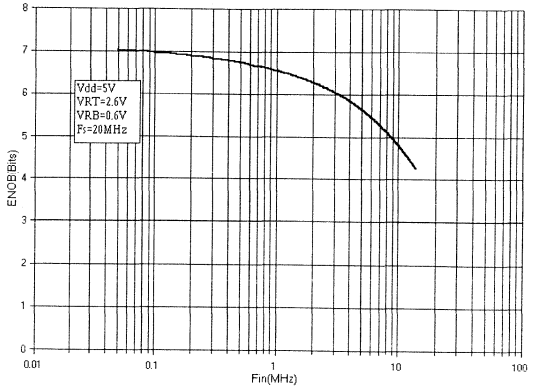
Graph 5. Reference Resistance vs. Temperature



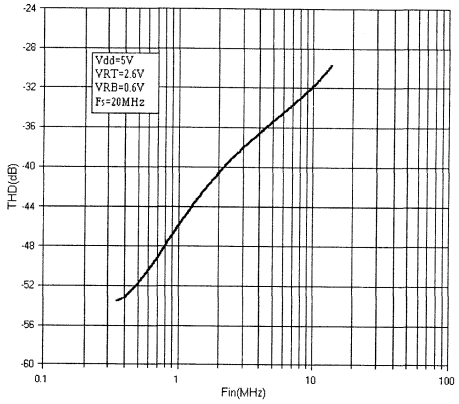
Graph 6. SNR vs. Input Frequency



Graph 7. SINAD vs. Input Frequency



Graph 8. ENOB vs. Input Frequency



Graph 9. THD vs. Input Frequency

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MP8776

CMOS
8-Bit High Speed, Low Power
Analog-to-Digital Converter with Power Down

FEATURES

- 8-Bit Resolution
- Sampling Rate to 30 MHz
- Low Power: 110 mW typ. (excluding reference)
- Power Down Mode: 100μA (typ)
- DNL = ±1/4 LSB, INL = ±1/2 LSB (typ)
- Internal S/H Function
- Single Supply: 5 V
- V_{IN} Range: 0 V to V_{DD}
- V_{REF} Range: 1 V to V_{DD}
- Latch-Up Tolerant
- ESD Protection: 2000 V Minimum
- 3 State Digital Outputs
- 20 Pin PDIP, SOIC and SSOP Packages
- 24 Pin Package Available: MP8786
- 3 V Version: MP87L76
- Improved Version of MP8775

APPLICATIONS

- Wireless Communications
- Digital Cellular Telephones
- Telecommunications
- CCD's and Scanners
- Video Boards
- Digital Color Copiers
- Battery Powered Devices

3

GENERAL DESCRIPTION

The MP8776 is an 8-bit Analog-to-Digital Converter designed for high speed digitizing applications requiring low power. The MP8776 offers exceptional performance, flexible input architecture, low power consumption, power down capability, latch-up tolerant operation and is manufactured using an advanced 5 volt CMOS process.

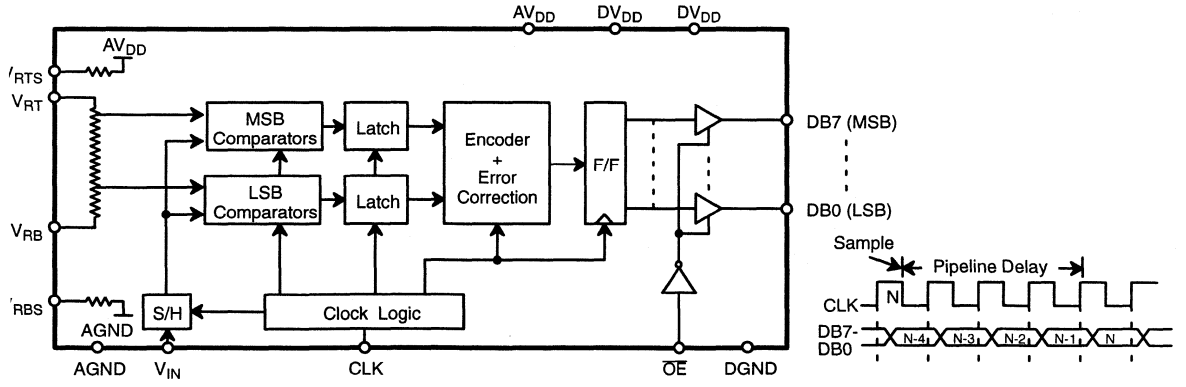
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8776 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP8776.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 volt supply. Power consumption is 110 mW (typ) at FS = 20 MHz. Power down is accomplished by dropping V_{RT} below 0.55 V.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP8776 is available in surface mount (SOIC), shrink small outline (SSOP) and plastic dual-in-line (PDIP) packages.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

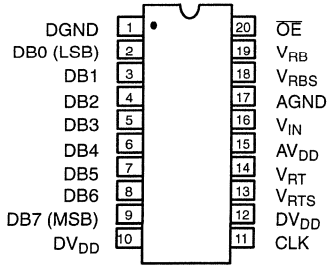


ORDERING INFORMATION

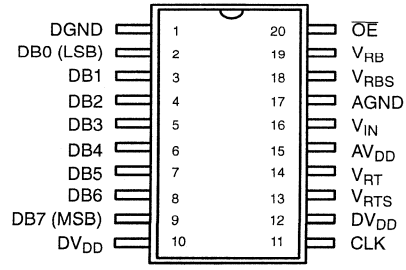
Package Type	Temperature Range	Part No.
SOIC	–40 to +85°C	MP8776AS
PDIP	–40 to +85°C	MP8776AN
SSOP	–40 to +85°C	MP8776AQ

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV_{DD}	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV_{DD}	Digital Power Supply
13	V_{RTS}	Generates 2.6 V if tied to V_{RT}
14	V_{RT}	Top Reference
15	AV_{DD}	Analog Power Supply
16	V_{IN}	Analog Input
17	AGND	Analog Ground
18	V_{RBS}	Generates 0.6 V if tied to V_{RB}
19	V_{RB}	Bottom Reference
20	$\overline{OE}$	Output Enable

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 20 MHz (50% Duty Cycle), V_{RT} = 2.6 V, V_{RB} = 0.6 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS	0.01		20	MHz	For specified performance
	FS			30	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL		±1/4	±1/2	LSB	
Integral Non-Linearity	INL		±1/2	1	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±35		mV	
Full Scale Error	EFS		±35		mV	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	455	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1	V_{RB}		0.6		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
	V_{REF}		2		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
Self Bias 2	V_{RT}		2.3		V	V_{RB} = AGND, Short V_{RT} and V_{RTS}
ANALOG INPUT[2]						
Bandwidth (–1 dB)[4]	BW		14		MHz	
Input Voltage Range	V_{IN}	0		AV_{DD}	V	
Input Capacitance Sample[5]	C_{IN}		22		pF	Clock High
Input Capacitance Convert[5]	C_{IN}		7		pF	Clock Low
Aperture Delay	t_{AP}		10		ns	
Aperture Jitter	t_{AJ}		30		ps	
DYNAMIC PERFORMANCE						F_{IN} = 1 MHz
Signal to Noise Ratio	SNR		46		dB	
Signal to Noise plus Distortion	SINAD		42		dB	
Harmonic Distortion	THD		–46		dB	
Effective No. of Bits	ENOB		6.8		Bits	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	3.5			V	
Logical "0" Voltage	V_{IL}			1.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 6.*)[7]						
Clock Period	1/FS	50			ns	For Specified Performance
High Pulse Width	t_{PWH}	25			ns	For Specified Performance
Low Pulse Width	t_{PWL}	25			ns	For Specified Performance

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=GND to DV_{DD}
Data Valid Delay[2, 8]	t_{DL}		20		ns	
Data Enable Delay[2, 8]	t_{DEN}		20	25	ns	
Data 3-state Delay[2, 8]	t_{DHZ}		12	15	ns	
Pipeline Delay				3.5	clock cycles	Constant relationship between clock and output
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		22	35	mA	Does not include ref. current
POWER DOWN						
Power Down Point	V_{RTPD}	0.4	0.55		V	Chip goes to power down mode
Power Up Point				0.9	V	when V_{RT} < 0.55 V
Power Down Current	I_{DDPD}			100	µA	Does not include ref. current
Power Control Delay	PDD			200	ns	V_{RT} @ 0.4→0.9 V

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 10.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 11.*) Accuracy is a function of the sampling rate (FS).
2 Guaranteed. Not tested.
3 Specified values guarantee functionality. Refer to other parameters for accuracy.
4 The bandwidth represents the gain of the ADC and does not imply accuracy
5 See V_{IN} input equivalent circuit (*Figure 2.*). Switched capacitor analog input requires driver with low output resistance.
6 All inputs have diodes to V_{DD} and GND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.
7 t_R, t_F should be limited to >5 ns for best results.
8 Depends on the RC load connected to the output pin.
9 AGND and DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted) [1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP, SSOP ..... 680 mW
Derates above 75°C ..... 9 mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

THEORY OF OPERATION

Analog to Digital Conversion

The MP8776 uses a two step, sub-ranging architecture to convert analog voltages into 256 digital codes.

A full conversion (sampling V_{IN}, converting MSB & LSB, and performing any error correction) requires 3 1/2 clock cycles to complete (*see Figure 6.*) The pipelined architecture allows the chip to maintain a one conversion per cycle sample rate. Digital logic combines the MSB and LSB data and performs error correction to produce 8-bit output codes.

Internal Reference Bias

The MP8776 includes two on-chip resistors that can be used to bias the reference ladder without external circuitry. These two resistors are designed to track the reference ladder and are used to create a voltage divider between the supplies (AV_{DD} and AGND).

To use this feature, simply connect V_{RT} to V_{RTS} and connect V_{RB} to V_{RBS}. This will nominally generate:

AV_{DD} x (0.3/2.5) at V_{RB}, and

AV_{DD} x (1.3/2.5) at V_{RT}

This will generate 0.6 V at V_{RB} and 2.6 V at V_{RT} (see *Figure 1.*) Bypass capacitors on V_{RT} and V_{RB} are suggested to stabilize the ladder.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

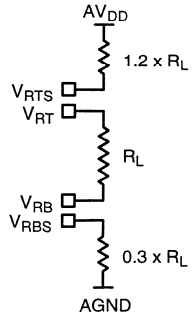


Figure 1. Internal Reference Bias

Transfer Characteristics

The ideal ADC is a linear building block that has infinite bandwidth and no phase distortion. A real ADC, however, exhibits finite bandwidth and non-constant group delay characteristics as well as non-linear behavior due to the non-zero INL characteristic. When modeling the ADC as a linear element and a quantizer, the circuit shown in *Figure 2.* can be used in order to represent the ADC's bandwidth.

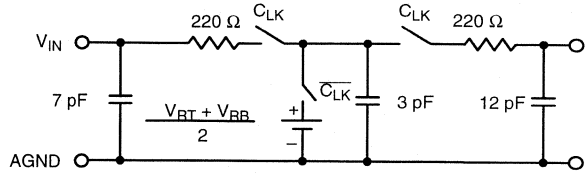


Figure 2. Input Equivalent Circuit

Sample and Hold Timing

The ADC's internal sample and hold tracks the input signal when CLK is high. After a delay of t_{AP} from the falling clock edge, the analog signal is sampled and held for conversion as seen in *Figure 3.*

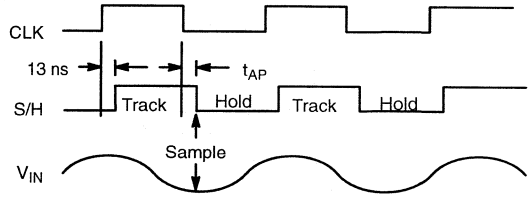


Figure 3. Sample and Hold Timing

Output Enable ($\overline{OE}$)

The $\overline{OE}$ pin controls the state of the digital output drivers. When forced low, the drivers are active. When pulled high the drivers are 3-stated. Please note that the $\overline{OE}$ pin only controls the output drivers; the rest of the chip is still active. Therefore if the clock is running, the internal registers are updated even if the digital outputs are 3-stated (*Figure 4.*).

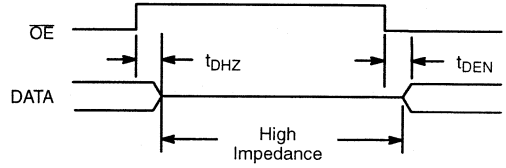


Figure 4. Output Enable/Disable Timing Diagram

Power Down Mode

For systems that are battery powered, the MP8776 has a power down feature to help extend battery life. When the voltage at the V_{RT} pin drops below 0.4 V, the chip goes into power down mode. In this state, conversions are halted, the outputs are 3-stated and I_{DD} drops to less than 100 µA. Then, when the voltage at the V_{RT} pin rises above 0.9 V, the chip will power up. Note that after power up, four clock cycles are required to get valid data at the digital outputs (see *Figure 6.*). One way to achieve power down is to disconnect or disable the buffer/amp driving V_{RT}, and let the internal reference resistance pull V_{RT} down. Remember, any bypass capacitors at V_{RT} will increase the time for V_{RT} to drop below 0.4 V.

APPLICATION NOTES

Power Supplies and Grounding

AV_{DD} and DV_{DD} should be connected to the sample power supply source (*Figure 5.*). The power supply (AV_{DD} and DV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to GND, placed as close to the chip as possible.

AGND and DGND pins are connected internally through the P-substrate. AGND and DGND pins should be connected together as close to the chip as possible.

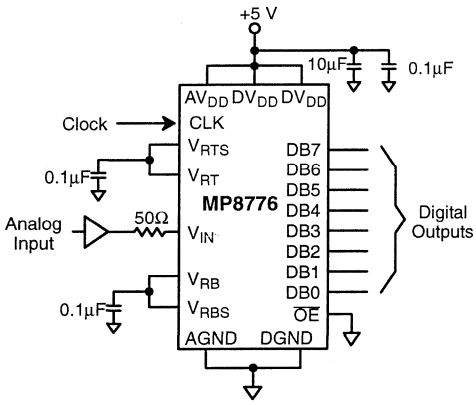


Figure 5. Typical Circuit Connections

The Analog Input

When designing with the MP8776, the following points can help optimize performance.

1. Driving the analog input – The input impedance can be represented as a switched capacitor type input circuit, ie. the input impedance changes with the phase of the input clock. *Figure 2.* shows an equivalent input circuit. In many applications, the input impedance can be treated as capacitive. For fast signals and a high driving impedance, a wide bandwidth op amp is recommended.
2. It is important to note that op amps have inductive output impedances at high frequencies which is a consequence of the emitter impedance of the typical push-pull output stage. The resulting transient ringing should be damped by inserting a resistor in series with the ADC input – typically about 50Ω. See *Figure 5.* The exact value may be obtained from the op amp manufacturer's data sheet.
3. Signals should not exceed V_{DD} +0.5V or go below GND –0.5V. All pins have internal protection diodes that will protect them from short transients (*See Note 2, Absolute Maximum Ratings*) outside the supply range.

Digital Outputs

Refer to *Figure 6.* for details on the data availability timing. The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion. The output enable pin ($\overline{OE}$) should not be left unconnected. If it is not controlled by an active signal, it must be tied to ground.

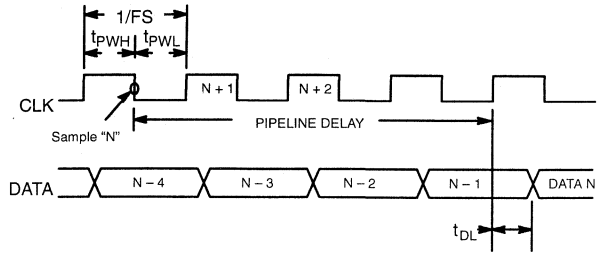


Figure 6. Data Available Timing

Dynamic Reference Control

The MP8776 allows for dynamically adjusted V_{RT} and V_{RB}. When this is done, V_{RT} and V_{RB} have to be kept static during a certain period.

The A/D conversion is done in a two-step method. During the first clock period, the MSB comparator bank compares the V_{IN} with the reference voltage string in order to determine in which subrange the exact V_{IN} lies. During the subsequent clock period, an LSB comparator bank compares a subrange of the V_{REF} to the V_{IN}. Thus, the reference inputs have to be stable during two compare cycles. This implies that while the ADC is clocked with FS, the conversion only occurs at a rate of FS/2. Every second sample and resulting data must be discarded because the reference changes during its conversion.

The reference inputs V_{RT} and V_{RB} have to have settled to within 1 LSB, at least 50 ns before the rising edge which occurs after the sampling instant. The reference has to be kept constant until (t_{AP} + 10 ns) after the second rising edge. See *Figure 7.* for timing details. The digital data of the N + 1, N +3, N + 5 etc. samples are invalid if the reference is changed every second clock cycle. The data for the N, N + 2, N + 4 etc. samples are valid.

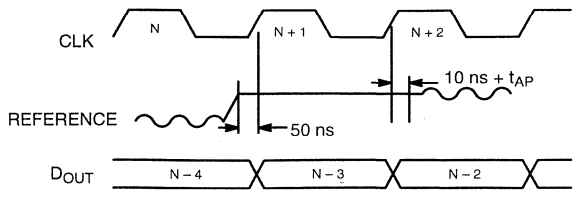


Figure 7. Dynamic Reference Control

LINEARITY DEFINITION

The Ideal ADC

The transfer function for an ideal A/D converter is shown in *Figure 8.*

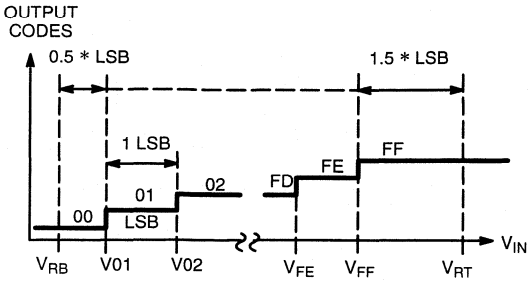


Figure 8. Ideal A/D Transfer Function

The first transition for the data bits takes place when:

$V_{IN} = V01 = V_{RB} + 0.5 * LSB$

The last transition of the data bits takes place when:

$V_{IN} = V_{FF} = V_{RT} - 1.5 * LSB$

where: $LSB = V_{REF} / 256$
$= (V_{FF} - V01) / 254$

and $V_{REF} = (V_{RT} - V_{RB})$

The Real ADC

In a "real" converter, the code-to-code transitions do not fall exactly every $V_{REF}/256$ volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A specification of Max DNL = ± 0.5 LSB means that all codes are within 0.5 LSB and 1.5 LSB. For example, if V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is between 8 and 24 mV.

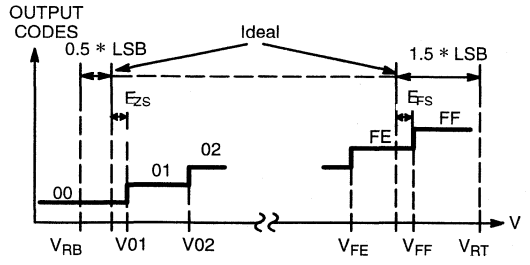


Figure 9. Real A/D Transfer Curve

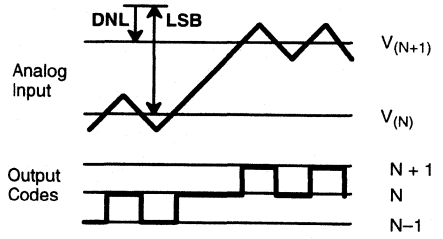


Figure 10. DNL Measurement

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) are:

DNL (01) = V02 – V01 – LSB
: : :
DNL (FE) = $V_{FF} - V_{FE}$ – LSB
Thus $DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$
Code Width (N) = $V_{(N+1)} - V_{(N)}$

Similarly, the zero scale and full scale errors are defined as:

EFS (full scale error) = $V_{FF} - (V_{RT} - 1.5 * LSB)$
EZS (zero scale error) = V01 – (V_{RB} + 0.5 * LSB)
where: LSB = [$V_{RT} - V_{RB}$] / 256

Figure 9. shows the zero scale and full scale error terms while *Figure 10.* shows the definition of DNL.

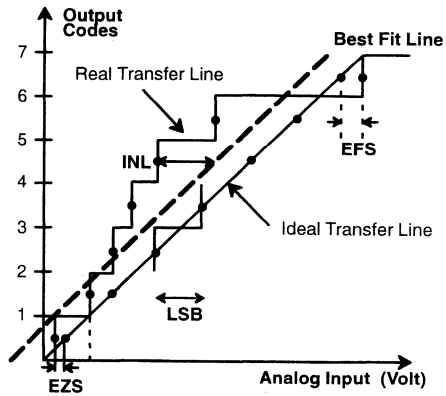


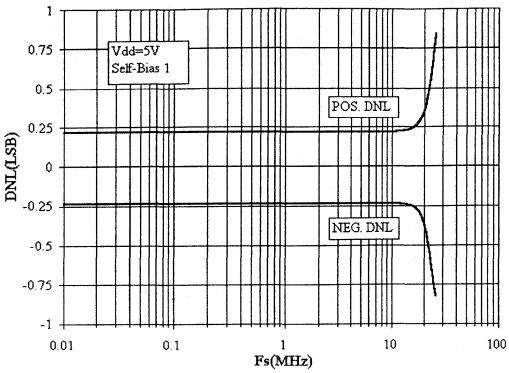
Figure 11. INL Error Calculation (3-Bit)

Figure 11. gives a visual definition of the INL error. The graph shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

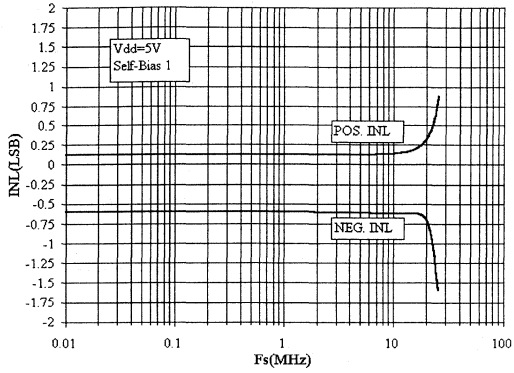
After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition, the best fit line makes equal the positive and the negative INL errors. This may change an INL of –1 to +2 LSBs relative to the ideal line into a ±1.5 relative to the best fit line.

3

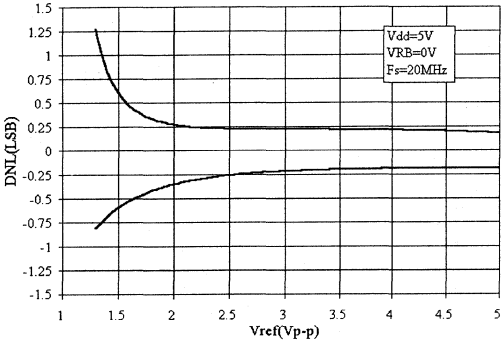
PERFORMANCE CHARACTERISTICS



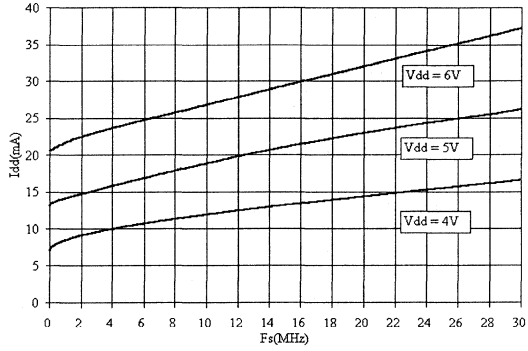
Graph 1. DNL vs. Sampling Frequency



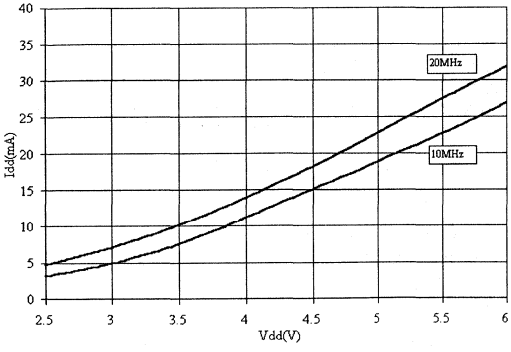
Graph 2. INL vs. Sampling Frequency



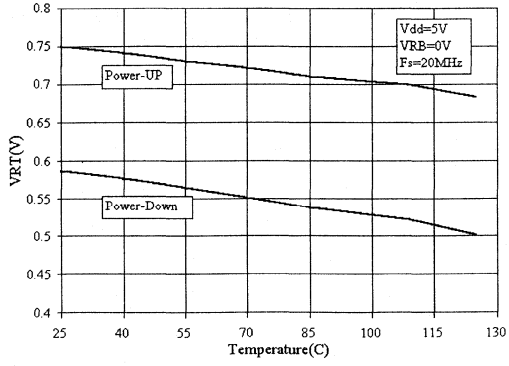
Graph 3. DNL vs. Reference Voltage



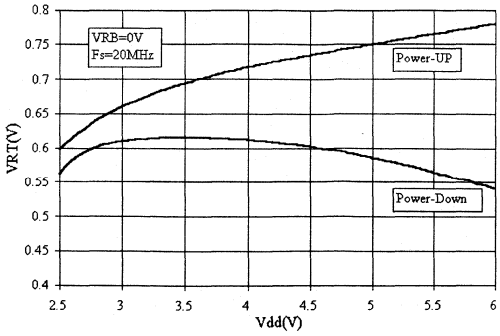
Graph 4. Supply Current vs. Sampling Frequency



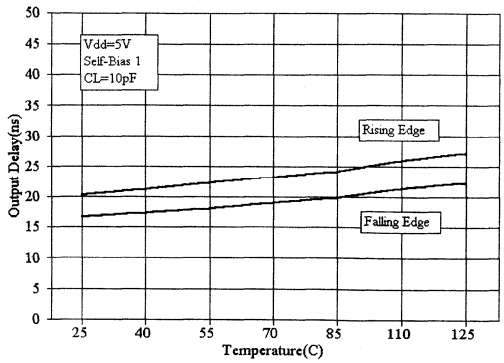
Graph 5. Supply Current vs. Supply Voltage



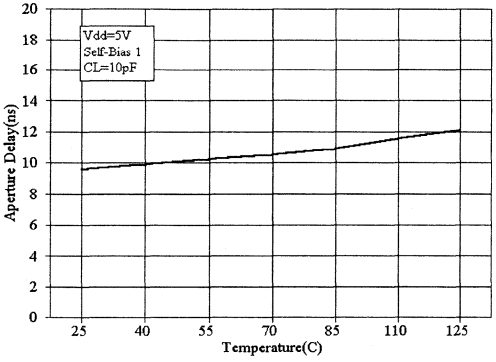
Graph 6. Power Up/Down Voltage vs. Temperature



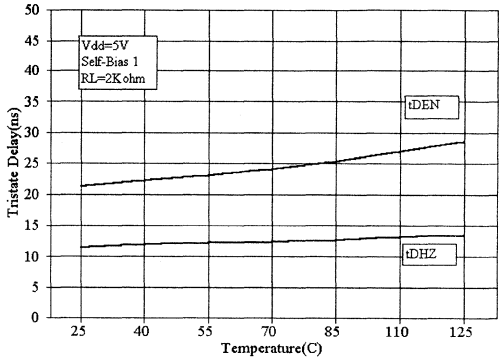
Graph 7. Power Up/Down Voltage vs. Supply Voltage



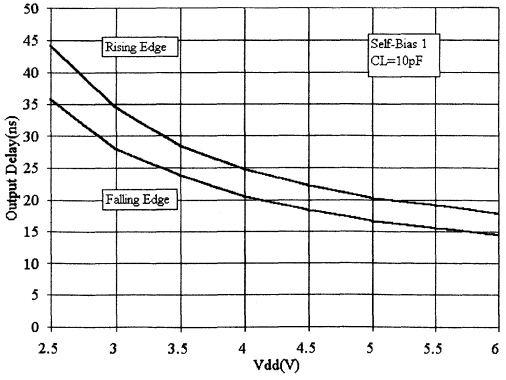
Graph 8. Output Delay (t_{DL}) vs. Temperature



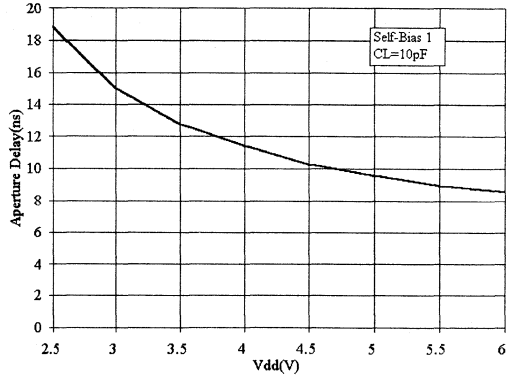
Graph 9. Aperture Delay (t_{AP}) vs. Temperature



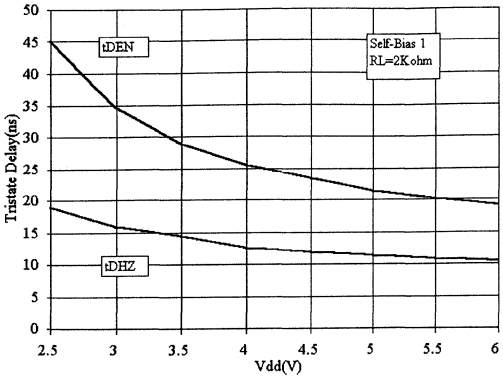
Graph 10. 3-state/Enable Delay vs. Temperature



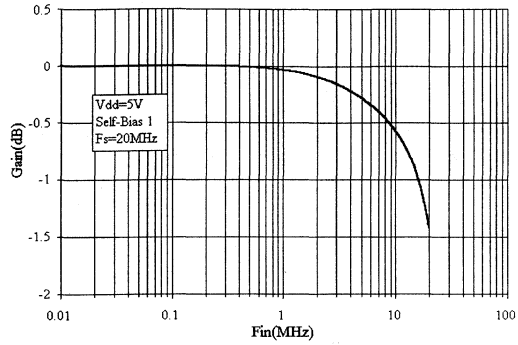
Graph 11. Output Delay vs. Supply Voltage



Graph 12. Aperture Delay (t_{DL}) vs. Supply Voltage



Graph 13. 3-state/Enable Delay vs. Supply Voltage



Graph 14. Gain vs. Input Frequency

MP8780

CMOS
8-Bit Video
Analog-to-Digital Converter

FEATURES

- **10 MHz Input Bandwidth (–0.3 dB)**
- **SNR > 44 dB @ Fin 2.4 MHz**
- **1.2 to 5.0 Volts (Peak to Peak) Input Range**
- **1/2 LSB Dynamic DNL at 14.4 MHz**
- **3/4 LSB Dynamic DNL at 17.7 MHz**
- **Monotonic. No Missing Codes**
- **Latch Up Free CMOS Technology**
- **High ESD Protection - 4000 Volts Minimum**

BENEFITS

- **Optimized Combination of Performance, Power, Packaging and Cost for Video Digitizing Applications**
- **Excellent Video Digitizing Performance**
- **Smaller Board Space**
- **Lower System Power**

3

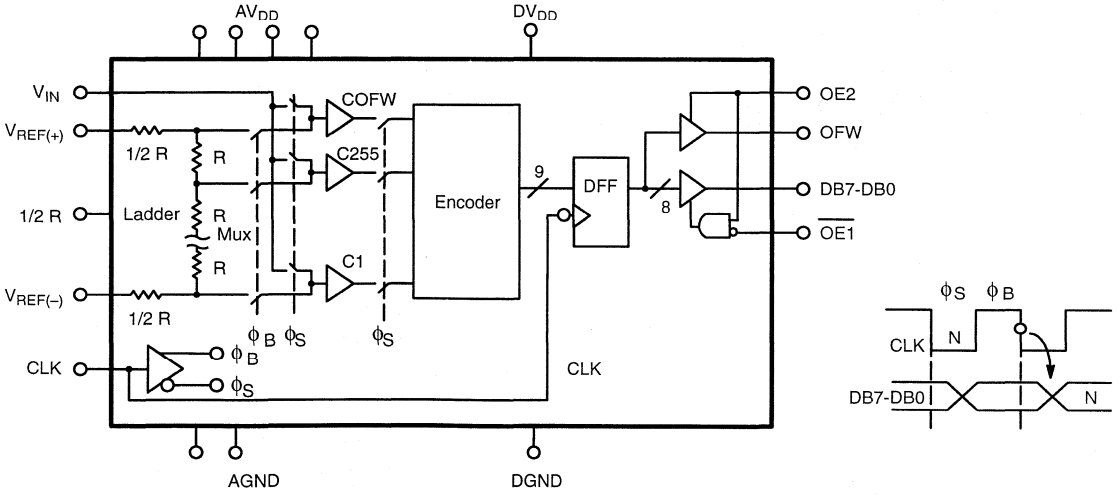
GENERAL DESCRIPTION

The MP8780 is a CMOS 8-bit high speed Analog-to-Digital Converter designed and specified for applications in imaging and video digitizing. With Signal to Noise Ratio greater than 44 dB in the Video Input Bandwidth and encode rates up to 20 MHz, the MP8780 easily meets the requirements needed to digitize standard American and European video signals.

A fast digital interface simplifies connection to most modern DSP and CPU chips.

Careful design and layout have reduced static sensitivity, while our proprietary latch-up free process virtually eliminates the need for many of the diode protection schemes used in the past.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

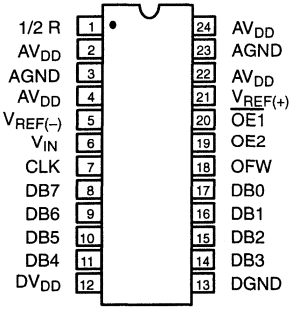


ORDERING INFORMATION

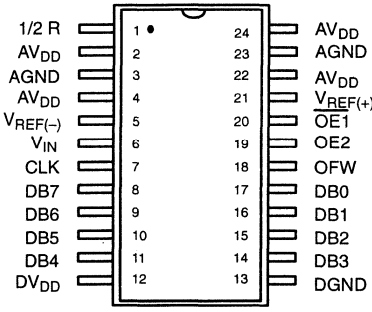
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP8780JN	±1	1 1/2
SOIC	–40 to +85°C	MP8780JS	±1	1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	50% Point of Reference on Resistance Ladder
2	AV_{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground
4	AV_{DD}	Analog Power Supply Voltage
5	$V_{REF(-)}$	Lower Reference Voltage Input
6	V_{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Output Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV_{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow flag
19	OE2	Output Enable Control Pin
20	$\overline{OE1}$	Output Enable Control Pin
21	$V_{REF(+)}$	Upper Reference Voltage Input
22	AV_{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground
24	AV_{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 15 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance)
$V_{REF(+)}$ = 2.5 V, $V_{REF(-)}$ = GND, Temp = 25°C

Parameter	Symbol	MP8780J Min	MP8780J Typ	MP8780J Max	Units	Conditions
RESOLUTION		8			Bits	
ACCURACY[1]						
Differential Non-Linearity	DNL		1/2	1	LSB	
Integral Non-Linearity	INL		1	1 1/2	LSB	
Zero Scale Error	EZS		–27		mV	
Full Scale Error	EFS		12		mV	
DNL[6]	DNL		1/4		LSB	F_S = 10MHz
INL[6]	INL		3/4		LSB	F_S = 10MHz
DYNAMIC ACCURACY[6]						
(Histogram Test)						F_S (MHz) / F_{IN} (MHz) / V_{REF} (V)
Differential Non-Linearity			1/2		LSB	14.4 / 2.0 / 4
Differential Non-Linearity			1/2		LSB	14.4 / 2.0 / 2.5
Differential Non-Linearity			3/4		LSB	17.7 / 2.0 / 4
Differential Non-Linearity			3/4		LSB	17.7 / 2.0 / 2.5
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			V	
Differential Ref. Voltage	V_{REF}	1.2		V_{DD}–GND	V	
Ladder Resistance	R_L	180	225	285	Ω	
Ladder Temp. Coefficient[6]	R_{TCO}			2000	ppm/°C	
ANALOG INPUT[2, 6]						
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Impedance (*See Figure 3.*)	C_{INA}		50		pF	
Aperture						
Aperture Delay	t_{AP}		15		ns	
Aperture Uncertainty	t_{AJ}		45		ps	
Clock Kickback Pulse			10		pA•s	V_{REF}=2.5 V
			20		pA•s	V_{REF}=4.0 V
Input Bandwidth (–0.3 dB)	BW		10		MHz	
DIGITAL INPUTS[3] (Tmin to Tmax)						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Current (CLK)		–100		100	µA	V_{IN}=0 to V_{DD}
Current ($\overline{0E1}$: Res to GND)		–5		50	µA	V_{IN}=0 to V_{DD}
Current (0E2: Res to V_{DD})		–50		5	µA	V_{IN}=0 to V_{DD}
Input Capacitance[6]	C_{IND}		5		pF	
Clock Timing (*See Figure 1.*)[6]						
Rise & Fall Time[4]	t_R, t_F			8	ns	
"High" Time (Autozero/Autobalance)	t_B	20			ns	
"Low" Time (Sampling)	t_S	20			ns	

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ELECTRICAL CHARACTERISTICS TABLE CONT'D

Description	Symbol	MP8780J Min	Typ	Max	Units	Conditions
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	V_{DD}–0.5			V	
Logical "1" Source Current	I_{OH}	4			mA	
Logical "0" Voltage	V_{OL}			0.4	V	
Logical "0" Sink Current	I_{OL}	4			mA	
3-state Leakage	I_{OZ}	–10		10	uA	V_{OUT}=0 to V_{DD}
Min Data Hold Time (*See Figure 1.*)[6]	t_{HLD}	12	15		ns	
Max Data Valid Delay[6]	t_{DL}		30	33	ns	
Data Enable Delay (*See Figure 2.*)[6]	t_{DEN}			20	ns	
Data Tristate Delay[6]	t_{DHZ}			20	ns	
POWER SUPPLIES[7]						
Operating Voltage[5]	V_{DD}	4		6	V	
I_{DD}	I_{DD}		50	85	mA	
AC PARAMETERS[6]						
Differential Gain Error			2		%	F_S = 3 x NTSC
Differential Phase Error			1		Degree	
Signal Noise Ratio (RMS/RMS)	SNR					F_S (MHz) / F_{IN} (MHz)
			46		dB	14.4 / 2.4
			44		dB	17.7 / 2.4

NOTES:
1. Linearity (DNL, INL) is a function of clock frequency. INL is specified as the best straight line fit. See characterization chart.
2. See V_{IN} Input Equivalent Circuit (*Figure 3.*). Switched capacitor analog input requires input buffer with lowest output resistance possible.
3. All inputs have current leakage to V_{DD} and GND. OE2 has pull-up transistor. $\overline{OE1}$ has pull-down transistors. These DC currents will not exceed the specified values for any input voltage between 0 and V_{DD}.
4. CLK Input spec to meet MP8780 aperture specifications. Actual rise/fall timing can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. Guaranteed. Not production tested.
7. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 13mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

TIMING DIAGRAMS

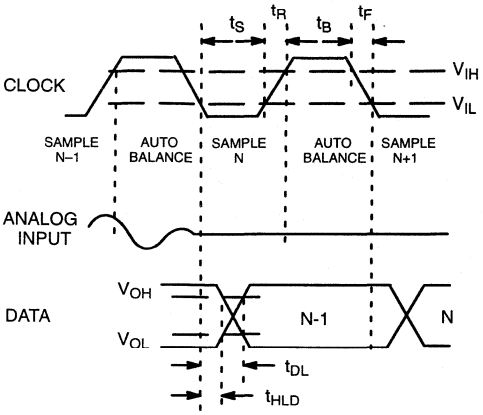


Figure 1. MP8780 Timing Diagram

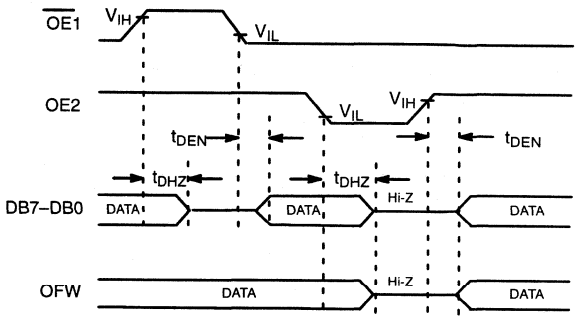


Figure 2. Output Enable/Disable Timing Diagram

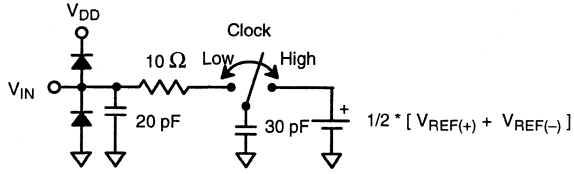


Figure 3. Analog Input Equivalent Circuit

THEORY OF OPERATION

The MP8780 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the sample clock. A complete conversion cycle is accomplished in 1.5 cycles. Data is transferred from the comparator latches to the output register each cycle at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). Phase B connects the comparators to the reference tap points. Phase S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

The ideal transfer function for MP8780 is shown in *Figure 4.*

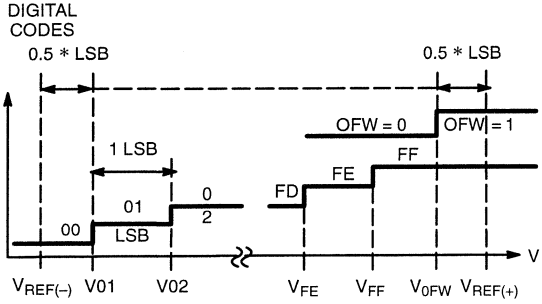


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{0FW}) takes place at:

$V_{IN} = V_{0FW} = V_{REF(-)} = 0.5\ LSB$

Thus the first and the last transitions for the data bits take place at:

$V_{IN} = V01 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF}/256 = (V_{FF} - V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

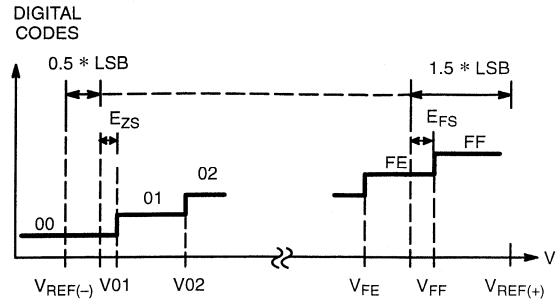


Figure 5. Real A/D Transfer Curve

The formulas define the various error relationships for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}).

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

E_{FS} (full scale error) = $V_{FF} - [\ V_{REF(+)} - 1.5 * LSB\ ]$

E_{ZS} (zero scale error) = $V_{01} - [\ V_{REF(-)} + 0.5 * LSB\ ]$

INL (i) = Σ DNL (i)

Figure 5. shows the effect of the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages only increase the DNL accuracy at the two extreme points. In the MP8780, such adjustments have little impact at frequencies lower than 10 MHz. Refer to the characterization data for frequency dependence.

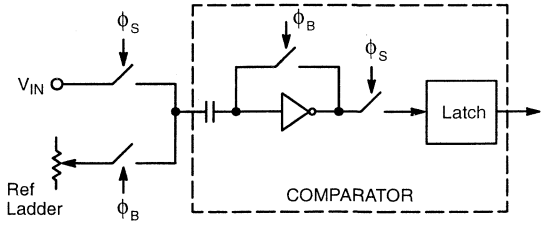


Figure 6. MP8780 Comparator

$\overline{OE1}$	OE2	OFW	DB0-DB7
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

The MP8780 uses the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S), one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if $(dv/dt) * t_{AJ} \approx V_{REF}/256$, an internal 1 LSB of error results.

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

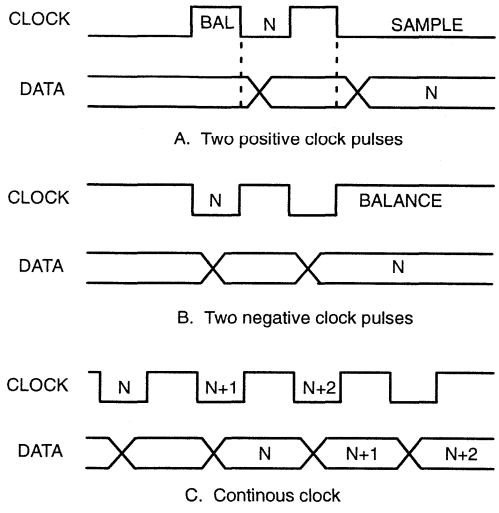


Figure 7. Relationship of Data to Clock

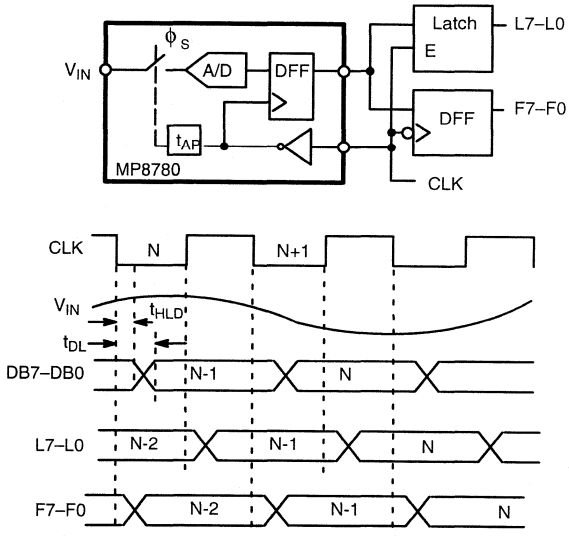


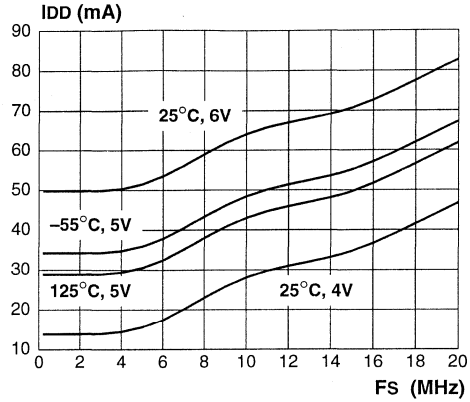
Figure 8. MP8780 Functional Equivalent Circuit and Interface Timing

A system can clock the MP8780 continuously or it may choose to give clock pulses intermittently when a conversion is desired. The timing of *Figure 7B.* keeps the MP8780 comparators in balance and ready to sample the analog input. This mode draws the most current from AV_{DD}. The timing of *Figure 7A* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

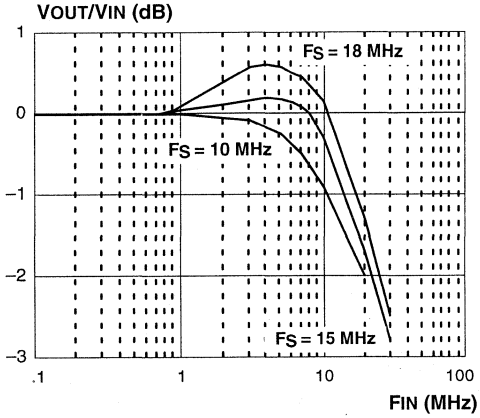
If another DFF is to follow the ADC, we recommend that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge, then care must be taken to avoid the overlay of the clock edge with the changing outputs. If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

CHARACTERIZATION CHARTS

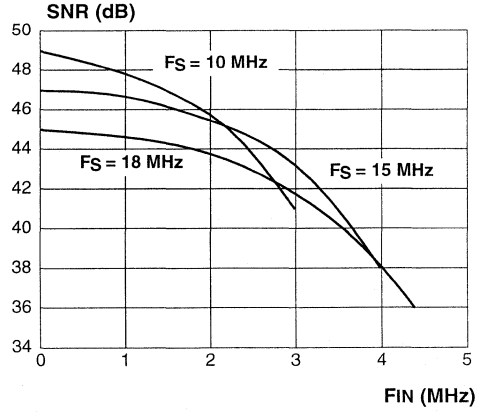
Unless Otherwise Specified: V_{DD} = 5 V, F_S = 15 MHz (50% Duty Cycle)
$V_{REF(+)}$ = 2.5 V, $V_{REF(-)}$ = GND, Temp = 25°C



Supply Current (IDD)
vs. Sampling Rate (FS)
vs. Temperature (T = –55, 25, 125°C)
vs. Supply Voltage (VDD = 4, 5, 6V)



Input Sinewave Signal Attenuation
vs. Input Bandwidth (FIN)
vs. Sampling Rate (FS = 10, 15, 18 MHz)



Signal-to-Noise Ratio (SNR)
vs. Input Bandwidth (FIN)
vs. Sampling Rate (FS = 10, 15, 18 MHz)

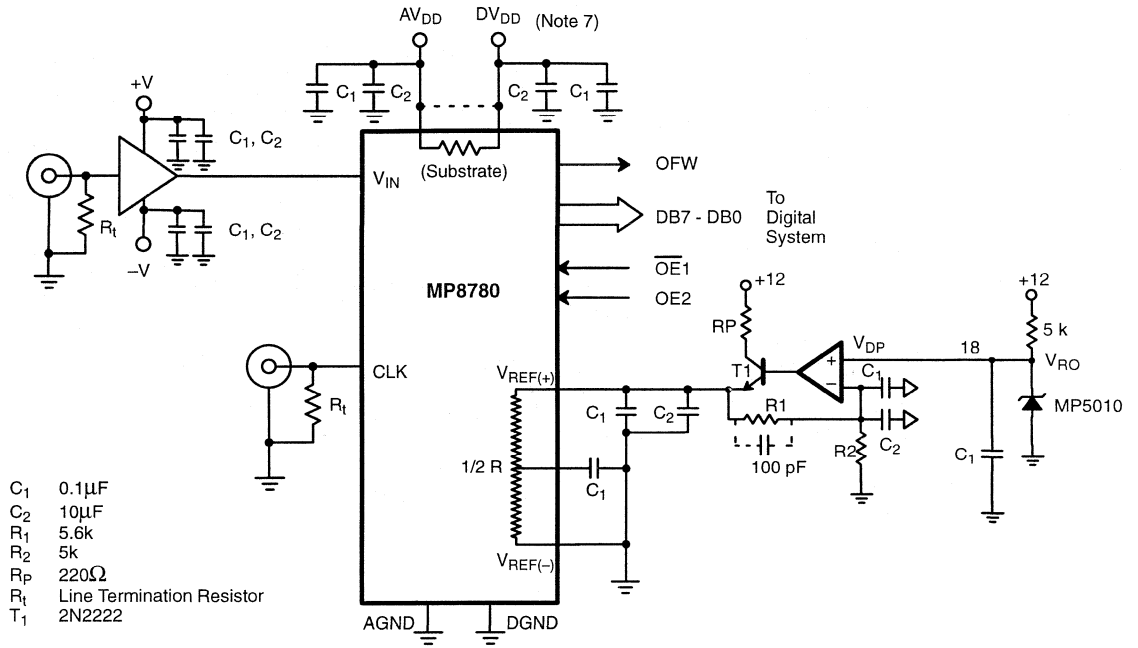


Figure 9. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP8780.

1. No signals should exceed V_{DD} +0.5 V or GND –0.5 V.
2. Any input pin which can see a signal below GND or above V_{DD} should be protected by diode clamps (1N4148 or HP5082-2835) from input pin to the supplies. All MP8780 inputs have input protection diodes which will protect the device from short transients outside the supply range.
3. The design of a PC board will affect the accuracy of MP8780. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. Separate low impedance ground paths will reduce noise levels.
7. DV_{DD} should not be shared with other digital circuitry to avoid conversion errors caused by digital supply transients. In case a separate DV_{DD} for the MP8780 cannot be provided, then DV_{DD} should be connected to AV_{DD} next to the MP8780.
8. DV_{DD} and AV_{DD} are connected inside the MP8780 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not be driving long wires as the capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

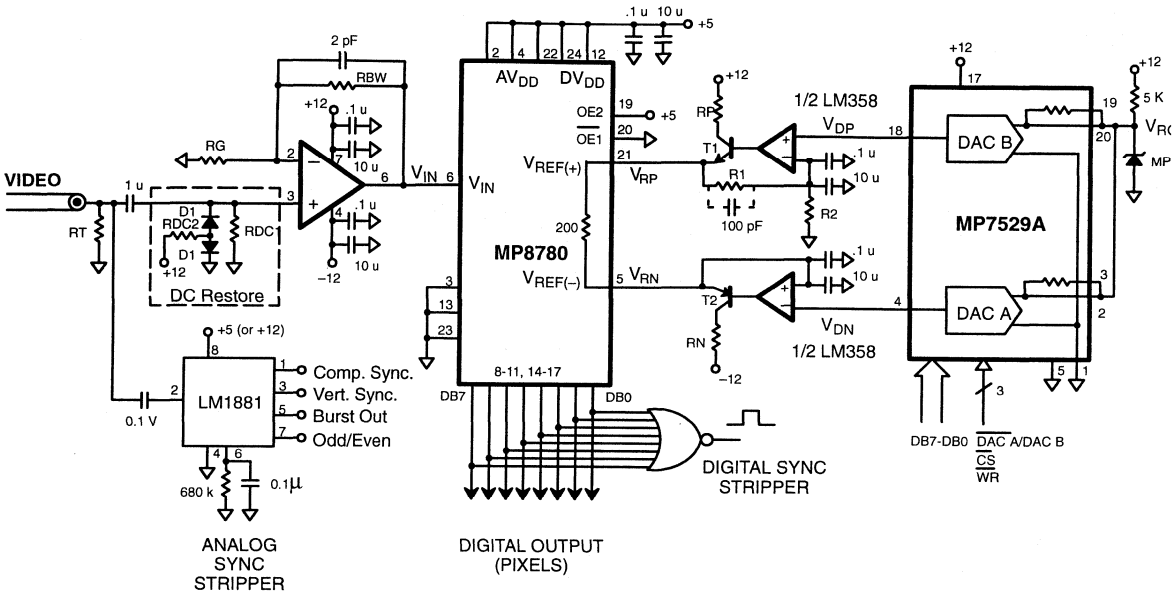


Figure 10. Video Digitizer

D_1	1N4148 (any diode would do)
T_1	2N3903, 2N3904
T_2	2N3905, 2N3906
U_1	EL2030 (others under test)
R_T	75Ω
R_{BW}	750Ω
R_G	750Ω
R_{DC1}	100kΩ
R_{DC2}	100kΩ
R_1	5.6k
R_2	5k
R_P	220Ω
R_N	390Ω

MP8782

CMOS
5 MSPS, 10-Bit High Speed
Analog-to-Digital Converter

FEATURES

- 10-Bit Resolution
- 5 MHz Sampling Rate
- DNL = ±1 LSB, INL = ±2 LSB
- Internal S/H Function
- Single 5 V Power Supply
- V_{IN} DC Range: 0 V to V_{DD}
- V_{REF} DC Range: 1 V to V_{DD}
- Low Power: 175 mW
- Bipolar Range using RTS & RBS; +1.4 V to –1.4 V
- R1 - R7 Reference Ladder Taps (1/8th – 7/8th points)
- Aperture Delay Sync Signal
- MINV & LINV Digital Output Format Controls
- PHASE Control
- Overflow and Underflow bits
- Dual 3-State Controls ($\overline{OE1}$ & OE2)
- Three-State Digital Outputs
- Latch-Up Free
- 3 V Version: MP87L82

APPLICATIONS

- Digital Color Copiers
- Digital Cellular Telephones
- Precision CCDs and Scanners
- Medical Scanners
- Ultrasonics
- Digital Radio

BENEFITS

- Simplified Analog Design
- Rugged
- Few External Components, no S/H Needed
- Reduced Board Space

3

GENERAL DESCRIPTION

The MP8782 is a full featured 10-bit, 5 MSPS, Analog-to-Digital Converter for applications that require high speed and high accuracy. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The MP8782 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the MP8782 includes a S/H function and internal resistors that allows this part to digitize analog input signals between – V_{RT} to V_{DD} using a single supply.
(Unipolar and Bipolar Conversion capability)

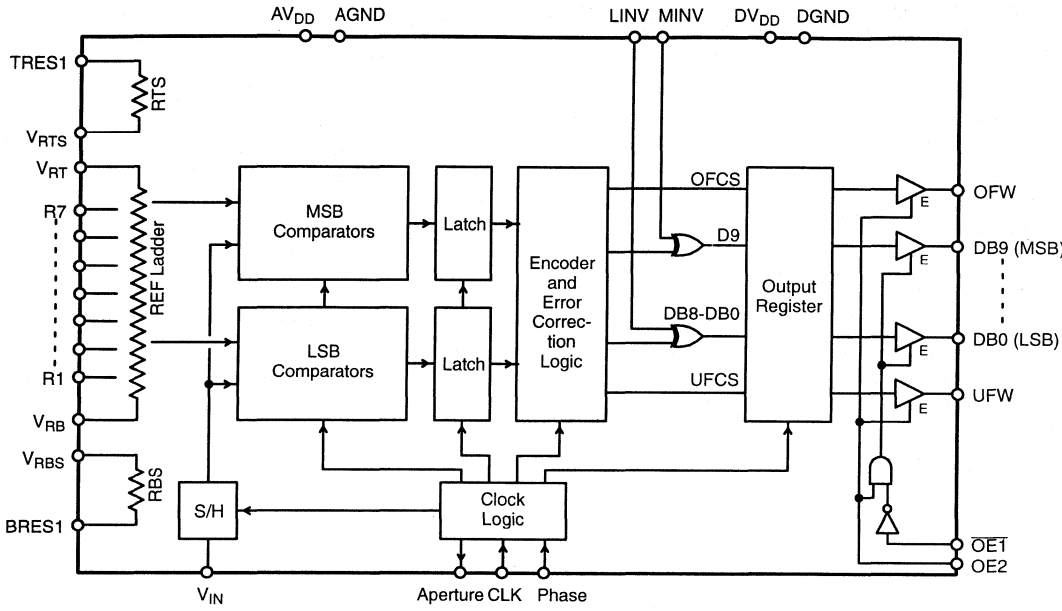
The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 1.0 V at V_{RB} and 4.0 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R7) can be used to externally trim any INL errors, or to shape the A/D converter transfer function.

This device operates from a single 5 V supply. Power consumption from a 5 V supply is typically 175 mW at F_S=5MHz, and only 150 mW at F_S=1MHz.

ORDERING INFORMATION

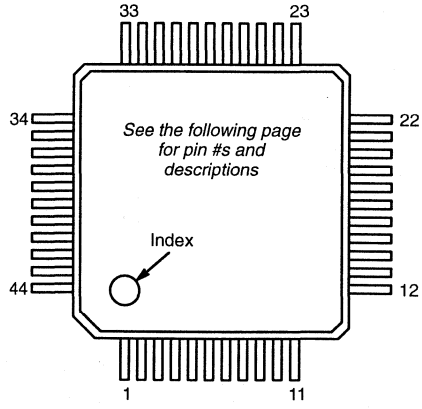
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP8782AE	±1	±2

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



44 Pin PQFP
Q44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{RT}	Top of Ladder
2	R7	Reference Ladder Tap @ 7/8
3	R6	Reference Ladder Tap @ 3/4
4	R5	Reference Ladder Tap @ 5/8
5	R4	Reference Ladder Tap @ 1/2
6	AV_{DD}	Analog Power Supply
7	A_{IN}	Analog Input
8	AGND	Analog Ground
9	R3	Reference Ladder Tap @ 3/8
10	R2	Reference Ladder Tap @ 1/4
11	R1	Reference Ladder Tap @ 1/8
12	V_{RBS}	Bottom Bias Resistor Terminal 2
13	N/C	No Connection
14	V_{RB}	Bottom of Ladder
15	Bres1	Bottom Bias Resistor Terminal 1
16	DGND	Digital Ground
17	OE2	Output Enable 2 (Input, Active High)
18	$\overline{OE1}$	Output Enable 1 (Input, Active Low)
19	UFW	Underflow (Output)
20	DB0	Data Output Bit 0 (LSB)
21	DB1	Data Output Bit 1
22	N/C	No Connection
23	DB2	Data Output Bit 2
24	DB3	Data Output Bit 3
25	DB4	Data Output Bit 4
26	N/C	No Connection
27	PHASE	Clock Polarity Control (Input)
28	LINV	Non MSB Digital Output Format (Input)
29	MINV	MSB Digital Output Format (Input)
30	N/C	No Connection
31	DB5	Data Output Bit 5
32	DB6	Data Output Bit 6
33	DB7	Data Output Bit 7
34	N/C	No Connection
35	N/C	No Connection
36	DB8	Data Output Bit 8
37	DB9	Data Output Bit 9 (MSB)
38	OFW	Overflow (Output)
39	CLK	Clock Input
40	Aperture	Aperture Delay Sync (Output)
41	DV_{DD}	Digital Power Supply
42	Tres1	Top Bias Resistor Terminal 1
43	V_{RTS}	Top Bias Resistor Terminal 2
44	N/C	No Connection

The MP8782 is the full featured version of Exar's 5 MSPS 10-bit A/D Converter. The MP8784 is one alternate pinout with reduced pin count and reduced features.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, FS = 5 MHz (50% Duty Cycle), $V_{RT} = 4.0$, $V_{RB} = 1.0$, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution			10		Bits	
Sampling Rate	FS			5	MHz	
ACCURACY (A, S Grades)[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		10		LSB	
Full Scale Error	EFS		6		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}			AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L		375		Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Top Internal Reference	V_{RTS}		4		V	V_{RT} connected to V_{RTS} &
Bottom Internal Reference	V_{RBS}		1		V	V_{RB} connected to V_{RBS}
ANALOG INPUT[2]						
Input Bandwidth (–1 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance Sample[5]	C_{IN}		25		pF	
Input Capacitance Convert[5]			5		pF	
Aperture Delay	t_{AP}		25		ns	
Aperture Delay from Aperture Out			0		ns	5pF Load
Aperture Uncertainty (Jitter)	t_{AJ}		50		ps	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	4			V	
Logical "0" Voltage	V_{IL}			1	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE1}$, MINV, LINV (Internal Res to DGND)[7]			15		µA	
$\overline{OE2}$, Phase (Internal Res to DV_{DD})[7]			15		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1*)						
Clock Period	1/FS		200		ns	
Rise & Fall Time[8]	t_R, t_F		5		ns	
"High" Pulse Width	t_{PWH}		100		ns	
"Low" Pulse Width	t_{PWL}		100		ns	
Duty Cycle			50		%	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		40		ns	
Data Enable Delay	t_{DEN}		25		ns	
Data Tristate Delay	t_{DHZ}		25		ns	
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9, 10]	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		35	45	mA	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} equivalent circuit (*Figure 8.*). Switched capacitor analog input requires driver with low output resistance.

6. All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE}$ has internal pull down. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Internal resistor to DGND biases unconnected input to active low logical level.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 The AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

10 The AV_{DD} & DV_{DD} pins should go to the same voltage and separately decoupled.

Specifications are subject to change without notice

3

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V
RTS & RBS terminals ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
PQFP Package Dissipation @ 75°C ..... 800 mW
Derates above 75°C ..... 11mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

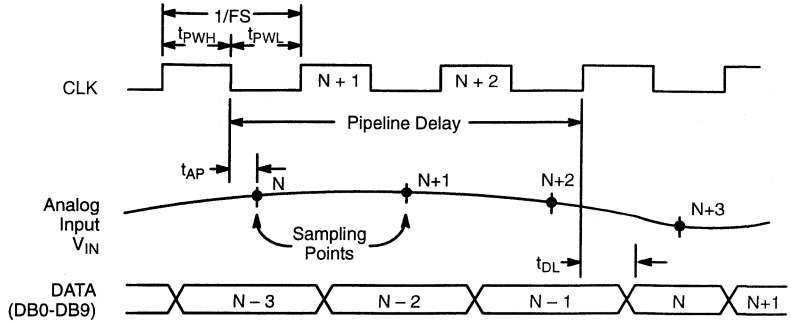


Figure 1. MP8782 Timing Diagram

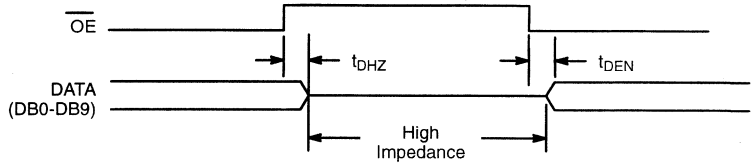
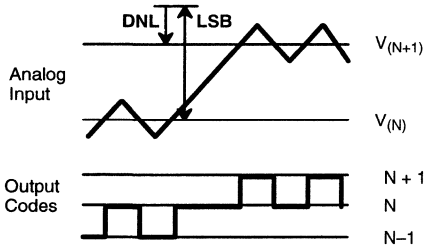


Figure 2. 3-State Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 1024

$\mathbf{DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB}$

Figure 3. DNL Measurement

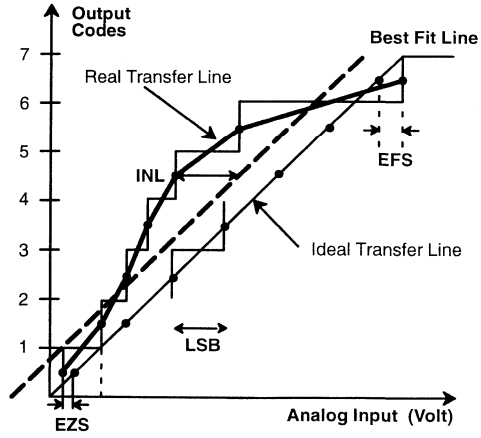


Figure 4. INL Error Calculation

APPLICATION NOTES

V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

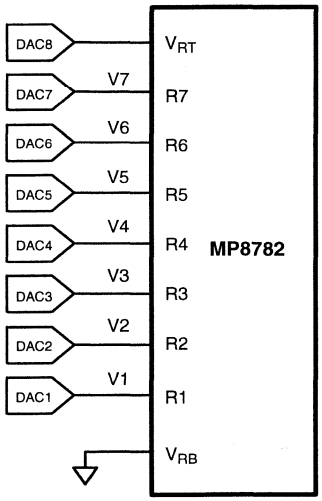
The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

The application resistors, RTS and RBS allow for applied voltages in the range of AV_{DD} + 5 V to AGND – 5V. If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

The reference tap pins (R1-R7) should be decoupled with 0.1µF to 1µF capacitors. This will help stabilize the internal reference voltages thus reducing any INL errors.

The reference tap pins (R1-R7) can be used to create piecewise-linear transfer functions. By forcing custom voltages on these pins, an eight segment transfer function can be made. See *Figure 5. and Figure 6.*



DAC MP7228

Only the Ladder detail shown.

Figure 5. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

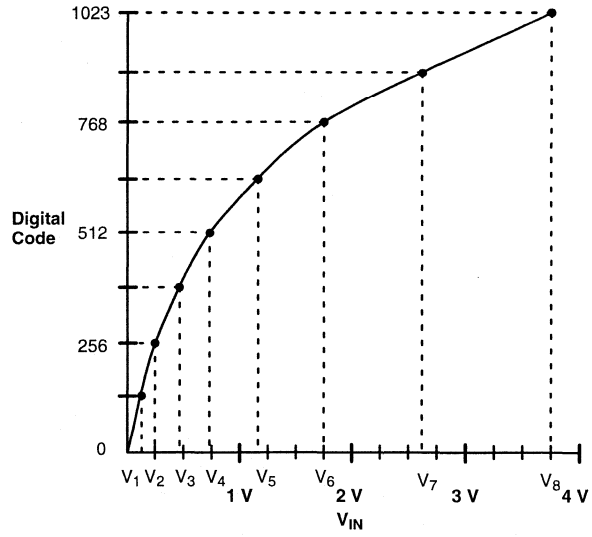


Figure 6. A Piecewise Linear, Logarithmic Transfer Function

OPTIONS on the 8782 DIE & OPERATION NOTES:

OFW & UFW Overflow & Underflow (outputs)

These signals indicate when the Analog Input (V_{IN}) goes outside the V_{RB} to V_{RT} range. Both pins are normally at low logic levels. When $V_{IN} > V_{RT}$, OFW will go high and the data bits (DB0 – DB9) will show full scale (i.e. all 1s if MINV & LINV are low). When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0s if MINV & LINV are low).

$\overline{OE1}$ & OE2 Output Enable (inputs)

These signals control the 3-state drivers on the digital outputs DB0 – DB9, OFW and UFW. During normal operation $\overline{OE1}$ should be held low and OE2 should be held high so that all outputs are enabled (NOTE: internal resistors will pull $\overline{OE1}$ and OE2 to these levels if they are not connected). When $\overline{OE1}$ is driven high DB0 – DB9 go into high impedance mode. When OE2 is driven low DB0 – DB9, OFW and UFW all go into high impedance mode (please refer to the truth table below). These controls operate asynchronous to the clock and they only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode.

$\overline{OE1}$	OE2	DBO-DB9	OFW & UFW
0	1	enabled	enabled
1	1	3-state	enabled
X	0	3-state	3-state

PHASE Clock Polarity Control (input)

This signal controls the phase relationship between the signal applied at the CLK pin and the internal clock signals. When PHASE is high, V_{IN} is sampled at the high to low CLK transition and the digital data changes after a low to high CLK transition. When PHASE is low, V_{IN} is sampled at the low to high CLK transition and the digital data changes after a high to low CLK transition. See timing diagram *Figure 7.* PHASE has an internal pull up device.

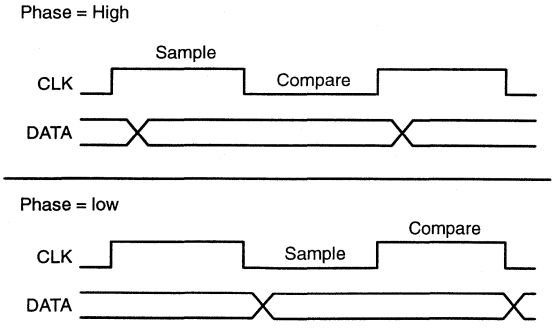


Figure 7. Clock Phase Relationship

APERTURE Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event.

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition and the digital data changes at the low to high clock transition. The diagram *Figure 8.* shows an equivalent input circuit.

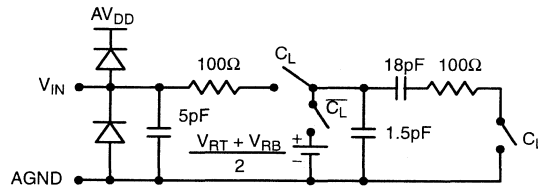


Figure 8. Equivalent Input Circuit

MINV & LINV Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB9 (*see Table 1.)* Normally both pins are held low so the data is in straight binary format (all 0s when $V_{IN}=V_{RB}$; all 1s when $V_{IN}=V_{RT}$). If MINV is pulled high, then the MSB (DB9) will be inverted. If LINV is pulled high, then the LSB's (DB0 – DB8) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV LINV	0 0	0 1	1 0	1 1
V_{IN} V_{RT}	111 . . . 11 111 . . . 10	100 . . . 00 100 . . . 01	011 . . . 11 011 . . . 10	000 . . . 00 000 . . . 01
mid scale	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11
	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
V_{RB}	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

3

MINV & LINV are meant to be static digital signals. If they are to change during operation, they should only change when the CLK is low (assuming PHASE is high, if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. See the simplified logic circuit *Figure 9.* MINV and LINV have internal pull down devices.

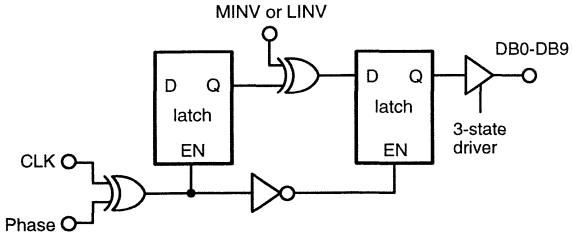


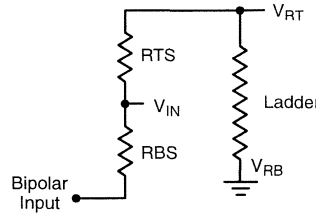
Figure 9. MINV, LINV Simplified Logic Circuit

RTS & RBS Internal Bias Resistors

Two matched resistors are provided on the chip. These resistors can be used to generate on chip reference voltages, or to extend the analog input range. Each resistor has a value equal to 1/3 of the reference ladder resistor.

By connecting RTS between AV_{DD} (5 volts) and V_{RT}, and connecting RBS between AGND and V_{RB}, the reference ladder will be biased to 1 volt at V_{RB} and 4 volts at V_{RT}.

A bipolar input range ($+V_{RT}$ to $-V_{RT}$) can be achieved by connecting RTS and RBS as shown in *Figure 10. (a) and (b),* and fixing V_{RT} with a positive reference voltage. Due to current density limitations for RTS and RBS, V_{RT} should be limited to +1.4 volts in this configuration. The protection pads used for the resistor terminals are designed to allow voltages that go beyond the supply rails.



(a) Bipolar Input Configuration

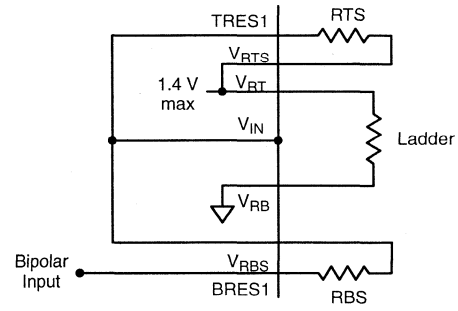
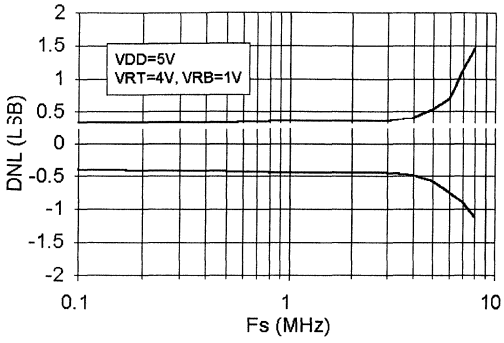


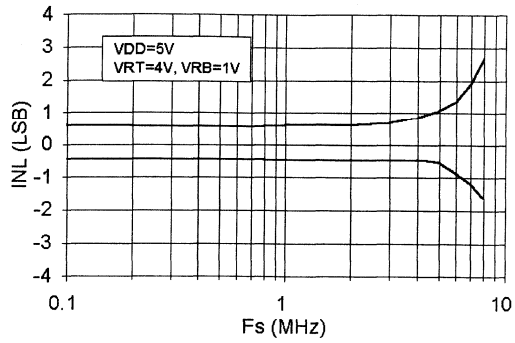
Figure 10. (b) Bipolar Input Connections

R1 thru R7 Reference Ladder Taps. These taps connect to every eighth point along the reference ladder; R1 is 1/8th up from V_{RB}, R7 is 7/8ths up from V_{RB} (or 1/8th down from V_{RT}). Normally these pins should have 0.1 µF capacitors to AGND, this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. An eight segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

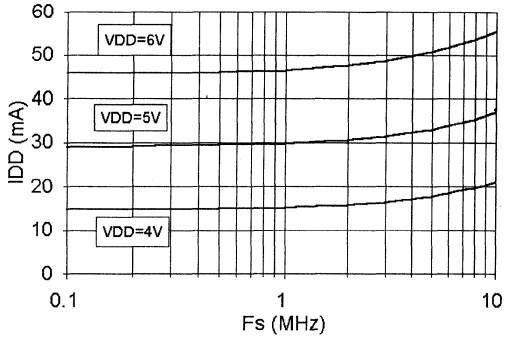
PERFORMANCE CHARACTERISTICS



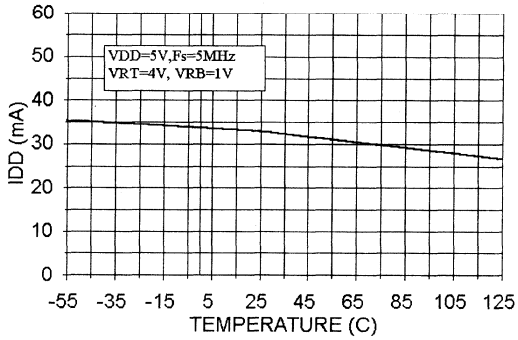
Graph 1. DNL vs. Sampling Frequency



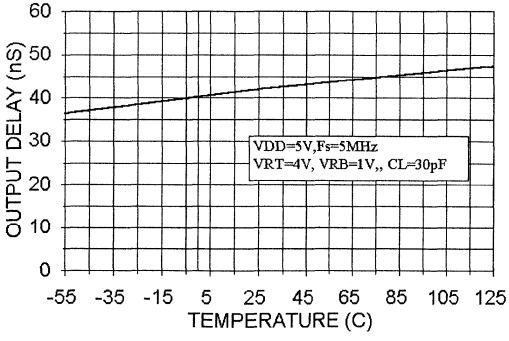
Graph 2. INL vs. Sampling Frequency



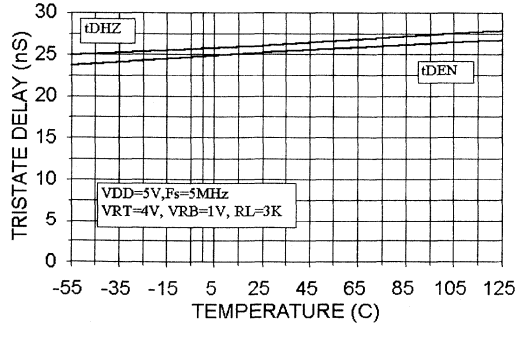
Graph 3. Power Supply Current vs. Sampling Frequency



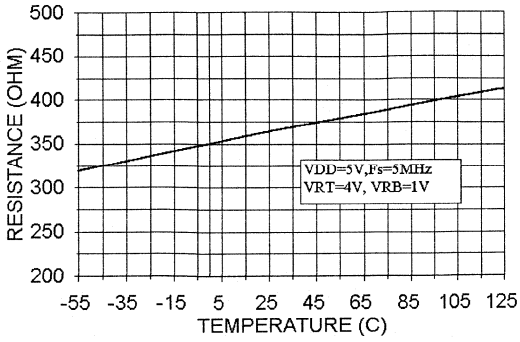
Graph 4. Power Supply Current vs. Temperature



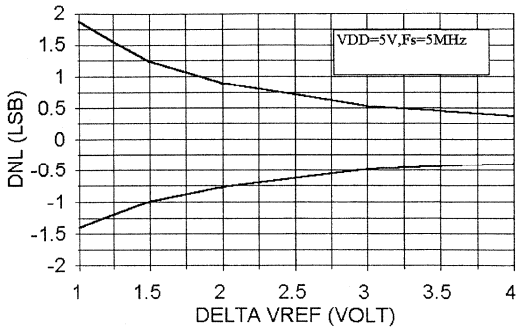
Graph 5. Output Delay vs. Temperature



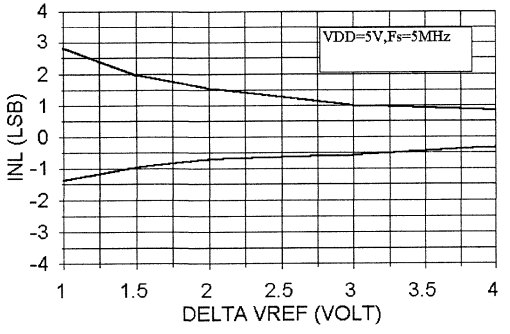
Graph 6. 3-state Delay vs. Temperature



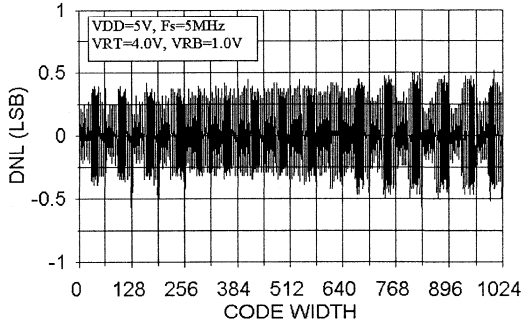
Graph 7. Reference Resistance vs. Temperature



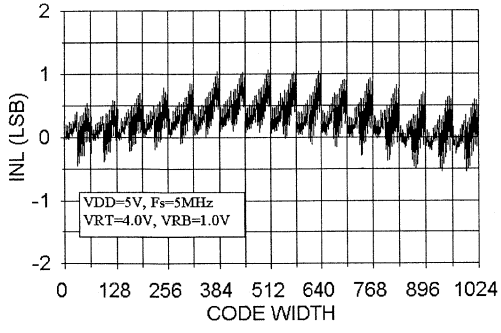
Graph 8. DNL vs. ΔV_{REF}



Graph 9. DNL vs. ΔV_{REF}



Graph 10. DNL Error Plot



Graph 11. INL Error Plot

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MP8784

CMOS
5 MSPS, 10-Bit, High Speed
Analog-to-Digital Converter

FEATURES

- **10-Bit Resolution**
- **5 MHz Sampling Rate**
- **DNL = ±1 LSB, INL = ±2 LSB**
- **Internal S/H Function**
- **Single 5 V Power Supply**
- **V_{IN} DC Range: 0 V to V_{DD}**
- **V_{REF} DC Range: 1 V to V_{DD}**
- **Low Power: 175 mW**
- **Three-State Digital Outputs**
- **Latch-Up Free**
- **3 V Version: MP87L84**

APPLICATIONS

- **Digital Color Copiers**
- **Digital Cellular Telephones**
- **Precision CCDs and Scanners**
- **Medical Scanners**
- **Ultrasonics**
- **Digital Radio**

BENEFITS

- **Simplified Analog Design**
- **Rugged**
- **Few External Components, no S/H Needed**
- **Reduced Board Space**

3

GENERAL DESCRIPTION

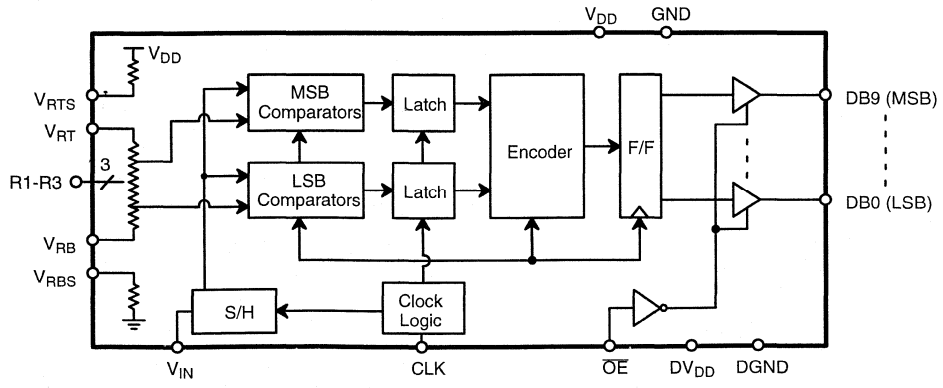
The MP8784 is a 10 bit, 5 MSPS, Analog-to-Digital Converter for applications that require high speed and high accuracy. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The MP8784 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the MP8784 includes an on-chip S/H function that allows this part to digitize analog input signals between AGND and AV_{DD}.

The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 1.0 V at V_{RB} and 4 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R3) can be used to externally trim any INL errors.

This device operates from a single 5 V supply. Power consumption from a 5 V supply is typically 175 mW at F_S=5MHz, and only 150 mW at F_S=1MHz.

SIMPLIFIED BLOCK DIAGRAM

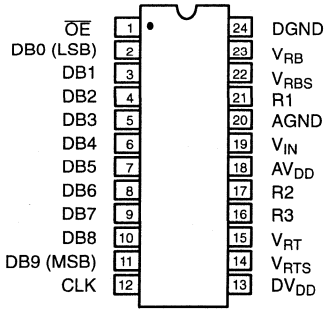


ORDERING INFORMATION

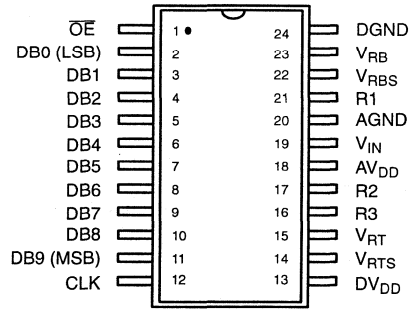
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP8784AN	±1	±2
SOIC	–40 to +85°C	MP8784AS	±1	±2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	CLK	Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV_{DD}	Digital Power Supply
14	V_{RTS}	Top Internal Reference
15	V_{RT}	Top of Reference
16	R3	3/4 Reference Tap Point
17	R2	1/2 Reference Tap Point
18	AV_{DD}	Analog Power Supply
19	V_{IN}	Analog Input Voltage
20	AGND	Analog Ground
21	R1	1/4 Reference Tap Point
22	V_{RBS}	Bottom Internal Reference
23	V_{RB}	Bottom of Reference
24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 5 MHz (50% Duty Cycle), V_{RT} = 4.0, V_{RB} = 1.0, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	FS			5	MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		10		LSB	
Full Scale Error	EFS		6		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}			AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L		375		Ω	
Ladder Temp. Coefficient[2]	R_{TCO}		2000		ppm/°C	
Top Internal Reference	V_{RTS}		4		V	V_{RT} connected to V_{RTS} &
Bottom Internal Reference	V_{RBS}		1		V	V_{RB} connected to V_{RBS}
ANALOG INPUT[2]						
Input Bandwidth (–1 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance Sample[5]	C_{IN}		25	40	pF	
Input Capacitance Convert[5]			5	12	pF	
Aperture Delay	t_{AP}		25	30	ns	
Aperture Uncertainty (Jitter)	t_{AJ}		50		ps	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	4			V	
Logical "0" Voltage	V_{IL}			1	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$ (Internal Res to DGND)[7]			15		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1*)						
Clock Period	1/FS		200		ns	
Rise & Fall Time[8]	t_R, t_F		5		ns	
"High" Pulse Width	t_{PWH}		100		ns	
"Low" Pulse Width	t_{PWL}		100		ns	
Duty Cycle			50		%	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		40	45	ns	
Data Enable Delay	t_{DEN}		25	30	ns	
Data 3-state Delay	t_{DHZ}		25	30	ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9, 10]	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		35	45	mA	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} equivalent circuit (*Figure 8.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE}$ has internal pull down. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Internal resistor to DGND biases unconnected input to active low logical level.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 The AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

10 The AV_{DD} & DV_{DD} pins should be tied together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC ..... 1000 mW
Derates above 75°C ..... 14mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

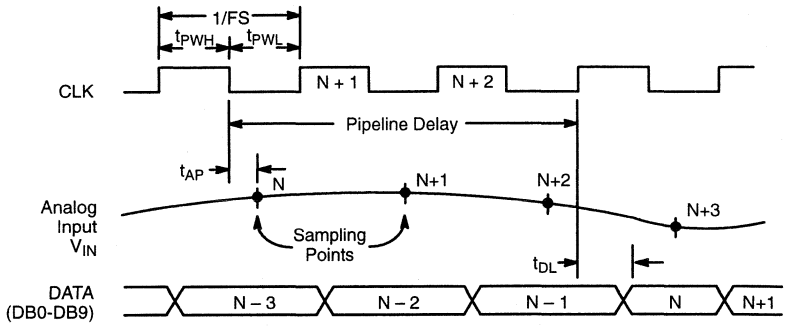


Figure 1. MP8784 Timing Diagram

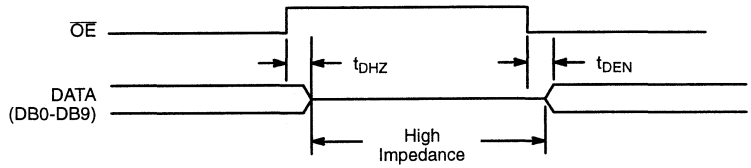


Figure 2. 3-State Timing Diagram

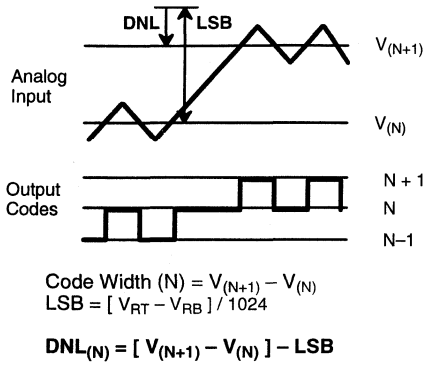


Figure 3. DNL Measurement

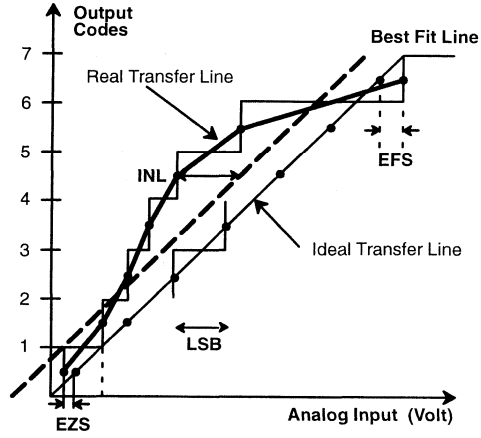


Figure 4. INL Error Calculation

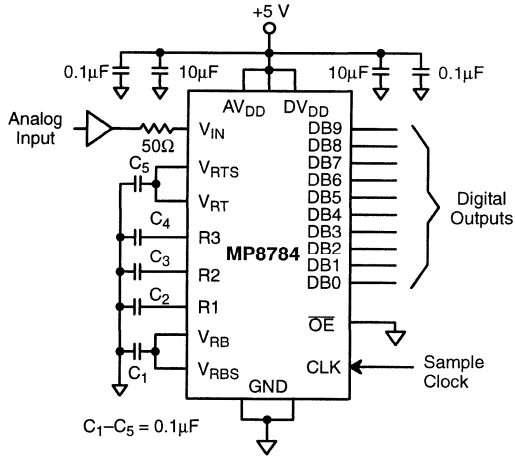


Figure 5. Typical Circuit Connections

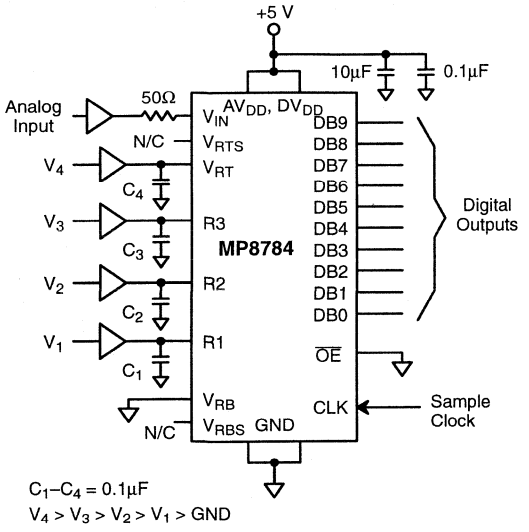


Figure 6. Creating a Piece Wise Linear Transfer Function

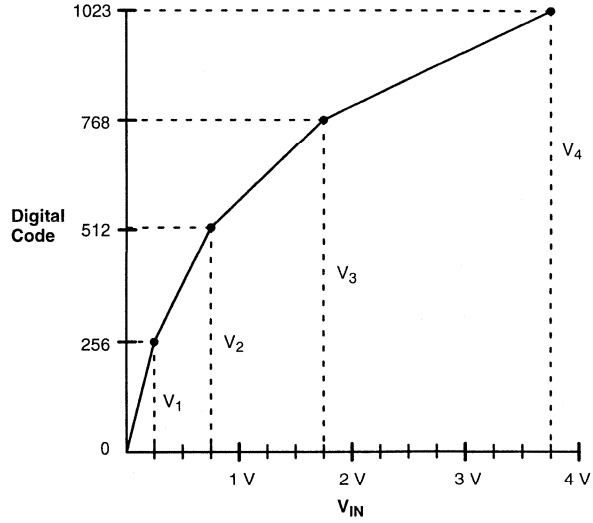


Figure 7. A Piece Wise Linear, Logarithmic Transfer Function

APPLICATION NOTES

Signals should not exceed AV_{DD} or DV_{DD} +0.5V or go below DGND or AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. *Figure 8.* shows an equivalent input circuit.

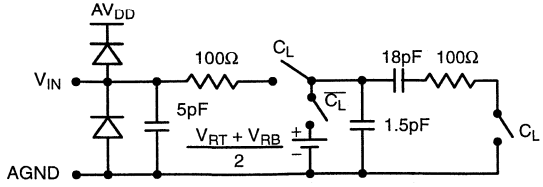


Figure 8. Equivalent Input Circuit

RTS & RBS Internal Bias Resistors

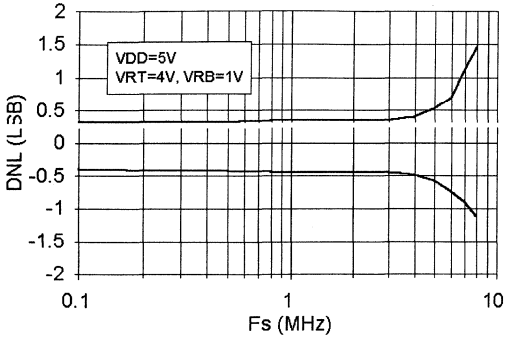
Two matched resistors are provided on the chip. These resistors can be used to generate on chip reference voltages. Each resistor has a value equal to 1/3 of the reference ladder resistor. By connecting RTS to V_{RT}, and connecting RBS to V_{RB}, the reference ladder will be biased to 1 volt at V_{RB} and 4 volts at V_{RT}.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

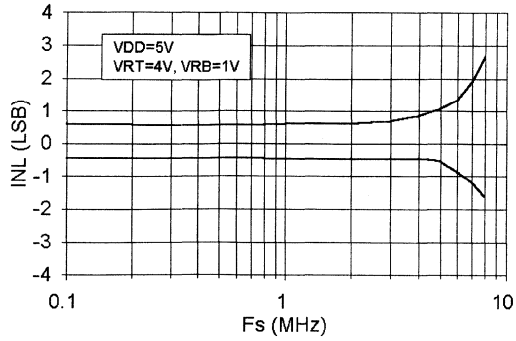
R1 thru R3 Reference Ladder Taps

These taps connect to every eighth point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS}; this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. A four segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

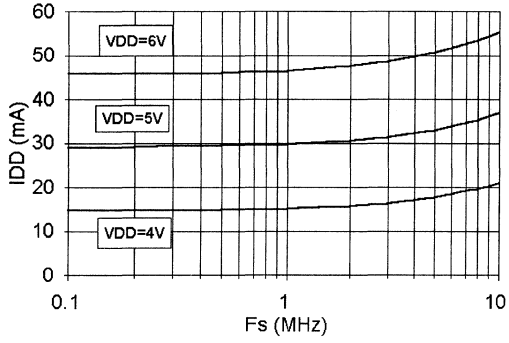
PERFORMANCE CHARACTERISTICS



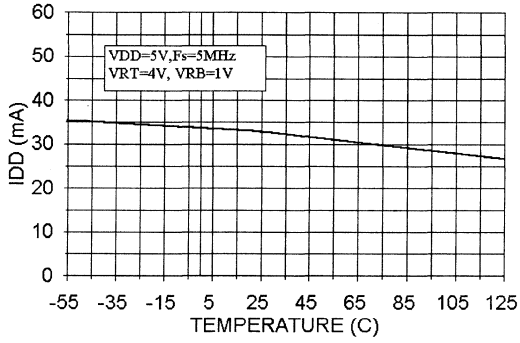
Graph 1. DNL vs. Sampling Frequency



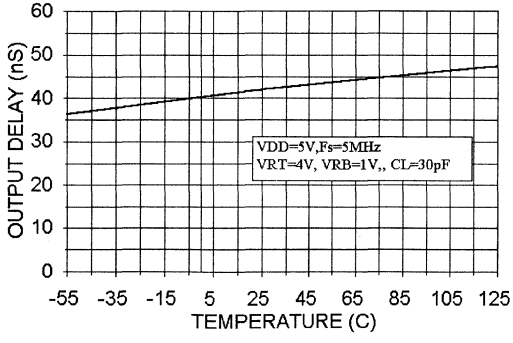
Graph 2. INL vs. Sampling Frequency



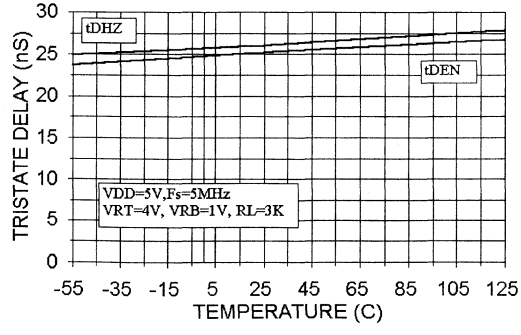
Graph 3. Power Supply Current vs. Sampling Frequency



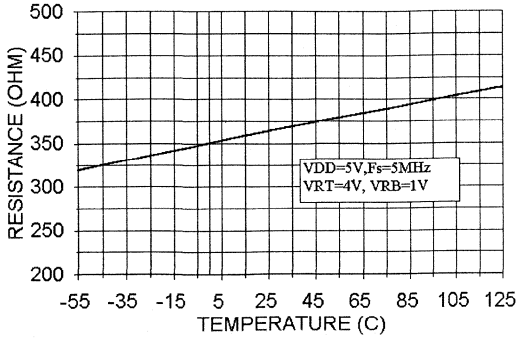
Graph 4. Power Supply Current vs. Temperature



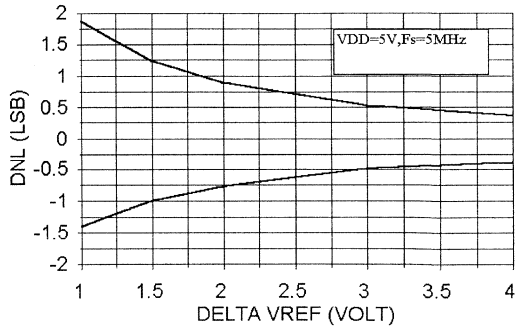
Graph 5. Output Delay vs. Temperature



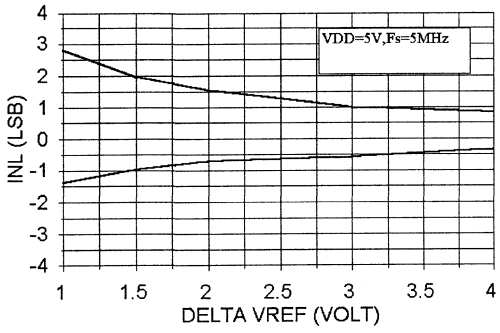
Graph 6. 3-State Delay vs. Temperature



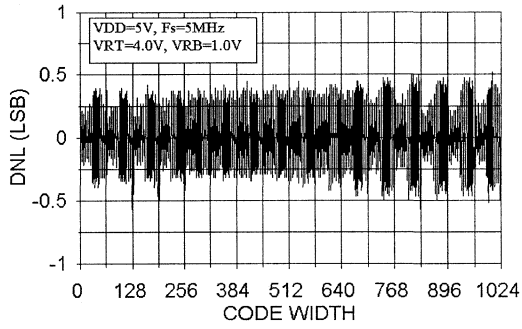
Graph 7. Reference Resistance vs. Temperature



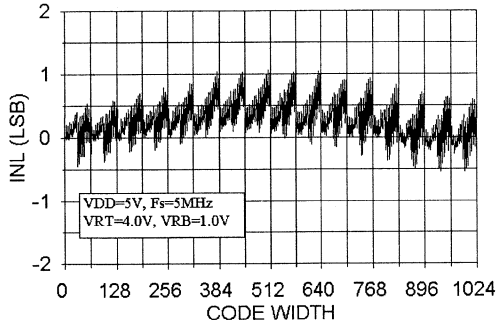
Graph 8. DNL vs. ΔV_{REF}



Graph 9. DNL vs. ΔV_{REF}



Graph 10. DNL Error Plot



Graph 11. INL Error Plot

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MP8784A

CMOS
15 MSPS, 10-Bit, High Speed
Analog-to-Digital Converter

FEATURES

- 10-Bit Resolution
- 15 MHz Sampling Rate
- DNL = ±1 LSB, INL = ±2 LSB
- Internal S/H Function
- Single 5 V Power Supply
- V_{IN} DC Range: 0 V to V_{DD}
- V_{REF} DC Range: 1 V to V_{DD}
- Low Power: 175 mW
- Three-State Digital Outputs
- Latch-Up Free

APPLICATIONS

- Digital Color Copiers
- Digital Cellular Telephones
- Precision CCDs and Scanners
- Medical Scanners
- Ultrasonics
- Digital Radio

BENEFITS

- Simplified Analog Design
- Rugged
- Few External Components, no S/H Needed
- Reduced Board Space

3

GENERAL DESCRIPTION

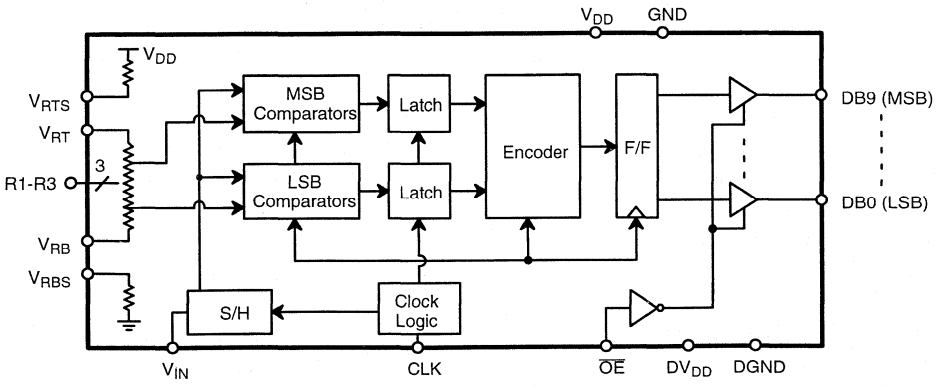
The MP8784A is a 10 bit, 15 MSPS, Analog-to-Digital Converter for applications that require high speed and high accuracy. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The MP8784A uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the MP8784A includes an on-chip S/H function that allows this part to digitize analog input signals between AGND and AV_{DD}.

The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 1.0 V at V_{RB} and 4 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R3) can be used to externally trim any INL errors.

This device operates from a single 5 V supply. Power consumption from a 5 V supply is typically 175 mW at F_S=15 MHz.

SIMPLIFIED BLOCK DIAGRAM



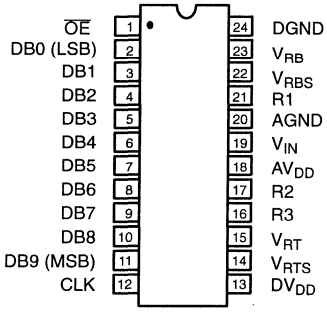
TQM™
Planned

ORDERING INFORMATION

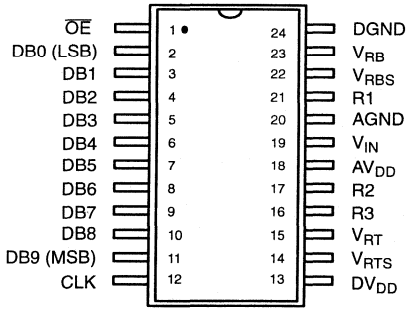
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP8784AAN	±1	±2
SOIC	–40 to +85°C	MP8784AAS	±1	±2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	CLK	Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV_{DD}	Digital Power Supply
14	V_{RTS}	Top Internal Reference
15	V_{RT}	Top of Reference
16	R3	3/4 Reference Tap Point
17	R2	1/2 Reference Tap Point
18	AV_{DD}	Analog Power Supply
19	V_{IN}	Analog Input Voltage
20	AGND	Analog Ground
21	R1	1/4 Reference Tap Point
22	V_{RBS}	Bottom Internal Reference
23	V_{RB}	Bottom of Reference
24	DGND	Digital Ground

MP8785

CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- 8-Bit Resolution
- 20 MHz Sampling Rate
- DNL = ±1/2 LSB, INL = ±1 LSB (typ)
- Internal S/H Function
- Single Supply: 5 V
- V_{IN} DC Range: 0 V to V_{DD}
- V_{REF} DC Range: 1 V to V_{DD}
- Low Power: 85 mW typ. (excluding reference)
- Latch-Up Free
- ESD Protection: 1500 V Minimum
- 20 Pin Package Available: MP8775
- Power Down Available: MP8776
- 3 V Version: MP87L85

APPLICATIONS

- Digital Color Copiers
- Cellular Telephones
- CCD's and Scanners
- Video Capture Boards

3

GENERAL DESCRIPTION

The MP8785 is an 8-bit Analog-to-Digital Converter. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

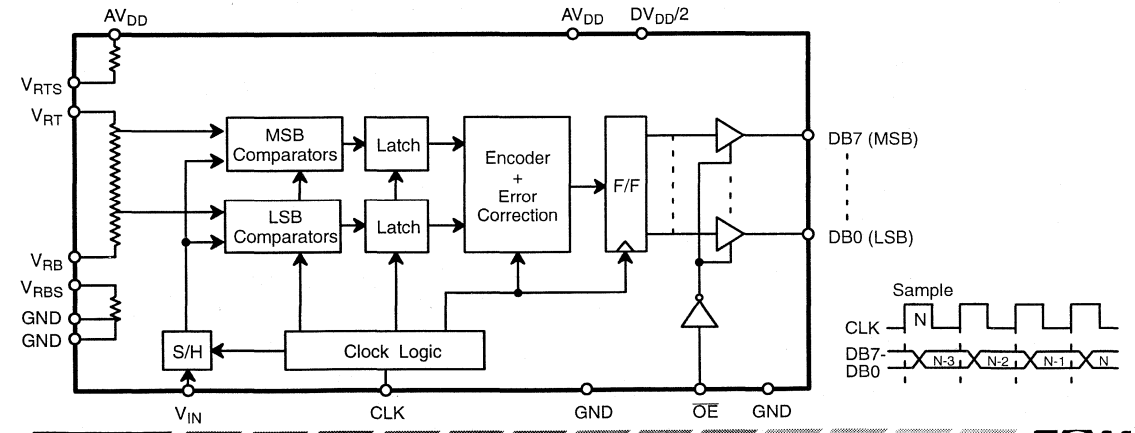
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8785 includes an on-chip S/H function which allows the user to digitize analog input signals between AGND and AV_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP8785.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 V supply. Power consumption is 85 mW at FS = 20 MHz.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP8785 is available in Plastic dual-in-line (PDIP) and Surface Mount (SOIC) packages in EIAJ and Jedec.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

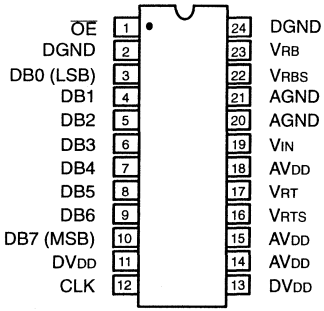


ORDERING INFORMATION

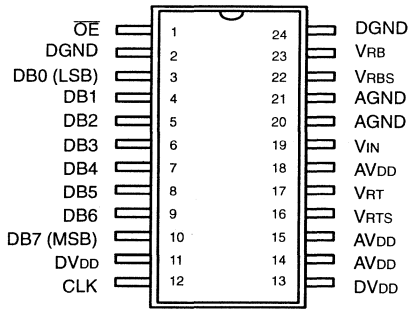
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC (EIAJ)	–40 to +85°C	MP8785AR	±3/4	1 1/2
SOIC (Jedec)	–40 to +85°C	MP8785AS	±3/4	1 1/2
Plastic Dip (0.300")	–40 to +85°C	MP8785AN	±3/4	1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (EIAJ, 0.300") – RN24
24 Pin SOIC (Jedec, 0.300") – S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DGND	Digital Ground
3	DB0	Data Output Bit 0 (LSB)
4	DB1	Data Output Bit 1
5	DB2	Data Output Bit 2
6	DB3	Data Output Bit 3
7	DB4	Data Output Bit 4
8	DB5	Data Output Bit 5
9	DB6	Data Output Bit 6
10	DB7	Data Output Bit 7 (MSB)
11	DV_{DD}	Digital Power Supply
12	CLK	Sampling Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV_{DD}	Digital Power Supply
14	AV_{DD}	Analog Power Supply
15	AV_{DD}	Analog Power Supply
16	V_{RTS}	Generates 2.6 V if tied to V_{RT}
17	V_{RT}	Top Reference
18	AV_{DD}	Analog Power Supply
19	V_{IN}	Analog Input
20	AGND	Analog Ground
21	AGND	Analog Ground
22	V_{RBS}	Generates 0.6 V if tied to V_{RB}
23	V_{RB}	Bottom Reference
24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 15 MHz (50% Duty Cycle), V_{RT} = 2.6 V, V_{RB} = 0.6 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8				Bits
Sampling Rate	FS			20	MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±3/4	LSB	@ 15 MHz
Differential Non-Linearity	DNL			±1/2	LSB	@ 10 MHz
Integral Non-Linearity	INL			±1 1/2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±1 1/4		LSB	
Full Scale Error	EFS		±1 1/4		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	455	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.6		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		2		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		2.3		V	
ANALOG INPUT						
Input Bandwidth (–1 dB)[4]	BW		14		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance[5]	C_{IN}		16		pF	
Aperture Delay	t_{AP}	15	20	25	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	4.0			V	
Logical "0" Voltage	V_{IL}			1.0	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[7]						
Clock Period	1/FS		50		ns	
High Pulse Width	t_{PWH}		25		ns	
Low Pulse Width	t_{PWL}		25		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2, 8]	t_{DL}	18	20	25	ns	
Data Enable Delay[2]	t_{DEN}	16	20	25	ns	
Data 3-state Delay[2]	t_{DHZ}	10	12	15	ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
AC PARAMETERS						
Differential Gain Error	dg		2		%	FS = 4 x NTSC
Differential Phase Error	d_{ph}		1		Degree	FS = 4 x NTSC
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}		5		V	
Current (AGND + DGND)	I_{DD}		17	25	mA	Does not include ref. current

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 t_R, t_F should be limited to >5 ns for best results.

8 Depends on the RC load connected to the output pin.

9 AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 850mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

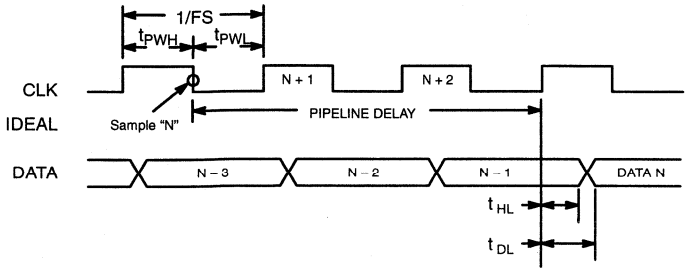


Figure 1. MP8785 Timing Diagram

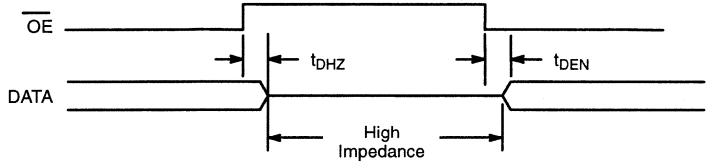
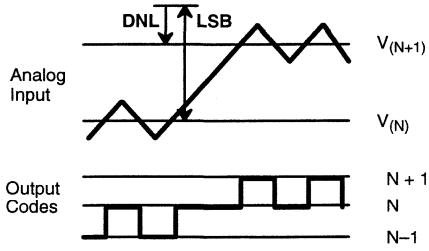


Figure 2. Output Enable/Disable Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 256

$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$

Figure 3. DNL Measurement

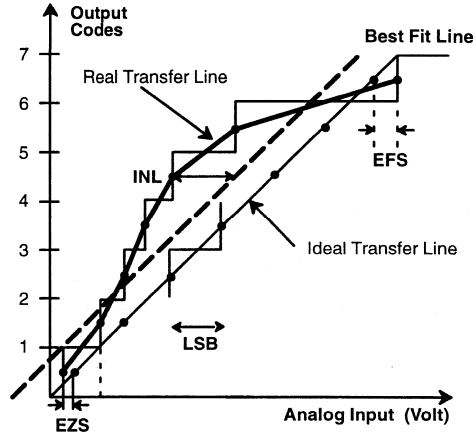


Figure 4. INL Error Calculation

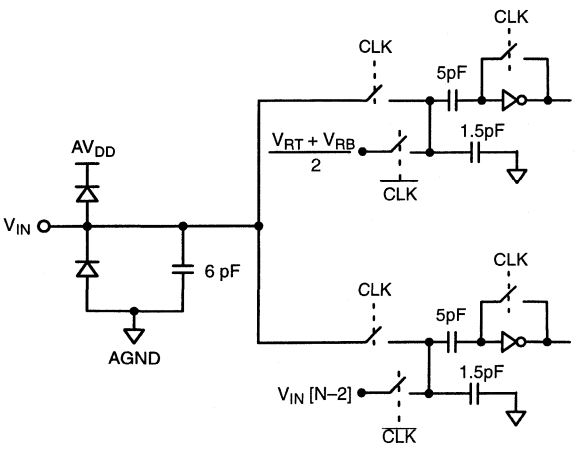


Figure 5. Equivalent Input Circuit

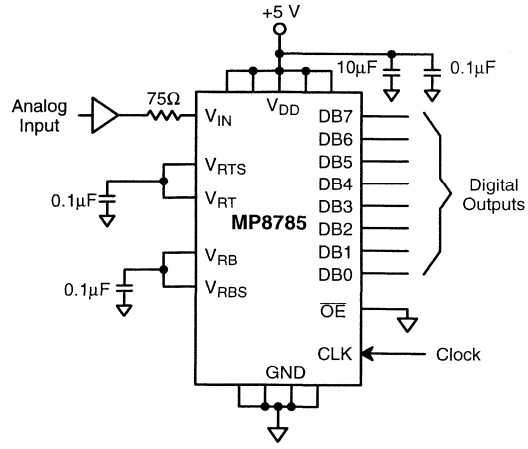


Figure 6. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed V_{DD} +0.5V or go below GND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P-substrate. DC voltage differences between GND pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

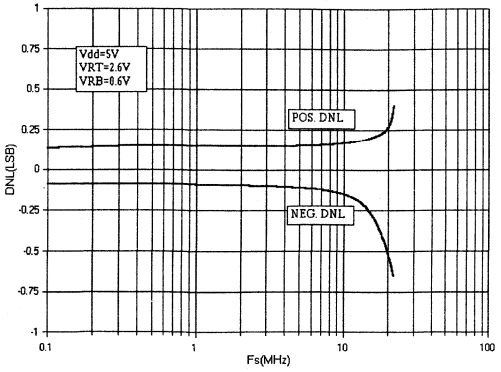
It is possible for the data valid delay (t_{DL}) to be equal to or greater than the high pulse width of the sampling clock (t_{PWH}), See *Figure 1.* This can cause timing related errors. For sample rates above 14 MSPS, use only the rising edge of the sample clock (CLK) to latch data from the MP8785 to other parts of the system.

The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.6 V at V_{RB} and 2.6 V at V_{RT} (see *Figure 5.).*

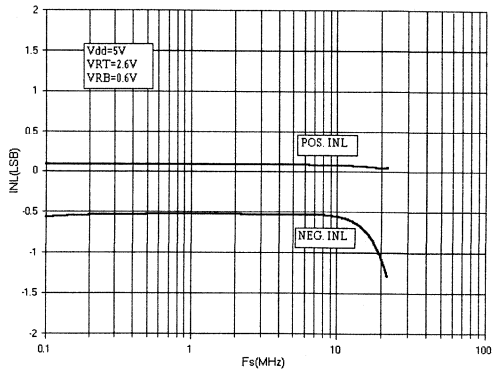
If the internal reference pins V_{RTS} and/or V_{RBS} are not used, they should be left unconnected.

The output enable pin ($\overline{OE}$) should not be left unconnected. If not controlled by an active signal then it must be tied to DGND.

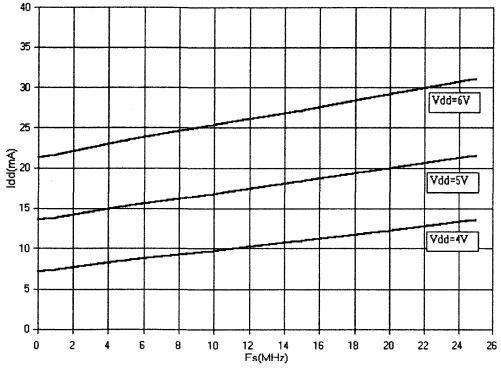
PERFORMANCE CHARACTERISTICS



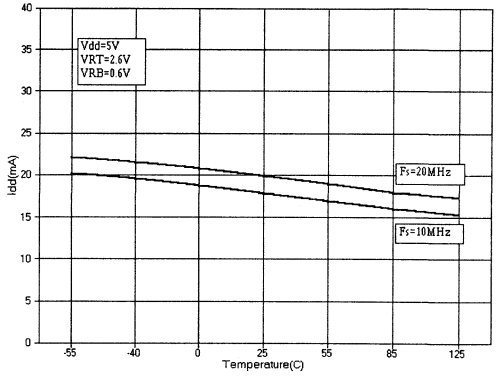
Graph 1. DNL vs. Sampling Frequency



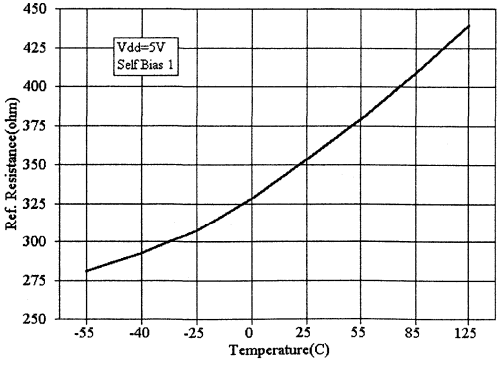
Graph 2. INL vs. Sampling Frequency



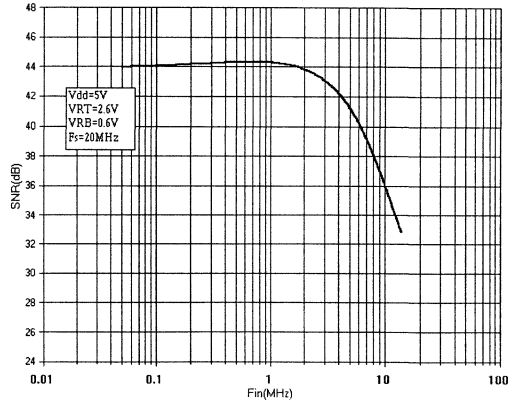
Graph 3. Supply Current vs. Sampling Frequency



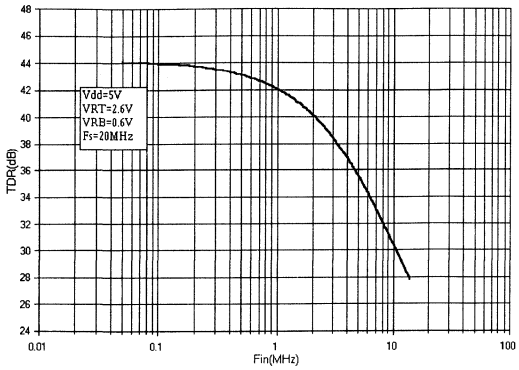
Graph 4. Supply Current vs. Temperature



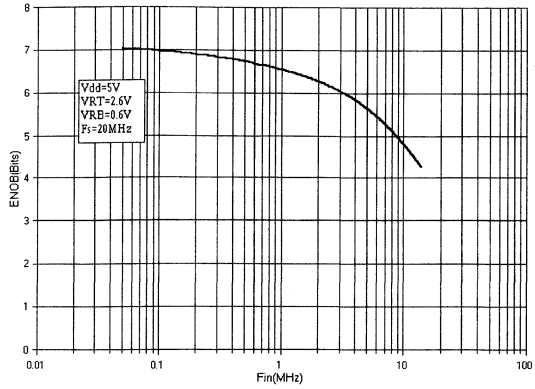
Graph 5. Reference Resistance vs. Temperature



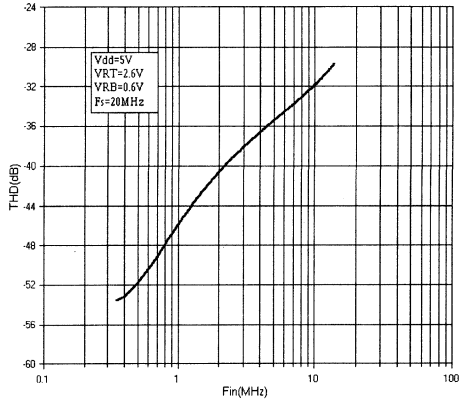
Graph 6. SNR vs. Input Frequency



Graph 7. SINAD vs. Input Frequency



Graph 8. ENOB vs. Input Frequency



Graph 9. THD vs. Input Frequency

MP8786

CMOS

30 MSPS, 8-Bit High Speed, Low Power Analog-to-Digital Converter with Power Down

FEATURES

- 8-Bit Resolution
- Sampling Rate to 30 MHz
- Low Power: 110 mW typ. (excluding reference)
- Power Down Mode: 100µA (typ)
- DNL = ±1/4 LSB, INL = ±1/2 LSB (typ)
- Internal S/H Function
- Single Supply: 5 V
- V_{IN} Range: 0 V to V_{DD}
- V_{REF} Range: 1 V to V_{DD}
- Latch-Up Free
- ESD Protection: 2000 V Minimum
- 3 State Digital Outputs
- 20 Pin Package Available: MP8776
- 3 V Version: MP87L86
- Improved Version of MP8785

APPLICATIONS

- Wireless Communications
- Digital Cellular Telephones
- Telecommunications
- CCDs and Scanners
- Video Boards
- Digital Color Copiers
- Battery Powered Devices

3

GENERAL DESCRIPTION

The MP8786 is an 8-bit Analog-to-Digital Converter designed for high speed digitizing applications requiring low power. The MP8786 offers exceptional performance, flexible input architecture, low power consumption, power down capability, latch-up tolerant operation and is manufactured using an advanced 5 volt CMOS process.

This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8786 includes an on-chip S/H function which allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP8786.

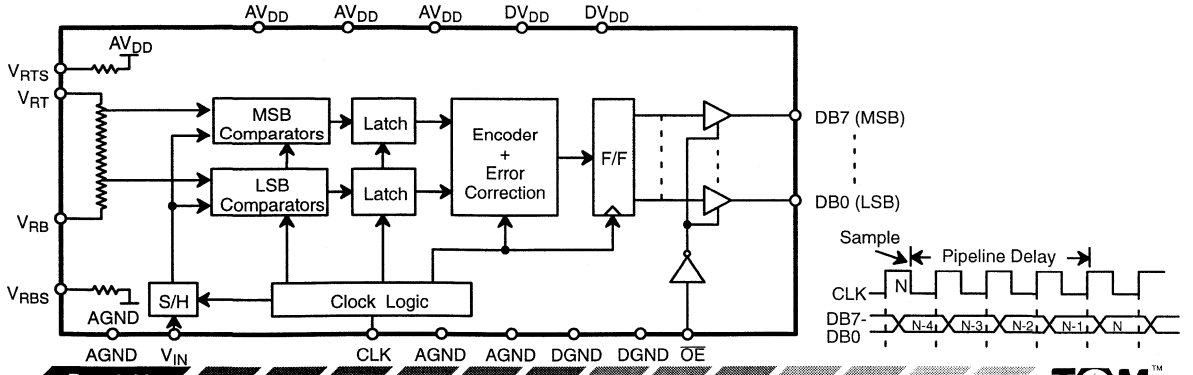
The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

When board space is at a premium, designers may prefer to use the MP8776 which is available in a 20 pin package.

The device operates from a single +5 volt supply. Power consumption is 110 mW (typ) at FS = 20 MHz. Power down is accomplished by dropping V_{RT} below 0.55 V.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP8786 is available in surface mount (SOIC) in Jedec and EIAJ, shrink small outline (SSOP) and plastic dual-in-line (PDIP) packages.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

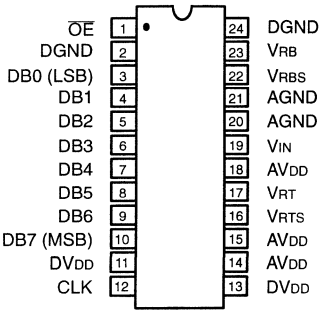


ORDERING INFORMATION

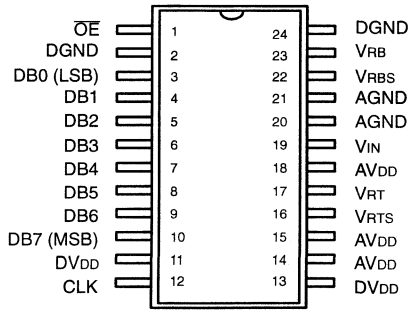
Package Type	Temperature Range	Part No.
SOIC (EIAJ)	–40 to +85°C	MP8786AR
SOIC (Jedec)	–40 to +85°C	MP8786AS
Plastic Dip	–40 to +85°C	MP8786AN
SSOP	–40 to +85°C	MP8786AQ

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (EIAJ, 0.300") – RN24
24 Pin SOIC (Jedec, 0.300") – S24
24 Pin SSOP – A24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DGND	Ground (outputs)
3	DB0	Data Output Bit 0 (LSB)
4	DB1	Data Output Bit 1
5	DB2	Data Output Bit 2
6	DB3	Data Output Bit 3
7	DB4	Data Output Bit 4
8	DB5	Data Output Bit 5
9	DB6	Data Output Bit 6
10	DB7	Data Output Bit 7 (MSB)
11	DV_{DD}	Power Supply (outputs)
12	CLK	Sampling Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV_{DD}	Digital Power Supply
14	AV_{DD}	Power Supply
15	AV_{DD}	Power Supply
16	V_{RTS}	Generates 2.6 V if tied to V_{RT}
17	V_{RT}	Top Reference
18	AV_{DD}	Power Supply
19	V_{IN}	Analog Input
20	AGND	Ground
21	AGND	Ground
22	V_{RBS}	Generates 0.6 V if tied to V_{RB}
23	V_{RB}	Bottom Reference
24	DGND	Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 20 MHz (50% Duty Cycle), V_{RT} = 2.6 V, V_{RB} = 0.6 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS	0.01		20	MHz	For specified performance
	FS			30	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL		±1/4	±1/2	LSB	
Integral Non-Linearity	INL		±1/2	1	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±35		mV	
Full Scale Error	EFS		±35		mV	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	455	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1	V_{RB}		0.6		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
	V_{REF}		2		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
Self Bias 2	V_{RT}		2.3		V	V_{RB} = AGND, Short V_{RT} and V_{RTS}
ANALOG INPUT[2]						
Bandwidth (–1 dB)[4]	BW		14		MHz	
Input Voltage Range	V_{IN}	0		AV_{DD}	V	
Input Capacitance Sample[5]	C_{IN}		22		pF	Clock High
Input Capacitance Convert[5]	C_{IN}		7		pF	Clock Low
Aperture Delay	t_{AP}		10		ns	
Aperture Jitter	t_{AJ}		30		ps	
DYNAMIC PERFORMANCE[2]						F_{IN} = 1 MHz
Signal to Noise Ratio	SNR		46		dB	
Signal to Noise plus Distortion	SINAD		42		dB	
Harmonic Distortion	THD		–46		dB	
Effective No. of Bits	ENOB		6.8		Bits	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	3.5			V	
Logical "0" Voltage	V_{IL}			1.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 6.*)[7]						
Clock Period	1/FS	50			ns	For Specified Performance
High Pulse Width	t_{PWH}	25			ns	For Specified Performance
Low Pulse Width	t_{PWL}	25			ns	For Specified Performance

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5					V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4			V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10				µA	V_{OUT}=GND to DV_{DD}
Data Valid Delay[2, 8]	t_{DL}		20				ns	
Data Enable Delay[2, 8]	t_{DEN}		20	25			ns	
Data 3-state Delay[2, 8]	t_{DHZ}		12	15			ns	
Pipeline Delay				3.5			clock cycles	Constant relationship between clock and output
POWER SUPPLIES								
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}		5				V	
Current (AV_{DD} + DV_{DD})	I_{DD}		22	35			mA	Does not include ref. current
POWER DOWN								
Power Down Point	V_{RTPD}	0.4	0.55				V	Chip goes to power down mode
Power Up Point				0.9			V	when V_{RT} < 0.55 V
Power Down Current	I_{DDPD}			100			µA	Does not include ref. current
Power Control Delay	PDD			200			ns	V_{RT} @ 0.4→0.9 V

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 10.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 11.*) Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 The bandwidth represents the gain of the ADC and does not imply accuracy

5 See V_{IN} input equivalent circuit (*Figure 2.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to V_{DD} and GND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

7 t_R, t_F should be limited to >5 ns for best results.

8 Depends on the RC load connected to the output pin.

9 AGND and DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted) [1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP, SSOP ..... 750 mW
Derates above 75°C ..... 10 mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

THEORY OF OPERATION

Analog to Digital Conversion

The MP8786 uses a two step, subranging architecture to convert analog voltages into 256 digital codes.

A full conversion (sampling V_{IN}, converting MSB & LSB, and performing any error correction) requires four clock cycles to complete (*see Figure 6.*) The pipelined architecture allows the chip to maintain a one conversion per cycle sample rate. Digital logic combines the MSB and LSB data and performs error correction to produce 8-bit output codes.

Internal Reference Bias

The MP8786 includes two on-chip resistors that can be used to bias the reference ladder without external circuitry. These two resistors are designed to track the reference ladder and are used to create a voltage divider between the supplies (AV_{DD} and AGND).

To use this feature simply connect V_{RT} to V_{RTS} and connect V_{RB} to V_{RBS}. This will nominally generate:

AV_{DD} x (0.3/2.5) at V_{RB}, and

AV_{DD} x (1.3/2.5) at V_{RT}

This will generate 0.6 V at V_{RB} and 2.6 V at V_{RT} (*Figure 1.*) Bypass capacitors on V_{RT} and V_{RB} are suggested to stabilize the ladder.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

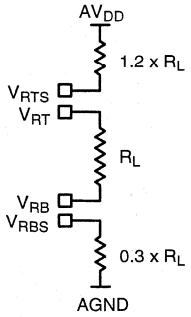


Figure 1. Internal Reference Bias

Transfer Characteristics

The ideal ADC is a linear building block that has infinite bandwidth and no phase distortion. A real ADC, however, exhibits finite bandwidth and non-constant group delay characteristics as well as non-linear behavior due to the non-zero INL characteristic. When modeling the ADC as a linear element and a quantizer, the circuit shown in *Figure 2.* can be used in order to represent the ADC's bandwidth.

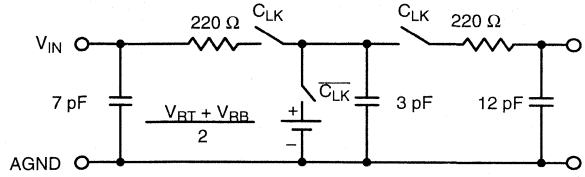


Figure 2. Input Equivalent Circuit

Sample and Hold Timing

The ADC's internal sample and hold tracks the input signal when CLK is high. After a delay of t_{AP} from the falling clock edge, the analog signal is sampled and held for conversion as seen in *Figure 3.*

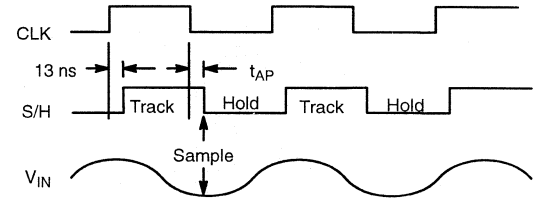


Figure 3. Sample and Hold Timing

Output Enable ($\overline{OE}$)

The $\overline{OE}$ pin controls the state of the digital output drivers. When forced low, the drivers are active. When pulled high the drivers are 3-stated. Please note that the $\overline{OE}$ pin only controls the output drivers, the rest of the chip is still active. Therefore if the clock is running, the internal registers are updated even if the digital outputs are 3-stated (*Figure 4.*).

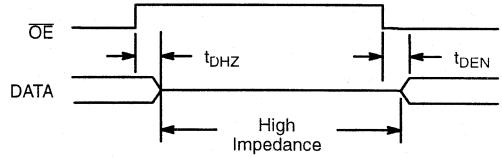


Figure 4. Output Enable/Disable Timing Diagram

Power Down Mode

For systems that are battery powered, the MP8786 has a power down feature to help extend battery life. When the voltage at the V_{RT} pin drops below 0.4 V, the chip goes into power down mode. In this state, conversions are halted, the outputs are 3-stated and I_{DD} drops to less than 100 µA. Then, when the voltage at the V_{RT} pin rises above 0.9 V, the chip will power up. Note that after power up, four clock cycles are required to get valid data at the digital outputs (see *Figure 6.*) One way to achieve power down is to disconnect or disable the buffer/amp driving V_{RT}, and let the internal reference resistance pull V_{RT} down. Remember, any bypass capacitors at V_{RT} will increase the time for V_{RT} to drop below 0.4 V.

APPLICATION NOTES

Power Supplies and Grounding

AV_{DD} and DV_{DD} should be connected to the sample power supply source (*Figure 5.*). The power supply (AV_{DD} and DV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to GND, placed as close to the chip as possible.

AGND and DGND pins are connected internally through the P-substrate. AGND and DGND pins should be connected together as close to the chip as possible.

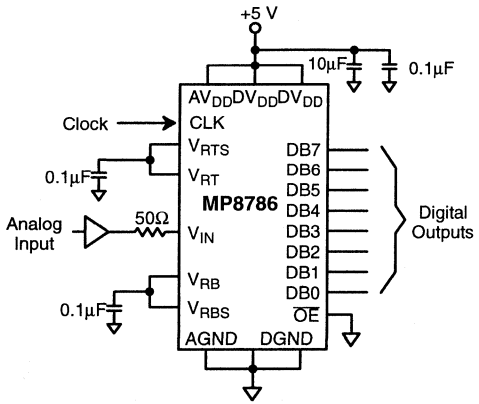


Figure 5. Typical Circuit Connections

The Analog Input

When designing with the MP8786, the following points can help optimize performance.

1. Driving the analog input – The input impedance can be represented as a switched capacitor type input circuit, ie. the input impedance changes with the phase of the input clock. *Figure 2.* shows an equivalent input circuit. In many applications, the input impedance can be treated as capacitive. For fast signals and a high driving impedance, a wide bandwidth op amp is recommended.
2. It is important to note that op amps have inductive output impedances at high frequencies which is a consequence of the emitter impedance of the typical push-pull output stage. The resulting transient ringing should be damped by inserting a resistor in series with the ADC input – typically about 50Ω. See *Figure 5.* The exact value may be obtained from the op amp manufacturer's data sheet.
3. Signals should not exceed V_{DD} +0.5V or go below GND –0.5V. All pins have internal protection diodes that will protect them from short transients (*See Note 2, Absolute Maximum Ratings*) outside the supply range.

Digital Outputs

Refer to *Figure 6.* for details on the data availability timing. The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion. The output enable pin ($\overline{OE}$) should not be left unconnected. If it is not controlled by an active signal, it must be tied to ground.

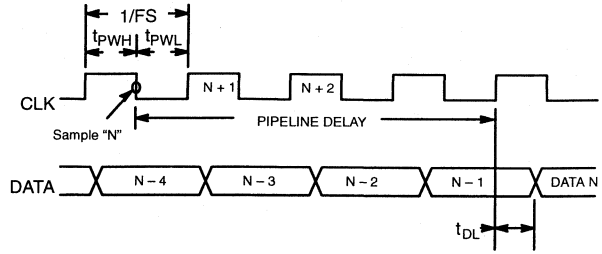


Figure 6. Data Available Timing

Dynamic Reference Control

The MP8786 allows for dynamically adjusted V_{RT} and V_{RB}. When this is done, V_{RT} and V_{RB} have to be kept static during a certain period.

The A/D conversion is done in a two-step method. During the first clock period, the MSB comparator bank compares the V_{IN} with the reference voltage string in order to determine in which subrange the exact V_{IN} lies. During the subsequent clock period, an LSB comparator bank compares a subrange of the V_{REF} to the V_{IN}. Thus, the reference inputs have to be stable during two compare cycles. This implies that while the ADC is clocked with FS, the conversion only occurs at a rate of FS/2. Every second sample and resulting data must be discarded because the reference changes during its conversion.

The reference inputs V_{RT} and V_{RB} have to have settled to within 1 LSB, at least 50 ns before the rising edge which occurs after the sampling instant. The reference has to be kept constant until (t_{AP} + 10 ns) after the second rising edge. See *Figure 7.* for timing details. The digital data of the N + 1, N +3, N + 5 etc. samples are invalid if the reference is changed every second clock cycle. The data for the N, N + 2, N + 4 etc. samples are valid.

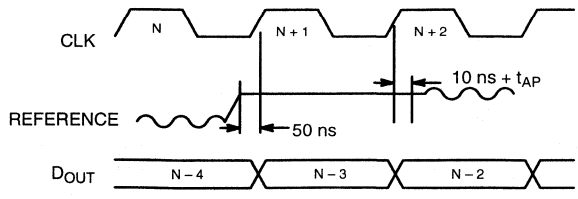


Figure 7. Dynamic Reference Control

LINEARITY DEFINITION

The Ideal ADC

The transfer function for an ideal A/D converter is shown in *Figure 8.*

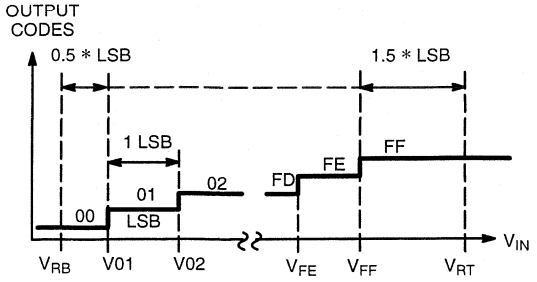


Figure 8. Ideal A/D Transfer Function

The first transition for the data bits takes place when:

$V_{IN} = V01 = V_{RB} + 0.5 * LSB$

The last transition of the data bits takes place when:

$V_{IN} = V_{FF} = V_{RT} - 1.5 * LSB$

where: $LSB = V_{REF} / 256$
$= (V_{FF} - V01) / 254$

and $V_{REF} = (V_{RT} - V_{RB})$

The Real ADC

In a "real" converter, the code-to-code transitions do not fall exactly every $V_{REF}/256$ volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A specification of Max DNL = ±0.5 LSB means that all codes are within 0.5 LSB and 1.5 LSB. For example, if V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is between 8 and 24 mV.

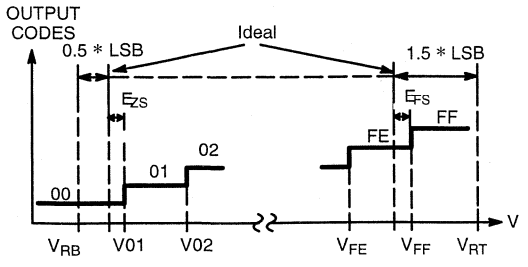


Figure 9. Real A/D Transfer Curve

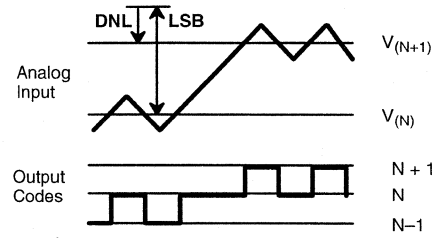


Figure 10. DNL Measurement

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) are:

DNL (01) = V02 – V01 – LSB
: : :
DNL (FE) = $V_{FF} - V_{FE}$ – LSB
Thus $DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$
Code Width (N) = $V_{(N+1)} - V_{(N)}$

Similarly, the zero scale and full scale errors are defined as:

EFS (full scale error) = $V_{FF} - (V_{RT} - 1.5 * LSB)$
EZS (zero scale error) = $V01 - (V_{RB} + 0.5 * LSB)$
where: $LSB = [V_{RT} - V_{RB}] / 256$

Figure 9. shows the zero scale and full scale error terms while *Figure 10.* shows the definition of DNL.

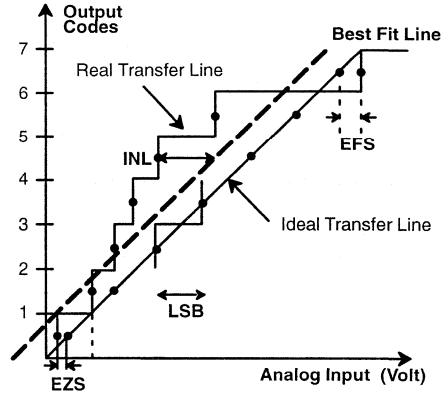
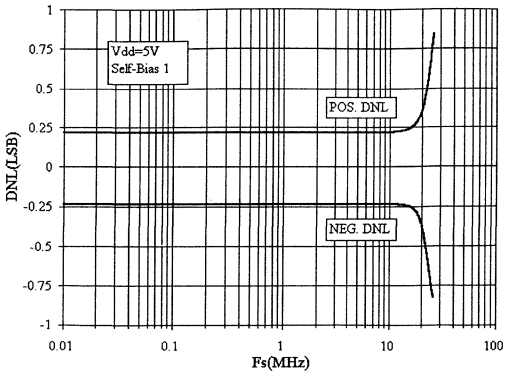


Figure 11. INL Error Calculation (3-Bit)

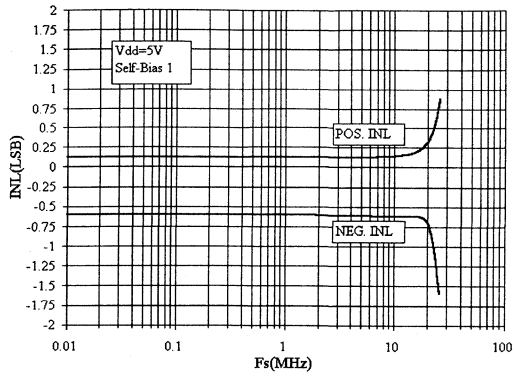
Figure 11. gives a visual definition of the INL error. The graph shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the best fit line makes equal the positive and and the negative INL errors. This may change an INL of –1 to +2 LSBs relative to the ideal line into a ±1.5 relative to the best fit line.

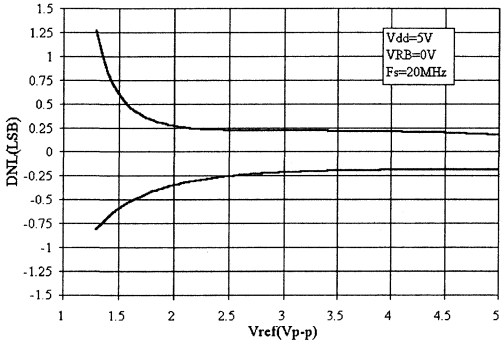
PERFORMANCE CHARACTERISTICS



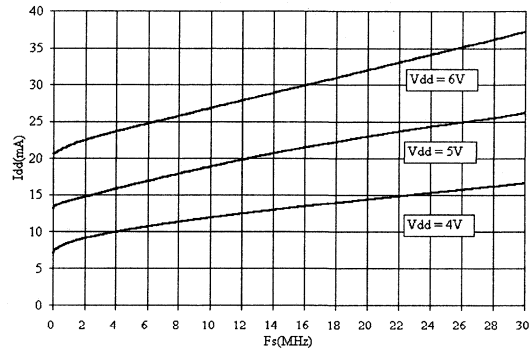
Graph 1. DNL vs. Sampling Frequency



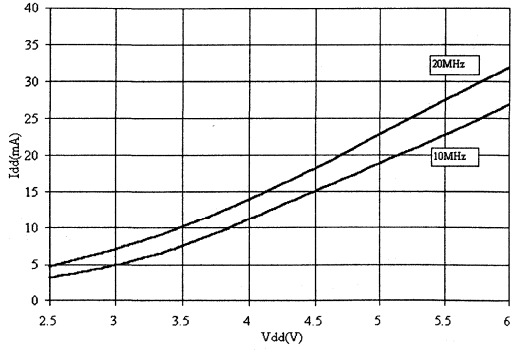
Graph 2. INL vs. Sampling Frequency



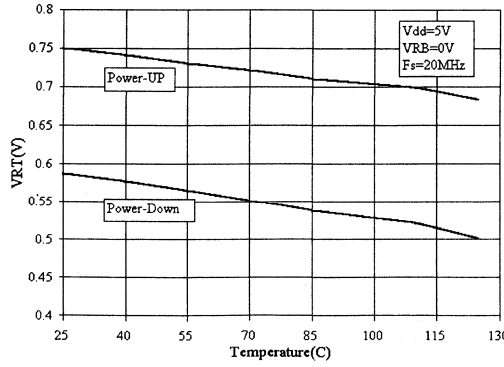
Graph 3. DNL vs. Reference Voltage



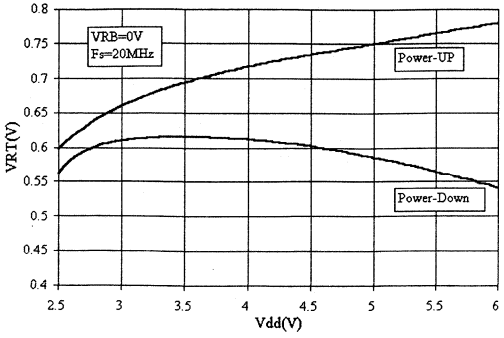
Graph 4. Supply Current vs. Sampling Frequency



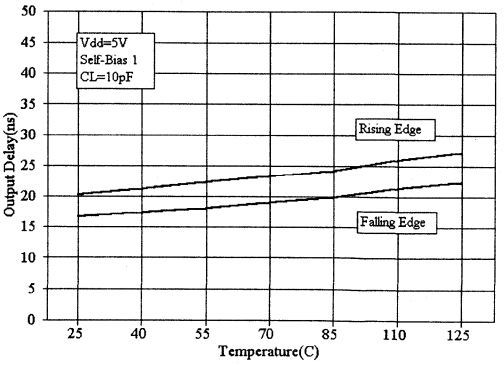
Graph 5. Supply Current vs. Supply Voltage



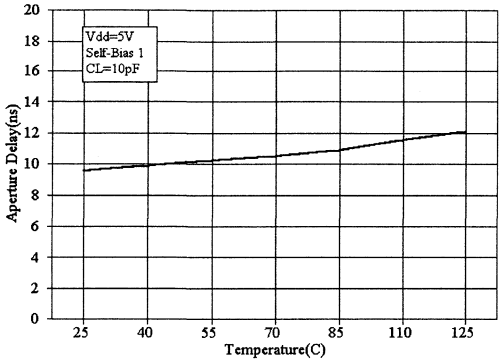
Graph 6. Power Up/Down Voltage vs. Temperature



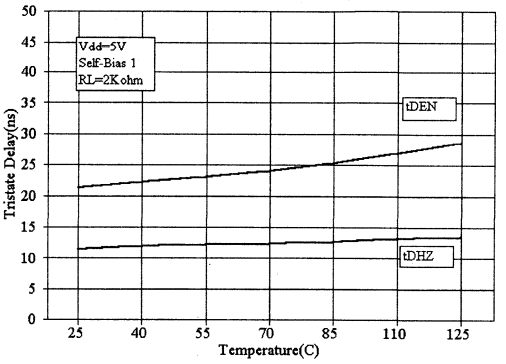
Graph 7. Power Up/Down Voltage vs. Supply Voltage



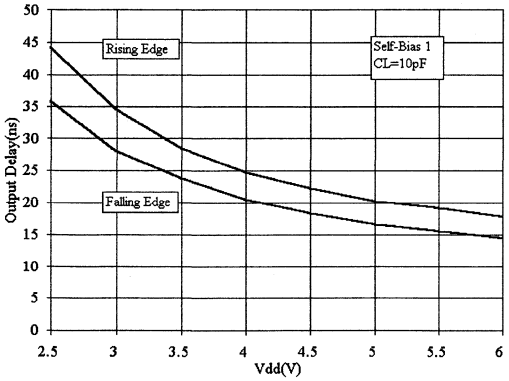
Graph 8. Output Delay (t_{DL}) vs. Temperature



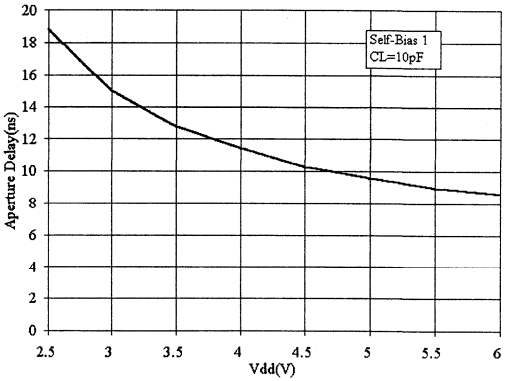
Graph 9. Aperture Delay (t_{AP}) vs. Temperature



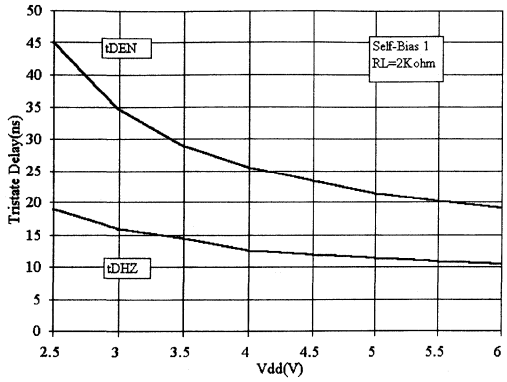
Graph 10. 3-State/Enable Delay vs. Temperature



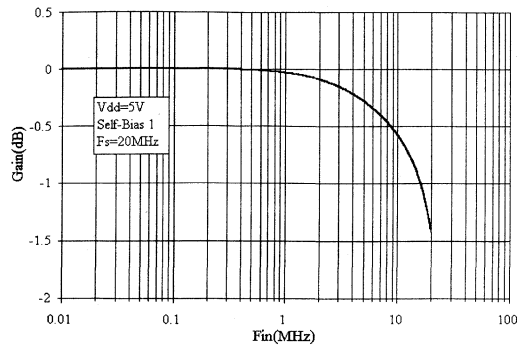
Graph 11. Output Delay vs. Supply Voltage



Graph 12. Aperture Delay (t_{DL}) vs. Supply Voltage



Graph 13. 3-State/Enable Delay vs. Supply Voltage



Graph 14. Gain vs. Input Frequency

MP8790

2 MSPS, CMOS 12-Bit Analog-to-Digital Converter with Parallel and Serial Logic Interface Port

FEATURES

- 12-Bit ADC with DNL = ±1 LSB, INL = ±2 LSB
- SNR > 60 dB
- Sampling Frequency ≤ 2 MHz
- Internal Track and Hold: Input –3 dB Frequency = 10 MHz
- Single 5 V Supply
- Rail-to-Rail Input Range
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 200 mW (typ)
- 15 Equally Spaced Ladder Taps for Non-Linear Transfer Function
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode
- Serial and Parallel Port
- Overflow and Underflow Outputs
- Precision Aperture Output
- Latch-Up Free
- 28 Pin Package: MP8791 & MP8792

APPLICATIONS

- Instrumentation
- DAS
- Radar
- Medical Imaging
- Ultrasound
- Broadcast and Studio Video
- Magnetic Resonance Signal Acquisition
- Digital Oscilloscopes
- Spectrum Analysis
- Digital Radio

3

GENERAL DESCRIPTION

The MP8790 is a 12-bit 2-step high speed Analog-to-Digital Converter with DNL = ±1 LSB and INL = ±2 LSB. The MP8790 contains an internal track and hold which allows for analog input signals as fast as 2 MHz and can convert signals at a 2 MSPS rate.

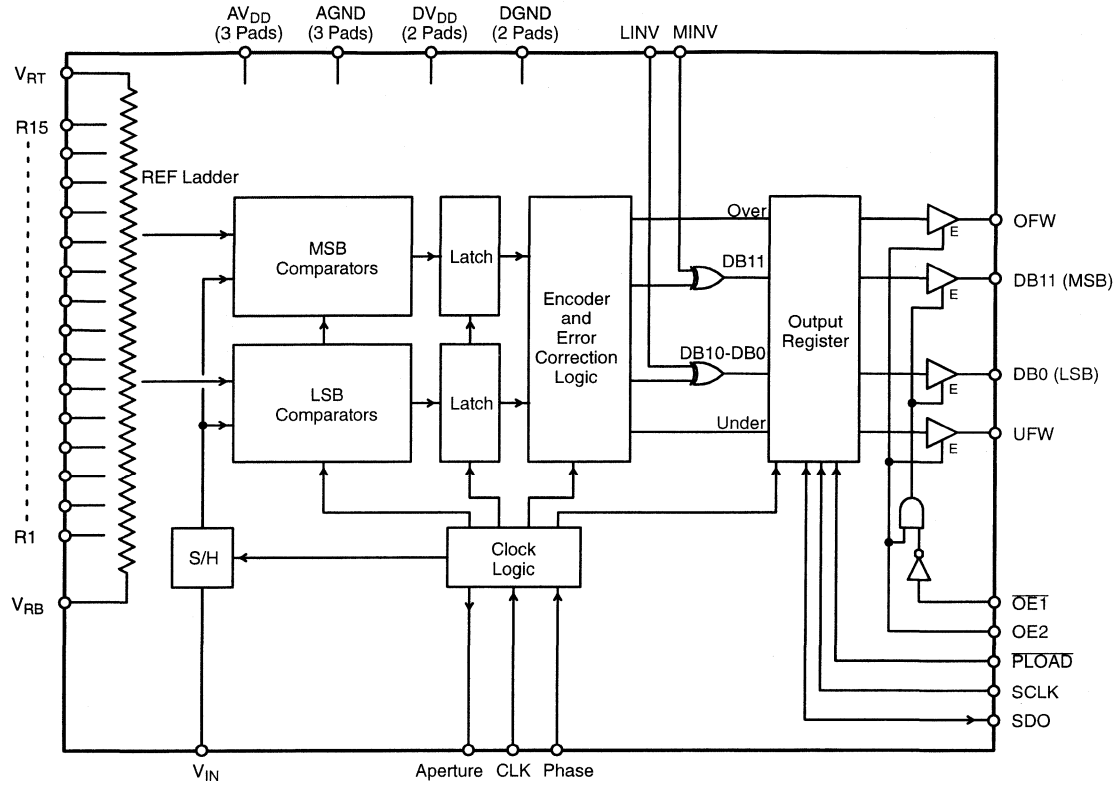
The MP8790 operates with a single supply ranging from +3 V to +5 V while consuming less than 200 mW of power (typical). Separate pins for reference ladder terminals and power supplies allow flexibility for various A_{IN}, ΔV_{REF}, and power supply ranges.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay. The digital output port is also equipped with a 3-state function, as well as a serial data port. LINV and MINV enable binary and 2's complement data formatting. The 15 ladder tap pins (R1-R15) can accommodate transfer function adjustment, linearity, and speed enhancement.

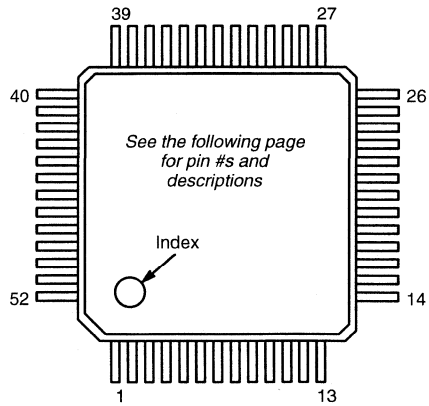
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP8790AE	±1	2 1/2

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS



52 Pin PQFP
QN52 (10 mm X 10 mm)
Contact Factory for Package Drawing

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	R10	Ref. Resistor Ladder Tap (10/16 V_{REF})
2	R12	Ref. Resistor Ladder Tap (12/16 V_{REF})
3	R11	Ref. Resistor Ladder Tap (11/16 V_{REF})
4	R3	Ref. Resistor Ladder Tap (3/16 V_{REF})
5	R13	Ref. Resistor Ladder Tap (13/16 V_{REF})
6	R4	Ref. Resistor Ladder Tap (4/16 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/16 V_{REF})
8	R15	Ref. Resistor Ladder Tap (15/16 V_{REF})
9	R2	Ref. Resistor Ladder Tap (2/16 V_{REF})
10	R6	Ref. Resistor Ladder Tap (6/16 V_{REF})
11	V_{RB}	Negative Reference
12	V_{RT}	Positive Reference
13	R14	Ref. Resistor Ladder Tap (14/16 V_{REF})
14	AV_{DD}	Analog Positive Supply
15	AV_{DD}	Analog Positive Supply
16	AGND	Analog Ground
17	AGND	Analog Ground
18	MINV	Invert MSB (Active High)
19	LINV	Invert LSB (Active High)
20	UFW	Underflow Bit
21	DB0	Data Output Bit 0 (LSB)
22	DB1	Data Output Bit 1
23	DB2	Data Output Bit 2
24	DB3	Data Output Bit 3
25	DB4	Data Output Bit 4
26	DB5	Data Output Bit 5

PIN NO.	NAME	DESCRIPTION
27	SDO	Serial Data Out
28	DV_{DD}	Digital Positive Supply
29	DV_{DD}	Digital Positive Supply
30	DGND	Digital Ground
31	DGND	Digital Ground
32	PHASE	Phase Clock Polarity Control
33	SCK	Serial CLK
34	Aperture	Aperture Delay Sync
35	OFW	Overflow
36	OE2	Output Enable (Active High)
37	$\overline{OE}$	Output Enable (Active Low)
38	CLK	Clock
39	$\overline{PLOAD}$	Serial Shift Register Data Load
40	DB6	Data Output Bit 6
41	DB7	Data Output Bit 7
42	DB8	Data Output Bit 8
43	DB9	Data Output Bit 9
44	DB10	Data Output Bit 10
45	DB11	Data Output Bit 11
46	R7	Ref. Resistor Ladder Tap (7/16 V_{REF})
47	R9	Ref. Resistor Ladder Tap (9/16 V_{REF})
48	R5	Ref. Resistor Ladder Tap (5/16 V_{REF})
49	AGND	Analog Ground
50	V_{IN}	Analog Input
51	AV_{DD}	Analog Positive Supply
52	R8	Ref. Resistor Ladder Tap (8/16 V_{REF})

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 2 MHz (50% Duty Cycle), $V_{REF(+)}$ = 5.0 V, $V_{REF(-)}$ = AGND, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution			12		Bits	
Sampling Rate	FS		2		MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±3	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$	1.5		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT[2]						
Input Bandwidth (–3 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		20		ns	
Aperture Delay from Aperture Signal	t_{AP}		0		ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}		2.4		V	
Logical "0" Voltage	V_{IL}		0.8		V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE1}$, OE2, MINV, LINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	200	500		ns	Functional
Rise & Fall Time[7]	t_R, t_F		15		ns	Functional
"High" Time	t_{PWH}	100	220		ns	Functional
"Low" Time	t_{PWL}	100	220		ns	
Duty Cycle			50		%	
Serial Register Timing						
Shift Clock Period	t_{SC}		50		ns	
Shift Clock to Data Delay	t_{SD}		20		ns	
Minimum Pulse Width $\overline{PLOAD}$	t_S		50		ns	
Clock↑ to $\overline{PLOAD}$↓ For Valid D11	t_{CP}		0		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}		DV_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical "1" Source Current	I_{OH}		4		mA	V_{OH} = DV_{DD}-0.5
Logical "0" Voltage	V_{OL}		0.5		V	I_{LOAD} = 4 mA
Logical "0" Sink Current	I_{OL}		4		mA	V_{OL} = 0.5 V
Tristate Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		30		ns	
Data Enable Delay	t_{DEN}		20		ns	
Data Tristate Delay	t_{DHZ}		20		ns	
POWER SUPPLIES[8]						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		40	45	mA	
AC PARAMETERS[2]						
Signal Noise Ratio (N+D)	SINAD		66		dB	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

8 AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PQFP 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

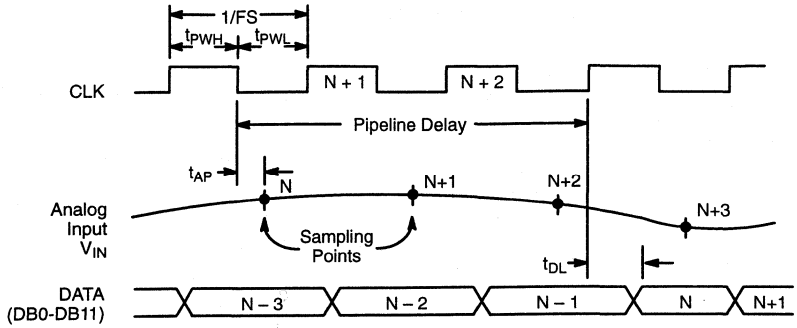


Figure 1. MP8790 Timing Diagram

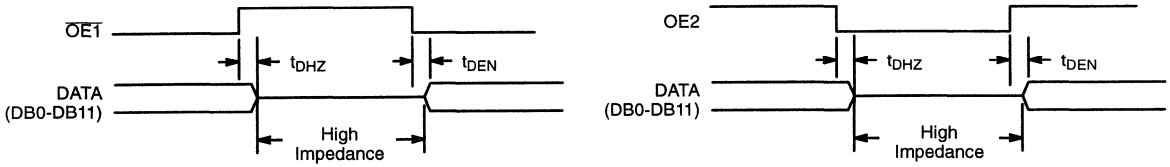
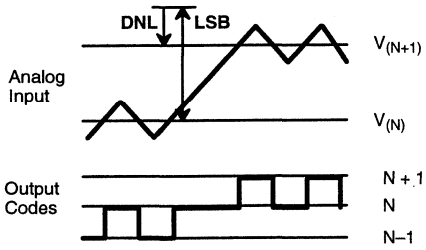


Figure 2. 3-State Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 1024

$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$

Figure 3. DNL Measurement

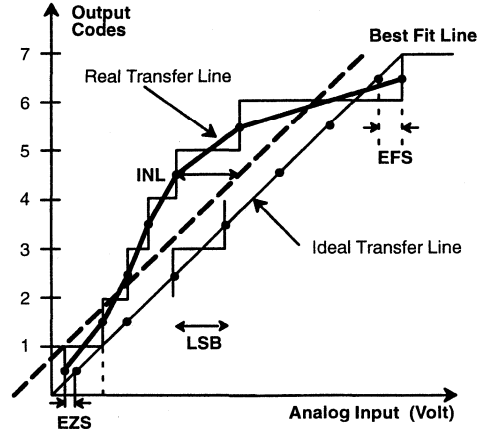


Figure 4. INL Error Calculation

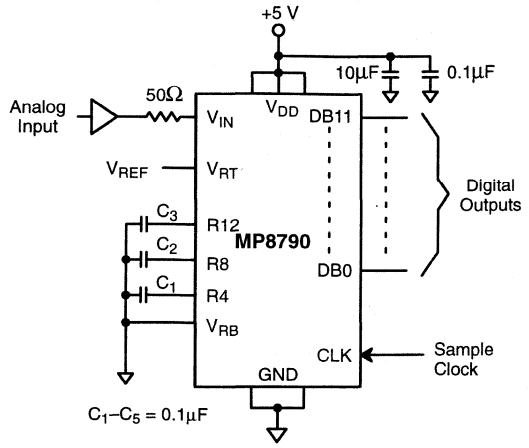


Figure 5. Typical Circuit Connections

OFW & UFW: Overflow & Underflow (Outputs)

These signals indicate when the Analog Input (V_{IN}) goes outside the V_{RB} to V_{RT} range. Both pins are normally at low logic levels. When $V_{IN} > V_{RT}$, OFW will go high and the data bits (DB0 – DB11) will show full scale (i.e. all 1's if MINV & LINV are low). When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0's if MINV & LINV are low).

$\overline{OE1}$ & OE2: Output Enable (inputs)

These signals control the 3-state drivers on the digital outputs DB0 – DB11, OFW and UFW. During normal operation, $\overline{OE1}$ should be held low and OE2 should be held high so that all outputs are enabled (NOTE: internal resistors will pull $\overline{OE1}$ and OE2 to these levels if they are not connected). When $\overline{OE1}$ is driven high, DB0 – DB11 goes into high impedances mode. When OE2 is driven low, DB0 – DB11, OFW and UFW all go into high impedance mode. These controls operate asynchronous to the clock and they only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. If possible, $\overline{OE1}$ should be in 3-state during Clock = 1 (PHASE = 1) to reduce digital noise coupling into A_{IN} during the sample time. Aperture provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

$\overline{OE1}$	OE2	DBO-DB9	OFW & UFW
0	1	enabled	enabled
1	1	3-state	enabled
X	0	3-state	3-state

PHASE Clock Polarity Control (input)

This signal controls the phase relationship between the signal applied at the CLK pin and the internal clock signals. When PHASE is high, V_{IN} is sampled at the high to low CLK transition and the digital data changes after a low to high CLK transition. When PHASE is low, V_{IN} is sampled at the low to high CLK transition and the digital data changes after a high to low CLK transition. See timing diagram *Figure 6.* PHASE has an internal pull up device.

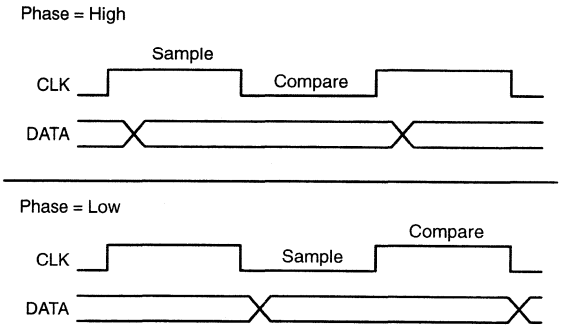


Figure 6. Clock Phase Relationship

SDO: Serial Data output

After the internal shift register is updated using the $\overline{PLOAD}$ signal, the SDO pin outputs the A/D result starting with the MSB (which appears just after the $\overline{PLOAD}$ strobe). Each bit is output on the rising edge of SCLK.

SCLK: Serial Data Port Clock

The SCLK controls the output of the serial port through SDO. SDO is updated on every rising edge of SCLK. The $\overline{PLOAD}$ signal will override the SCLK signal.

$\overline{PLOAD}$:

Serial data port shift register load: When $\overline{PLOAD}$ is low (i.e. level triggered not edge triggered) the current parallel data will be loaded into the shift register. $\overline{PLOAD}$ overrides SCLK. When $\overline{PLOAD}$ is high, the data can be shifted out through the SDO pin with SCLK.

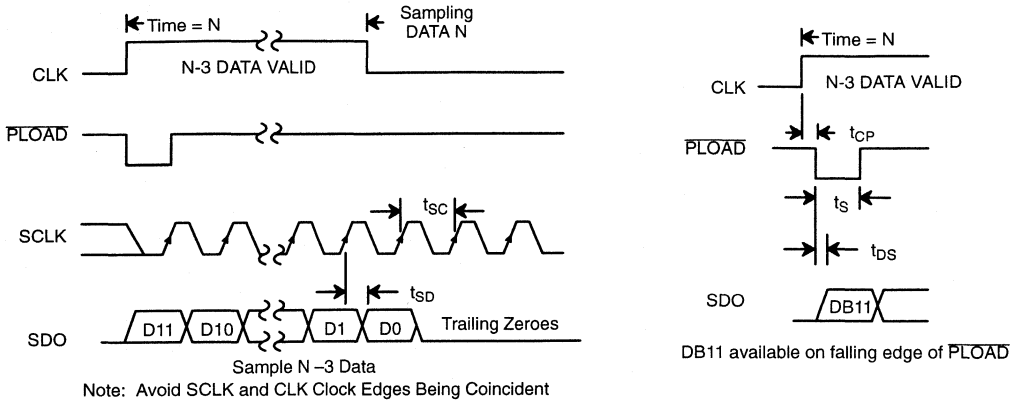


Figure 7. Serial Port Timing Chart
PHASE = 1

APERTURE: Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperture pin may also be used to control the $\overline{OE1}$ (outputs between 3-state and active mode). This will reduce the errors introduced by digital output coupling during the A_{IN} sample time.

MINV LINV	0 0	0 1	1 0	1 1
V_{RT}	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
	⋮	⋮	⋮	⋮
	100 . . . 01	111 . . . 10	000 . . . 01	011 . . . 10
V_{IN} mid scale	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
	⋮	⋮	⋮	⋮
V_{RB}	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

MINV & LINV: Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB11. Normally both pins are held low so the data is in straight binary format (all 0's when V_{IN}=V_{RB}; all 1's when V_{IN}=V_{RT}). If MINV is pulled high, then the MSB (DB11) will be inverted. If LINV is pulled high, then the LSBs (DB0 – DB10) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV & LINV are meant to be static digital signals. If they are to change during operation, they should only change when the CLK is low (assuming PHASE is high, if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV and LINV have internal pull down devices. Please see the simplified logic circuit *Figure 8.*

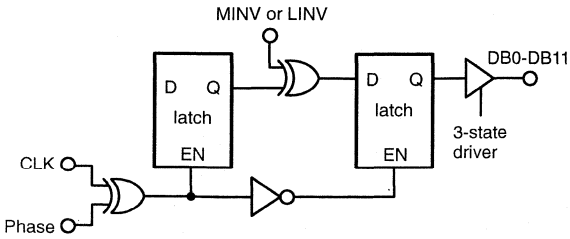


Figure 8. MINV, LINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *Figure 9.* shows an equivalent input circuit.

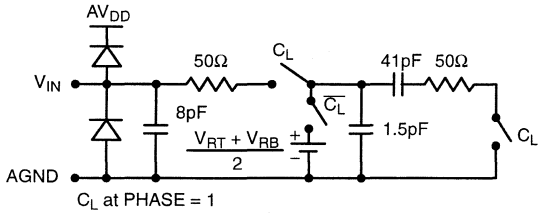


Figure 9. Equivalent Input Circuit

R1 thru R15: Reference Ladder Taps

These taps connect to every sixteenth point along the reference ladder; R1 is 1/16th up from V_{RB}, R7 is 15/16ths up from V_{RB} (or 1/16th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS}, this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. A 16 segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins. The internal interconnect resistance from the pin to the ladder is less than 3Ω for the even numbered taps, (i.e. R2,R4,R6, etc.) and is approximately 10Ω for the odd numbered taps.

Alternating the transfer curve may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

For Log shapes, the MP8790 is ideal since it provides 16 segments.

0.8 V maximum per tap is recommended for applications above 85°C. Up to 1.6 V is allowed for applications under 85°C.

APPLICATION NOTES

V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

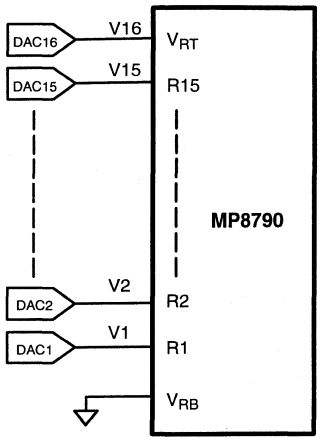
AGND & DGND pins are connected internally through the P– substrate. DC voltage differences between AGND and DGND pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

At least three of the reference tap pins (R4, R8, R12) should be decoupled with 0.1µF to 1µF capacitors. This will help stabilize the internal reference voltages thus reducing any INL errors.

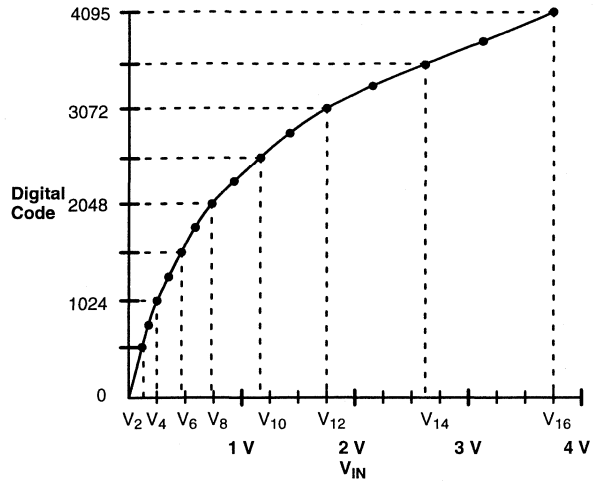
The reference tap pins (R1-R16) can be used to create piecewise-linear transfer functions. By forcing custom voltages on these pins, a 16 segment transfer function can be made. See *Figure 10. and Figure 11.*



DAC MP7642

Only the Ladder detail shown.

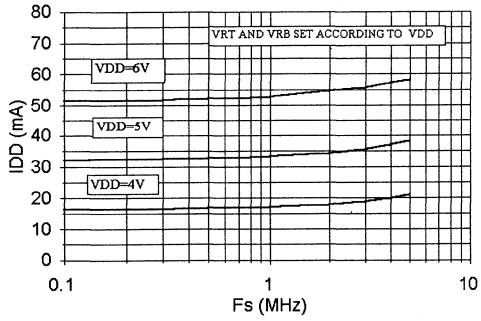
Figure 10. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function



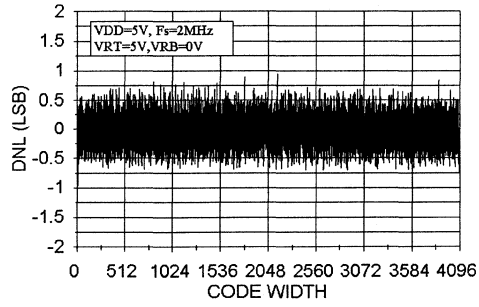
Even Voltages Shown

Figure 11. Example of a Piecewise Linear Transfer Function

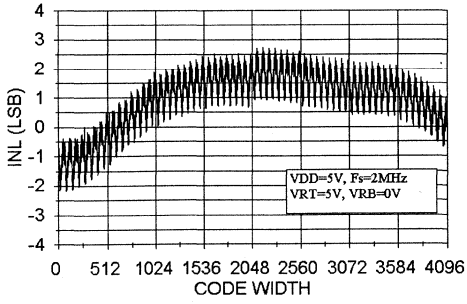
PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. F_S



Graph 2. DNL Error Plot



Graph 3. INL Error Plot

MP8791

CMOS, 2 MSPS, 12-Bit
Analog-to-Digital Converter
with Parallel Logic Interface Port

FEATURES

- **12-Bit ADC with DNL = ±1 LSB, INL = ±2 LSB**
- **SNR > 60 dB**
- **Sampling Frequency ≤ 2 MHz**
- **Internal Track and Hold: Input –3 dB Frequency = 10 MHz**
- **Single 5 V Supply**
- **Rail-to-Rail Input Range**
- **V_{REF} Range: 1.5 V to V_{DD}**
- **CMOS Low Power: 175 mW (typ)**
- **1/4, 1/2 and 3/4 Scale Reference Resistor Taps**
- **Three-State Outputs**
- **Binary and Two's Complement Digital Output Mode**
- **Latch-Up Proof**
- **Serial Version: MP87092**
- **3 V Version: MP87L91**

APPLICATIONS

- **Instrumentation**
- **DAS**
- **Radar**
- **Medical Imaging**
- **Ultrasound**
- **Broadcast and Studio Video**
- **Magnetic Resonance Signal Acquisition**
- **Digital Oscilloscopes**
- **Spectrum Analysis**

3

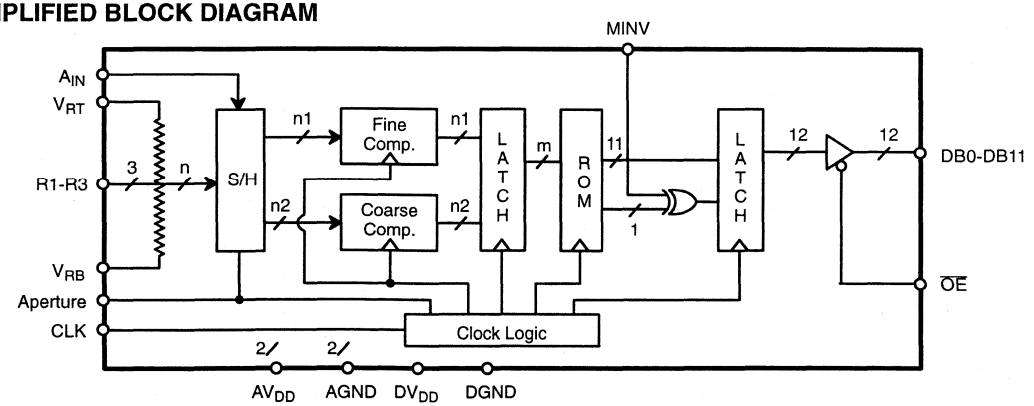
GENERAL DESCRIPTION

The MP8791 is a 2 MSPS 12-bit subranging Analog-to-Digital Converter with DNL = ±1 LSB and INL = ±2 LSB. The MP8791 contains an internal track and hold and an analog input bandwidth of 10 MHz.

The MP8791 operates with a single 5 V supply while consuming less than 200 mW of power (typical). Separate pins for reference ladder terminals and power supplies allow flexibility for various A_{IN}, ΔV_{REF}, and power supply ranges.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. The digital output port is also equipped with a 3-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment, linearity, and speed enhancement can be accommodated.

SIMPLIFIED BLOCK DIAGRAM

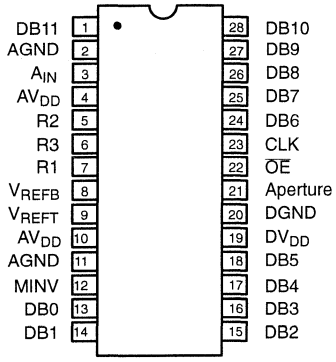


ORDERING INFORMATION

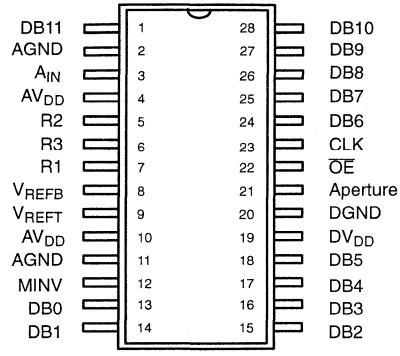
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	MP8791AN	±1	2 1/2
SOIC	–40 to +85°C	MP8791AS	±1	2 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28
Contact Factory for Availability of Smaller PDIP Packages



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB11	Data Output Bit 11 (MSB)
2	AGND	Analog Ground
3	A_{IN}	Analog Input
4	AV_{DD}	Analog Positive Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{REFB}	Negative Reference
9	V_{REFT}	Positive Reference
10	AV_{DD}	Analog Positive Supply
11	AGND	Analog Ground
12	MINV	Invert MSB (Active High)
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1

PIN NO.	NAME	DESCRIPTION
15	DB2	Data Output Bit 2
16	DB3	Data Output Bit 3
17	DB4	Data Output Bit 4
18	DB5	Data Output Bit 5
19	DV_{DD}	Digital Positive Supply
20	DGND	Digital Negative Supply
21	Aperture	Delayed Clock, indicates sample point
22	$\overline{OE}$	Output Enable (Active Low)
23	CLK	Clock
24	DB6	Data Output Bit 6
25	DB7	Data Output Bit 7
26	DB8	Data Output Bit 8
27	DB9	Data Output Bit 9
28	DB10	Data Output Bit 10

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 2 MHz (50% Duty Cycle), $V_{REF(+)}$ = 5.0 V, $V_{REF(-)}$ = AGND, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution			12		Bits	
Sampling Rate	FS			2	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±3	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$	1.5		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Bandwidth (–3 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		35	40	ns	
Aperture Delay from Aperture Signal	t_{AP}		0		ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}		2.4		V	
Logical "0" Voltage	V_{IL}		0.8		V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE}$, MINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	200	500		ns	Functional
Rise & Fall Time[7]	t_R, t_F		15		ns	Functional
"High" Time	t_{PWH}	100	220		ns	Functional
"Low" Time	t_{PWL}	100	220		ns	Functional
Duty Cycle			50		%	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}	28	30	35	ns	
Data Enable Delay	t_{DEN}		25	30	ns	
Data 3-state Delay	t_{DHZ}		25	30	ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
POWER SUPPLIES[8] (Tmin to Tmax)						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}			45	mA	
AC PARAMETERS						
Signal Noise Ratio (N+D)	SNR		66		dB	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

8 AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PQFP 450mW
Derates above 75°C ..... 6mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

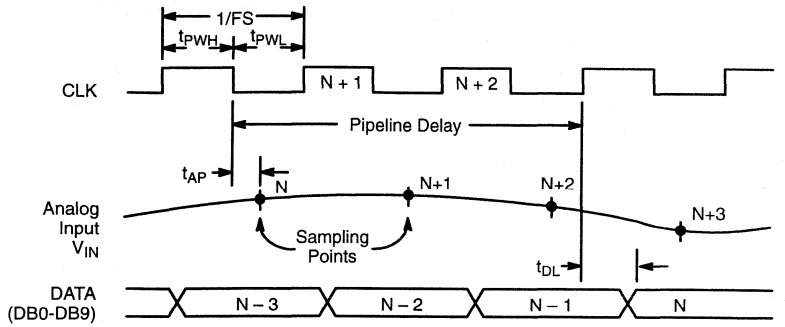


Figure 1. Timing Diagram

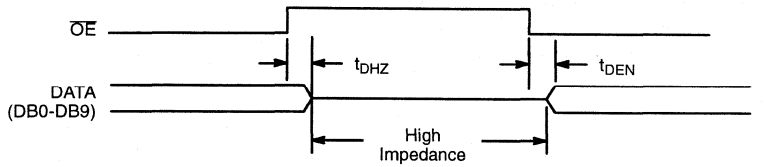


Figure 2. 3-State Timing Diagram

OVERVIEW OF THE MP8791 PINS & OPERATION NOTES :

$\overline{OE}$: Output Enable (Input)

This signal controls the 3-state drivers on the digital outputs DB0 - DB11. During normal operation, $\overline{OE}$ should be held low so that all outputs are enabled (NOTE: an internal resistor will pull $\overline{OE}$ to this level if it is not connected). When $\overline{OE}$ is driven high, DB0 - DB11 goes into high impedance mode. This control operates asynchronously to the clock and only controls the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. If possible, $\overline{OE}$ should be in 3-state during Clock = 1 to reduce digital noise coupling into A_{IN} during the sample time. Aperture provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

APERTURE: Aperture Delay Sync (Output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperture pin may also be used to control the $\overline{OE}$ (outputs between 3-state and active mode). This will reduce the errors introduced by digital output coupling during the A_{IN} sample time.

MINV: Digital Output Format (Input)

This signal controls the format of the digital output data bits DB0 – DB11. Normally it is held low so the data is in straight binary format (all 0's when $V_{IN} = V_{RB}$; all 1's when $V_{IN} = V_{RT}$). If MINV is pulled high then the MSB (DB11) will be inverted.

MINV is meant to be a static digital signal. If it is to change during operation, it should only change when the CLK is low. Changing MINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV has an internal pull down device. This function is not available in the engineering sidebraze samples. For these samples, this pin must be tied to GND.

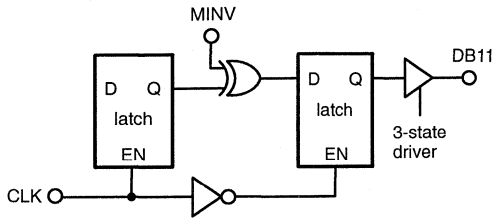


Figure 3. MINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *Figure 4.* shows an equivalent input circuit.

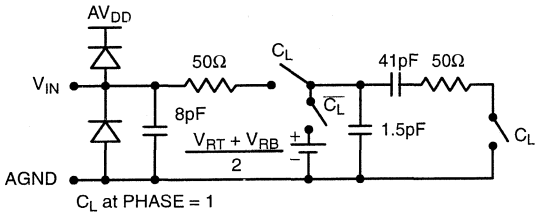


Figure 4. Equivalent Input Circuit

R1, R2, R3: Reference Ladder Taps

These taps connect to every 1/4 point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS}; this helps reduce the INL errors by stabilizing the reference ladder voltages.

These taps can also be used to alter the transfer curve of the ADC. A 4-segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

This may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

The internal interconnect resistance from each of the t_{AP} pins to the ladder is less than 3Ω.

1.6V maximum per tap is recommended for applications above 85°C. Up to 3.2V is allowed for applications under 85°C.

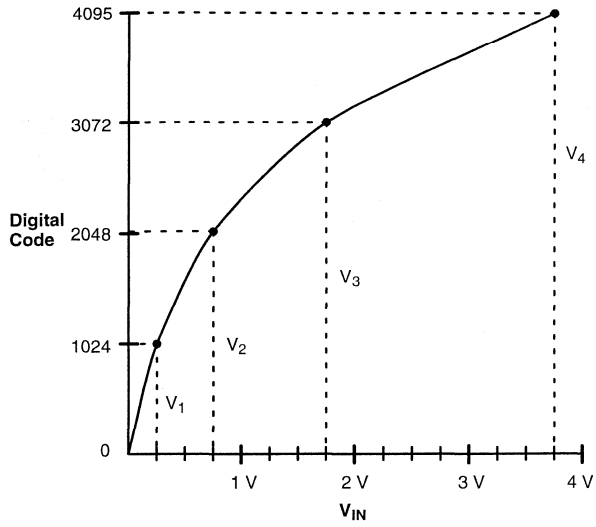
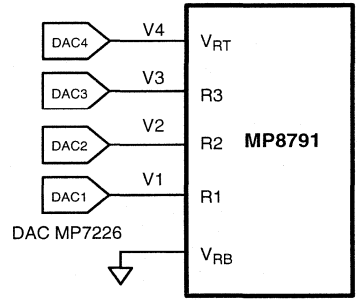


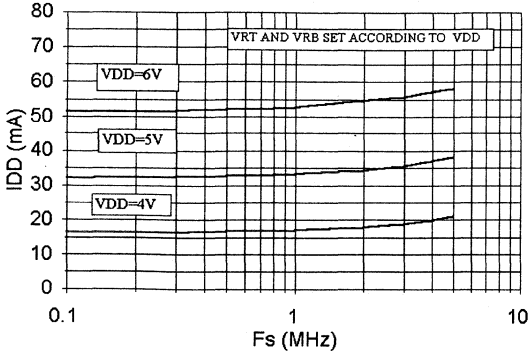
Figure 5. A Piecewise Linear Transfer Function



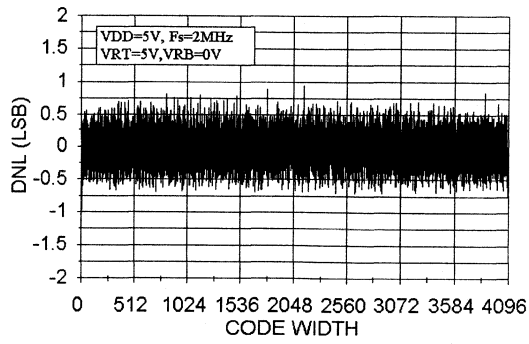
Only the Ladder detail shown.

Figure 6. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

PERFORMANCE CHARACTERISTICS

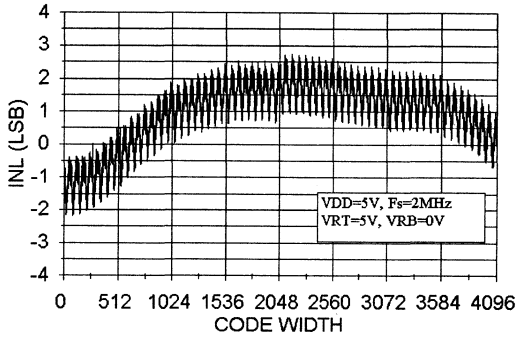


Graph 1. I_{DD} vs. F_S



Graph 2. DNL Error Plot

3



Graph 3. INL Error Plot

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MP8795

CMOS
1 MSPS, Very Low Power, 10-Bit
Analog-to-Digital Converter

FEATURES

- **Power Down; Lower Consumption – 3 mW (typ)**
- **10-Bit Resolution**
- **Sampling Rates from <1 kHz to 1.5 MHz**
- **DNL better than 1/2 LSB (typ) up to 1.5 MHz**
- **Very Low Power CMOS - 30 mW (typ)**
- **Input Range between GND and V_{DD}**
- **No S/H Required for Analog Signals less than 100 kHz**
- **No S/H Required for CCD Signals less than 1.5 MHz**
- **Single Power Supply (4 to 6 Volts)**
- **Latch-Up Free**
- **High ESD Protection: 4000 Volts Minimum**
- **3 V Version: MP87L95**
- **20 Pin Package: MP8796**

BENEFITS

- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer Can Adapt Input Range & Scaling**

APPLICATIONS

- **µP/DSP Interface and Control Applications**
- **High Resolution Imaging – Scanners, Copiers, Facsimile**
- **Radar Pulse Analysis**
- **Low Power A/D Applications**

3

GENERAL DESCRIPTION

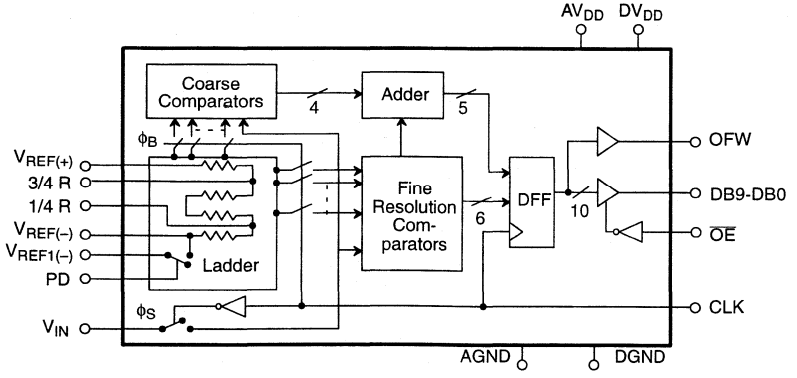
The MP8795 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter that operates over a wide range of input and sampling conditions. The MP8795 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 1.5 MHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 1.5 MHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP8795 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

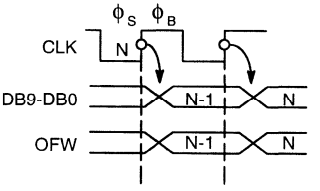
Scaled reference resistor taps 1/4 R and 3/4 R allow for customizing the transfer curve. Digital outputs offer 3-state operation and all digital pins are CMOS and TTL compatible.

The MP8795 uses a two step technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



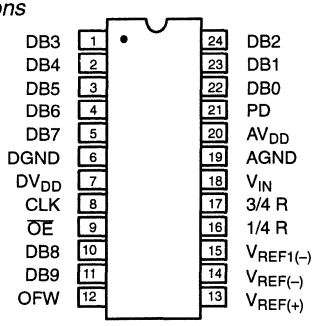


ORDERING INFORMATION

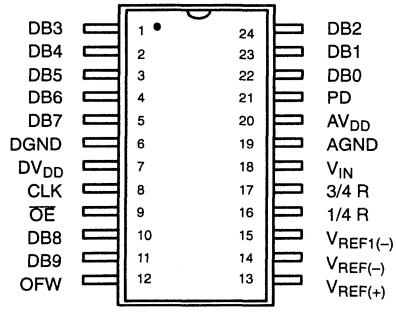
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP8795AN	±1	2
SOIC	–40 to +85°C	MP8795AS	±1	2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(-)}$	Lower Reference Voltage
15	$V_{REF1(-)}$	Lower Reference Voltage
16	1/4 R	Reference Ladder Tap @ 1/4 FS
17	3/4 R	Reference Ladder Tap @ 3/4 FS
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	PD	Power Down
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 1 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.6, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		1	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL		±3/4	±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+1.00		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance[1]			12		Ω	
Ladder Switch Off Leakage[1]	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	1 LSB Error
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, $\overline{OE}$ (Internal Res to DGND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	500			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	Functional
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}	0		±5	µA	V_{OUT} = 0 to V_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30	35	ns	
Data Valid Delay[1]	t_{DL}		35	45	ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C_{OUT}=15 pF
Data Enable Delay[1]	t_{DEN}		25	30	ns	
Data 3-state Delay[1]	t_{DHZ}		15	30	ns	
Clock to PD Set-up Time[1]	t_{CLKS1}			400	ns	
Clock to PD Hold Time[1]	t_{CLKH1}			600	ns	
Power Down Delay[1]	t_{PD}			300	ns	
Power Up Delay[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{DDOWN}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

NOTES:

1 Guaranteed. Not tested.

2 Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).

3 See V_{IN} input equivalent circuit (*see Figure 9.*).

4 Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.

5 Specified values guarantee functional device. Refer to other parameters for accuracy.

6 System can clock MP8795 with any duty cycle as long as all timing conditions are met.

7 Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.

8 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

CDIP, PDIP, SOIC 1000mW

Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

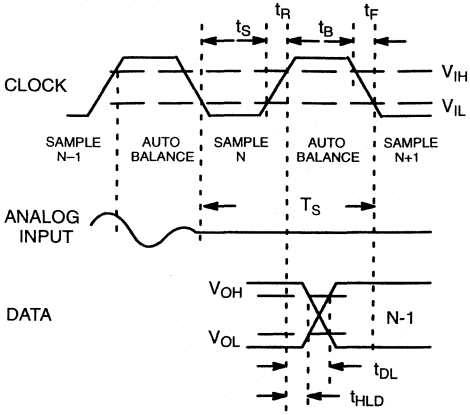


Figure 1. MP8795 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP8795 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

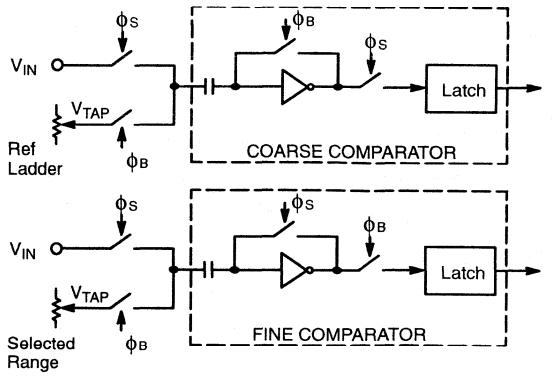


Figure 2. MP8795 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

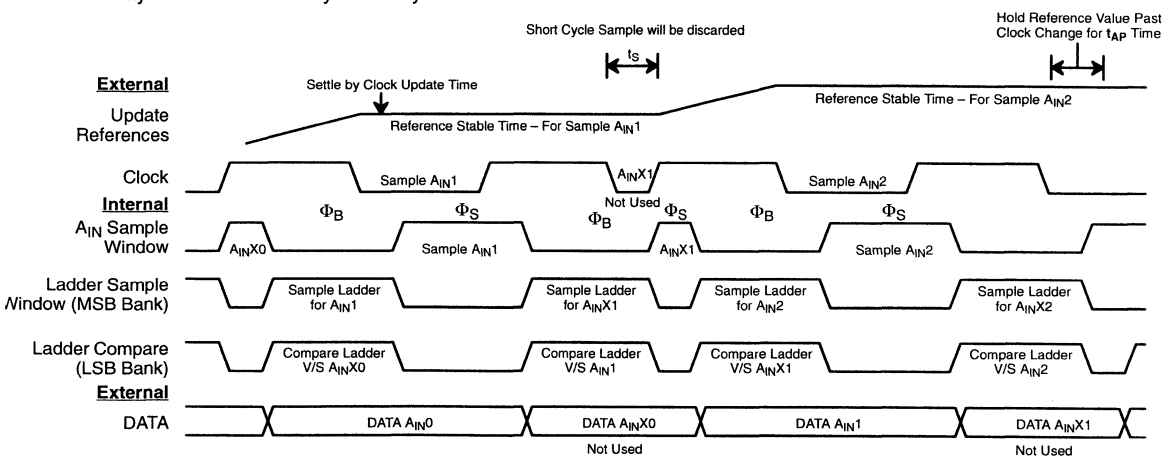


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

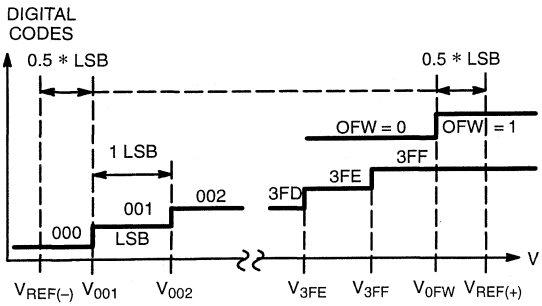


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(-)} - 1.5 * LSB$

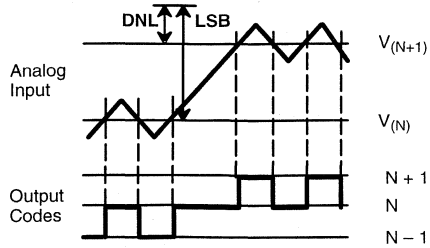
$LSB = V_{REF} / 1024 = (V_{3FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter, the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If $V_{REF} = 4.608$ V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

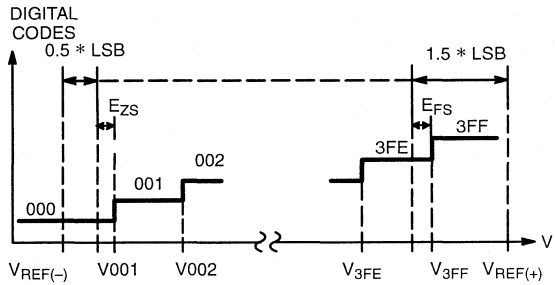


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition, the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSBs relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

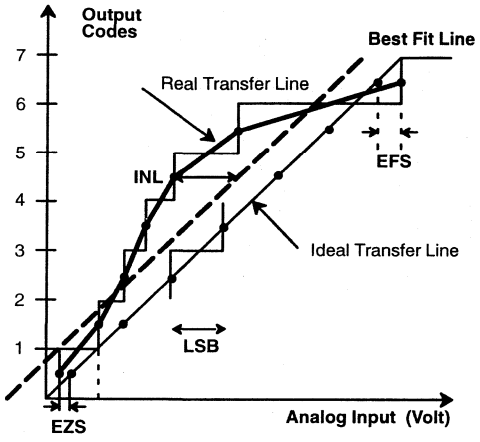


Figure 7. INL Error Calculation

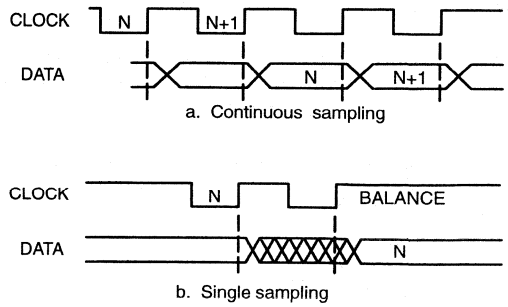


Figure 8. Relationship of Data to Clock

Analog Input

The MP8795 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP8795's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

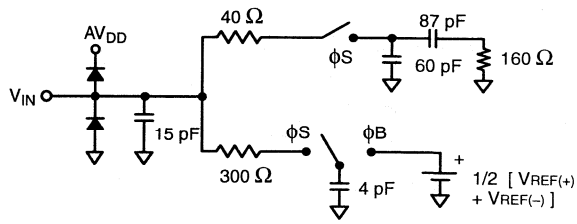


Figure 9. Analog Input Equivalent Circuit

Clock and Conversion Timing

A system will clock the MP8795 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP8795 in balance and ready to sample the analog input.

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE}$ controls the output buffers in an asynchronous mode.

$\overline{OE}$	OFW	DB9 – DB0
1	Valid	High Z
0	Valid	Valid

Table 2. Output Enable Logic

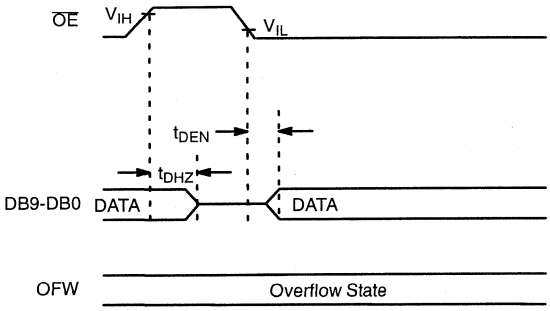


Figure 10. Output Enable/Disable Timing Diagram

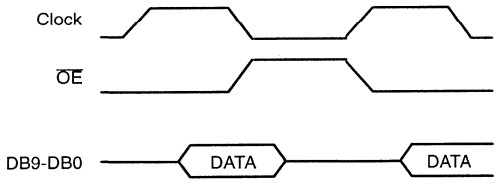


Figure 11. Preferred Output Control

Figure 11. shows the preferred output control where $\overline{OE}$ and clock are opposite phase. This provides a quiet time at the end of the A_{IN} sample phase.

The functional equivalent of the MP8795 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

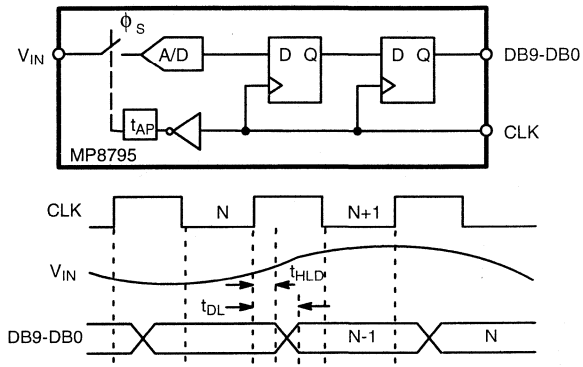


Figure 12. MP8795 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

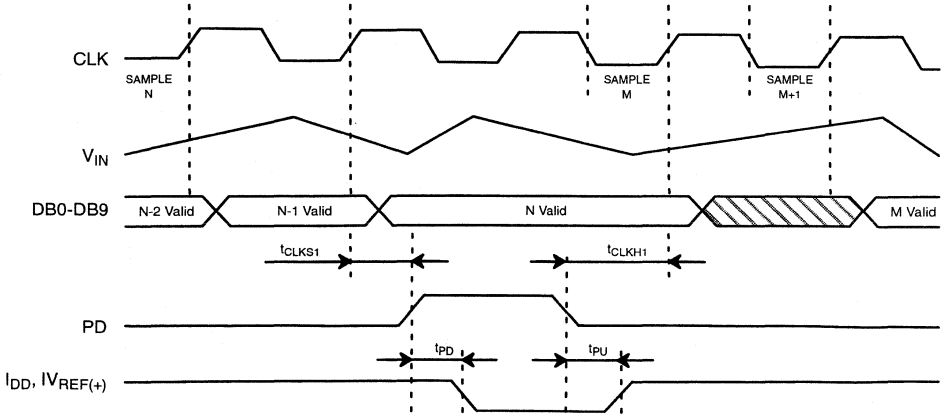


Figure 13. Power Down Timing Diagram

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance cap
R_T = Clock Transmission Line Termination

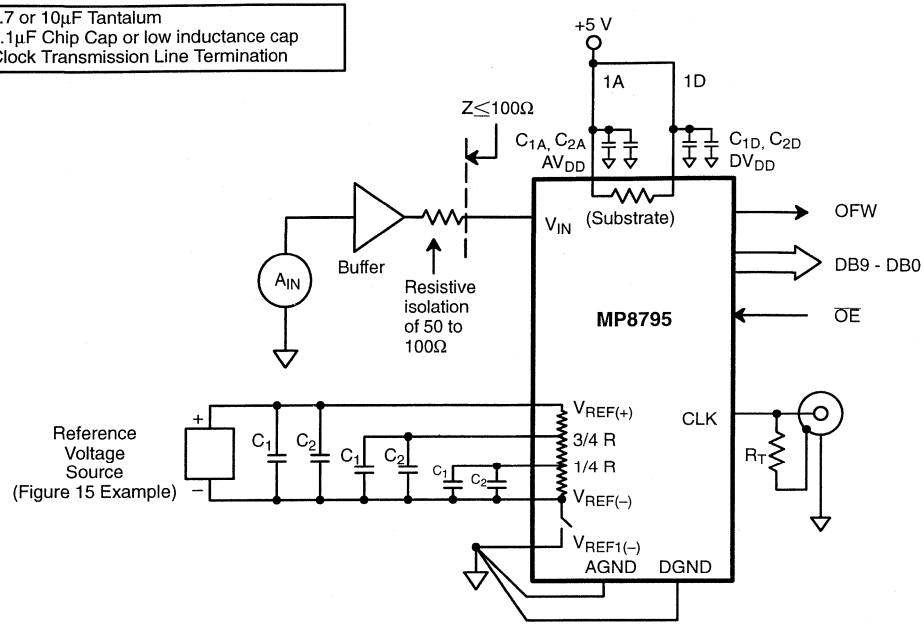


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP8795.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP8795 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP8795. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP8795.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP8795 should be connected to AV_{DD} next to the MP8795.
8. DV_{DD} and AV_{DD} are connected inside the MP8795 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

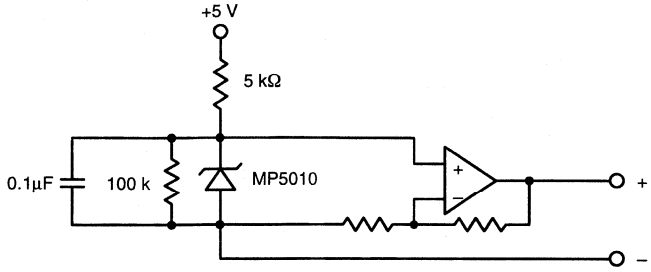
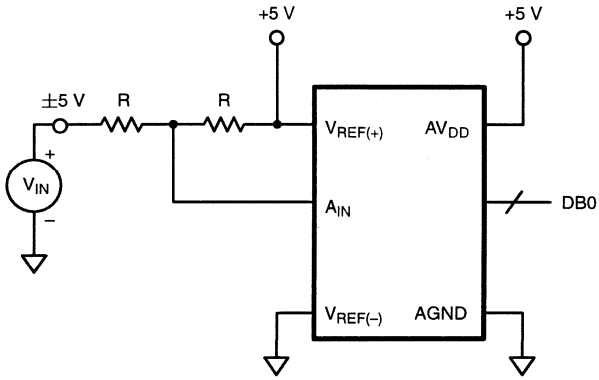


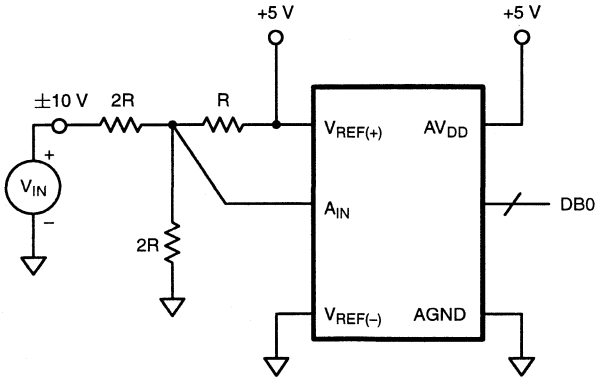
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

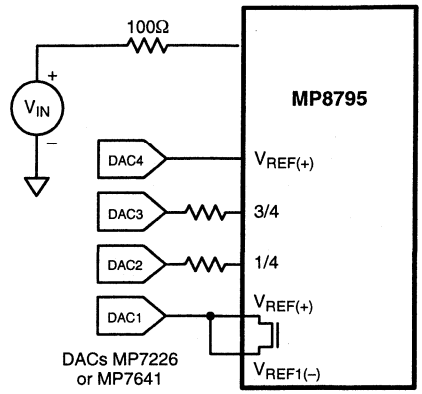
Figure 16. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 17. ±10 V Analog Input

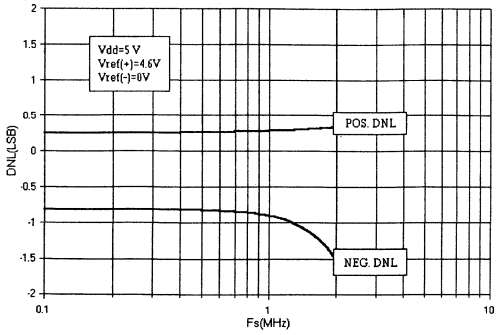


@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.

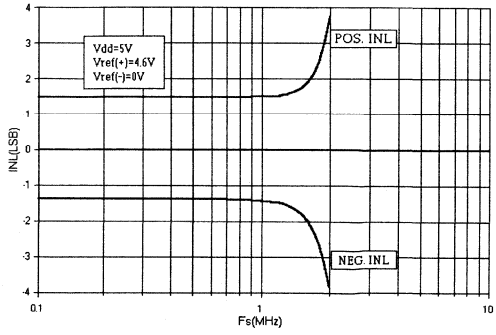
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/4 and 3/4 TAP.)

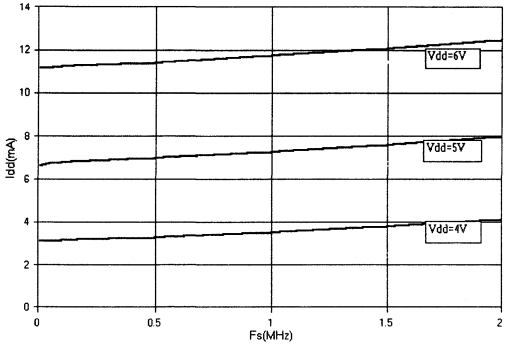
PERFORMANCE CHARACTERISTICS



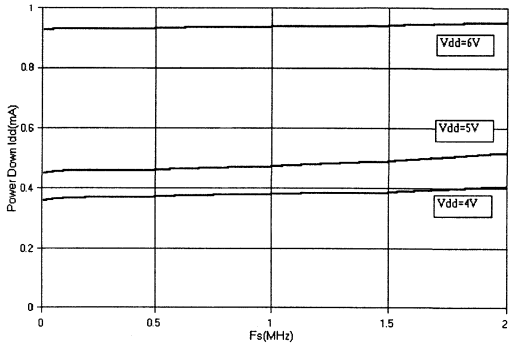
Graph 1. DNL vs. Sampling Frequency



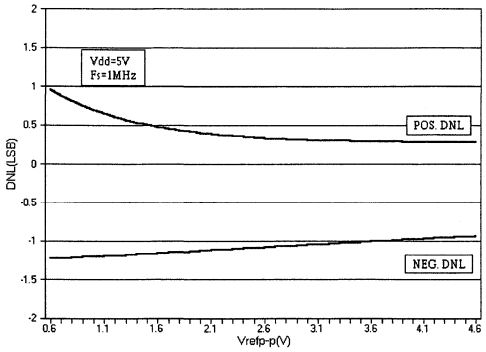
Graph 2. INL vs. Sampling Frequency



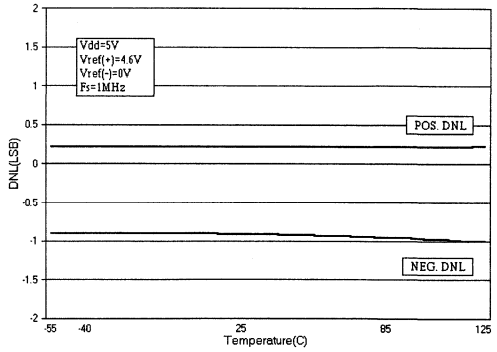
Graph 3. Supply Current vs. Sampling Frequency



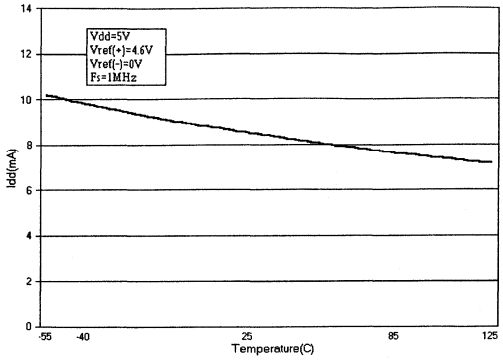
Graph 4. Power Down Current vs. Sampling Frequency



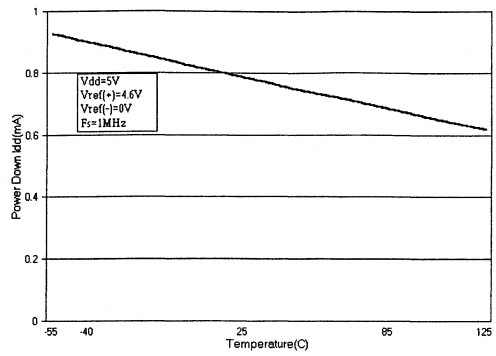
Graph 5. DNL vs. Reference Voltage



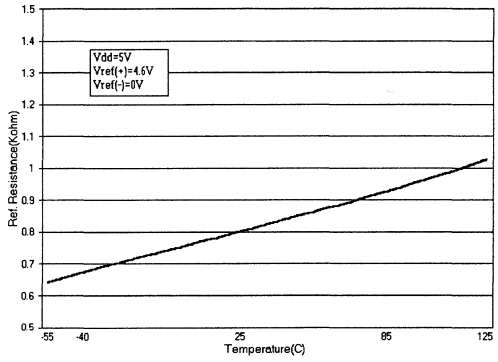
Graph 6. DNL vs. Temperature



Graph 7. Supply Current vs. Temperature



Graph 8. Power Down Current vs. Temperature



Graph 9. Reference Resistance vs. Temperature

MP8796

CMOS
1 MSPS, Very Low Power 10-Bit
Analog-to-Digital Converter

EXAR

FEATURES

- 10-Bit Resolution
- Sampling Rates from <1 kHz to 1.5 MHz
- DNL better than 1/2 LSB (typ) up to 1.5 MHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 1.5 MHz
- Single Power Supply (4 to 6 Volts)
- Latch-Up Free
- High ESD Protection: 4000 Volts Minimum
- 20 Pin SOIC Package Available

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- High Resolution Imaging – Scanners, Copiers, Facsimile
- Radar Pulse Analysis
- Low Power A/D Applications

3

GENERAL DESCRIPTION

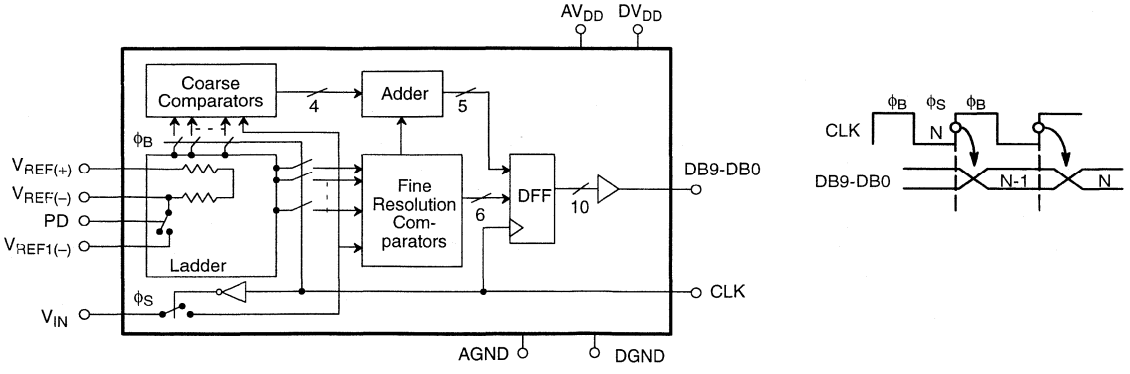
The MP8796 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter that operates over a wide range of input and sampling conditions. The MP8796 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 1.5 MHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 1.5 MHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP8796 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

All digital pins are CMOS and TTL compatible.

The MP8796 uses a two step technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

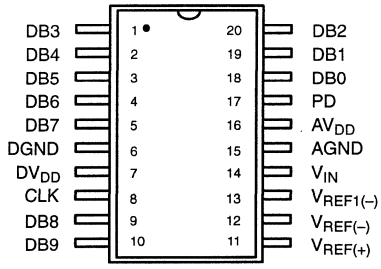


ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP8796AS	±1	2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin SOIC (Jedec, 0.300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	DataOutput Bit 4
3	DB5	DataOutput Bit 5
4	DB6	DataOutput Bit 6
5	DB7	DataOutput Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	DB8	DataOutput Bit 8
10	DB9	DataOutput Bit 9 (MSB)

PIN NO.	NAME	DESCRIPTION
11	$V_{REF(+)}$	Upper Reference Voltage
12	$V_{REF(-)}$	Lower Reference Voltage
13	$V_{REF1(-)}$	Lower Reference Voltage
14	V_{IN}	Analog Signal Input
15	AGND	Analog Ground
16	AV_{DD}	Analog V_{DD}
17	PD	Power Down
18	DB0	Data Output Bit 0 (LSB)
19	DB1	Data Output Bit 1
20	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S =$ 1 MHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)} = AGND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		1	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL		±3/4	±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+1.00		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
DYNAMIC ACCURACY[1]						Histogram Test
Differential Non-Linearity	DNL		±1/2		LSB	F_{IN} = 70 kHz
	DNL		±1		LSB	F_{IN} = 100 kHz
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance			12		Ω	
Ladder Switch Off Leakage	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	1 LSB Error
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, (Internal Res to DGND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	500			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	Functional

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Data Valid Delay[1]	t_{DL}		35	45	ns	
Clock to PD Set-up Time[1]	t_{CLKS1}			400	ns	
Clock to PD Hold Time[1]	t_{CLKH1}			600	ns	
Power Down Delay[1]	t_{PD}			300	ns	
Power Up Delay[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{DDOWN}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

NOTES:

1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP8796 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

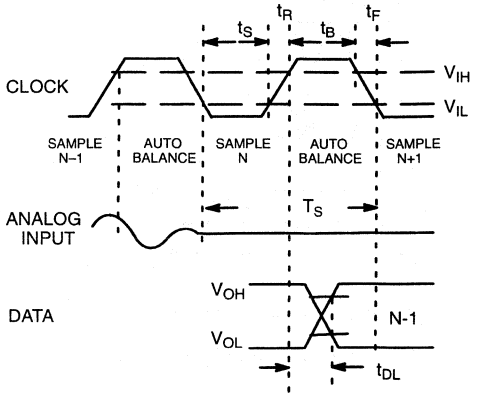


Figure 1. MP8796 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP8796 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 6.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

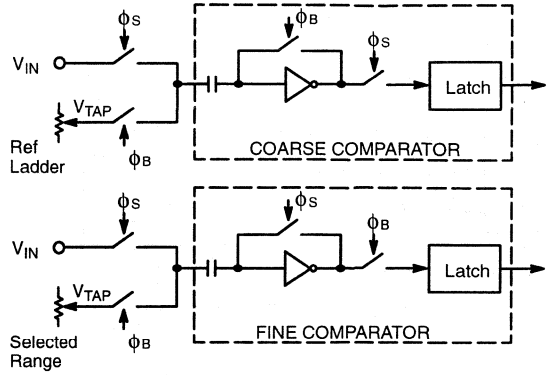


Figure 2. MP8796 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

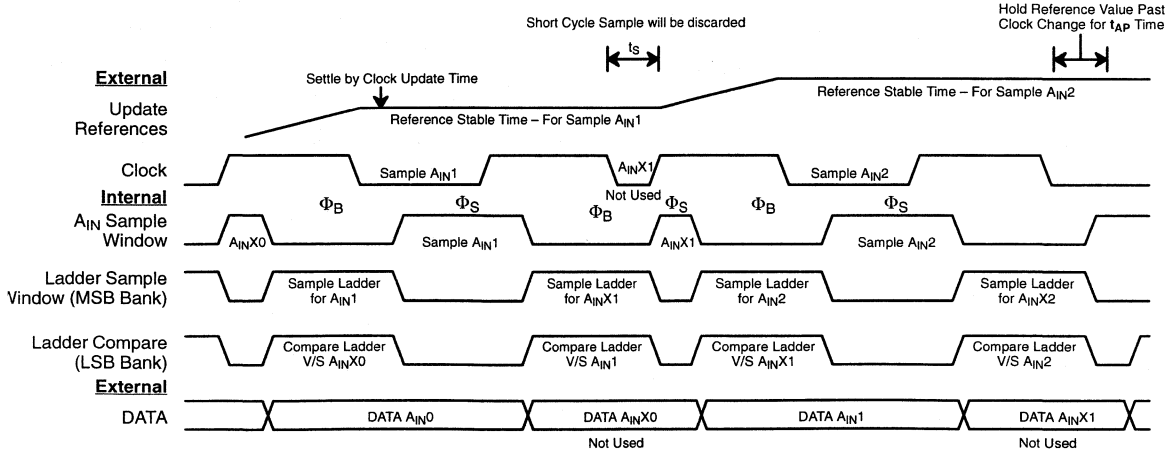


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

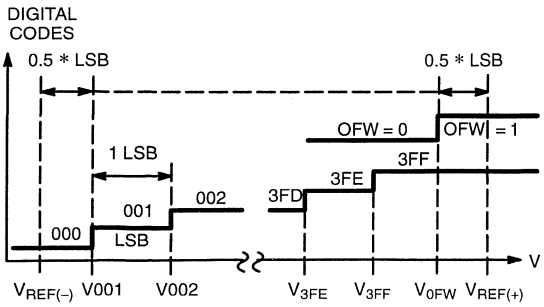


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(-)} - 1.5 * LSB$

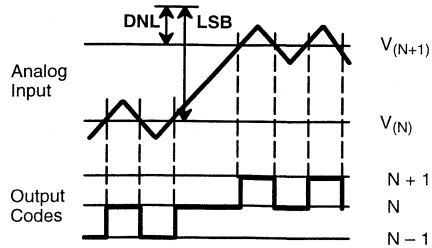
$LSB = V_{REF} / 1024 = (V_{3FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = V001 – [$V_{REF(-)}$ + 0.5 * LSB]

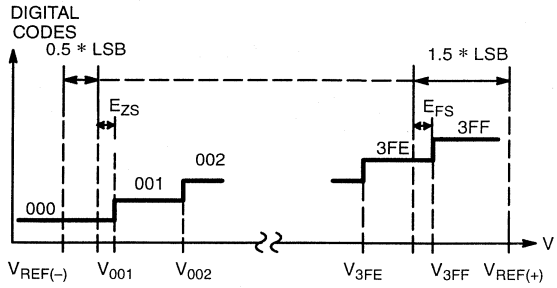


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the best fit line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSBs relative to the Ideal Line would be ±1.5 LSB's relative to the best fit line.

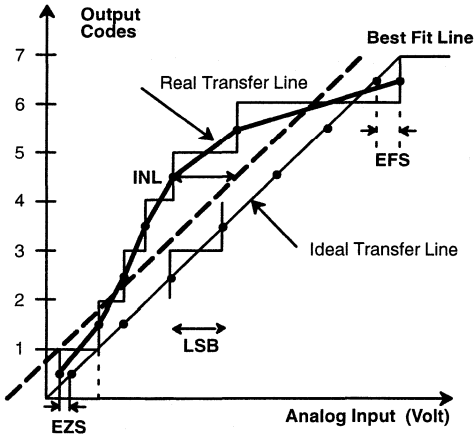


Figure 7. INL Error Calculation

Clock and Conversion Timing

A system will clock the MP8796 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP8796 in balance and ready to sample the analog input.

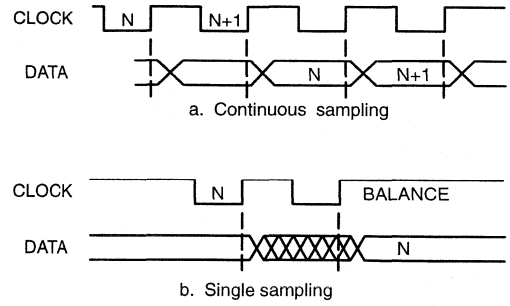


Figure 8. Relationship of Data to Clock

Analog Input

The MP8796 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP8796's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

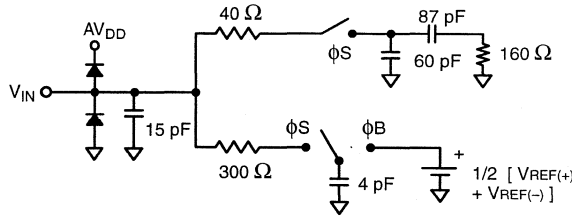


Figure 9. Analog Input Equivalent Circuit

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP8796 (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP} and t_{DL} are specified in the Electrical Characteristics table.

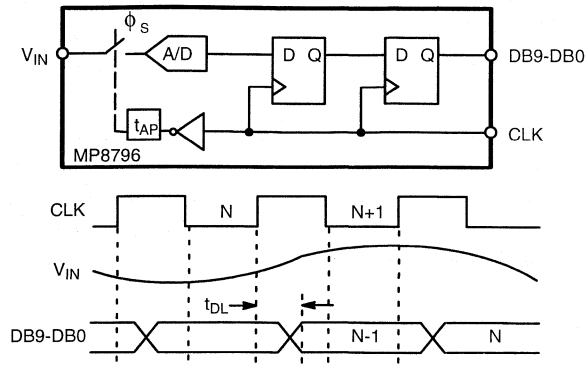


Figure 10. MP8796 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

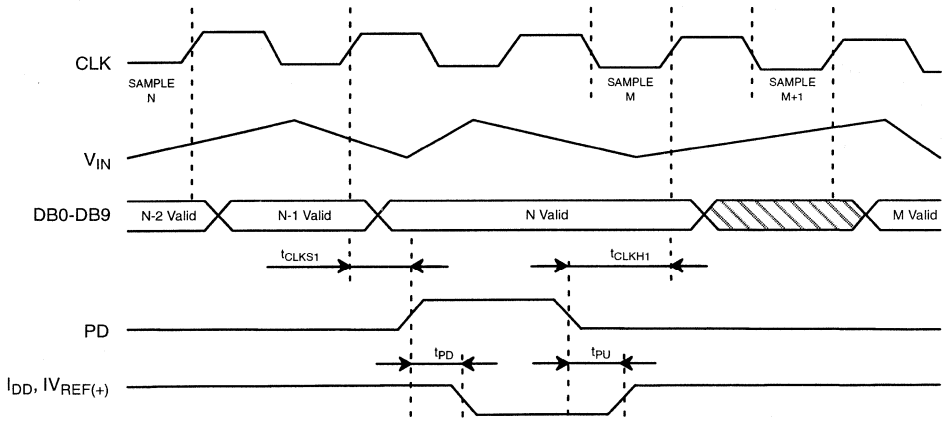


Figure 11. Power Down Timing Diagram

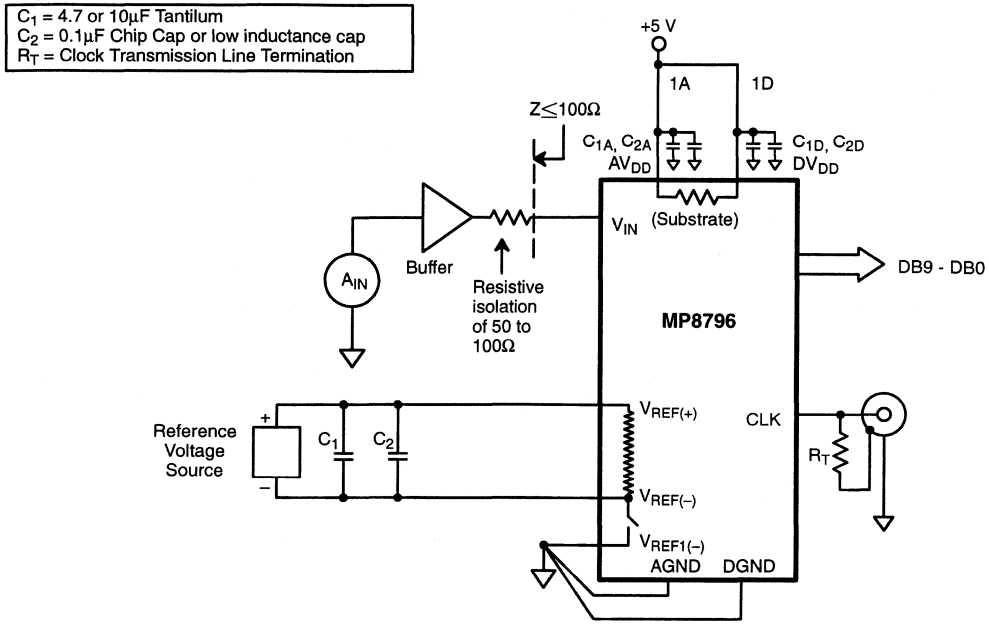


Figure 12. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP8796.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP8796 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP8796. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP8796.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP8796 should be connected to AV_{DD} next to the MP8796.
8. DV_{DD} and AV_{DD} are connected inside the MP8796 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

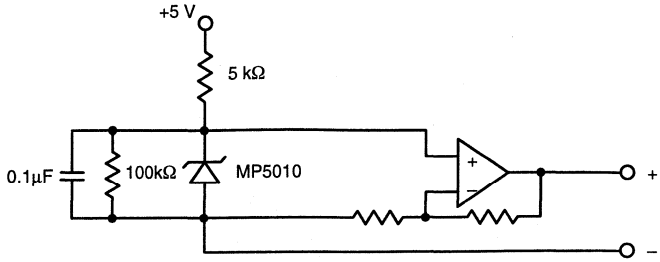
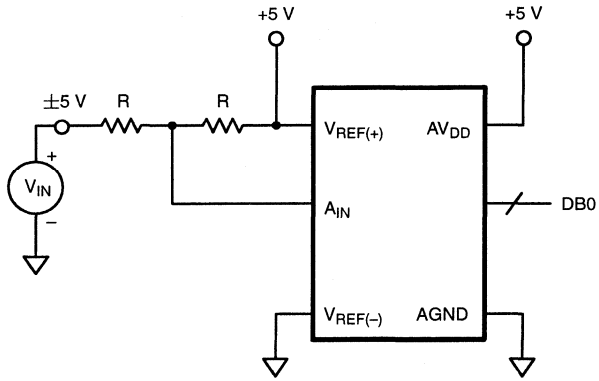


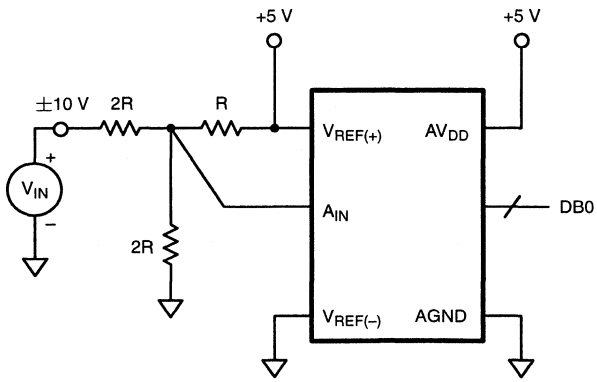
Figure 13. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

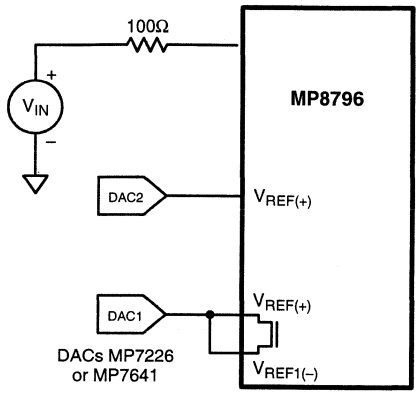
Figure 14. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

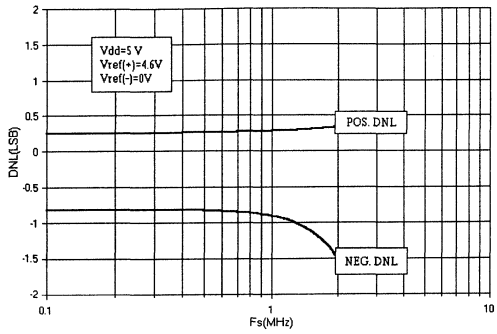
Figure 15. ±10 V Analog Input



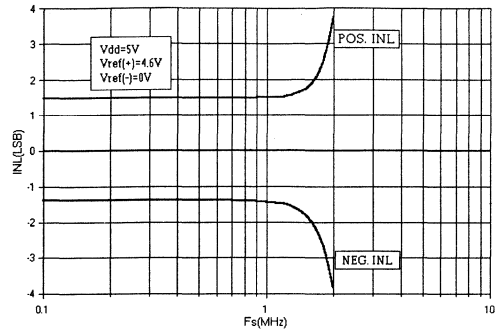
@ Power Down write values to DAC 1 = DAC 2 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

Figure 16. A/D Ladder with Programmed Control

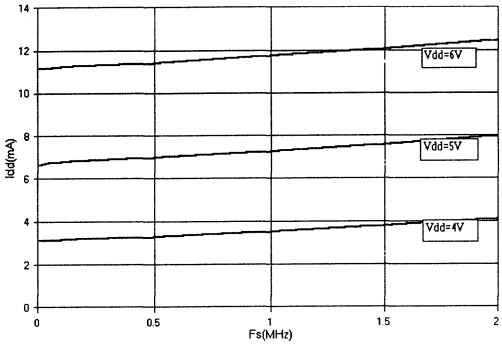
PERFORMANCE CHARACTERISTICS



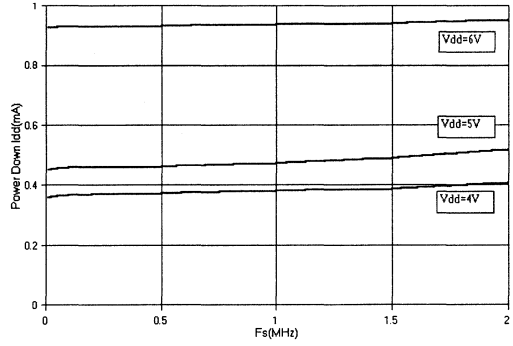
Graph 1. DNL vs. Sampling Frequency



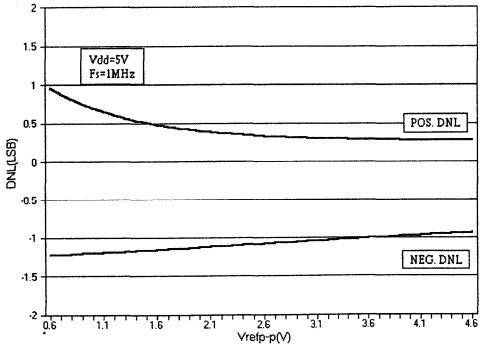
Graph 2. INL vs. Sampling Frequency



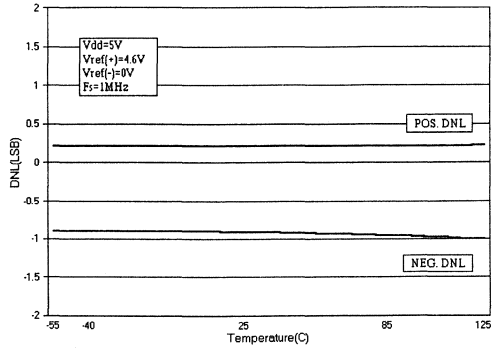
Graph 3. Supply Current vs. Sampling Frequency



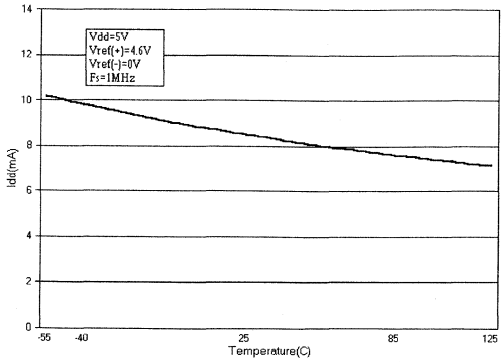
Graph 4. Power Down Current vs. Sampling Frequency



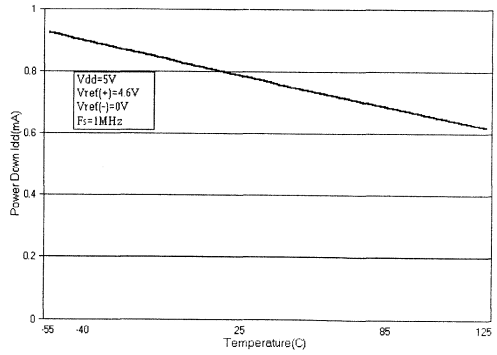
Graph 5. DNL vs. Reference Voltage



Graph 6. DNL vs. Temperature

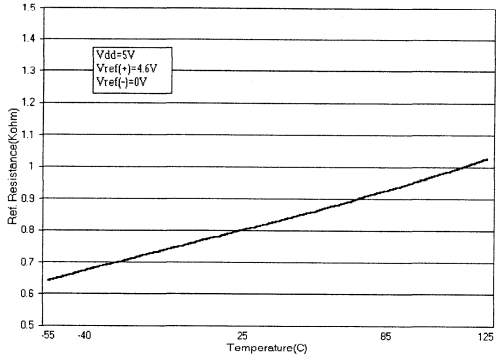


Graph 7. Supply Current vs. Temperature



Graph 8. Power Down Current vs. Temperature

3



Graph 9. Reference Resistance vs. Temperature

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MP8798

CMOS
Very Low Power, 1 MSPS 10-Bit
Analog-to-Digital Converter with 4-Channel Mux

FEATURES

- 10-Bit Resolution
- 4-Channel Mux
- Sampling Rates from <1 kHz to 1 MHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 1 MHz
- Single Power Supply (4 to 6 Volts)
- Latch-Up Free
- High ESD Protection: 4000 Volts Minimum
- 3 V Version: MP87L98

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- High Resolution Imaging – Scanners & Copiers
- Wireless Digital Communications
- Multiplexed Data Acquisition

3

GENERAL DESCRIPTION

The MP8798 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with 4-channel mux that operates over a wide range of input and sampling conditions. The MP8798 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 1 MHz. The elimination of the S/H, requirements, very low power, and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 1 MHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP8798 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap 1/2 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

The MP8798 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

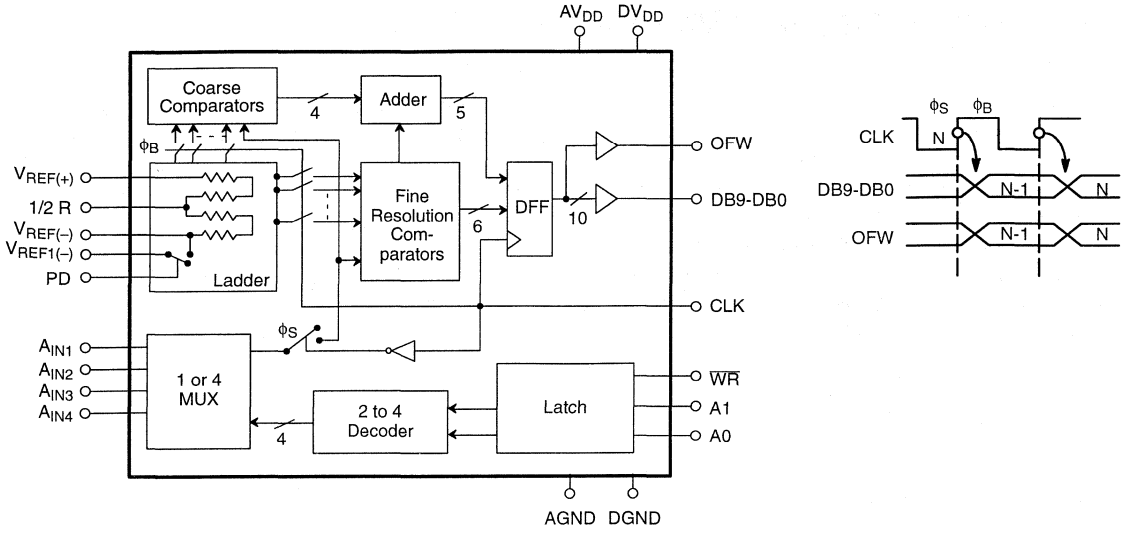
When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP8798 is available in plastic dual-in-line (PDIP), surface mount (SOIC), and shrink small outline (SSOP) packages.

ORDERING INFORMATION

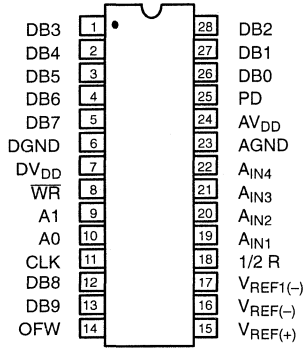
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP8798AS	±1	2
PDIP	–40 to +85°C	MP8798AN	±1	2
SSOP	–40 to +85°C	MP8798AQ	±1	2

SIMPLIFIED BLOCK AND TIMING DIAGRAM

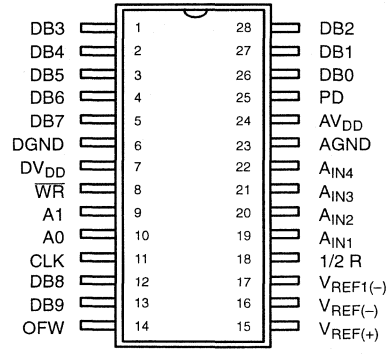


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (Jedec, 0.300") – S28
28 Pin SSOP – A28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	$\overline{WR}$	Write (Active Low)
9	A1	Address 1 Input
10	A0	Address 0 Input
11	CLK	Clock Input
12	DB8	Data Output Bit 8
13	DB9	Data Output Bit 9 (MSB)
14	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
15	$V_{REF(+)}$	Upper Reference Voltage
16	$V_{REF(-)}$	Lower Reference Voltage
17	$V_{REF1(-)}$	Lower Reference Voltage
18	1/2 R	Reference Ladder Tap
19	A_{IN1}	Analog Signal Input 1
20	A_{IN2}	Analog Signal Input 2
21	A_{IN3}	Analog Signal Input 3
22	A_{IN4}	Analog Signal Input 4
23	AGND	Analog Ground
24	AV_{DD}	Analog V_{DD}
25	PD	Power Down
26	DB0	Data Output Bit 0 (LSB)
27	DB1	Data Output Bit 1
28	DB2	Data Output Bit 2

3

TRUTH TABLE FOR INPUT CHANNEL SELECTION

$\overline{WR}$	A1	A0	SELECTED ANALOG INPUT
0	0	0	A_{IN1}
0	0	1	A_{IN2}
0	1	0	A_{IN3}
0	1	1	A_{IN4}
1	X	X	Previous selection

Note: $\overline{WR}$, A1, A0 are internally connected to GND through 500kΩ resistance.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 1 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.6, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		1	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL		±3/4	±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+0.50		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	ΔV_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance[1]			12		Ω	
Ladder Switch Off Leakage[1]	I_{LKG-SW}		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, (Internal Res to DGND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	1000			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5	µA	V_{OUT} = 0 to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30	35	ns	
Data Valid Delay[1]	t_{DL}		35	45	ns	
Write Pulse Width[1]	t_{WR}	40			ns	
Multiplexer Address Setup Time[1]	t_{AS}	80			ns	
Multiplexer Address Hold Time[1]	t_{AH}	0			ns	
Delay from $\overline{WR}$ to Multiplexer[1] Enable	t_{MUXEN1}			80	ns	
Power Down Time[1]	t_{PD}			300	ns	
Power Up Time[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{PD-DD}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

NOTES:

1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP8798 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} (to GND) ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
SOIC, PDIP 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

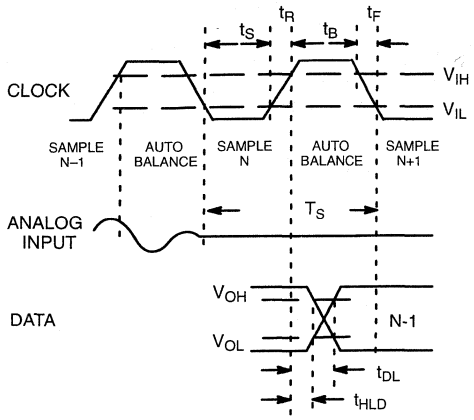


Figure 1. MP8798 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP8798 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

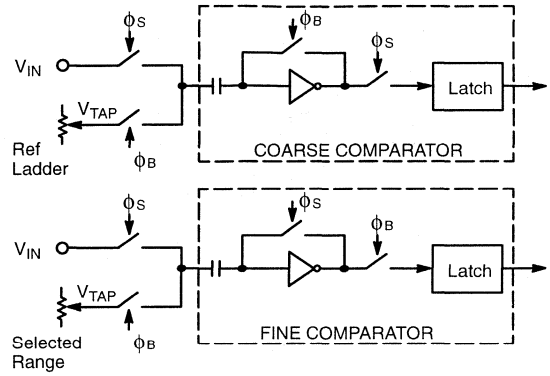


Figure 2. MP8798 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

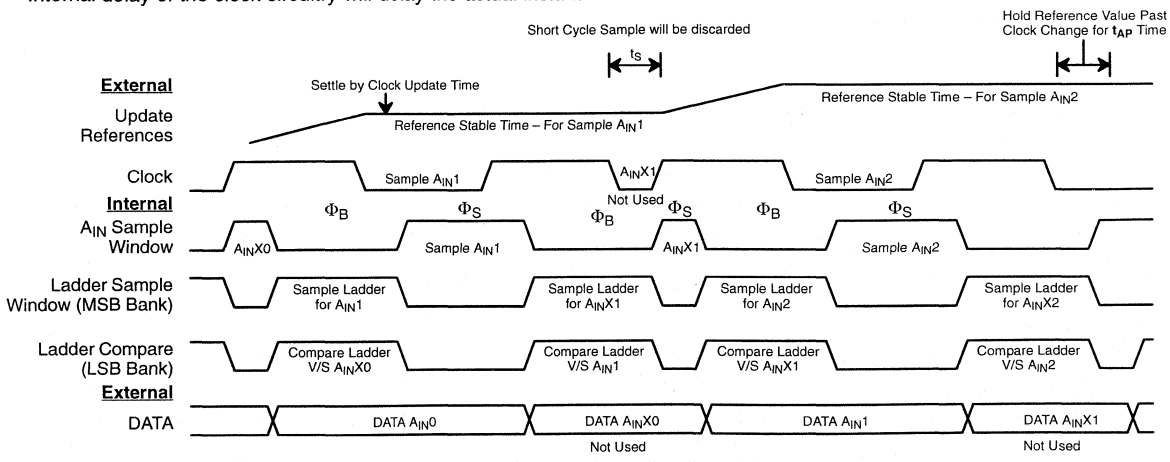


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

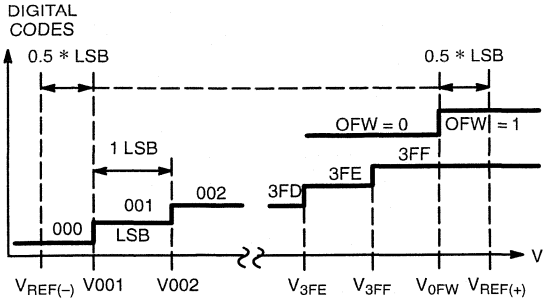


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(+)} - 1.5 * LSB$

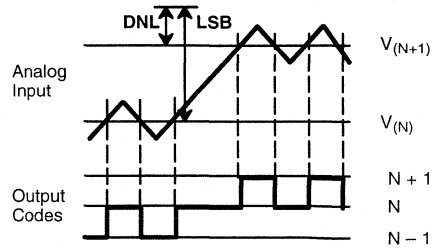
$LSB = V_{REF} / 1024 = (V_{3FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

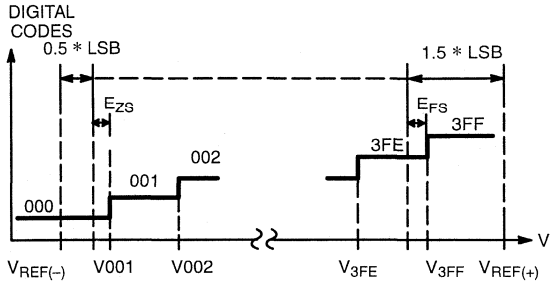


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the best fit line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the best fit line.

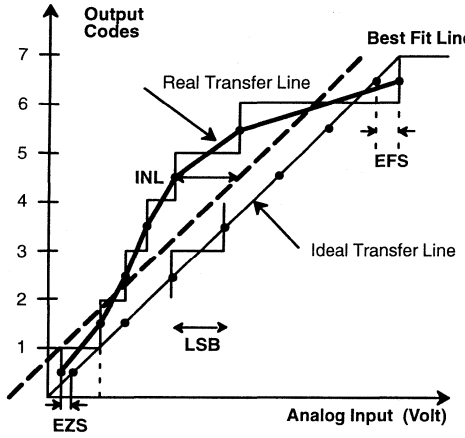


Figure 7. INL Error Calculation

Clock and Conversion Timing

A system will clock the MP8798 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP8798 in balance and ready to sample the analog input.

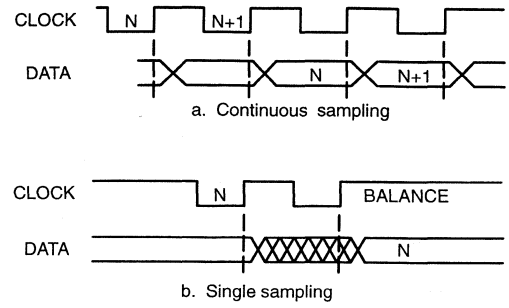


Figure 8. Relationship of Data to Clock

Analog Input

The MP8798 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP8798's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

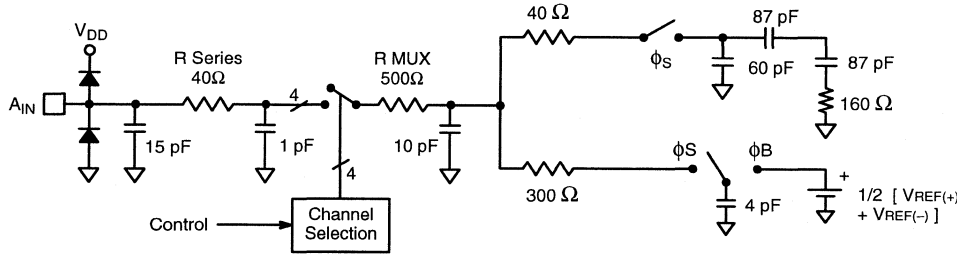


Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP8798 includes a 4-channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 10.*

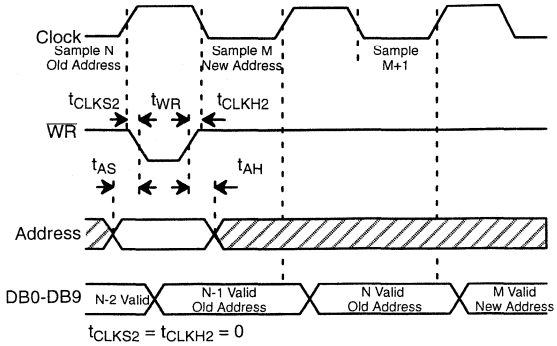


Figure 10. MUX Address Timing

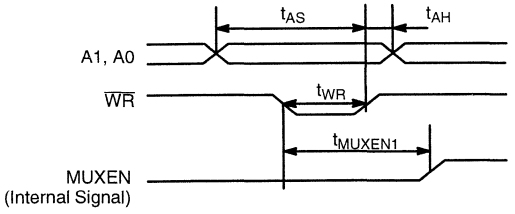


Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP8798 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

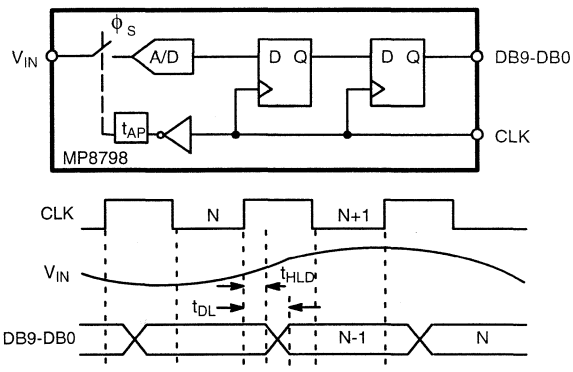


Figure 12. MP8798 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

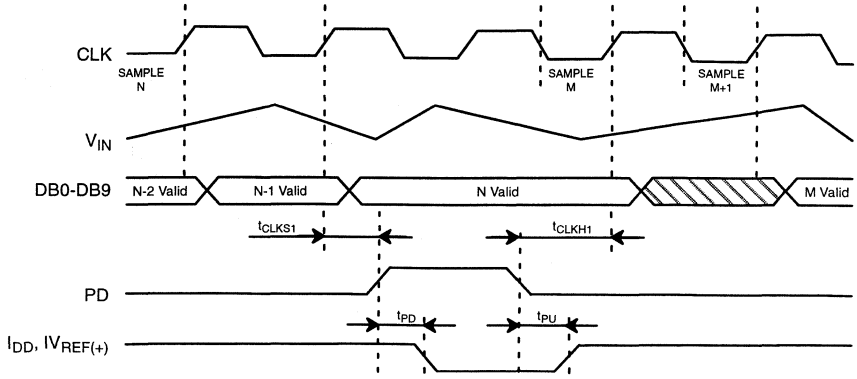


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance capacitor
R_T = Clock Transmission Line Termination

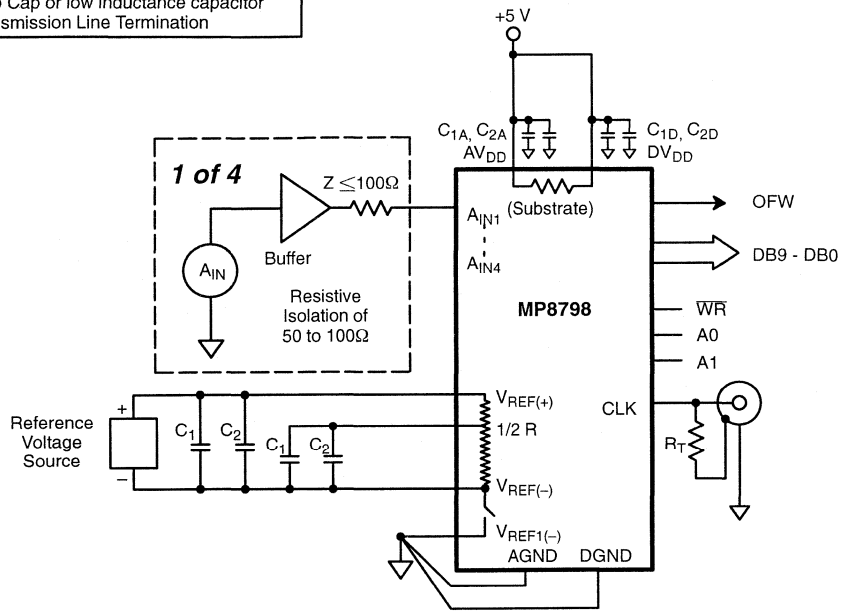


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP8798.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP8798 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP8798. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP8798.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP8798 should be connected to AV_{DD} next to the MP8798.
8. DV_{DD} and AV_{DD} are connected inside the MP8798 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

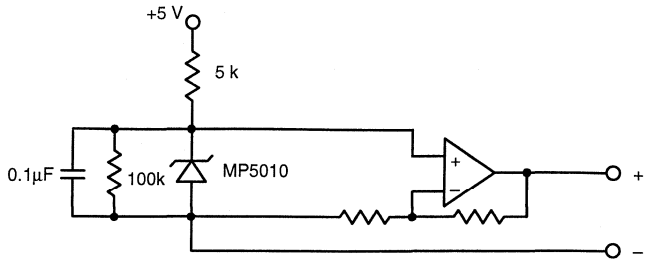
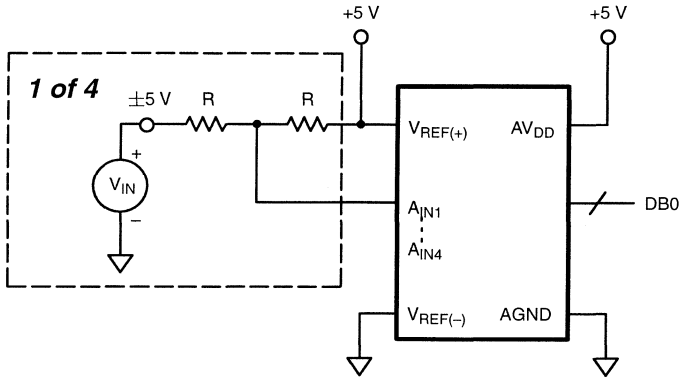


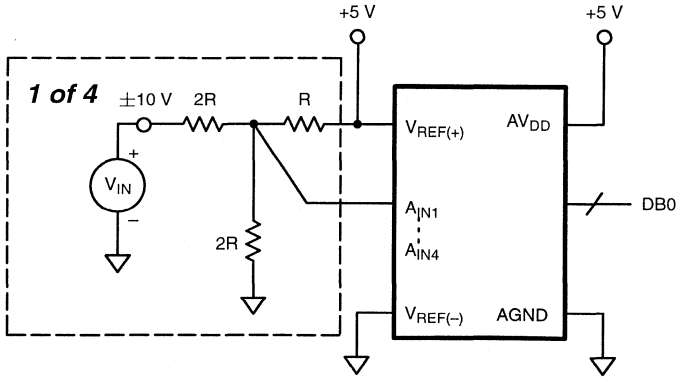
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

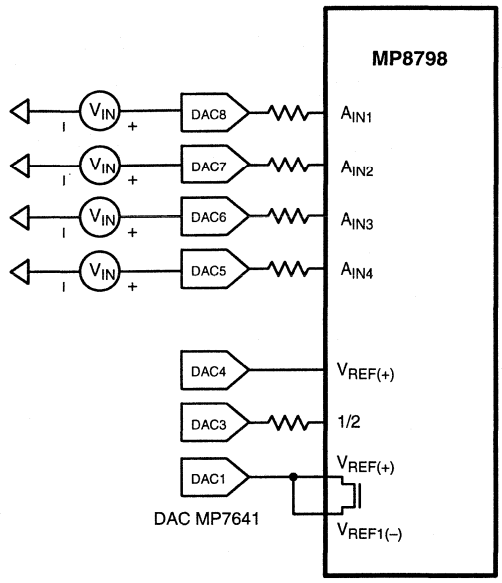
Figure 16. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 17. ±10 V Analog Input

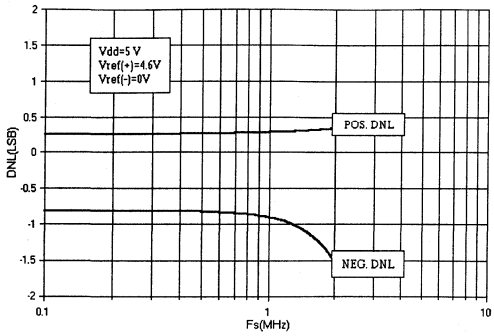


@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.

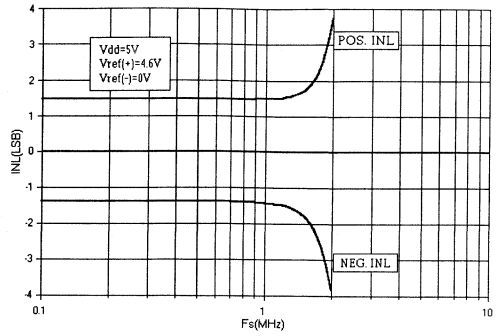
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder and A_{IN} with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/2 TAP.)

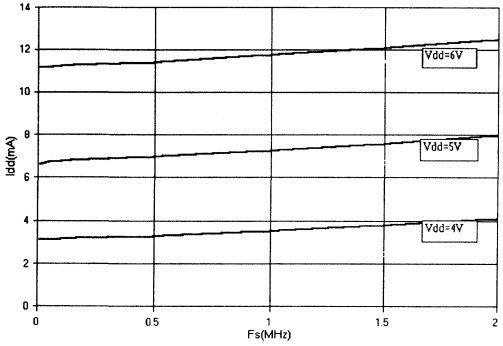
PERFORMANCE CHARACTERISTICS



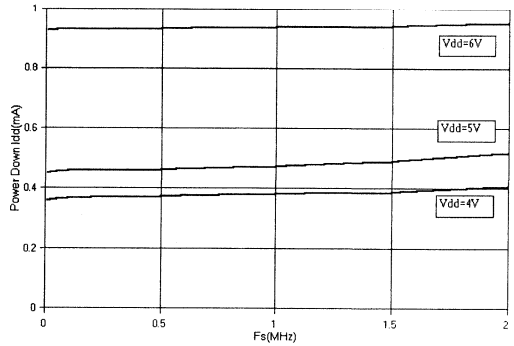
Graph 1. DNL vs. Sampling Frequency



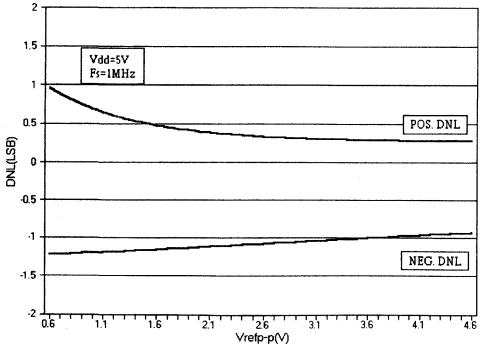
Graph 2. INL vs. Sampling Frequency



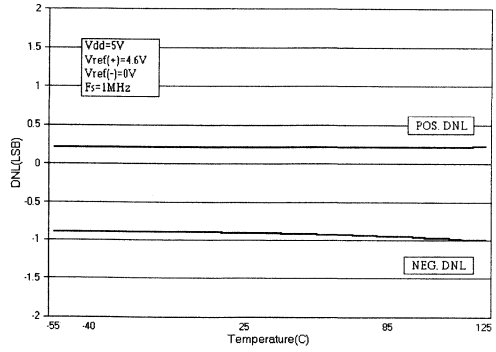
Graph 3. Supply Current vs. Sampling Frequency



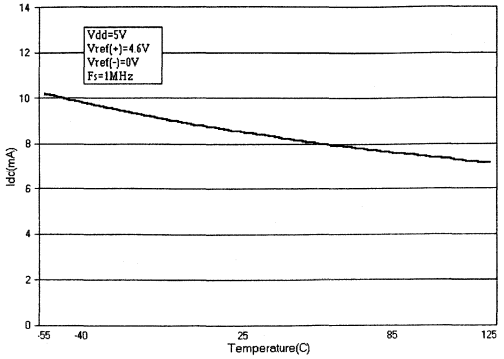
Graph 4. Power Down Current vs. Sampling Frequency



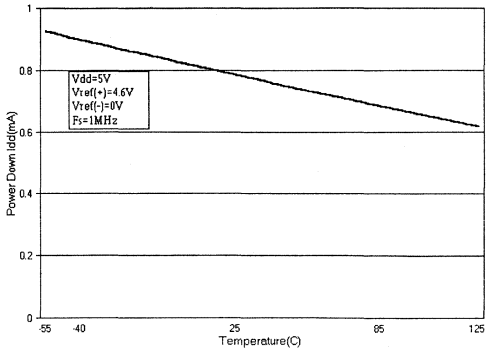
Graph 5. DNL vs. Reference Voltage



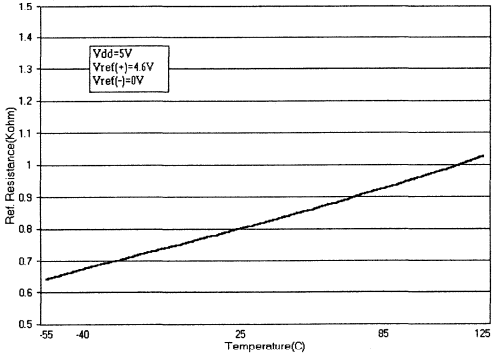
Graph 6. DNL vs. Temperature



Graph 7. Supply Current vs. Temperature



Graph 8. Power Down Current vs. Temperature



Graph 9. Reference Resistance vs. Temperature

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MP8799

CMOS
Very Low Power, 1 MSPS, 10-Bit
Analog-to-Digital Converter with 8-Channel Mux

FEATURES

- **10-Bit Resolution**
- **8-Channel Mux**
- **Sampling Rates from <1 kHz to 1 MHz**
- **Very Low Power CMOS - 30 mW (typ)**
- **Power Down; Lower Consumption – 3 mW (typ)**
- **Input Range between GND and V_{DD}**
- **No S/H Required for Analog Signals less than 100 kHz**
- **No S/H Required for CCD Signals less than 1 MHz**
- **Single Power Supply (4 to 6 Volts)**
- **Latch-Up Free**
- **High ESD Protection: 4000 Volts Minimum**
- **3 V Version: MP87L99**

BENEFITS

- **Reduced Board Space (Small Package)**
- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer can Adapt Input Range & Scaling**

APPLICATIONS

- **µP/DSP Interface and Control Applications**
- **High Resolution Imaging – Scanners & Copiers**
- **Wireless Digital Communications**
- **Multiplexed Data Acquisition**

3

GENERAL DESCRIPTION

The MP8799 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with 8-channel mux that operates over a wide range of input and sampling conditions. The MP8799 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 1 MHz. The elimination of the S/H requirements, very low power, and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications up to 1 MHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP8799 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap @ 1/4 R, 1/2 R and 3/4 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

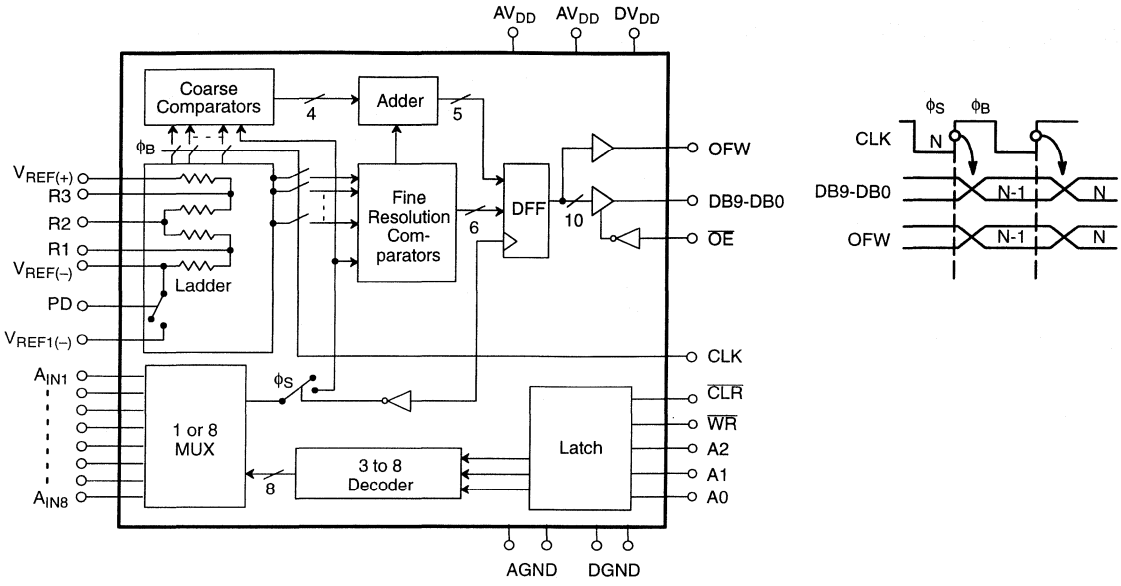
The MP8799 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

ORDERING INFORMATION

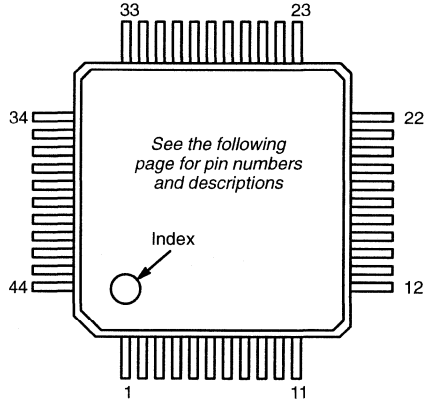
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP8799AE	±1	2

SIMPLIFIED BLOCK AND TIMING DIAGRAM



PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



44-Pin PQFP (10mm x 10mm)
QN44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB6	Data Output Bit 6
2	DB7	Data Output Bit 7
3	DGND	Digital Ground
4	DGND	Digital Ground
5	DV_{DD}	Digital V_{DD}
6	$\overline{CLR}$	Clear (Active Low)
7	$\overline{WR}$	Write (Active Low)
8	A2	Address 2
9	A1	Address 1
10	A0	Address 0
11	CLK	Clock Input
12	$\overline{OE}$	Output Enable (Active Low)
13	N/C	No Connect
14	DB8	Data Output Bit 8
15	DB9	Data Output Bit 9 (MSB)
16	OFW	Overflow Output
17	$V_{REF(+)}$	Upper Reference Voltage
18	$V_{REF(-)}$	Lower Reference Voltage
19	$V_{REF1(-)}$	Lower Reference Voltage
20	R1	Reference Ladder Tap
21	R2	Reference Ladder Tap
22	A_{IN8}	Analog Signal Input 8

PIN NO.	NAME	DESCRIPTION
23	R3	Reference Ladder Tap
24	N/C	No Connect
25	A_{IN1}	Analog Signal Input 1
26	A_{IN2}	Analog Signal Input 2
27	A_{IN3}	Analog Signal Input 3
28	A_{IN4}	Analog Signal Input 4
29	A_{IN5}	Analog Signal Input 5
30	AGND	Analog Ground
31	AV_{DD}	Analog V_{DD}
32	AV_{DD}	Analog V_{DD}
33	A_{IN6}	Analog Signal Input 6
34	AGND	Analog Ground
35	PD	Power Down
36	A_{IN7}	Analog Signal Input 7
37	DB0	Data Output Bit 0 (LSB)
38	DB1	Data Output Bit 1
39	DB2	Data Output Bit 2
40	DB3	Data Output Bit 3
41	DB4	Data Output Bit 4
42	DB5	Data Output Bit 5
43	N/C	No Connect
44	N/C	No Connect

3

TRUTH TABLE FOR INPUT CHANNEL SELECTION

$\overline{CLR}$	$\overline{WR}$	A2	A1	A0	Selected Analog Input
L	X	X	X	X	A_{IN1}
H	L	L	L	L	A_{IN1}
H	L	L	L	H	A_{IN2}
H	L	L	H	L	A_{IN3}
H	L	L	H	H	A_{IN4}
H	L	H	L	L	A_{IN5}
H	L	H	L	H	A_{IN6}
H	L	H	H	L	A_{IN7}
H	L	H	H	H	A_{IN8}
H	H	X	X	X	Previous Selection

Note: $\overline{CLR}$, $\overline{WR}$, A2, A1, A0 are internally connected to ground through 500kΩ resistance.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S =$ 1 MHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)} =$ AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		1	MHz	For Rated Performance
ACCURACY (A Grade)[2]						
Differential Non-Linearity	DNL			±1	LSB	LSB
Integral Non-Linearity	INL			2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+0.50		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance[1]			12		Ω	
Ladder Switch Off Leakage[1]	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, $\overline{OE}$ (Internal Res to DGND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	1000			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5	µA	V_{OUT} = 0 to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30	35	ns	
Data Valid Delay[1]	t_{DL}		35	45	ns	
Write Pulse Width[1]	t_{WR}	40			ns	
Multiplexer Address Setup Time[1]	t_{AS}	80			ns	
Multiplexer Address Hold Time[1]	t_{AH}	0			ns	
Delay from $\overline{WR}$ to Multiplexer[1] Enable	t_{MUXEN1}			80	ns	
Power Down Time[1]	t_{PD}			300	ns	
Power Up Time[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{PD-DD}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

NOTES:

1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 4.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP8799 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +7 V
$V_{REF(+)}$, $V_{REF(-)}$, $V_{REF1(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
All A_{INs} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PQFP 450mW
Derates above 75°C ..... 14mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

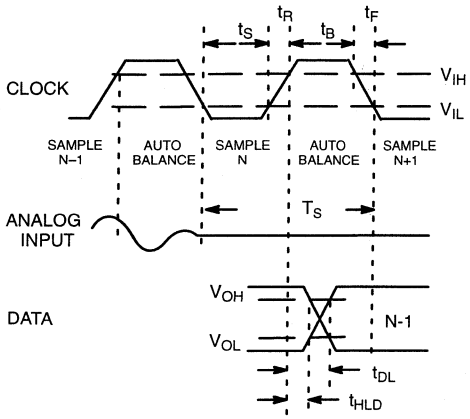


Figure 1. MP8799 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP8799 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

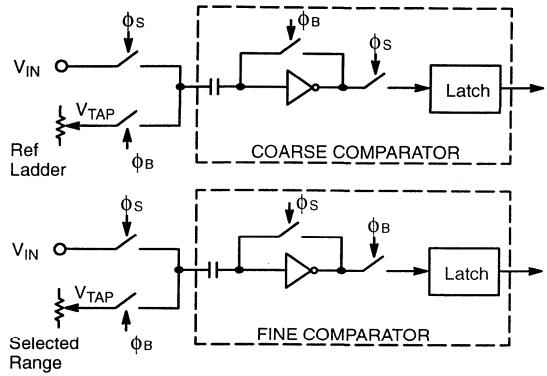


Figure 2. MP8799 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

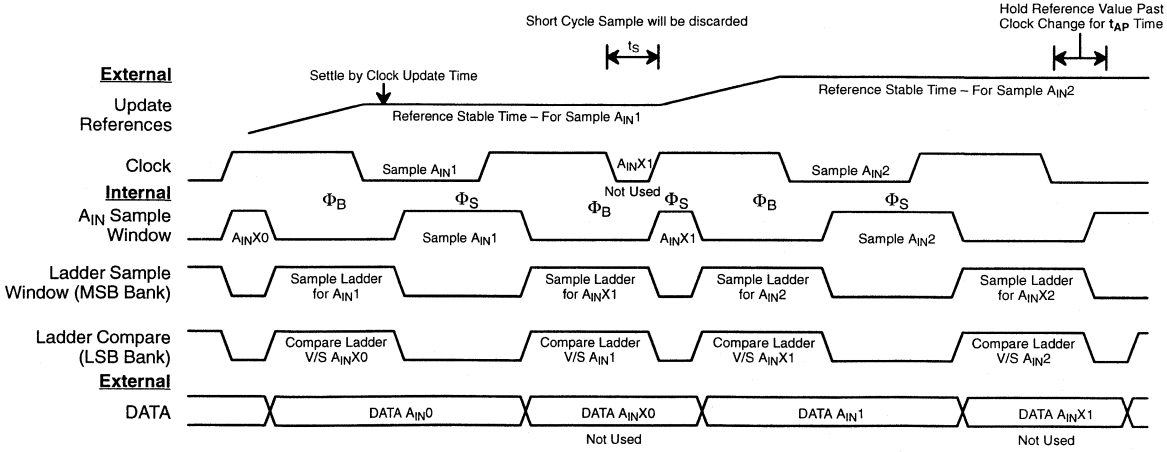


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

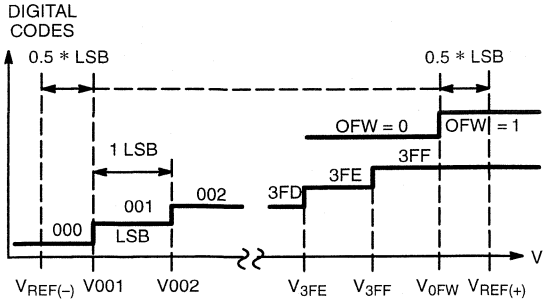


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(-)} - 1.5 * LSB$

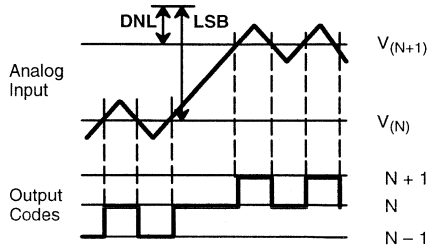
$LSB = V_{REF} / 1024 = (V_{3FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

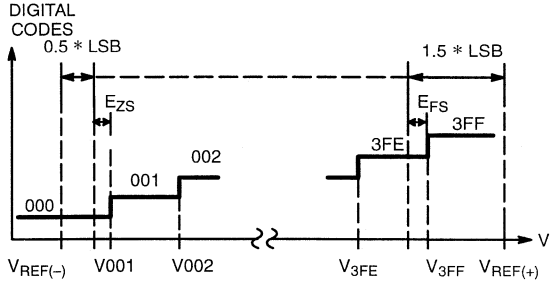


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the best fit line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the best fit line.

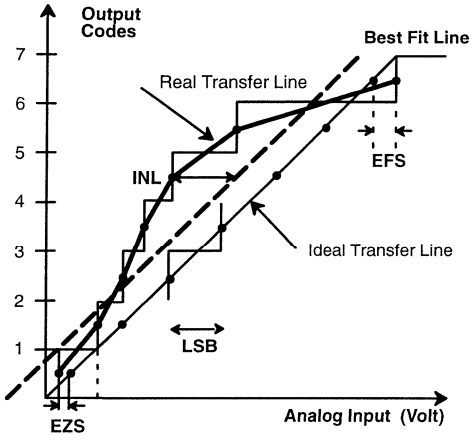


Figure 7. INL Error Calculation

Clock and Conversion Timing

A system will clock the MP8799 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP8799 in balance and ready to sample the analog input.

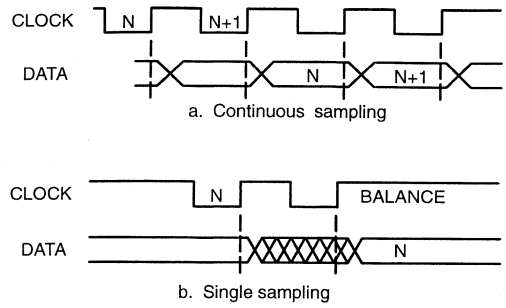


Figure 8. Relationship of Data to Clock

Analog Input

The MP8799 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP8799's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

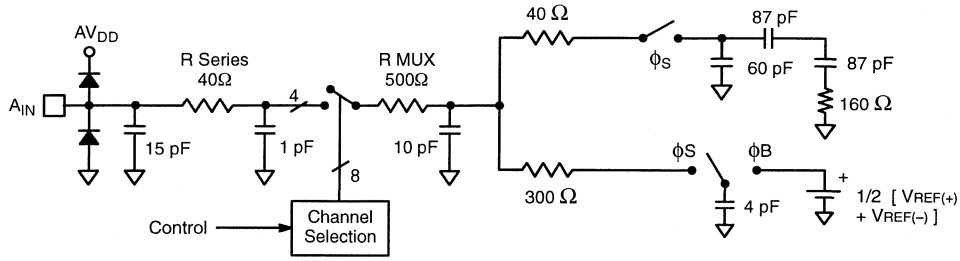


Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP8799 includes a 8-Channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 10.*

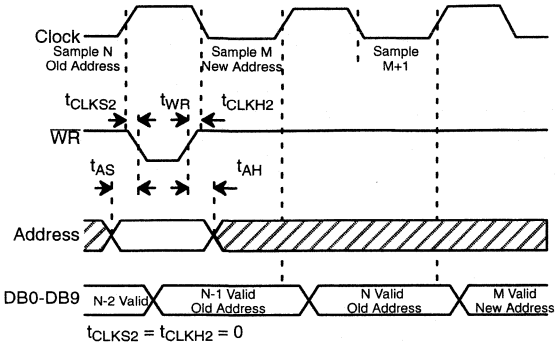


Figure 10. MUX Address Timing

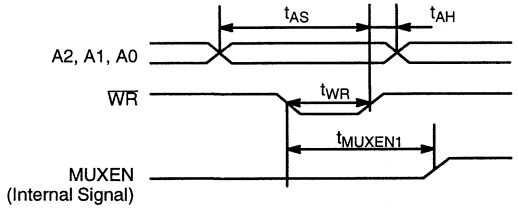


Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP8799 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

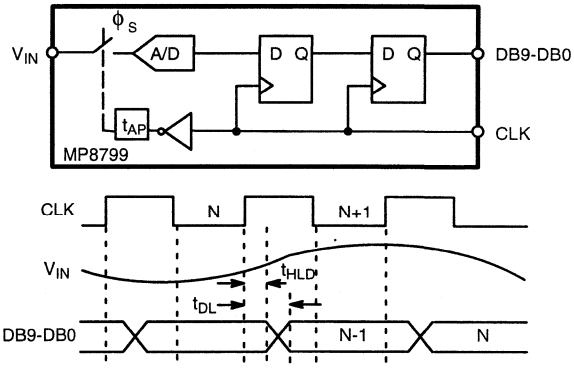


Figure 12. MP8799 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

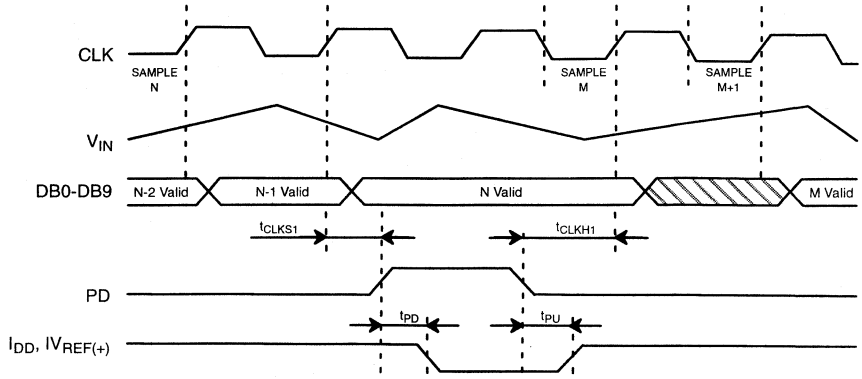


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance cap
R_T = Clock Transmission Line Termination

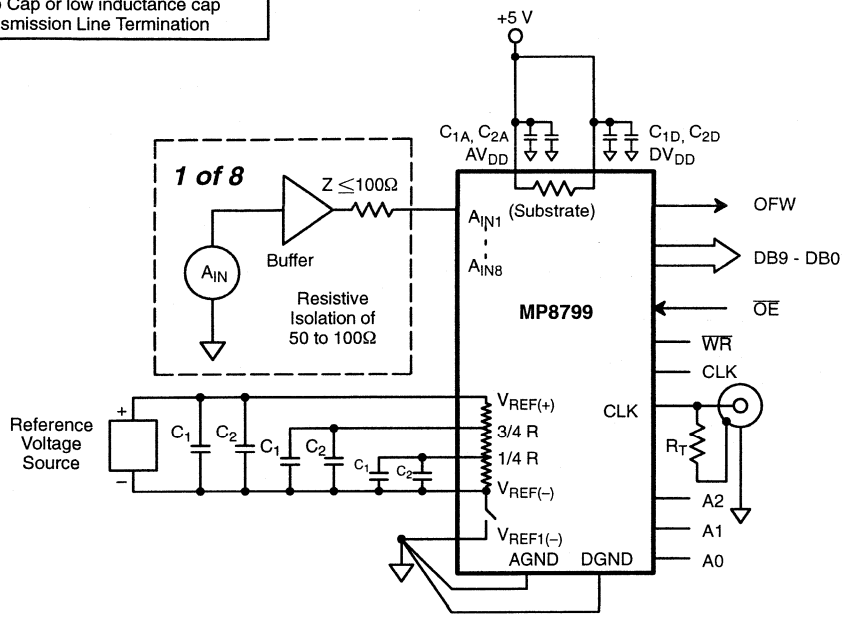


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP8799.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP8799 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP8799. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP8799.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP8799 should be connected to AV_{DD} next to the MP8799.
8. DV_{DD} and AV_{DD} are connected inside the MP8799 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

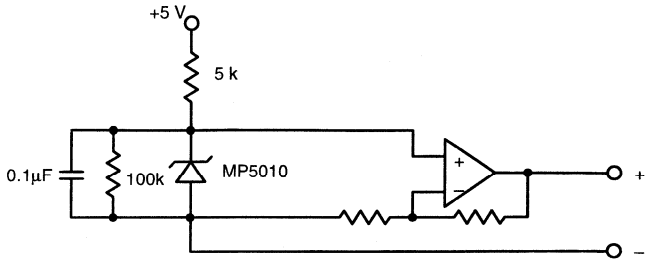
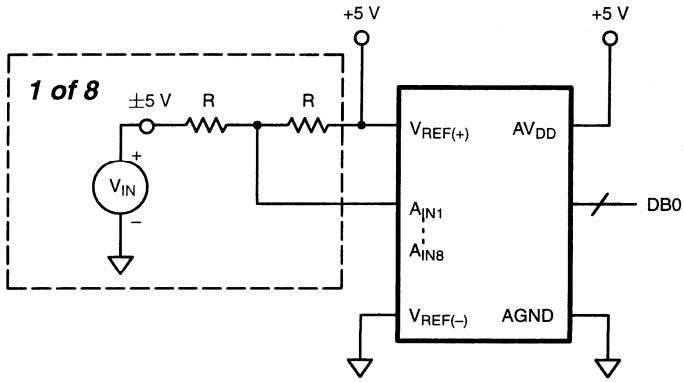


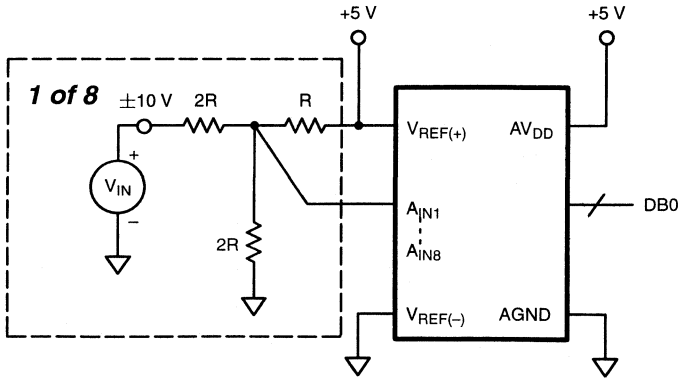
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

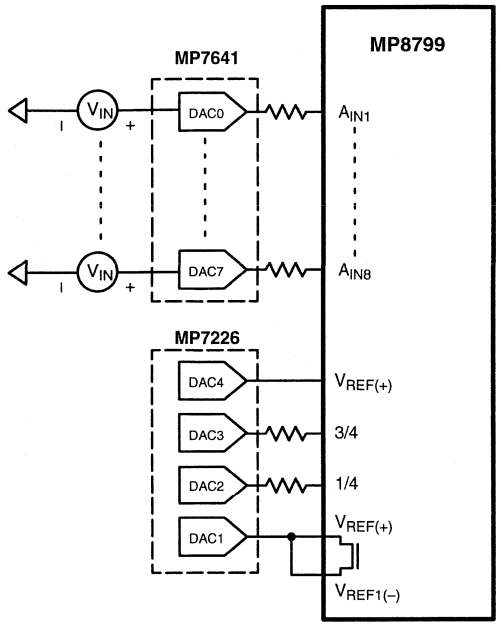
Figure 16. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 17. ±10 V Analog Input

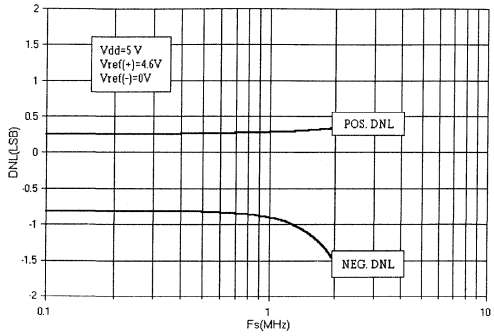


@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.

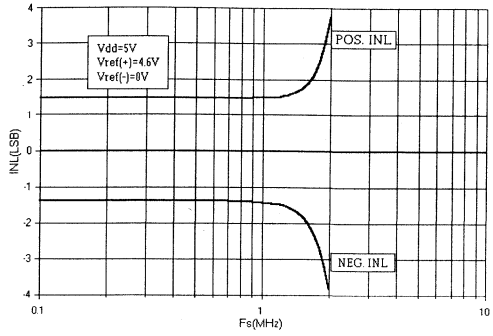
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder and A_{IN} with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/4 and 3/4 TAP.)

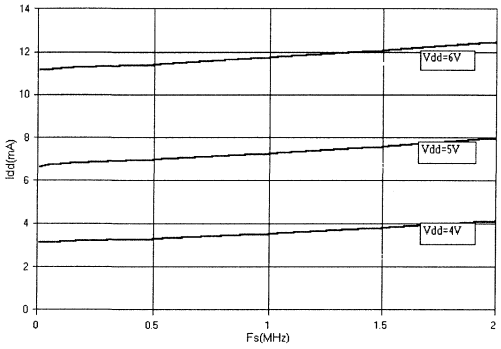
PERFORMANCE CHARACTERISTICS



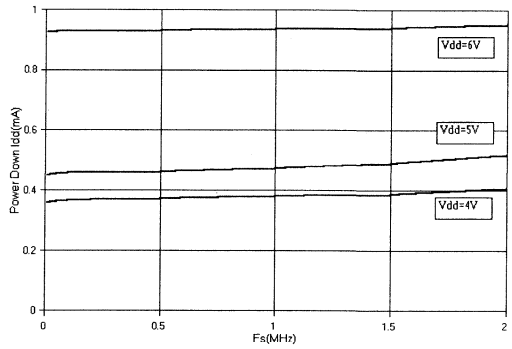
Graph 1. DNL vs. Sampling Frequency



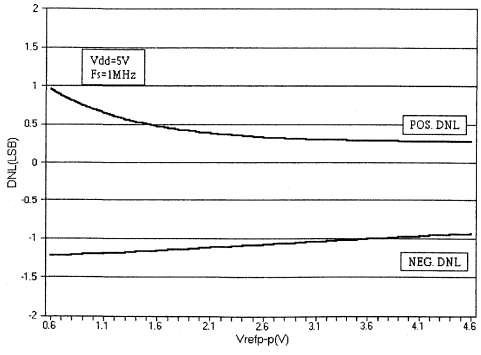
Graph 2. INL vs. Sampling Frequency



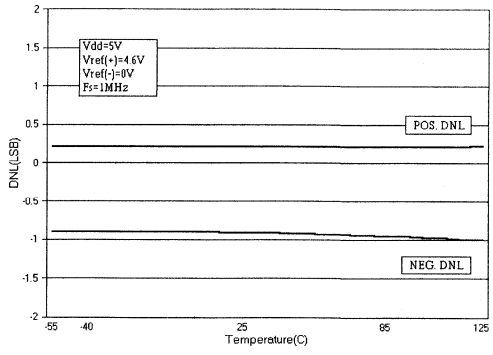
Graph 3. Supply Current vs. Sampling Frequency



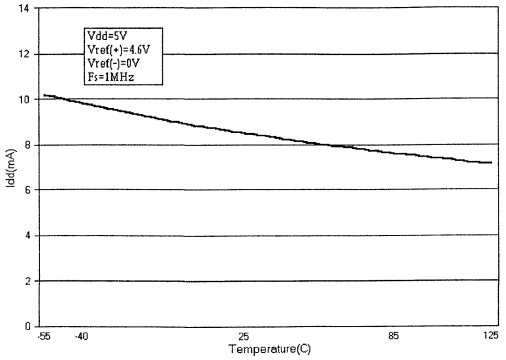
Graph 4. Power Down Current vs. Sampling Frequency



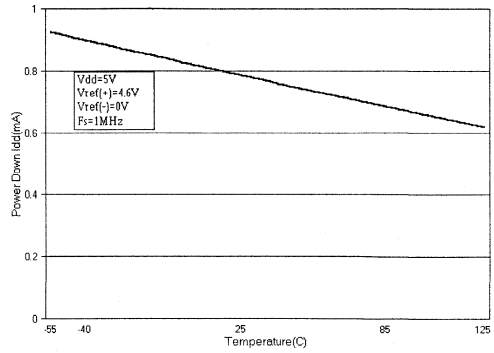
Graph 5. DNL vs. Reference Voltage



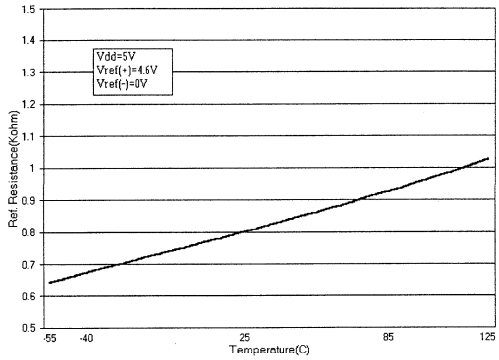
Graph 6. DNL vs. Temperature



Graph 7. Supply Current vs. Temperature



Graph 8. Power Down Current vs. Temperature



Graph 9. Reference Resistance vs. Temperature

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MP87091

CMOS 750 KSPS, 12-Bit
Analog-to-Digital Converter
with Parallel Logic Interface Port

FEATURES

- 12-Bit Monotonic ADC
- SNR > 66 dB
- Sampling Frequency ≤ 750 kHz
- Internal Track and Hold
- Single 5 V Supply
- Rail-to-Rail Input Range
- DNL = ±1 LSB, INL = ±2 LSB
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 175 mW (typ)
- 1/4, 1/2 and 3/4 Scale Reference Resistor Taps
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode
- Latch-Up Proof

APPLICATIONS

- Control Systems
- Instrumentation
- DAS
- Sonar

3

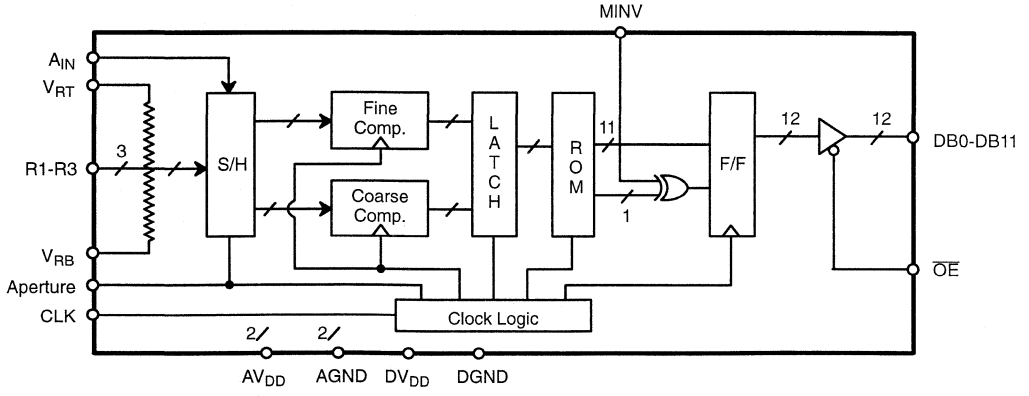
GENERAL DESCRIPTION

The MP87091 is a 750 kHz 12-bit subranging Analog-to-Digital Converter with an an internal track and hold.

The MP87091 operates with a single 5 V supply while consuming less than 175 mW of power (typical). Separate pins for V_{RT} and V_{RB} allow flexibility for various A_{IN} and ΔV_{REF}.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. The digital output port is also equipped with a three-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment, linearity, and speed enhancement can be accommodated.

SIMPLIFIED BLOCK DIAGRAM

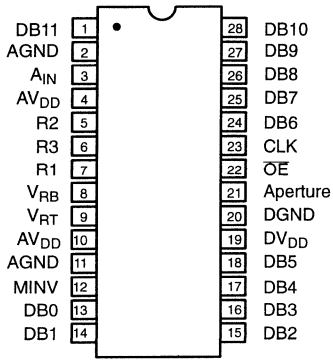


ORDERING INFORMATION

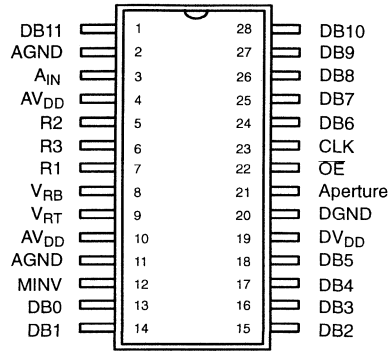
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	MP87091AN	±1	2 1/2
SOIC	–40 to +85°C	MP87091AS	±1	2 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB11	Data Output Bit 11 (MSB)
2	AGND	Analog Ground
3	A_{IN}	Analog Input
4	AV_{DD}	Analog Power Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{RB}	Bottom Reference
9	V_{RT}	Top Reference
10	AV_{DD}	Analog Power Supply
11	AGND	Analog Ground
12	MINV	Invert MSB (Active High)
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1

PIN NO.	NAME	DESCRIPTION
15	DB2	Data Output Bit 2
16	DB3	Data Output Bit 3
17	DB4	Data Output Bit 4
18	DB5	Data Output Bit 5
19	DV_{DD}	Digital Power Supply
20	DGND	Digital Ground
21	Aperture	Delayed Clock, indicates sample point
22	$\overline{OE}$	Output Enable (Active Low)
23	CLK	Clock
24	DB6	Data Output Bit 6
25	DB7	Data Output Bit 7
26	DB8	Data Output Bit 8
27	DB9	Data Output Bit 9
28	DB10	Data Output Bit 10

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 750 kHz (50% Duty Cycle), V_{RT} = 5.0 V, V_{RB} = AGND, TA = 25°C, A_{IN} Connected through 39Ω, Aperture Connected to $\overline{OE}$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		12			Bits	
Sampling Rate	FS			750	kHz	For rated accuracy
ACCURACY[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			2 1/2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Top Ref. Voltage	V_{RT}	1.5		AV_{DD}	V	
Bottom Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Bandwidth (–3 dB)[4]	BW		10		MHz	
Input Voltage Range	A_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		35		ns	
Aperture Delay from Aperture Signal			0		ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}		2.4		V	
Logical "0" Voltage	V_{IL}		0.8		V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE}$, MINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	1000	1333		ns	Functional
Rise & Fall Time[7]	t_R, t_F		15		ns	
"High" Time	t_{PWH}	500	667		ns	
"Low" Time	t_{PWL}	500	667		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}		DV_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 4 mA
Three-State Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		30		ns	
Data Enable Delay	t_{DEN}		25		ns	
Data Three-State Delay	t_{DHZ}		25		ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
POWER SUPPLIES[8] (Tmin to Tmax)						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}			45	mA	
AC PARAMETERS						
Signal Noise Ratio	SNR	66			dB	A_{IN} = 5 V p-p, 1 kHz

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 A 39 Ω resistor should be put in series with A_{IN} to dampen transients with inductive output impedance of typical op amps.

6 All inputs have diodes to V_{DD} and GND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

8 AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
A_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 450mW
Derates above 75°C ..... 6mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

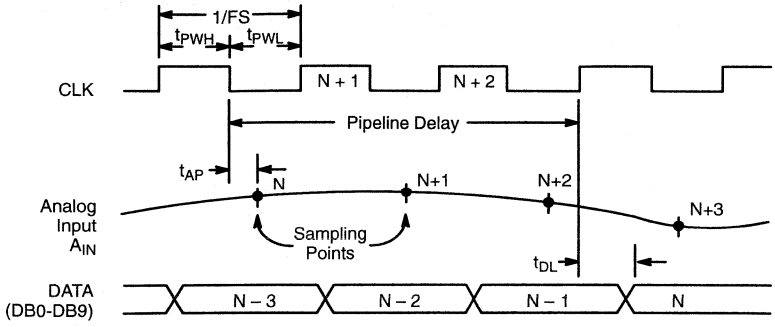


Figure 1. Timing Diagram

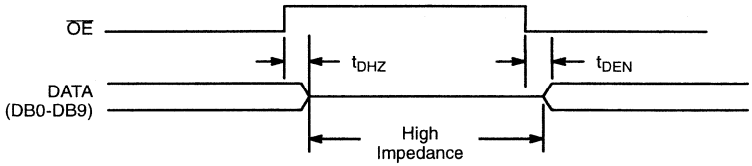


Figure 2. Three-State Timing Diagram

OVERVIEW OF THE MP87091 OPERATION

$\overline{OE}$: Output Enable (input)

This signal controls the 3-state drivers on the digital outputs DB0 - DB11. During normal operation $\overline{OE}$ should be held low so that all outputs are enabled (NOTE: an internal resistor will pull $\overline{OE}$ to this level if it is not connected). When $\overline{OE}$ is driven high DB0 - DB11 go into the high impedance mode. This control operates asynchronously to the clock and only controls the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. If possible, $\overline{OE}$ should be in three-state during Clock = 1 to reduce digital noise coupling into A_{IN} during the sample time. Aperture provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

APERTURE: Aperture Delay Sync (Output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperture pin may also be used to control the $\overline{OE}$ (outputs between three-state and active mode). This will reduce the errors introduced by digital output coupling during the A_{IN} sample time. Specifications are based on this connection.

MINV: Digital Output Format (input).

This signal controls the format of the digital output data bits DB0 – DB11. Normally it is held low so the data is in straight binary format (all 0's when $V_{IN} = V_{RB}$; all 1's when $V_{IN} = V_{RT}$). If MINV is pulled high then the MSB (DB11) will be inverted.

MINV is meant to be a static digital signal. If it is to change during operation it should only change when the CLK is low. Changing MINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV has a internal pull down device.

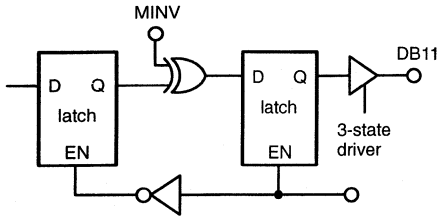


Figure 3. MINV Simplified Logic Circuit

A_{IN} Analog Input

A 50 to 75Ω resistor in series with this pin will minimize A_{IN} interaction with the signal source.

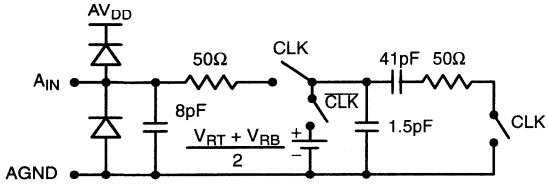


Figure 4. Equivalent Input Circuit

R1, R2, R3: Reference Ladder Taps.

These taps connect to every 1/4 point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to GND, this helps reduce the INL errors by stabilizing the reference ladder voltages.

These taps can also be used to alter the transfer curve of the ADC. A 4 segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

This may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

The internal interconnect resistance from each of the tAP pins to the ladder is less than 3Ω.

1.6V maximum per tap is recommended for applications above 85°C. Up to 3.2V is allowed for applications under 85°C.

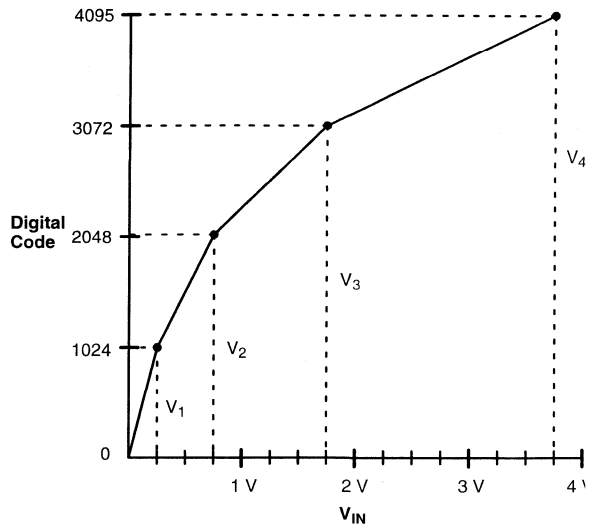
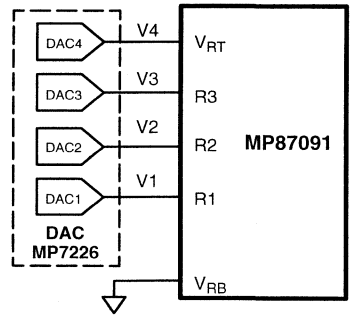


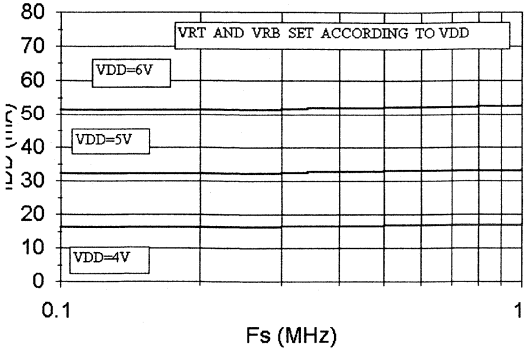
Figure 5. A Piecewise Linear Transfer Function



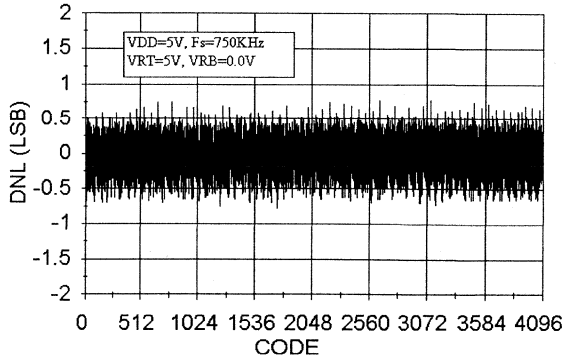
Only the Ladder detail shown.

Figure 6. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

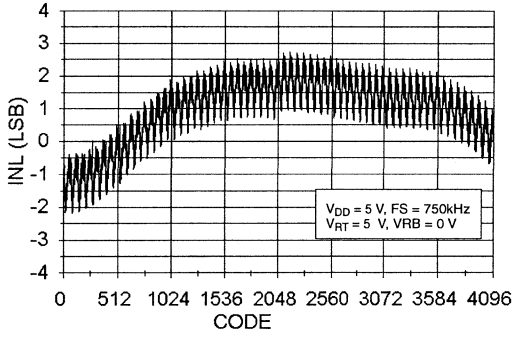
PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. F_S



Graph 2. DNL Error Plot



Graph 3. INL Error Plot

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MP87092

CMOS 750 KSPS, 12-Bit Analog-to-Digital Converter with Serial Logic Interface Port

FEATURES

- **12-Bit Monotonic ADC with DNL = ±1 LSB, INL = ±2 LSB**
- **SNR > 66 dB**
- **Sampling Frequency ≤ 750 kHz**
- **Internal Track and Hold**
- **Single 5 V Supply**
- **Rail-to-Rail Input Range**
- **V_{REF} Range: 1.5 V to V_{DD}**
- **CMOS Low Power: 175 mW (typ)**
- **Binary and Two's Complement Digital Output Mode**
- **Serial Port**
- **Underflow Outputs**
- **Precision Aperture Output**
- **6 Reference Resistor Taps**
- **Latch-Up Free**

APPLICATIONS

- **Control Systems**
- **Instrumentation**
- **DAS**
- **Sonar**

3

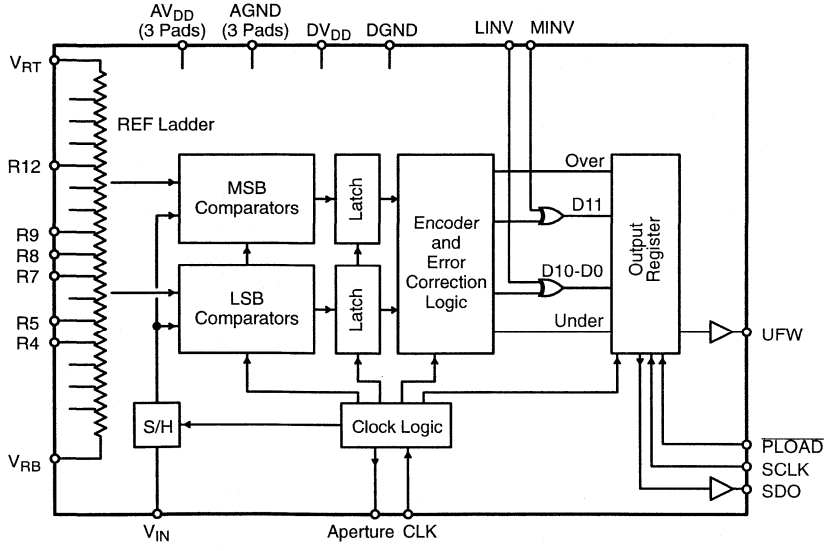
GENERAL DESCRIPTION

The MP87092 is a 12-bit 750 kHz subranging Analog-to-Digital Converter with an internal track and hold.

The MP87092 operates with a single supply ranging from +3 V to +5 V while consuming less than 175 mW of power (typical). Separate pins for V_{RT} and V_{RB} allow flexibility for analog input (V_{IN}) and the reference voltage range (ΔV_{REF}).

Data is presented at the output port every clock cycle after a 3 cycle pipeline delay. The digital output port is equipped with a serial data port. LINV and MINV enable binary and 2's complement data formatting. Access is provided to 6 ladder tap pins, providing for transfer function adjustment.

SIMPLIFIED BLOCK DIAGRAM

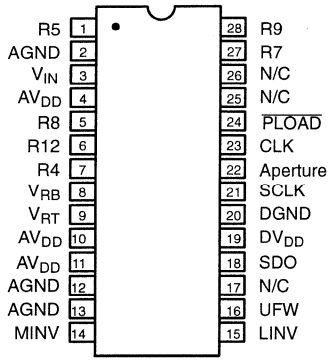


ORDERING INFORMATION

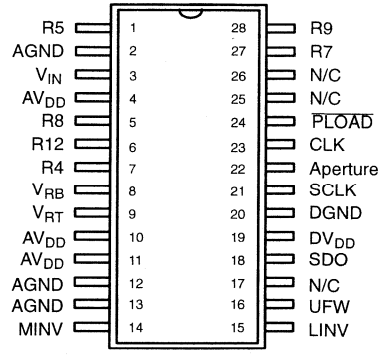
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	MP87092AN	±1	2 1/2
SOIC	–40 to +85°C	MP87092AS	±1	2 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28



28 Pin SOIC (EIAJ 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	R5	Ref. Resistor Ladder Tap (5/16 V_{REF})
2	AGND	Analog Ground
3	V_{IN}	Analog Input
4	AV_{DD}	Analog Positive Supply
5	R8	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R12	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R4	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{RB}	Negative Reference
9	V_{RT}	Positive Reference
10	AV_{DD}	Analog Positive Supply
11	AV_{DD}	Analog Positive Supply
12	AGND	Analog Ground
13	AGND	Analog Ground
14	MINV	Invert MSB (Active High)

PIN NO.	NAME	DESCRIPTION
15	LINV	Invert LSB (Active High)
16	UFW	Underflow Bit
17	N/C	No Connection
18	SDO	Serial Data Out
19	DV_{DD}	Digital Positive Supply
20	DGND	Digital Ground
21	SCLK	Serial Clock
22	Aperture	Aperture Delay Sync
23	CLK	Clock
24	$\overline{PLOAD}$	Serial Shift Register Data Load
25	N/C	No Connection
26	N/C	No Connection
27	R7	Ref. Resistor Ladder Tap (7/16 V_{REF})
28	R9	Ref. Resistor Ladder Tap (9/16 V_{REF})

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 750 kHz (50% Duty Cycle), $V_{REF(+)}$ = 5.0 V, $V_{REF(-)}$ = AGND, TA = 25°C, V_{IN} Connected through 39Ω

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		12			Bits	
Sampling Rate	FS			750	kHz	
ACCURACY[1]						
Differential Non-Linearity	DNL		±1/2	±1	LSB	
Integral Non-Linearity (*See Graph 3.*)	INL		±2	±3	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}	1.5		AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	4.5 to 5 V is recommended for specified performance
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Bandwidth (–3 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		20		ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}		2.4		V	
Logical "0" Voltage	V_{IL}		0.8		V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, MINV, LINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	1.33			µs	
Rise & Fall Time[7]	t_R, t_F		15		ns	
"High" Time	t_{PWH}	665			ns	
"Low" Time	t_{PWL}	665			ns	
Duty Cycle			50		%	
Serial Register Timing						
Shift Clock Period	t_{SC}	110			ns	
Shift Clock to Data Delay	t_{SD}		20		ns	
Minimum Pulse Width $\overline{PLOAD}$	t_S		50		ns	
Clock↑ to $\overline{PLOAD}$↓ For Valid D11	t_{CP}		0		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}		DV_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical "1" Source Current	I_{OH}		4		mA	V_{OH} = DV_{DD}-0.5
Logical "0" Voltage	V_{OL}		0.5		V	I_{LOAD} = 4 mA
Logical "0" Sink Current	I_{OL}		4		mA	V_{OL} = 0.5 V
Tristate Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		30		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
POWER SUPPLIES[8]						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		35	45	mA	
AC PARAMETERS						
Signal Noise Ratio	SNR	66			dB	V_{IN} = 5 Vp-p, 1 kHz

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).
2. Guaranteed. Not tested.
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5. A 39Ω resistor should be put in series with V_{IN} to dampen transients associated with inductive output impedance of typical op amps.
6. All inputs have diodes to DV_{DD} and DGND. Input(s) MINV and LINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7. Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
8. AGND & DGND pins are internally connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
Digital Outputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating @ 75°C
PDIP. SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

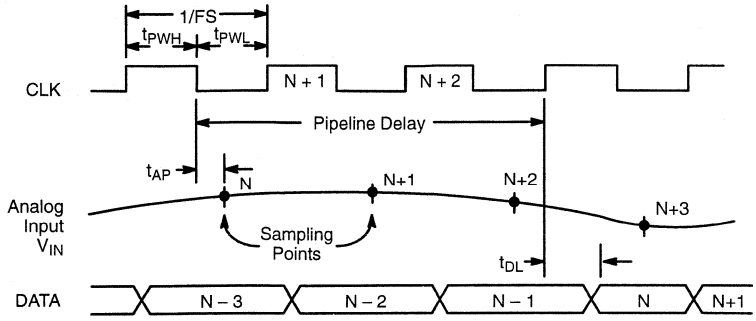
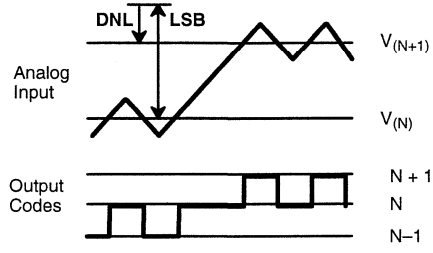


Figure 1. MP87092 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 4096

$DNL_{(N)}$ = [$V_{(N+1)} - V_{(N)}$] – LSB

Figure 2. DNL Measurement

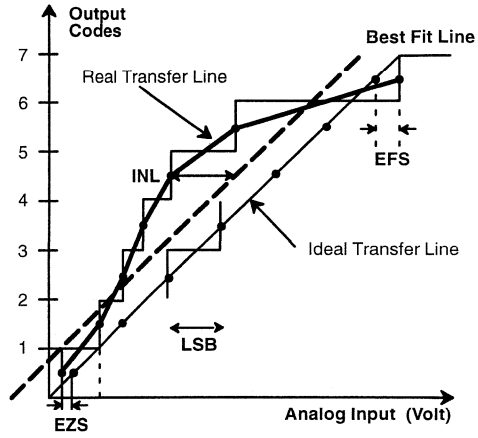


Figure 3. INL Error Calculation

UFW: Underflow (Output)

This signal indicates when the Analog Input (V_{IN}) goes outside the V_{RB} range, and is normally at a low logic level. When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0's if MINV & LINV are low).

SDO: Serial Data output

After the internal shift register is updated using the $\overline{\text{PLOAD}}$ signal, the SDO pin outputs the A/D result starting with the MSB (which appears just after the $\overline{\text{PLOAD}}$ strobe). Each bit is output on the rising edge of SCLK.

SCLK: Serial Data Port Clock

The SCLK controls the output of the serial port through SDO. SDO is updated on every rising edge of SCLK. The $\overline{\text{PLOAD}}$ signal will override the SCLK signal.

$\overline{\text{PLOAD}}$:

Serial data port shift register load: When $\overline{\text{PLOAD}}$ is low (i.e. level triggered not edge triggered) the current parallel data will be loaded into the shift register. $\overline{\text{PLOAD}}$ overrides SCLK. When $\overline{\text{PLOAD}}$ is high, the data can be shifted out through the SDO pin with SCLK.

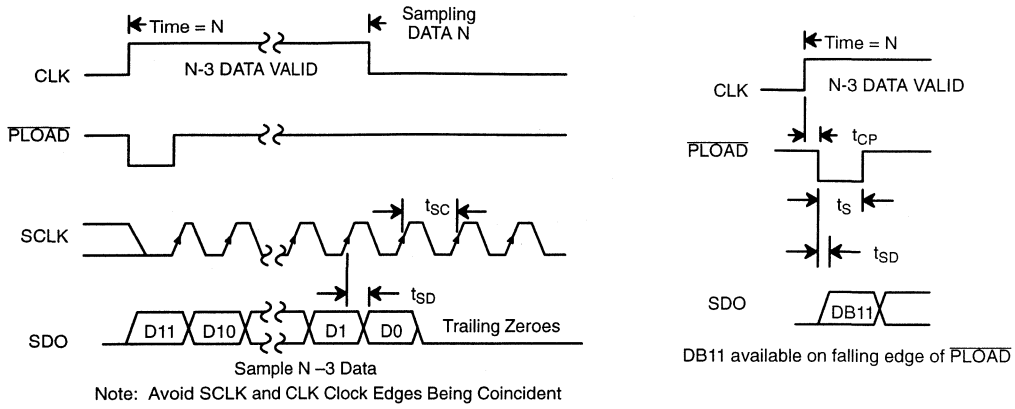


Figure 4. Serial Port Timing Chart

APERTURE: Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event.

MINV LINV	0 0	0 1	1 0	1 1
V_{RT}	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
	⋮	⋮	⋮	⋮
	100 . . . 01	111 . . . 10	000 . . . 01	011 . . . 10
V_{IN} mid scale	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
	⋮	⋮	⋮	⋮
V_{RB}	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

MINV & LINV: Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB11. Normally both pins are held low so the data is in straight binary format (all 0's when V_{IN}=V_{RB}; all 1's when V_{IN}=V_{RT}). If MINV is pulled high then the MSB (DB11) will be inverted. If LINV is pulled high then the LSBs (DB0 – DB10) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV & LINV are meant to be static digital signals. If they are to change during operation they should only change when the CLK is low (assuming PHASE is high, if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV and LINV have internal pull down devices. Please see the simplified logic circuit *NO TAG*

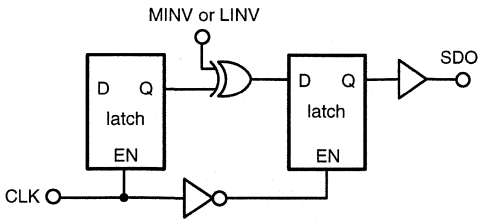


Figure 5. MINV, LINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *NO TAG* shows an equivalent input circuit.

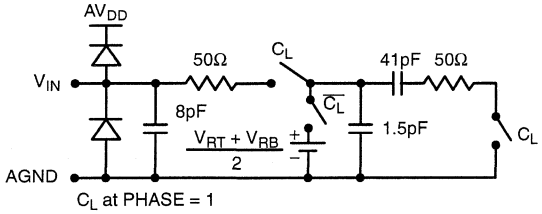


Figure 6. Equivalent Input Circuit

Reference Ladder Taps

These taps connect to every sixteenth point along the reference ladder; R4 is 4/16th up from V_{RB}, R7 is 7/16ths up from V_{RB}. These taps can be used to alter the transfer curve of the ADC. The internal interconnect resistance from the pin to the ladder is less than 3Ω for the even numbered taps, (i.e. R4,R6, etc.) and is approximately 10Ω for the odd numbered taps.

Altering the transfer curve may be desirable to enhance or minimize the probability of codes for a certain range of V_{IN}.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

0.8 V maximum per tap is recommended for applications above 85°C. Up to 1.6 V is allowed for applications under 85°C.

APPLICATION NOTES

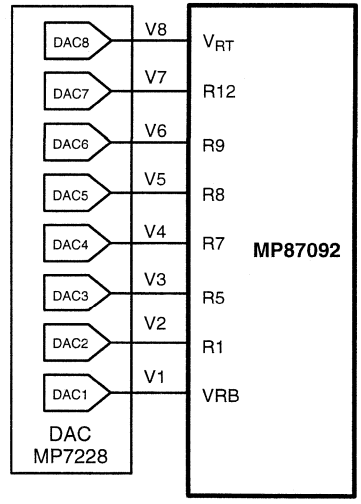
V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between any AGND or DGND pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

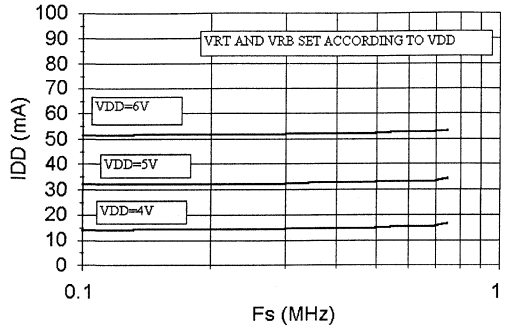
The reference tap pins (R1-R12) can be used to create piecewise-linear transfer functions. By forcing voltages on these pins, an 8 segment transfer function can be made. See *NO TAG*



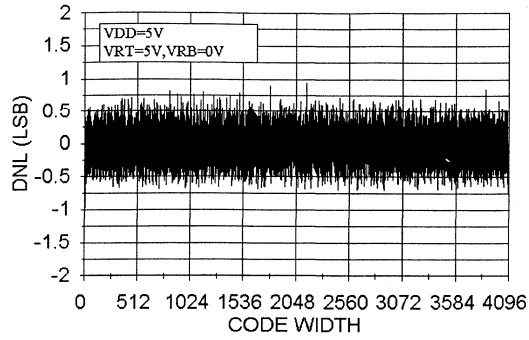
Only the Ladder detail shown.

Figure 7. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

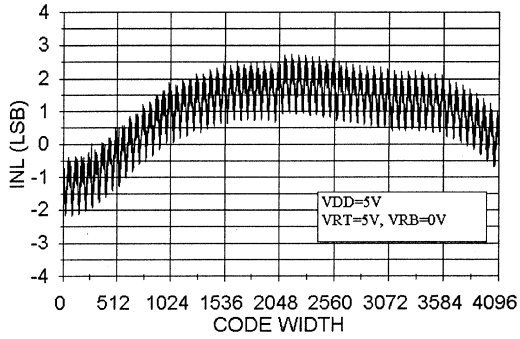
PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. F_S



Graph 2. DNL Error Plot



Graph 3. INL Error Plot

MP87095

CMOS
750 KSPS, Very Low Power, 10-Bit
Analog-to-Digital Converter

FEATURES

- 10-Bit Resolution
- Sampling Rates from <1 kHz to 750 KSPS
- DNL better than 1/2 LSB up to 750 kHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 750 kHz
- Single Power Supply (4 to 6.5 Volts)
- Latch-Up Free
- High ESD Protection: 4000 Volts Minimum
- 20 Pin Package: MP8796

BENEFITS

- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- Multiplexed Data Acquisition
- Radar Pulse Analysis
- Low Power A/D Applications

3

GENERAL DESCRIPTION

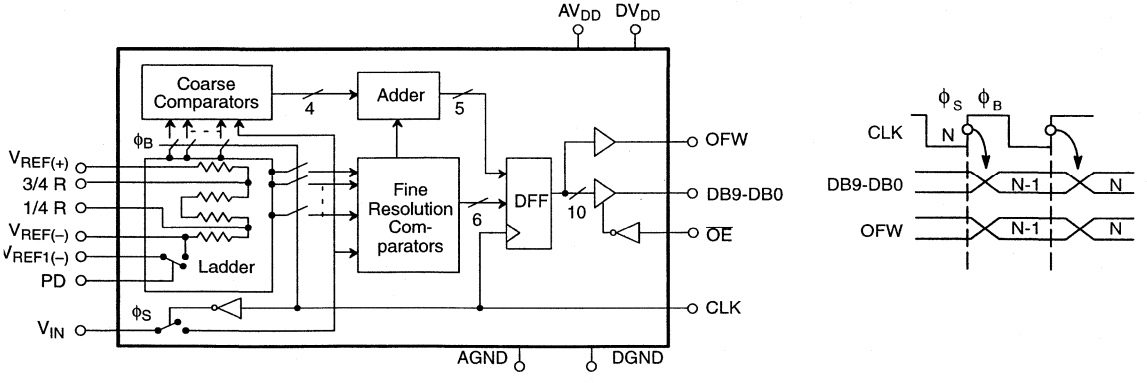
The MP87095 is a flexible, easy to use, precision 10-bit A/D Converter that operates over a wide range of input and sampling conditions. The MP87095 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 750 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications up to 750 kHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP87095 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor taps 1/4 R and 3/4 R allow for customizing the transfer curve. Digital outputs offer tri-state operation and all digital pins are CMOS and TTL compatible.

The MP87095 uses a subranging technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

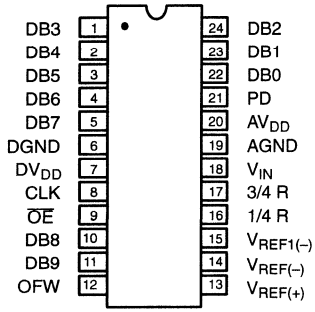
SIMPLIFIED BLOCK AND TIMING DIAGRAM



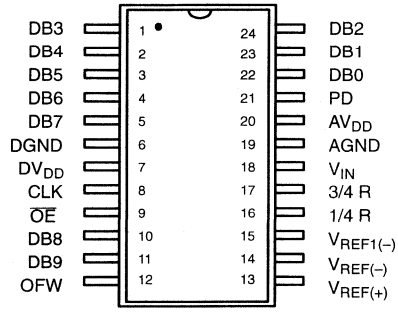
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP87095AN	±1	2
SOIC	–40 to +85°C	MP87095AS	±1	2

PIN CONFIGURATIONS



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(-)}$	Lower Reference Voltage
15	$V_{REF1(-)}$	Lower Reference Voltage
16	1/4 R	Reference Ladder Tap @ 1/4 FS
17	3/4 R	Reference Ladder Tap @ 3/4 FS
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	PD	Power Down
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S = 0.75$ MHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)} = AGND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		0.75	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+1.00		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance			12		Ω	
Ladder Switch Off Leakage	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	1 LSB Error
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, $\overline{OE}$ (Internal Res to GND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	500			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	Functional
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30	35	ns	
Data Valid Delay[1]	t_{DL}		35	45	ns	

3

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C_{OUT}=15 pF
Data Enable Delay[1]	t_{DEN}		25	30	ns	
Data Tristate Delay[1]	t_{DHZ}		15	30	ns	
Clock to PD Set-up Time[1]	t_{CLKS1}			400	ns	
Clock to PD Hold Time[1]	t_{CLKH1}			600	ns	
Power Down Delay[1]	t_{PD}			300	ns	
Power Up Delay[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{DDOWN}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

NOTES:

1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 5.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP87095 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

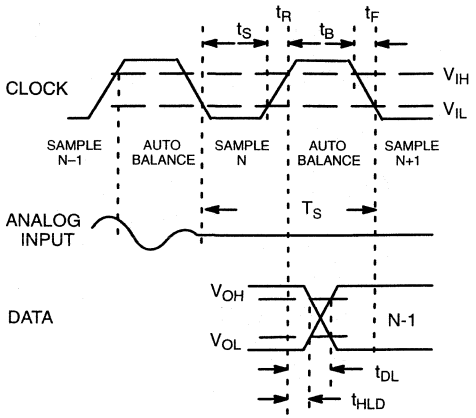


Figure 1. MP87095 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87095 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

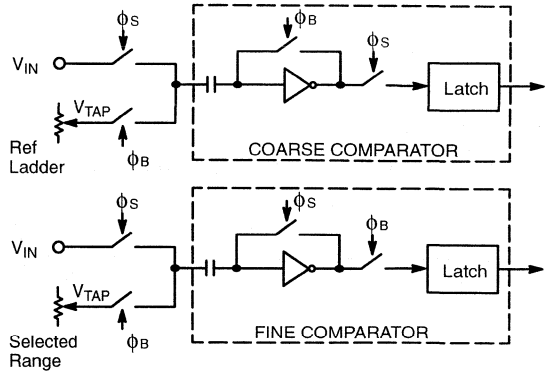


Figure 2. MP87095 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

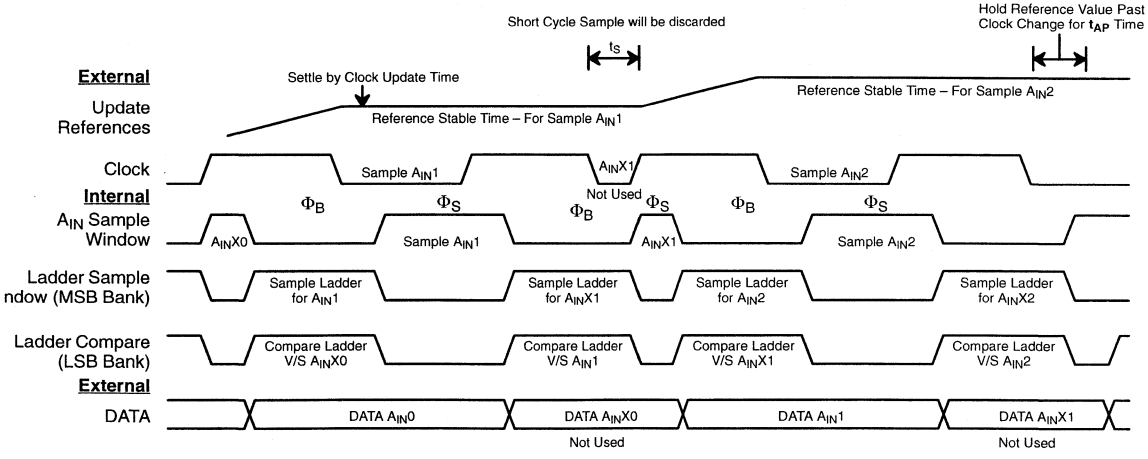


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

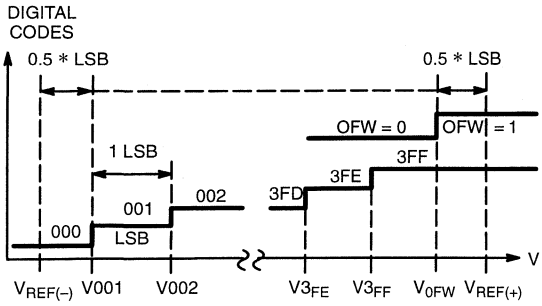


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V3_{FF} = V_{REF(-)} - 1.5 * LSB$

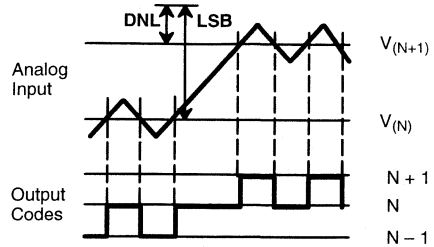
$LSB = V_{REF} / 1024 = (V3_{FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V3_{FF} - V3_{FE}$ – LSB

E_{FS} (full scale error) = $V3_{FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

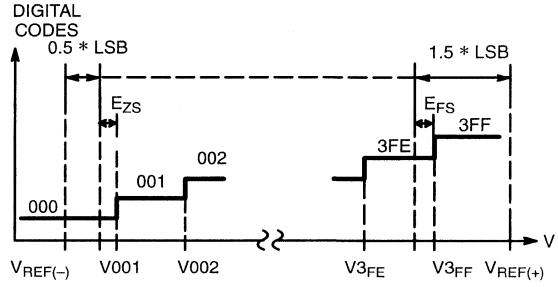


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

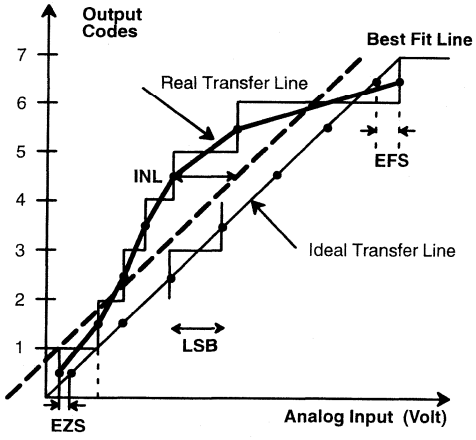


Figure 7. INL Error Calculation

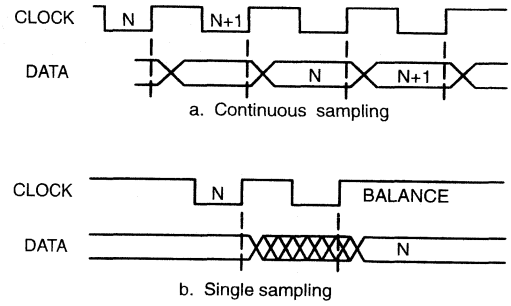


Figure 8. Relationship of Data to Clock

Analog Input

The MP87095 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87095's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

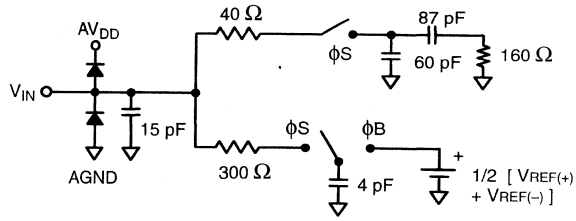


Figure 9. Analog Input Equivalent Circuit

Clock and Conversion Timing

A system will clock the MP87095 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87095 in balance and ready to sample the analog input.

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE}$ controls the output buffers in an asynchronous mode.

$\overline{OE}$	OFW	DB9 – DB0
1	Valid	High Z
0	Valid	Valid

Table 3. Output Enable Logic

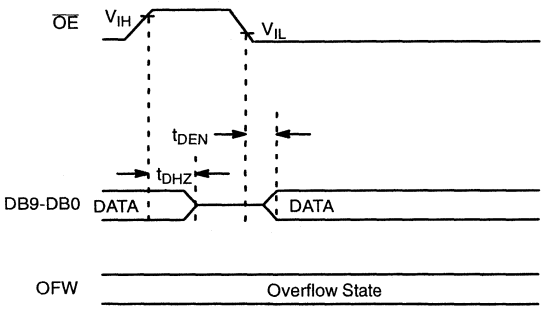


Figure 10. Output Enable/Disable Timing Diagram

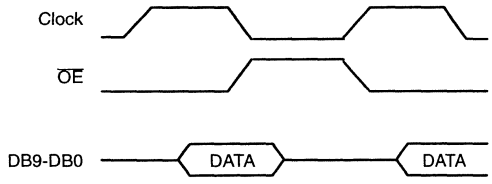


Figure 11. Preferred Output Control

Figure 11. shows the preferred output control where $\overline{OE}$ and clock are opposite phase. This provides a quiet time at the end of the A_{IN} sample phase.

The functional equivalent of the MP87095 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

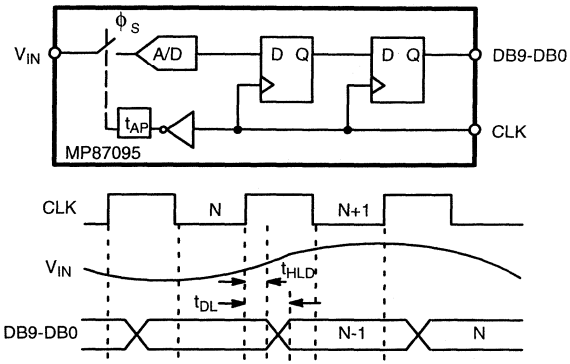


Figure 12. MP87095 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

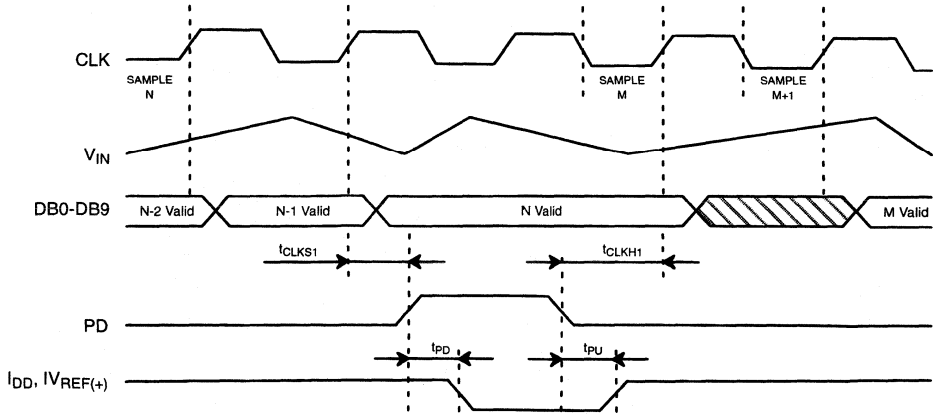


Figure 13. Power Down Timing Diagram

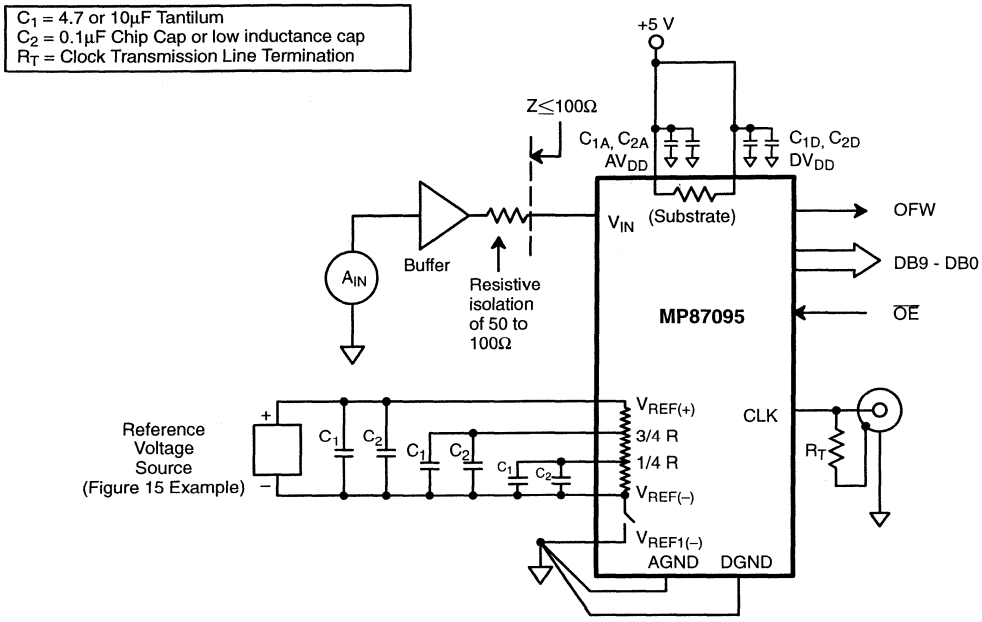


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87095.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87095. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87095.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87095 should be connected to AV_{DD} next to the MP87095.
8. DV_{DD} and AV_{DD} are connected inside the MP87095 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

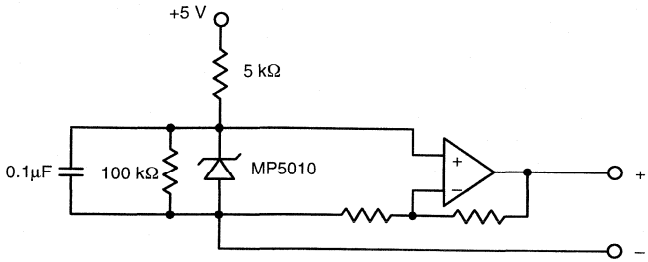
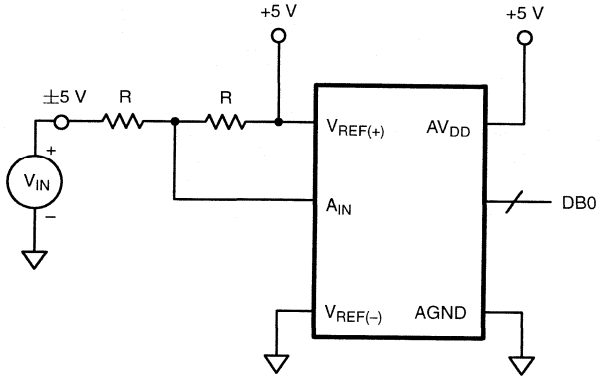


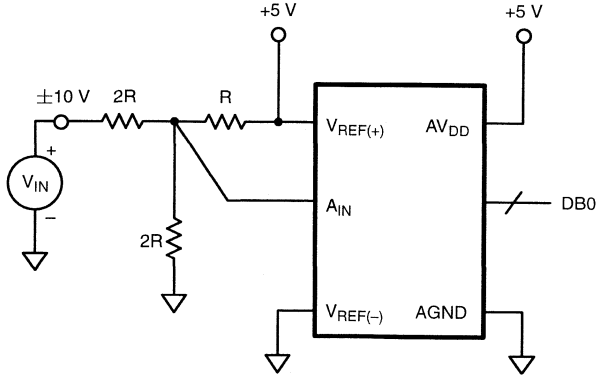
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

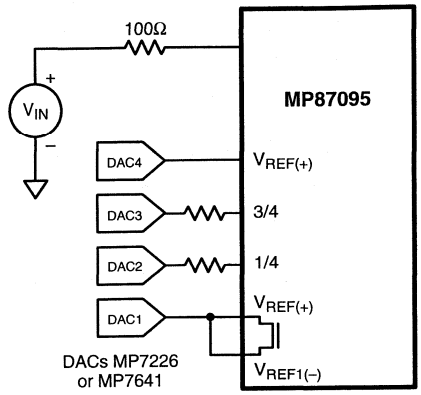
Figure 16. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

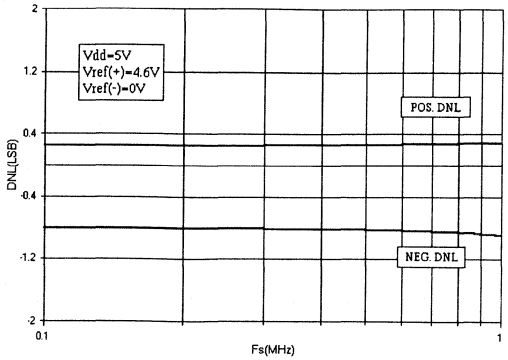
Figure 17. ±10 V Analog Input



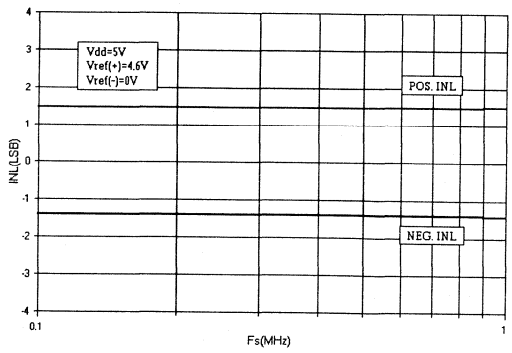
@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/4 and 3/4 TAP.)

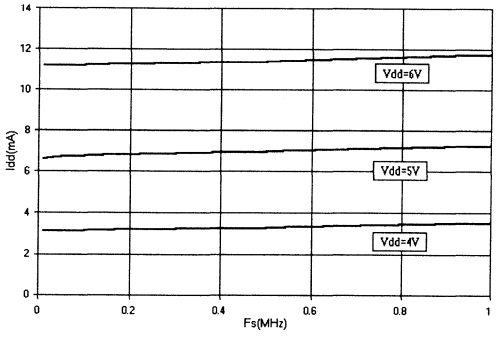
PERFORMANCE CHARACTERISTICS



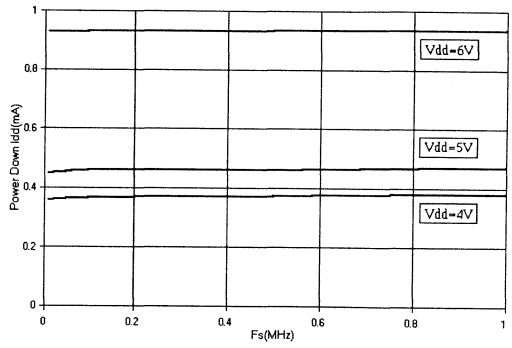
Graph 1. DNL vs. Sampling Frequency



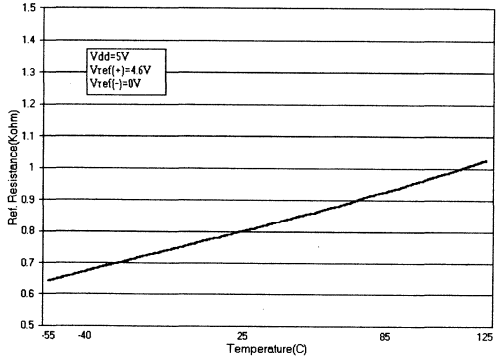
Graph 2. INL vs. Sampling Frequency



Graph 3. Supply Current vs. Sampling Frequency



Graph 4. Power Down Current vs. Sampling Frequency



Graph 5. Reference Resistance vs. Temperature

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MP87098

CMOS

Very Low Power, 750 KSPS, 10-Bit Analog-to-Digital Converter with 4-Channel Mux

FEATURES

- 10-Bit Resolution
- 4-Channel Mux
- Sampling Rates from <1 kHz to 750 kHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 750 kHz
- Single Power Supply (4 to 6 Volts)
- Latch-Up Free CMOS Technology
- High ESD Protection: 4000 Volts Minimum

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- Multiplexed Data Acquisition
- Low Power A/D Applications

3

GENERAL DESCRIPTION

The MP87098 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with a 4-channel mux that operates over a wide range of input and sampling conditions. The MP87098 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 750 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications up to 750 kHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP87098 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap 1/2 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

The MP87098 uses a subranging technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

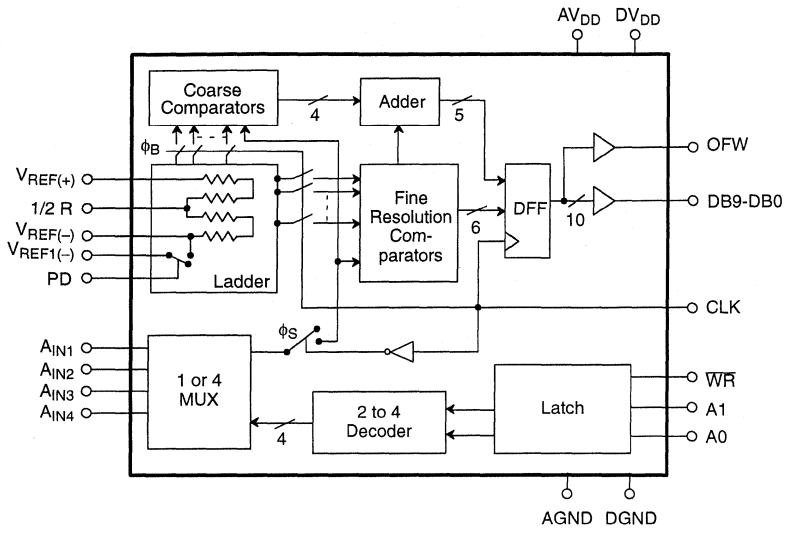
When the power down input is "high", the data outputs DB9 to DB0 hold their current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

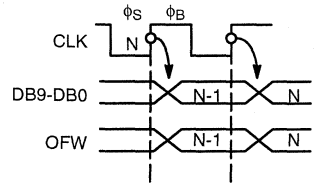
Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP87098 is available in Plastic dual-in-line (PDIP) and Surface Mount (SOIC), and Shrink Small Outline (SSOP) packages.

ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP87098AS	±1	2
PDIP	–40 to +85°C	MP87098AN	±1	2
SSOP	–40 to +85°C	MP87098AQ	±1	2

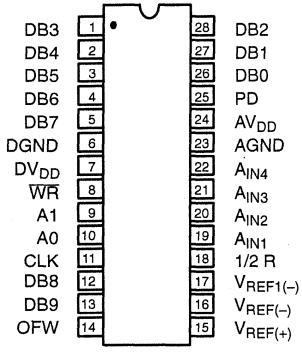
SIMPLIFIED BLOCK AND TIMING DIAGRAM



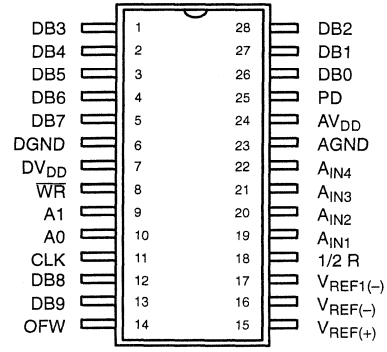


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (Jedec, 0.300") – S28
28 Pin SSOP – A28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	$\overline{WR}$	Write (Active Low)
9	A1	Address 1 Input
10	A0	Address 0 Input
11	CLK	Clock Input
12	DB8	Data Output Bit 8
13	DB9	Data Output Bit 9 (MSB)
14	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
15	$V_{REF(+)}$	Upper Reference Voltage
16	$V_{REF(-)}$	Lower Reference Voltage
17	$V_{REF1(-)}$	Lower Reference Voltage
18	1/2 R	Reference Ladder Tap
19	A_{IN1}	Analog Signal Input 1
20	A_{IN2}	Analog Signal Input 2
21	A_{IN3}	Analog Signal Input 3
22	A_{IN4}	Analog Signal Input 4
23	AGND	Analog Ground
24	AV_{DD}	Analog V_{DD}
25	PD	Power Down
26	DB0	Data Output Bit 0 (LSB)
27	DB1	Data Output Bit 1
28	DB2	Data Output Bit 2

3

TRUTH TABLE FOR INPUT CHANNEL SELECTION

$\overline{WR}$	A1	A0	SELECTED ANALOG INPUT
0	0	0	A_{IN1}
0	0	1	A_{IN2}
0	1	0	A_{IN3}
0	1	1	A_{IN4}
1	X	X	Previous selection

Note: $\overline{WR}$, A1, A0 are internally connected to GND through 500KΩ resistance.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, F_S = 750 kHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)}$ = AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	1		750	kHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL		±3/4	±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+0.50		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	ΔV_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance			12		Ω	
Ladder Switch Off Leakage	I_{LKG-SW}		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, (Internal Res to GND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	1000			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30	35	ns	
Data Valid Delay[1]	t_{DL}		35	45	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C_{OUT}=15 pF
Write Pulse Width[1]	t_{WR}	40			ns	
Multiplexer Address Setup Time[1]	t_{AS}	80			ns	
Multiplexer Address Hold Time[1]	t_{AH}	0			ns	
Delay from $\overline{WR}$ to Multiplexer[1] Enable	t_{MUXEN1}			80	ns	
Power Down Time[1]	t_{PD}			300	ns	
Power Up Time[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{PD-DD}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

3

NOTES:
1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 5.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP87098 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. They should go to the same potential and be separately decoupled.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to AGND, DGND) ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
SOIC, PDIP, SSOP 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

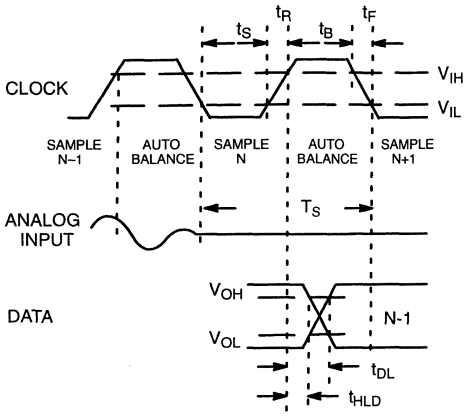


Figure 1. MP87098 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87098 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

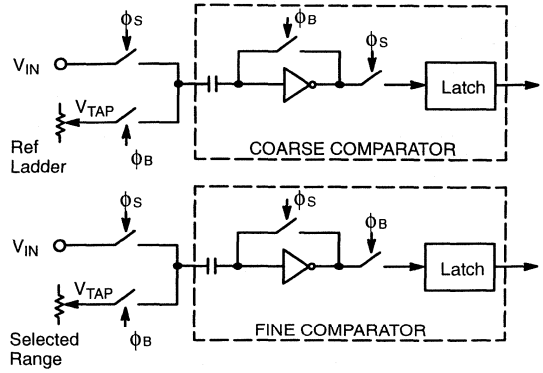


Figure 2. MP87098 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

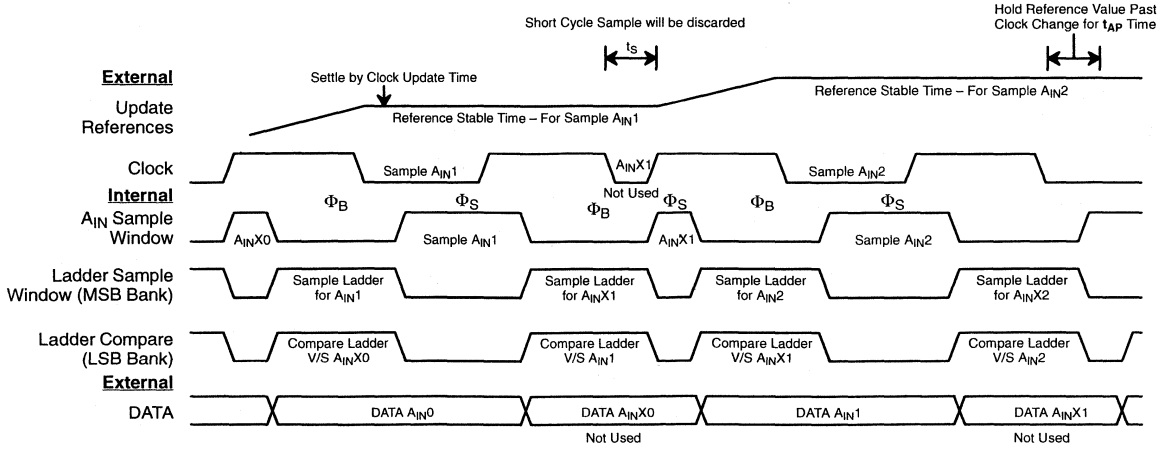


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

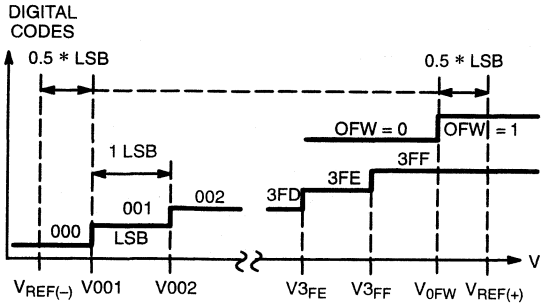


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V3_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 1024 = (V3_{FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.

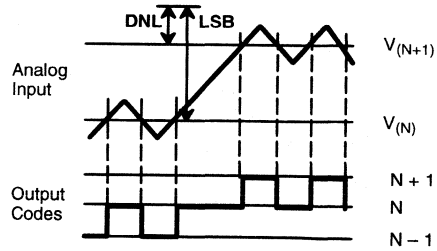


Figure 5. DNL Measurement On Production Tester

3

The formulas for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

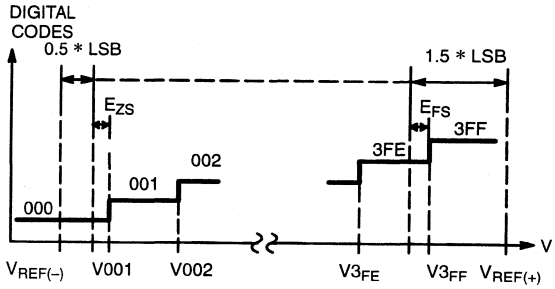


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

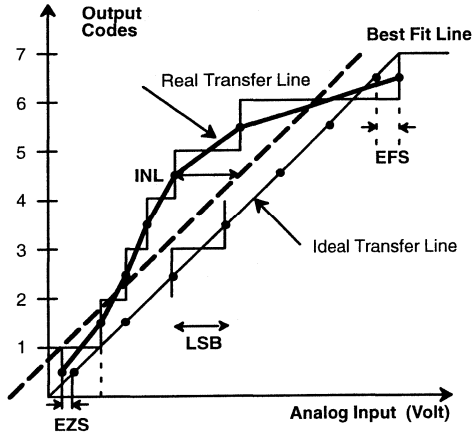


Figure 7. INL Error Calculation (Exaggerated for Visualization)

Clock and Conversion Timing

A system will clock the MP87098 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87098 in balance and ready to sample the analog input.

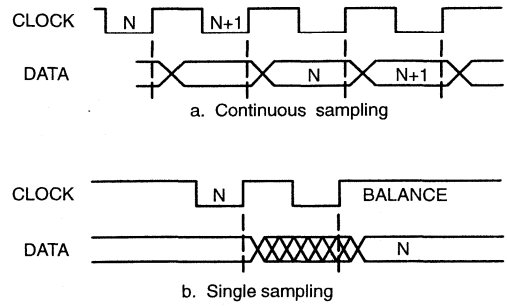


Figure 8. Relationship of Data to Clock

Analog Input

The MP87098 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87098's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

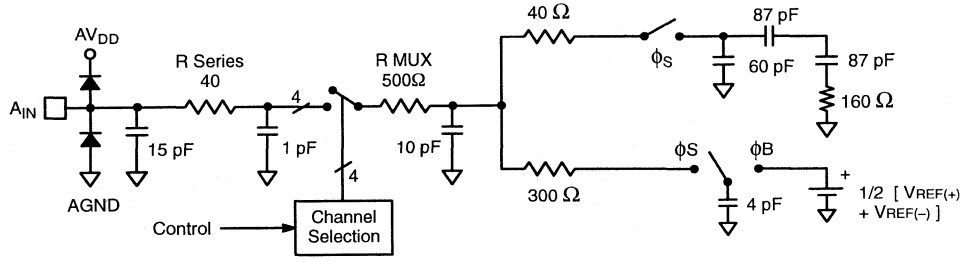


Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP87098 includes a 4-channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 10.* and *Figure 11.*

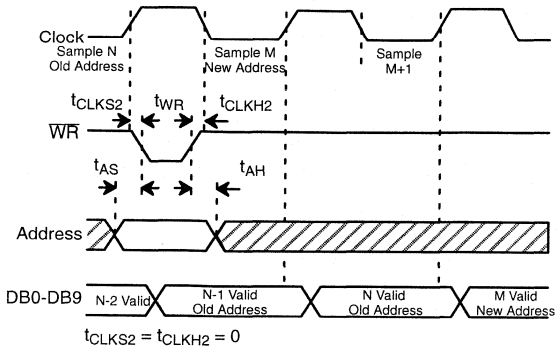


Figure 10. MUX Address Timing

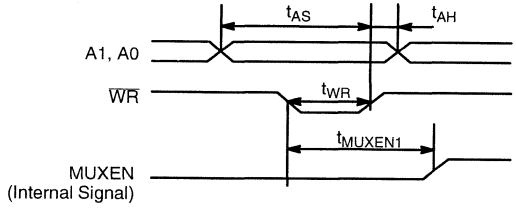


Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP87098 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts VIN with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

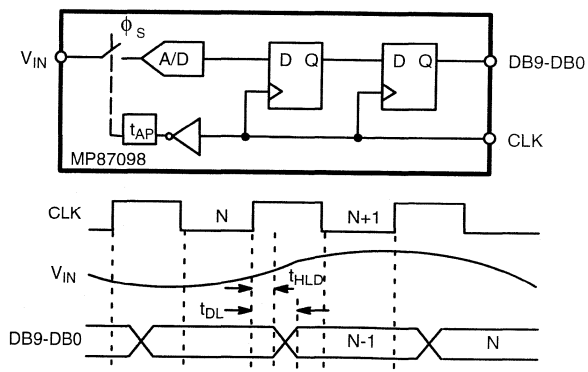


Figure 12. MP87098 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

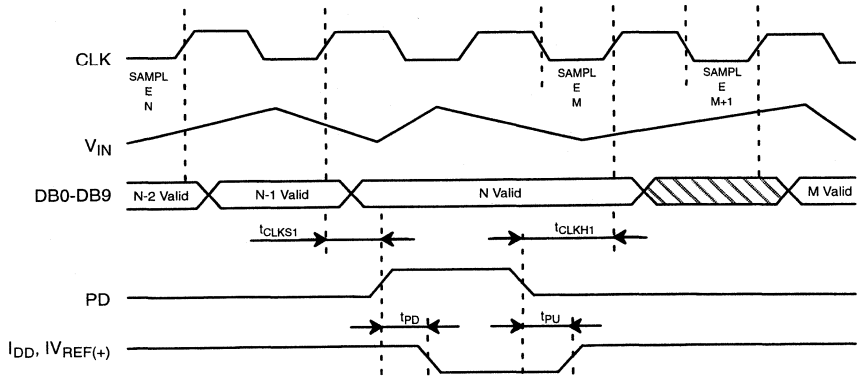


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance capacitor
R_T = Clock Transmission Line Termination

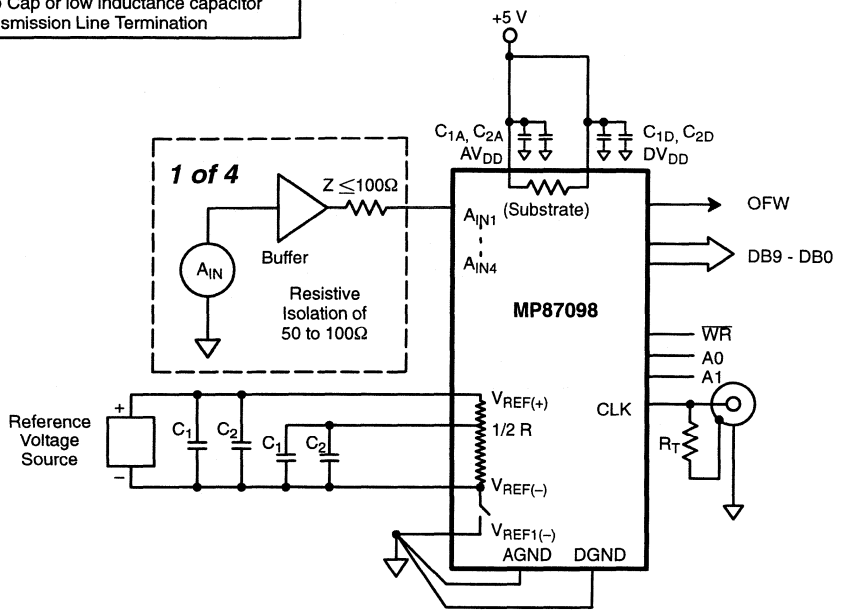


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87098.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87098. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87098.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87098 should be connected to AV_{DD} next to the MP87098.
8. DV_{DD} and AV_{DD} are connected inside the MP87098 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

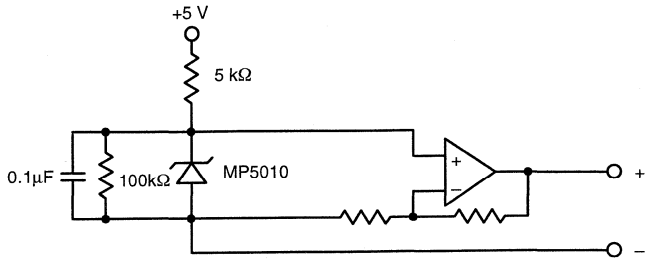
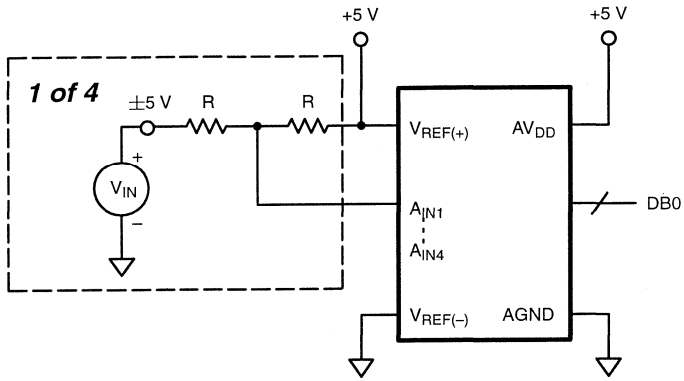


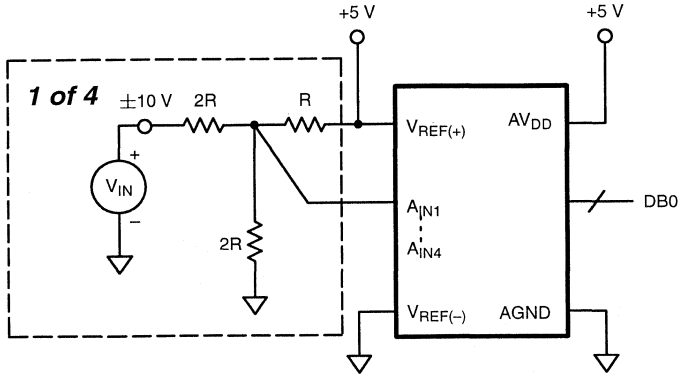
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

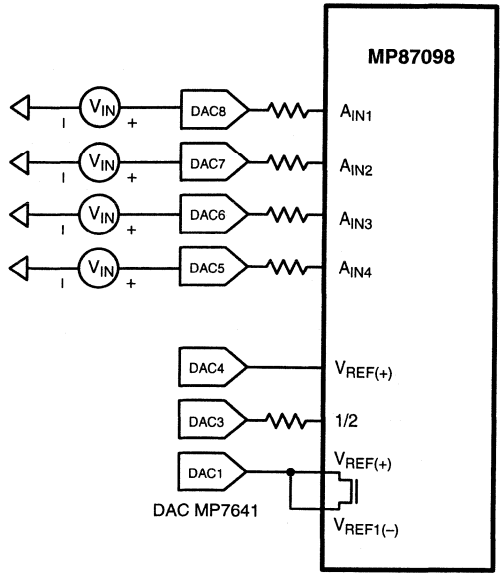
Figure 16. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 17. ±10 V Analog Input

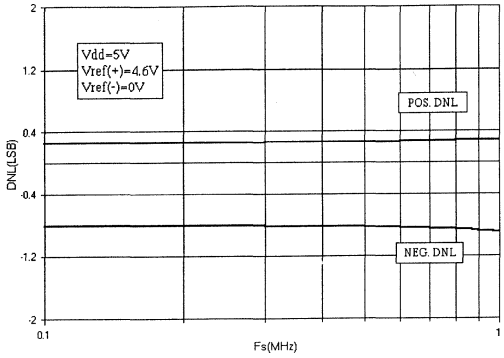


@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.

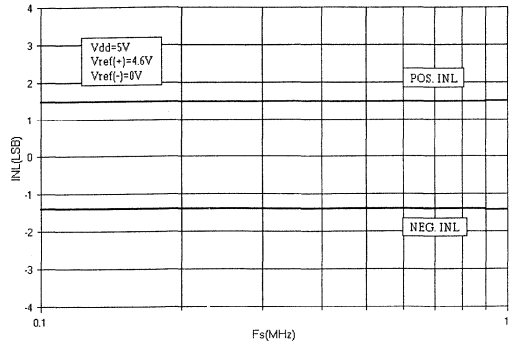
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder and A_{IN} with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/2 TAP.)

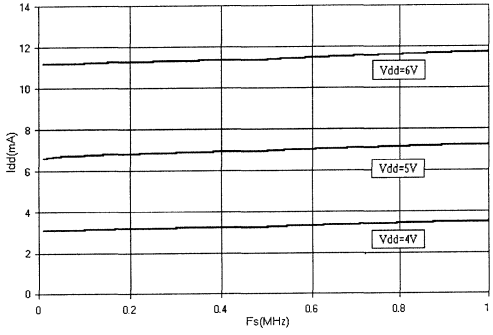
PERFORMANCE CHARACTERISTICS



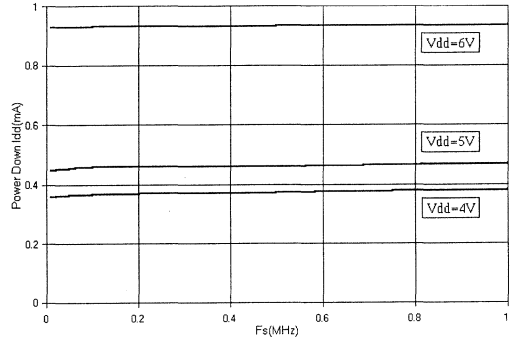
Graph 1. DNL vs. Sampling Frequency



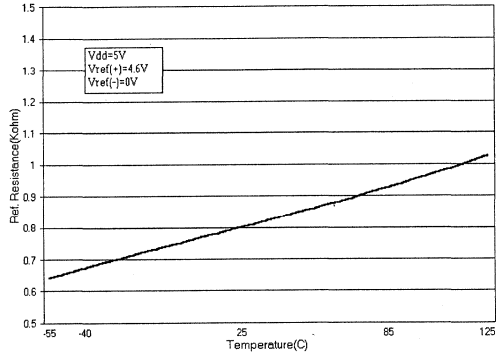
Graph 2. INL vs. Sampling Frequency



Graph 3. Supply Current vs. Sampling Frequency



Graph 4. Power Down Current vs. Sampling Frequency



Graph 5. Reference Resistance vs. Temperature

MP87099

CMOS
Very Low Power, 750 KSPS, 10-Bit
Analog-to-Digital Converter with 8-Channel Mux

FEATURES

- 10-Bit Resolution
- 8-Channel Mux
- Sampling Rates from <1 kHz to 750 kHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 750 kHz
- Single Power Supply (4 to 6 Volts)
- Latch-Up Free CMOS Technology
- High ESD Protection: 4000 Volts Minimum

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- Multiplexed Data Acquisition
- Low Power A/D Applications

3

GENERAL DESCRIPTION

The MP87099 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with 8-channel mux that operates over a wide range of input and sampling conditions. The MP87099 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 750 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications up to 750 kHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP87099 allows direct interface to any analog input range between GND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

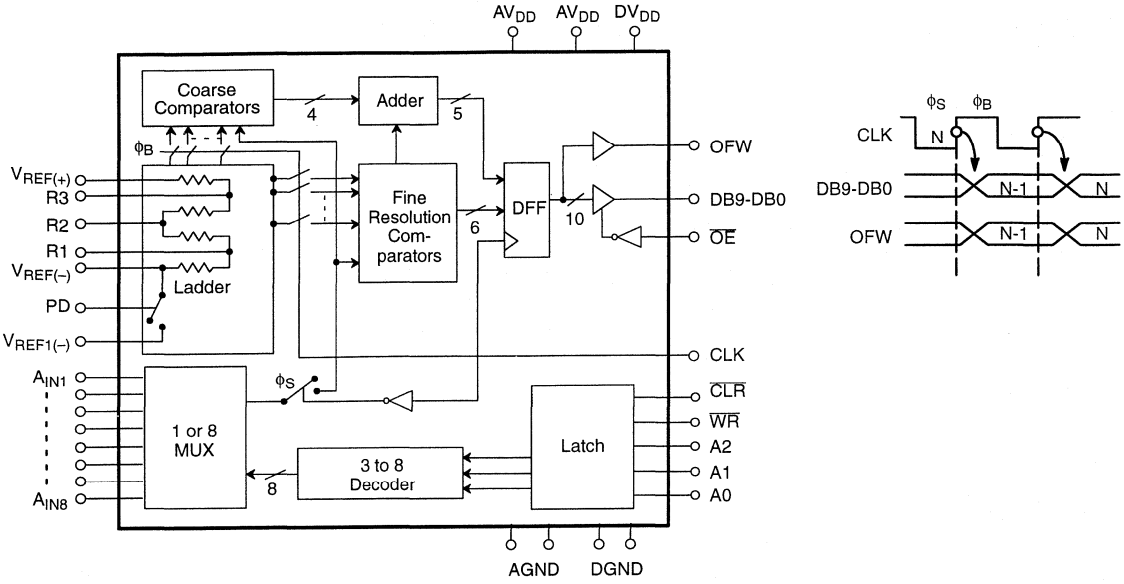
Scaled reference resistor tap @ 1/4 R, 1/2 R, and 3/4 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

The MP87099 uses a subranging technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

ORDERING INFORMATION

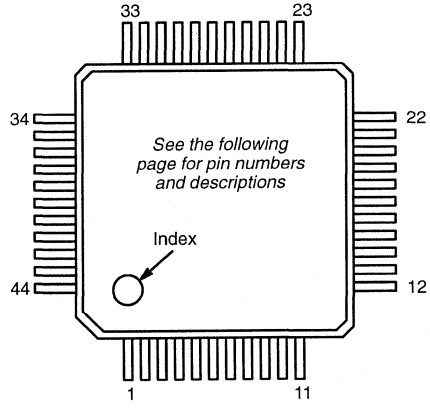
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP87099AE	±1	2

SIMPLIFIED BLOCK AND TIMING DIAGRAM



PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



44-Pin PQFP (10mm x 10mm)
QN44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB6	Data Output Bit 6
2	DB7	Data Output Bit 7
3	DGND	Digital Ground
4	DGND	Digital Ground
5	DV_{DD}	Digital V_{DD}
6	$\overline{CLR}$	Clear (Active Low)
7	$\overline{WR}$	Write (Active Low)
8	A2	Address 2
9	A1	Address 1
10	A0	Address 0
11	CLK	Clock Input
12	$\overline{OE}$	Output Enable (Active Low)
13	N/C	No Connect
14	DB8	Data Output Bit 8
15	DB9	Data Output Bit 9 (MSB)
16	OFW	Overflow Output
17	$V_{REF(+)}$	Upper Reference Voltage
18	$V_{REF(-)}$	Lower Reference Voltage
19	$V_{REF1(-)}$	Lower Reference Voltage
20	R1	Reference Ladder Tap
21	R2	Reference Ladder Tap
22	A_{IN8}	Analog Signal Input 8

PIN NO.	NAME	DESCRIPTION
23	R3	Reference Ladder Tap
24	N/C	No Connect
25	A_{IN1}	Analog Signal Input 1
26	A_{IN2}	Analog Signal Input 2
27	A_{IN3}	Analog Signal Input 3
28	A_{IN4}	Analog Signal Input 4
29	A_{IN5}	Analog Signal Input 5
30	AGND	Analog Ground
31	AV_{DD}	Analog V_{DD}
32	AV_{DD}	Analog V_{DD}
33	A_{IN6}	Analog Signal Input 6
34	AGND	Analog Ground
35	PD	Power Down
36	A_{IN7}	Analog Signal Input 7
37	DB0	Data Output Bit 0 (LSB)
38	DB1	Data Output Bit 1
39	DB2	Data Output Bit 2
40	DB3	Data Output Bit 3
41	DB4	Data Output Bit 4
42	DB5	Data Output Bit 5
43	N/C	No Connect
44	N/C	No Connect

3

TRUTH TABLE FOR INPUT CHANNEL SELECTION

$\overline{CLR}$	$\overline{WR}$	A2	A1	A0	Selected Analog Input
L	X	X	X	X	A_{IN1}
H	L	L	L	L	A_{IN1}
H	L	L	L	H	A_{IN2}
H	L	L	H	L	A_{IN3}
H	L	L	H	H	A_{IN4}
H	L	H	L	L	A_{IN5}
H	L	H	L	H	A_{IN6}
H	L	H	H	L	A_{IN7}
H	L	H	H	H	A_{IN8}
H	H	X	X	X	Previous Selection

Note: $\overline{CLR}$, $\overline{WR}$, A2, A1, A0 are internally connected to ground through 500k Ω resistance.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 750 kHz (50% Duty Cycle), $V_{REF(+)}$ = 4.6, $V_{REF(-)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	1		750	kHz	For Rated Performance
ACCURACY (A Grade)[2]						
Differential Non-Linearity	DNL		±3/4	±1	LSB	LSB
Integral Non-Linearity	INL			2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+0.50		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance			12		Ω	
Ladder Switch Off Leakage	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, $\overline{OE}$ (Internal Res to GND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	1000			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30	35	ns	
Data Valid Delay[1]	t_{DL}		35	45	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C_{OUT}=15 pF
Write Pulse Width[1]	t_{WR}	40			ns	
Multiplexer Address Setup Time[1]	t_{AS}	80			ns	
Multiplexer Address Hold Time[1]	t_{AH}	0			ns	
Delay from $\overline{WR}$ to Multiplexer[1] Enable	t_{MUXEN1}			80	ns	
Power Down Time[1]	t_{PD}			300	ns	
Power Up Time[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{PD-DD}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

3

NOTES:
1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 4.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP87099 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. They should go to the same voltage and be separately decoupled.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +7 V
$V_{REF(+)}$, $V_{REF(-)}$, $V_{REF1(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
All A_{INs} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PQFP 450mW
Derates above 75°C ..... 14mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

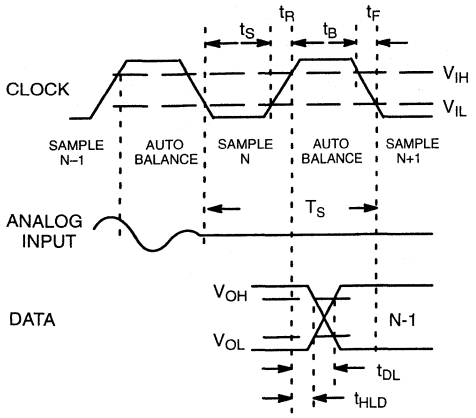


Figure 1. MP87099 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87099 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

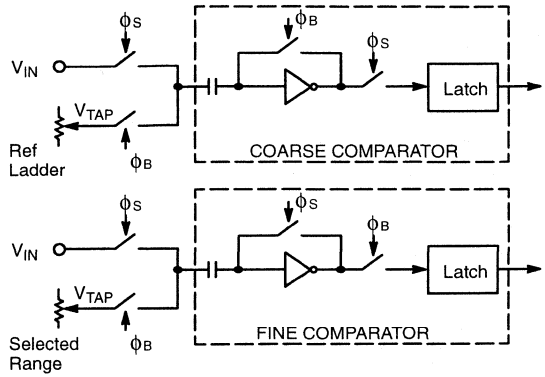


Figure 2. MP87099 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

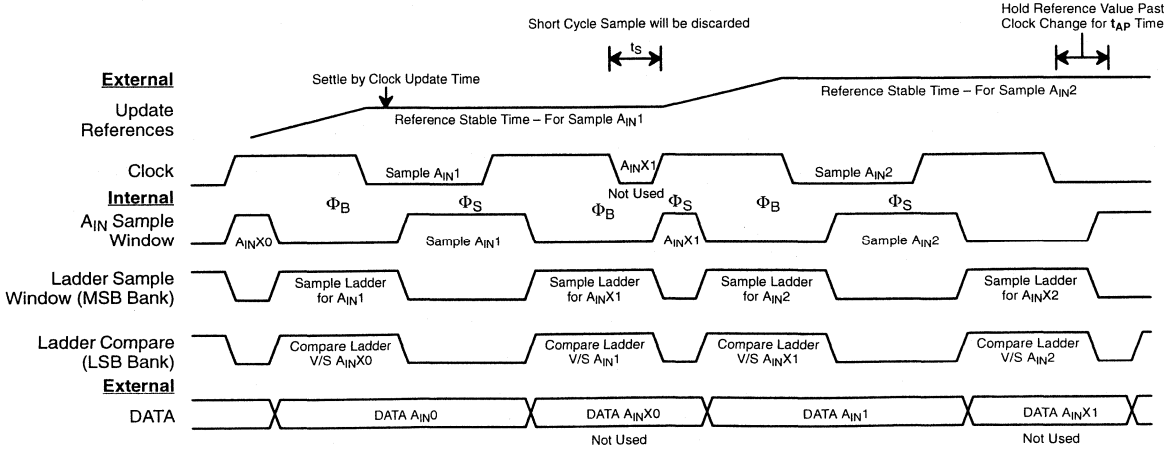


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

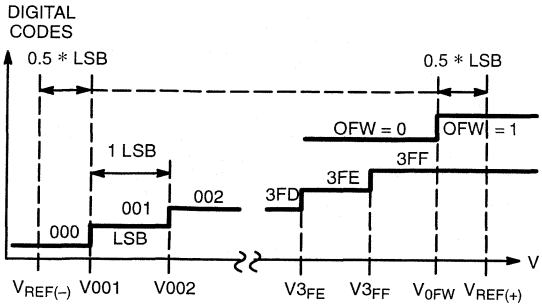


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V3_{FF} = V_{REF(-)} - 1.5 * LSB$

$LSB = V_{REF} / 1024 = (V3_{FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.

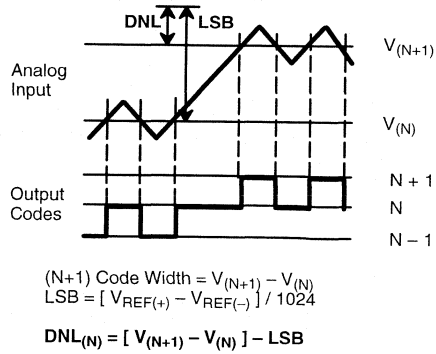


Figure 5. DNL Measurement On Production Tester

3

The formulas for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

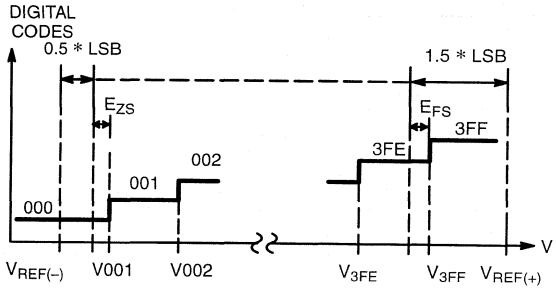


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

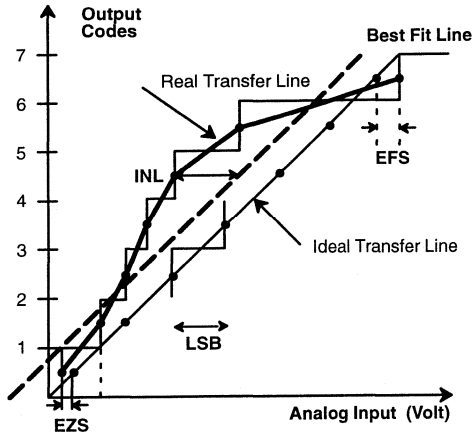


Figure 7. INL Error Calculation (Exaggerated for Visualization)

Clock and Conversion Timing

A system will clock the MP87099 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87099 in balance and ready to sample the analog input.

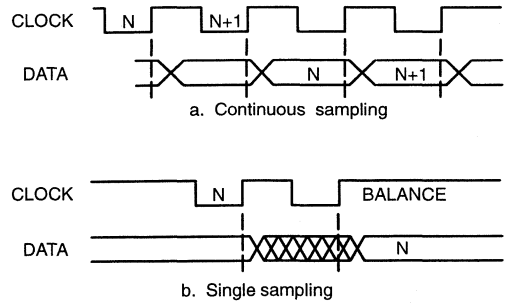


Figure 8. Relationship of Data to Clock

Analog Input

The MP87099 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87099's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

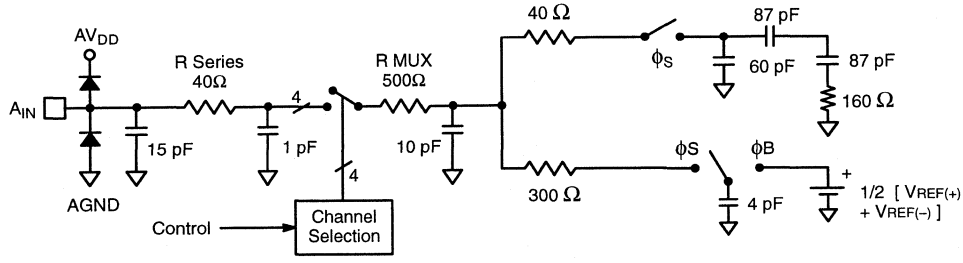


Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP87099 includes a 8-Channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 10.* and *Figure 11.*

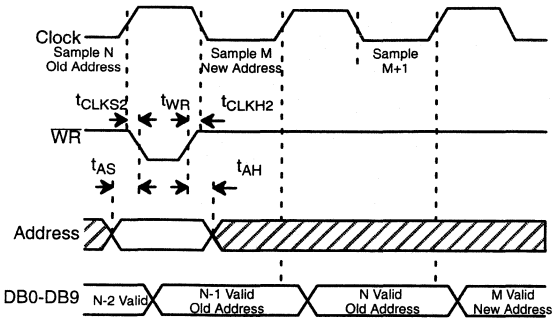


Figure 10. MUX Address Timing

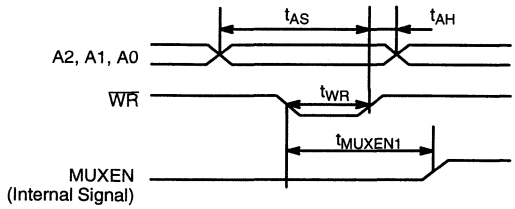


Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP87099 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts VIN with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

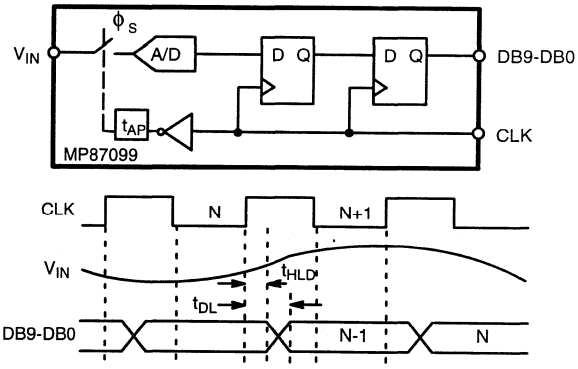


Figure 12. MP87099 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

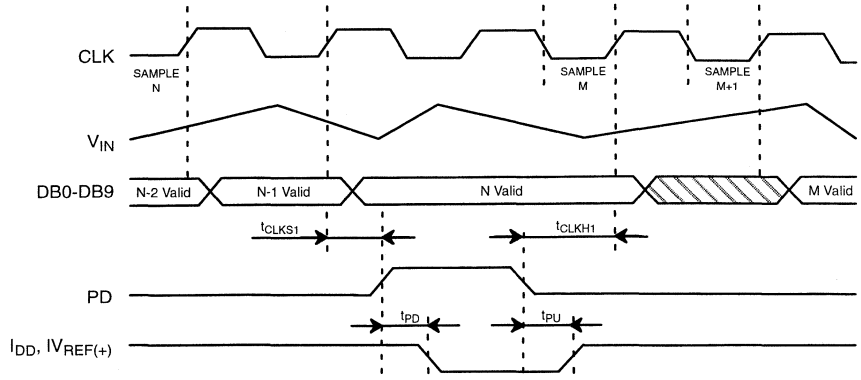


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance cap
R_T = Clock Transmition Line Termination

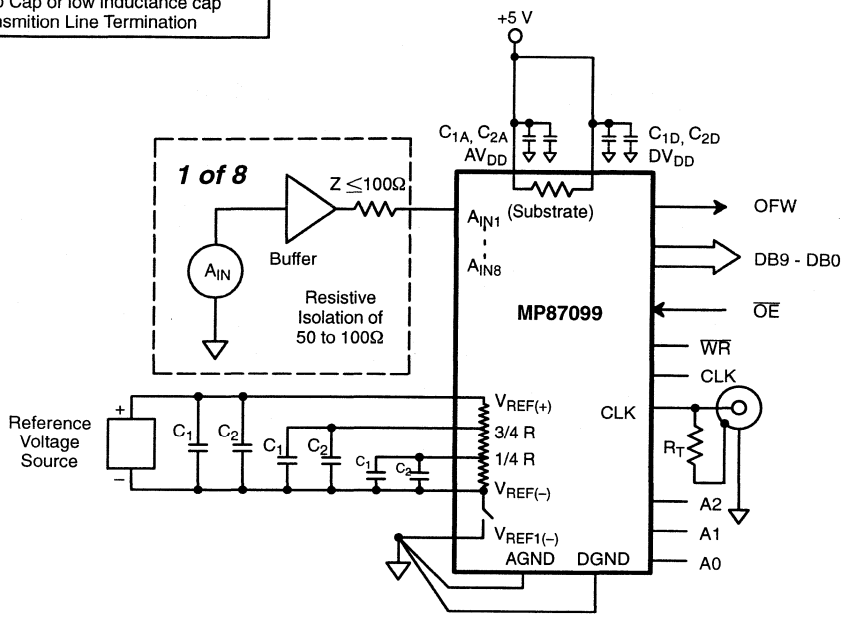


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87099.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87099. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87099.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87099 should be connected to AV_{DD} next to the MP87099.
8. DV_{DD} and AV_{DD} are connected inside the MP87099 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

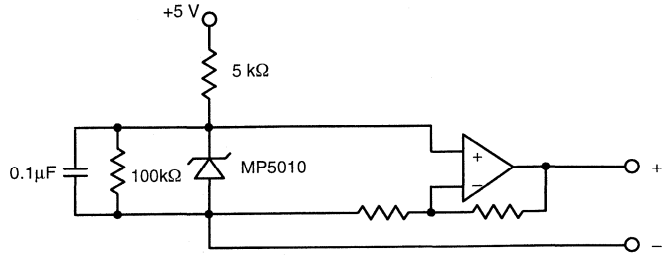
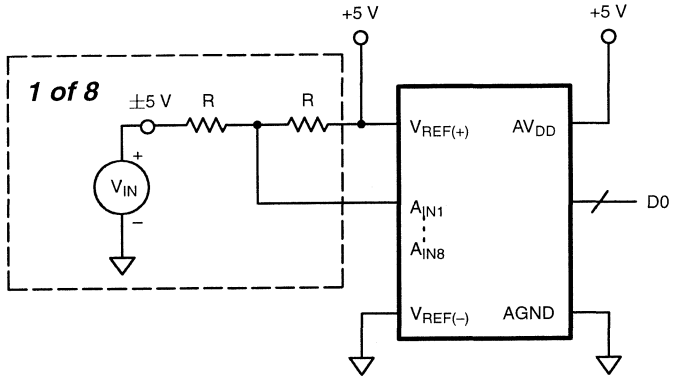


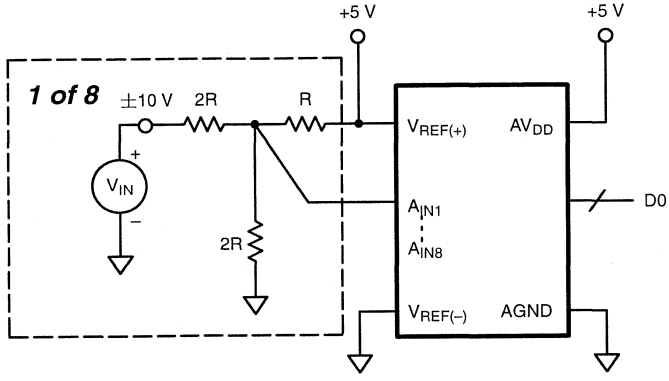
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

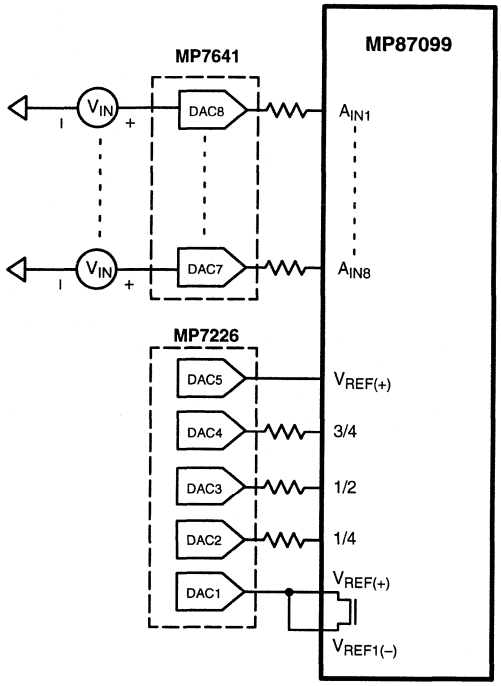
Figure 16. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

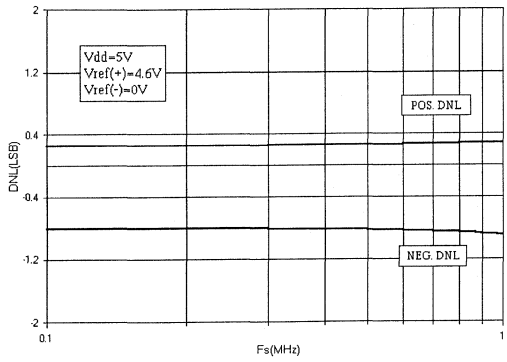
Figure 17. ±10 V Analog Input



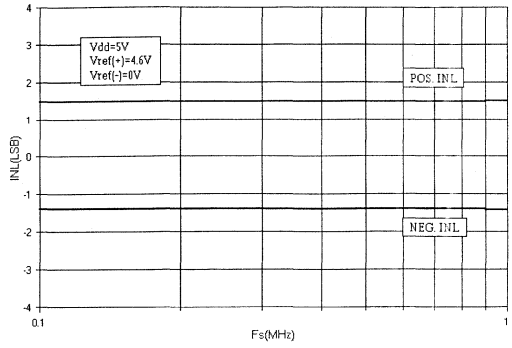
@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder and A_{IN} with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/4, 1/2 and 3/4 TAP.)

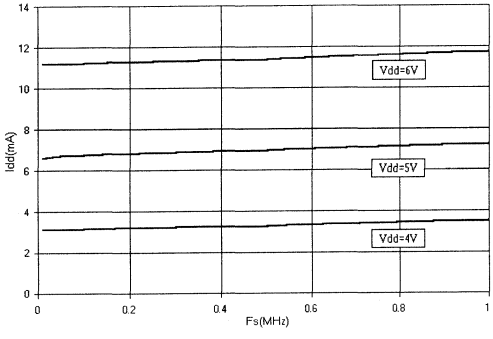
PERFORMANCE CHARACTERISTICS



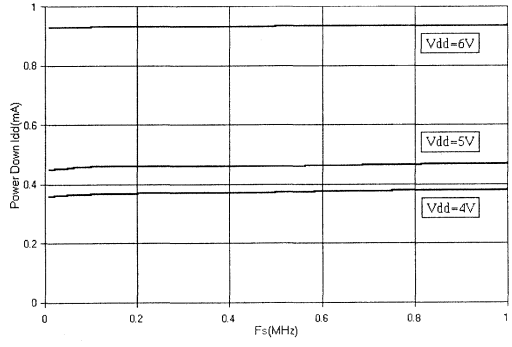
Graph 1. DNL vs. Sampling Frequency



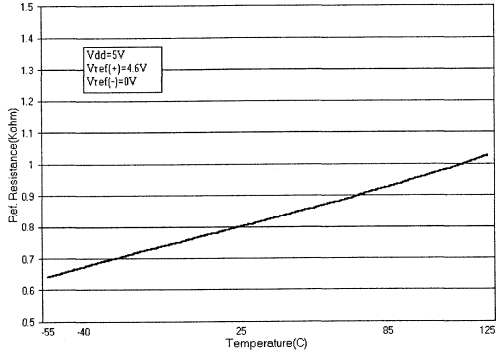
Graph 2. INL vs. Sampling Frequency



Graph 3. Supply Current vs. Sampling Frequency



Graph 4. Power Down Current vs. Sampling Frequency



Graph 5. Reference Resistance vs. Temperature

MP87198

CMOS
Very Low Power, 1 MSPS 10-Bit
Analog-to-Digital Converter with 4-Channel Mux

FEATURES

- 10-Bit Resolution
- 4-Channel Mux
- Sampling Rates from <1.5 kHz to 1.0 MHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 1 MHz
- Single Power Supply (4 to 6.5 Volts)
- Latch-Up Free CMOS Technology
- High ESD Protection: 4000 Volts Minimum

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- High Resolution Imaging – Scanners & Copiers
- Wireless Digital Communications
- Multiplexed Data Acquisition

3

GENERAL DESCRIPTION

The MP87198 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with 4-channel mux that operates over a wide range of input and sampling conditions. The MP87198 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 1 MHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 1 MHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP87198 allows direct interface to any analog input range between GND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap 1/2 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

The MP87198 uses a subranging technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

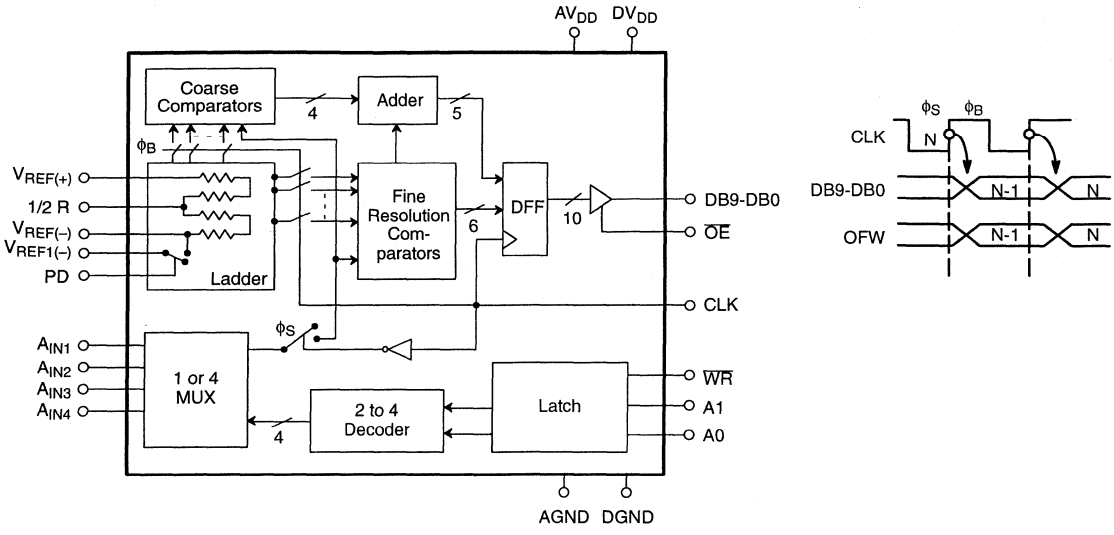
When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

Specified for operation over the commerical / industrial (–40 to +855C) temperature range, the MP87198 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC), and Shrunk Small Outline (SSOP) packages.

ORDERING INFORMATION

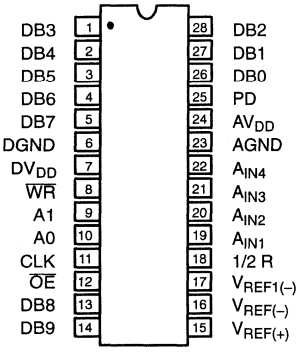
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP87198AS	±1	2
PDIP	–40 to +85°C	MP87198AN	±1	2
SSOP	–40 to +85°C	MP87198AQ	±1	2

SIMPLIFIED BLOCK AND TIMING DIAGRAM

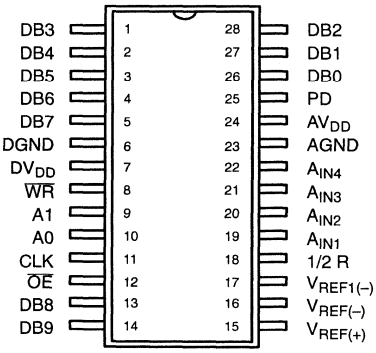


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (Jedec, 0.300") – S28
28 Pin SSOP – A28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	$\overline{WR}$	Write (Active Low)
9	A1	Address 1 Input
10	A0	Address 0 Input
11	CLK	Clock Input
12	$\overline{OE}$	Output Enable
13	DB8	Data Output Bit 8
14	DB9	Data Output Bit 9 (MSB)

PIN NO.	NAME	DESCRIPTION
15	$V_{REF(+)}$	Upper Reference Voltage
16	$V_{REF(-)}$	Lower Reference Voltage
17	$V_{REF1(-)}$	Lower Reference Voltage
18	1/2 R	Reference Ladder Tap
19	A_{IN1}	Analog Signal Input 1
20	A_{IN2}	Analog Signal Input 2
21	A_{IN3}	Analog Signal Input 3
22	A_{IN4}	Analog Signal Input 4
23	AGND	Analog Ground
24	AV_{DD}	Analog V_{DD}
25	PD	Power Down
26	DB0	Data Output Bit 0 (LSB)
27	DB1	Data Output Bit 1
28	DB2	Data Output Bit 2

3

TRUTH TABLE FOR INPUT CHANNEL SELECTION

$\overline{WR}$	A1	A0	SELECTED ANALOG INPUT
0	0	0	A_{IN1}
0	0	1	A_{IN2}
0	1	0	A_{IN3}
0	1	1	A_{IN4}
1	X	X	Previous selection

Note: $\overline{WR}$, A1, A0 are internally connected to GND through 500kΩ resistance.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, F_S = 1.0 MHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)}$ = AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		1	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+0.50		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	ΔV_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance[1]			12		Ω	
Ladder Switch Off Leakage	I_{LKG-SW}		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			100		kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		35	45	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
$\overline{OE}$, PD, (Internal Res to GND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	t_S	1000			ns	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	250		500,000	ns	
"Low" Time[6]	t_S	150		500,000	ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30	35	ns	
Data Valid Delay[1]	t_{DL}		35	45	ns	
Write Pulse Width[1]	t_{WR}	40			ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)				C_{OUT}=15 pF		
Multiplexer Address Setup Time[1]	t_{AS}	80			ns	
Multiplexer Address Hold Time[1]	t_{AH}	0			ns	
Delay from $\overline{WR}$ to Multiplexer[1] Enable	t_{MUXEN1}			80	ns	
Power Down Time[1]	t_{PD}			300	ns	
Power Up Time[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{PD-DD}		0.6	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10	mA	V_{IN} = 2 V

NOTES:

1 Guaranteed. Not tested.

2 Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 5.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).

3 See V_{IN} input equivalent circuit (*see Figure 9.*).

4 Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.

5 Specified values guarantee functional device. Refer to other parameters for accuracy.

6 System can clock MP87198 with any duty cycle as long as all timing conditions are met.

7 Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.

8 DV_{DD} and AV_{DD} are connected through the silicon substrate. They should go to the same voltage and be separately decoupled.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to AGND, DGND) ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... DGND –0.5 to DV_{DD} +0.5 V

V_{IN} ..... DGND –0.5 to DV_{DD} +0.5 V

All Inputs ..... DGND –0.5 to DV_{DD} +0.5 V

All Outputs ..... DGND –0.5 to DV_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

SOIC, PDIP, SSOP 1000mW

Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

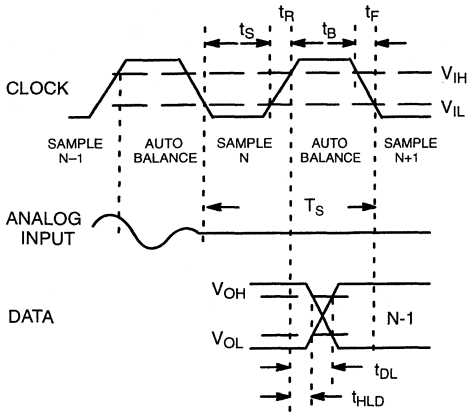


Figure 1. MP87198 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87198 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

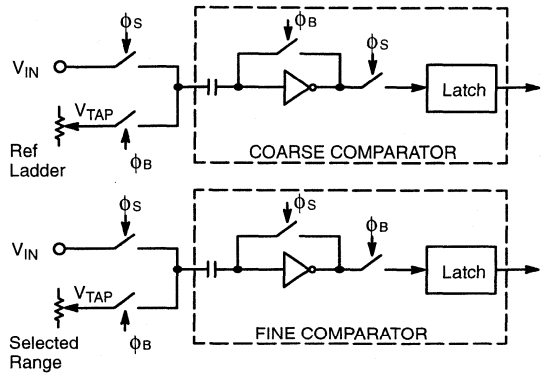


Figure 2. MP87198 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

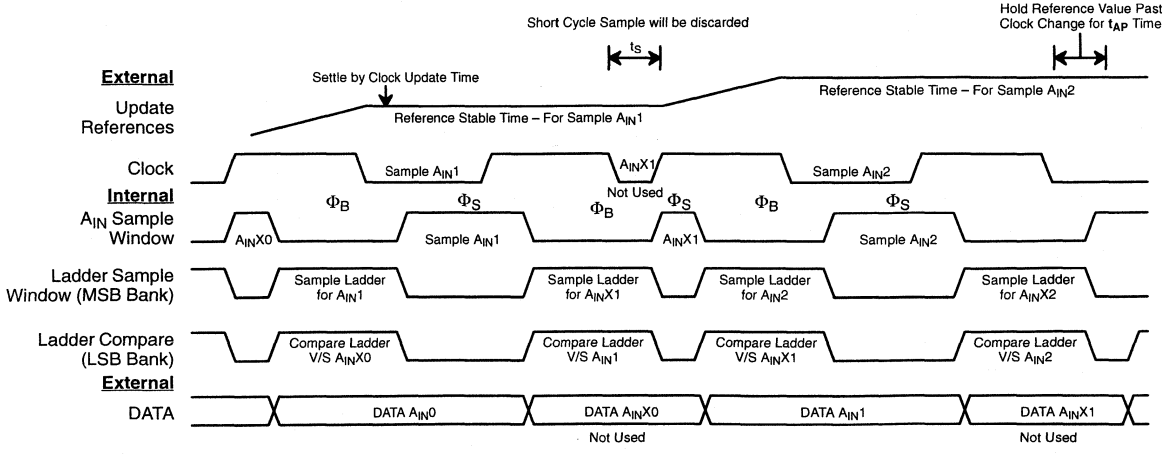


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

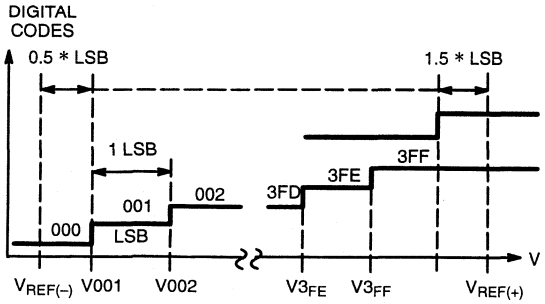


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V3_{FF} = V_{REF(+)} - 1.5 * LSB$

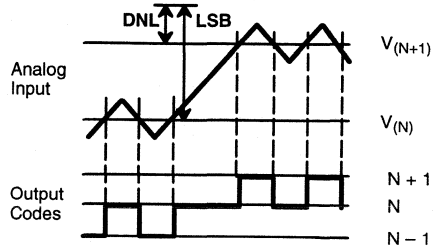
$LSB = V_{REF} / 1024 = (V3_{FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

3

The formulas for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

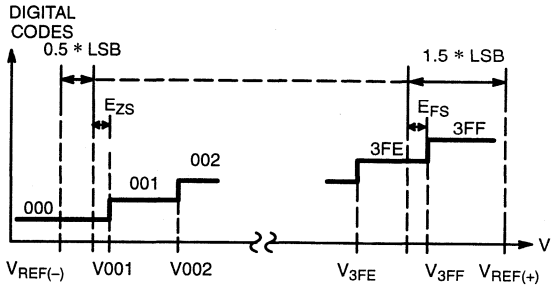


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

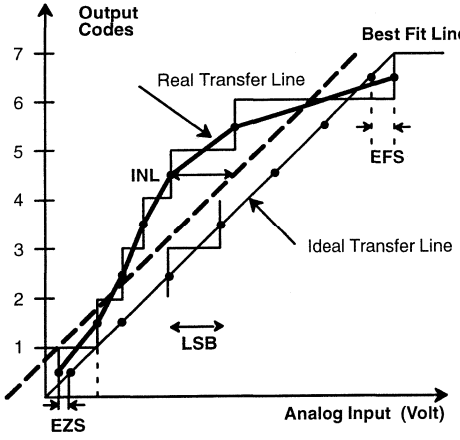


Figure 7. INL Error Calculation (Exaggerated for Visualization)

Clock and Conversion Timing

A system will clock the MP87198 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87198 in balance and ready to sample the analog input.

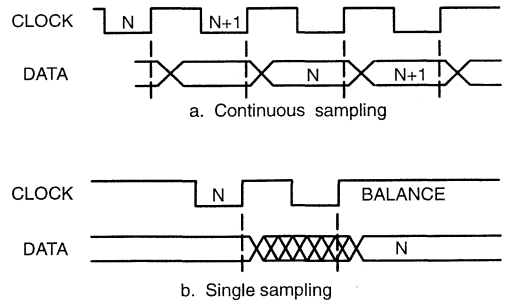


Figure 8. Relationship of Data to Clock

Analog Input

The MP87198 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87198's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *Figure 9.* shows the equivalent circuit for A_{IN}.

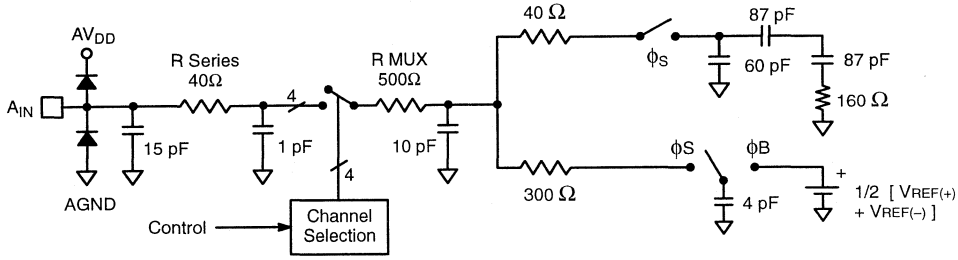


Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP87198 includes a 4-channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 10.* and *Figure 11.*

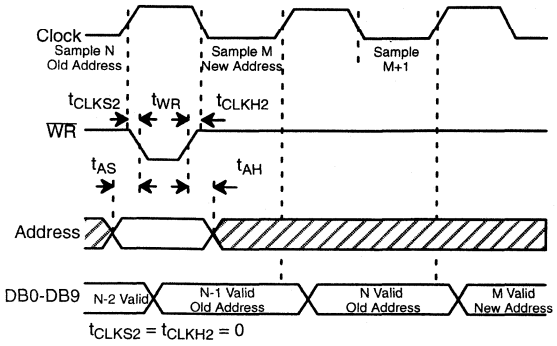


Figure 10. MUX Address Timing

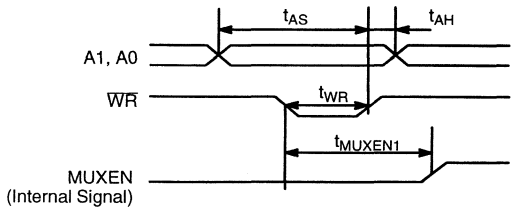


Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE}$ controls the output buffers in an asynchronous mode.

$\overline{OE}$	DB9 – DB0
1	High Z
0	Valid

Table 4. Output Enable Logic

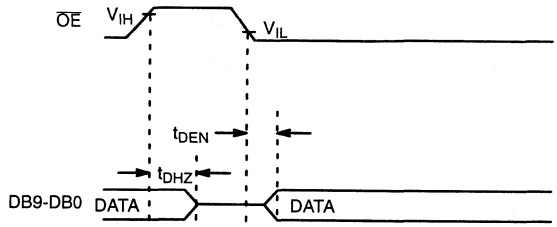


Figure 12. Output Enable/Disable Timing Diagram

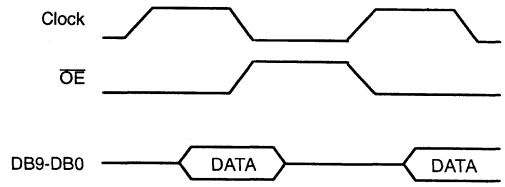


Figure 13. Preferred Output Control

The functional equivalent of the MP87198 (*Figure 14.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

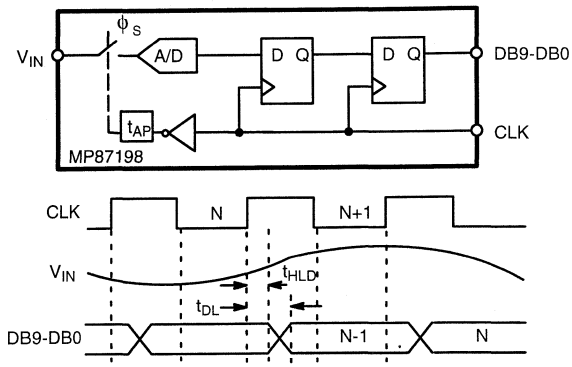


Figure 14. MP87198 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 15. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

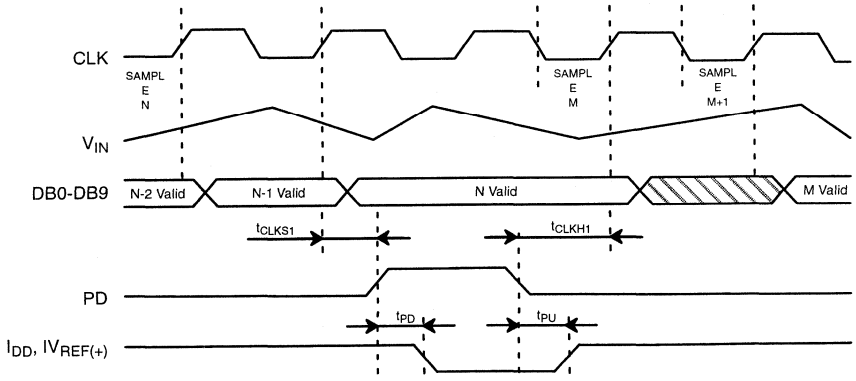


Figure 15. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance capacitor
R_T = Clock Transmission Line Termination

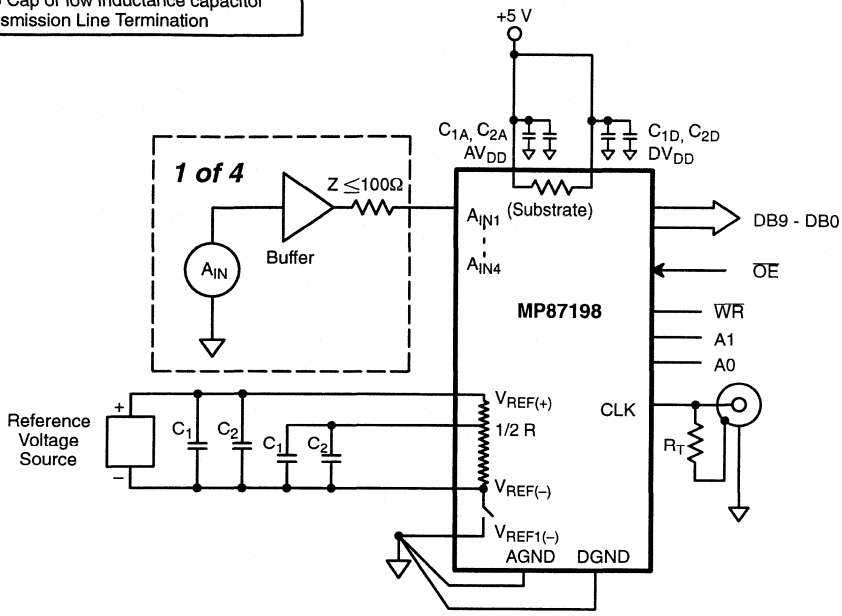


Figure 16. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87198.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87198. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87198.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87198 should be connected to AV_{DD} next to the MP87198.
8. DV_{DD} and AV_{DD} are connected inside the MP87198 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

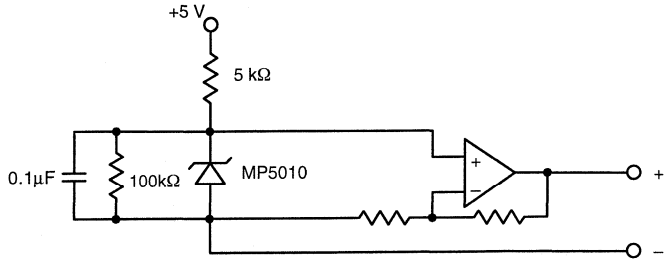
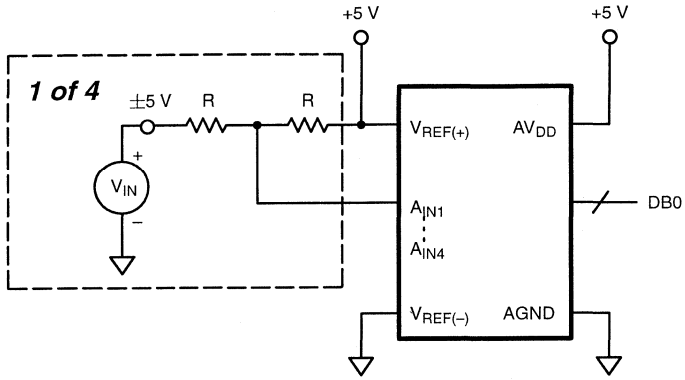


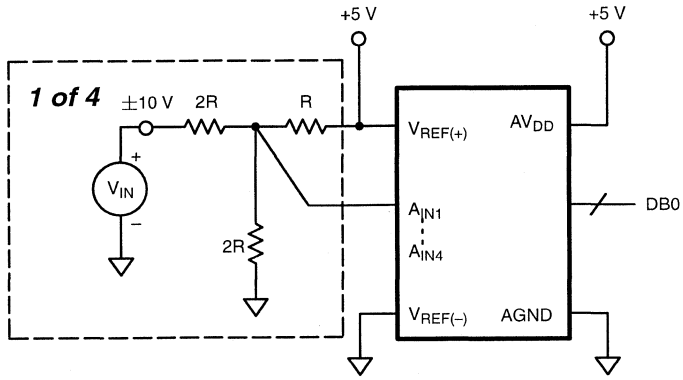
Figure 17. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

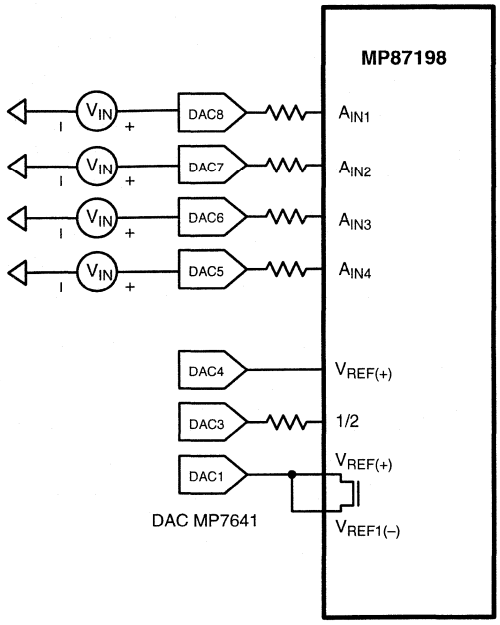
Figure 18. ±5 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

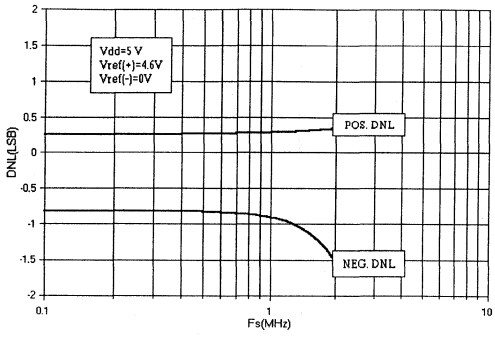
NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 19. ±10 V Analog Input

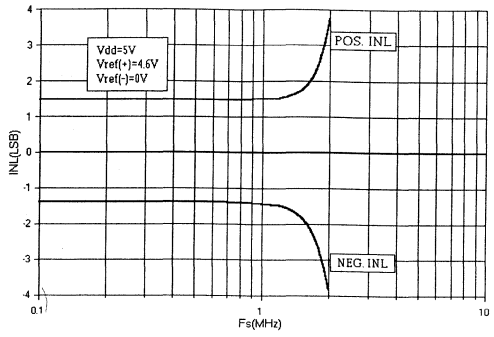


@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

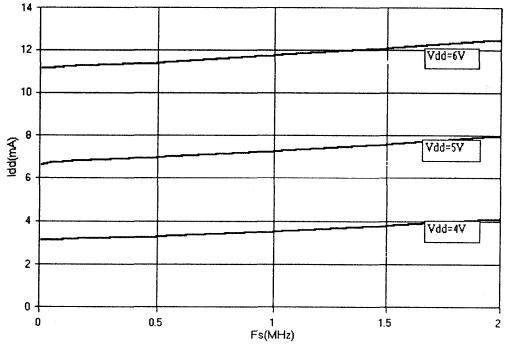
Figure 20. A/D Ladder and A_{IN} with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/2 TAP.)



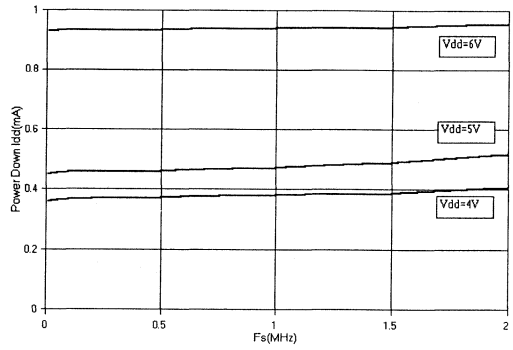
Graph 1. DNL vs. Sampling Frequency



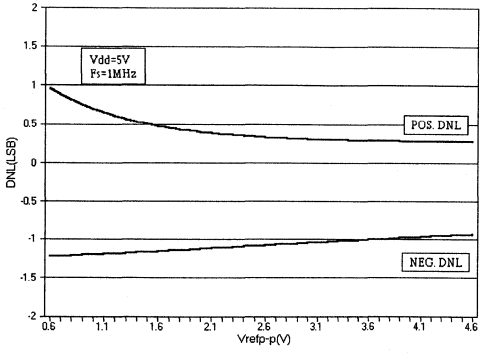
Graph 2. INL vs. Sampling Frequency



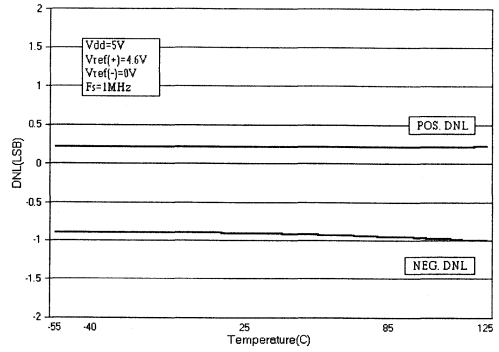
Graph 3. Supply Current vs. Sampling Frequency



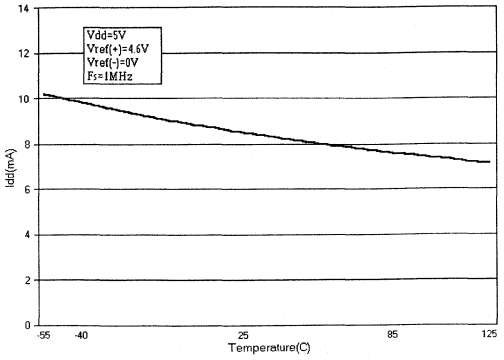
Graph 4. Power Down Current vs. Sampling Frequency



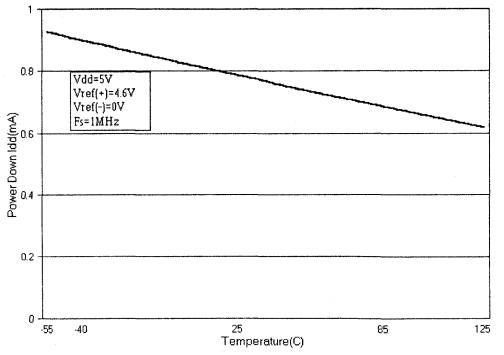
Graph 5. DNL vs. Reference Voltage



Graph 6. DNL vs. Temperature

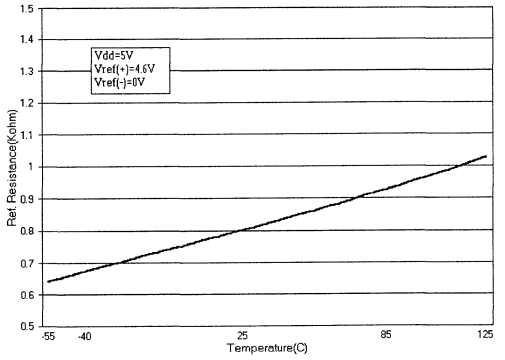


Graph 7. Supply Current vs. Temperature



Graph 8. Power Down Current vs. Temperature

3



Graph 9. Reference Resistance vs. Temperature

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MP8820

8-Bit Analog-to-Digital Converter with an 8-Channel MUX

FEATURES

- **Precision 7–Bit Plus Sign ADC**
- **8 Channel Analog Mux**
- **Single Reference to GND**
- **Input Referenced to User Supplied V_{MID}**
- **DNL= ±1/2 LSB, INL=± 1 LSB**
- **Single Supply: 5 V**
- **ESD Protection: 2000 V**

APPLICATIONS

- **Servo Control**
- **Low Cost Audio Control**
- **Voice Acquisition**

3

GENERAL DESCRIPTION

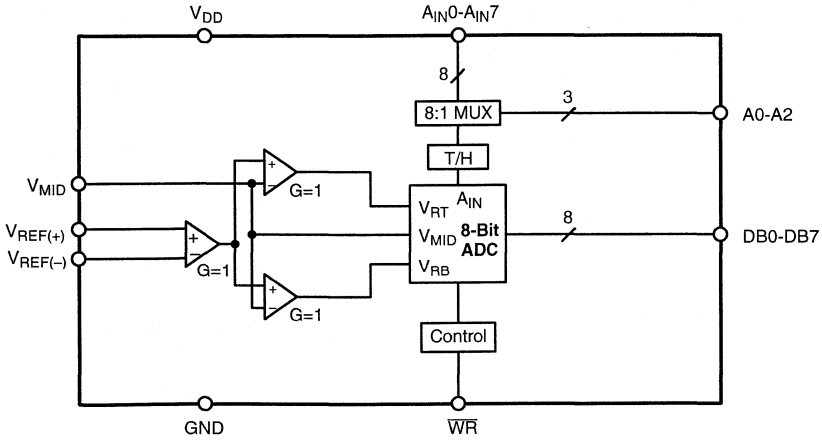
The MP8820 is a precision 1.6 MHz sampling 7-bit plus sign Analog-to-Digital Converter with an eight channel input mux and µP interface. The device has internal circuitry which receives the user supplied reference voltages $V_{REF(+)}$ and $V_{REF(-)}$, and generates the ADC reference voltages $V_{MID} \pm (V_{REF(+)} - V_{REF(-)})$. Since $V_{REF(+)}$ is internally buffered and $V_{REF(-)}$ is generally ground, this structure allows the user to easily generate an input range biased about a user-supplied V_{MID} from a grounded reference source.

The internal ADC reference voltages are capable of swinging to within 0.5 V of the supply rails, giving the MP8820 a wide range over which the effective channel gain can be adjusted.

The MP8820 uses a two-step flash conversion technique. The first section determines the sign and the 3 MSBs while the second segment converts the 4 LSBs. The ADC conversion begins when $\overline{WR}$ goes low and the data is valid 500 ns after the rising edge of $\overline{WR}$. The MP8820 operates from a single 5V supply and consumes only 175mW of power.

Specified for operation over the industrial (–40 to +85°C) temperature range, the MP8820 is available in Surface Mount (SOIC) and Shrunk Small Outline (SSOP) packages.

SIMPLIFIED BLOCK DIAGRAM

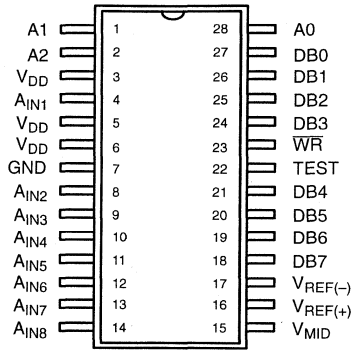


ORDERING INFORMATION

Package Type	Temperature Range	Part No.
SOIC	–40 to +85°C	MP8820AS
SSOP	–40 to +85°C	MP8820AQ

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin SOIC (0.300") – S28
28 Pin SSOP – A28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	A1	Analog Input Mux Address Bit 1
2	A2	Analog Input Mux Address Bit 2
3	V_{DD}	Positive Power Supply (5 V)
4	A_{IN0}	Analog Input 0
5	V_{DD}	Positive Power Supply (5 V)
6	V_{DD}	Positive Power Supply (5 V)
7	GND	Negative power supplies (0V)
8	A_{IN1}	Analog Input 1
9	A_{IN2}	Analog Input 2
10	A_{IN3}	Analog Input 3
11	A_{IN4}	Analog Input 4
12	A_{IN5}	Analog Input 5
13	A_{IN6}	Analog Input 6
14	A_{IN7}	Analog Input 7
15	V_{MID}	System Reference

PIN NO.	NAME	DESCRIPTION
16	$V_{REF(+)}$	Reference Voltage + Input Terminal
17	$V_{REF(-)}$	Reference Voltage – Input Terminal.
18	DB7 (MSB)	Data Output Bit 7
19	DB6	Data Output Bit 6
20	DB5	Data Output Bit 5
21	DB4	Data Output Bit 4
22	TEST	Test Mode Pin
23	$\overline{WR}$	Sample Window Control
24	DB3	Data Output Bit 3
25	DB2	Data Output Bit 2
26	DB1	Data Output Bit 1
27	DB0	Data Output Bit 0
28	A0	Analog Input Mux Address Bit 0

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, GND = 0 V, $V_{REF(+)}$ = 1.5 V, $V_{REF(-)}$ = 0 V, V_{MID} = 2.5 V.

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DC CHARACTERISTICS						
Resolution	N	8			Bits	
Differential Non-Linearity	DNL	–1	±1/4	1	LSB	
Differential Non-Linearity[2]	DNL	–1	±1/2	1	LSB	@ $V_{REF(+)} - V_{REF(-)}$ = 0.5 V
Integral Non-Linearity[7]	INL	–1	±1/2	1	LSB	
Integral Non-Linearity[4, 7]	INL	–1	±1/2	1	LSB	@ $V_{REF(+)} - V_{REF(-)}$ = 0.5 V
Monotonicity			Guaranteed			
Bipolar Zero Error	B_{ZE}	–25	10	25	mV	Offset is measured as the bipolar zero code transition, 01111111 to 10000000, relative to V_{MID}
Zero Scale Drift[2, 5]	Z_{SD}			50	µV/°C	
Full Scale Error					%FS	This is a measure of the internal reference translation. Ideally $V_{RT} - V_{MID} = V_{MID} - V_{RB} = V_{REF(+)} - V_{REF(-)}$
V_{MID} to V_{RT}	$+F_{SE}$	–5.0	2.5	5.0		
V_{MID} to V_{RB}	$-F_{SE}$	–5.0	2.5	5.0		
Full Scale Drift[2, 6]	F_{SD}		0.025		%FS/°C	
DC Input Range[1]	V_{INP-P}	1		3	Vpp	The analog input is specified as Vpp centered around V_{MID}
Aperture Delay	t_{AP}		50		ns	From rising edge of $\overline{WR}$
Input Capacitance	C_{IN}		25		pF	Measured with V_{IN} – DC = 2.5 V and $\overline{WR}$ = low
REFERENCE VOLTAGES						
Positive Reference Input Voltage	$V_{REF(+)}$	0.5		1.5	V	Reference voltage with respect to $V_{REF(-)}$
$V_{REF(+)}$ Input Resistance	RVR+		1		MΩ	
Internal Reference Settling Time	VR_{STL}		500		ns	Settling time required for ADC to make a proper conversion after ($V_{REF(+)} - V_{REF(-)}$) has changed
Negative Reference Input Voltage	$V_{REF(-)}$	0		$V_{REF(+)}$ –0.5	V	
$V_{REF(-)}$ Input Resistance	RVR–		1		KΩ	
V_{MID} Input Current	I_{VM}		0		mA	
V_{MID} Range	V_{MID}	2	2.5	3	V	$V_{MID} \le V_{DD} - 0.5 - [V_{REF(+)} - V_{REF(-)}]$ $V_{MID} \le V_{SS} + 0.5 + [V_{REF(-)} - V_{REF(-)}]$
POWER SUPPLIES						All GNDs are Chip Substrate
Positive Supply	V_{DD}	4.75	5	5.25	V	
Negative Supply	GND	0	0	0	V	
Power Supply Rejection Ratio[2]	PSRR			–48	dB	f = 1 kHz. Not tested.
Supply Current	I_{DD}			45	mA	
DIGITAL CHARACTERISTICS[3, 4]						
Digital Input High Voltage	V_{IH}	4			V	
Digital Input Low Voltage	V_{IL}			1	V	

3

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
DIGITAL CHARACTERISTICS (CONT'D)						
V_{OL}	V_{OL}			0.5	V	@ I_{OL} = 1 mA
V_{OH}	V_{OH}	4.5				@ I_{OH} = 1 mA
I_{IN}-Dig	I_{DL}	–50		50	µA	
3-State Leakage	I_{LK}	–50		50	µA	
Digital Timing Specifications						For testing, rise time = fall time = 10 ns. Output loading = 50 pF.
Write time (analog input tracking)	t_{WR}	150			ns	
Conversion Time	t_{CONV}		500		ns	
Input mux set-up time	t_{MSU}	150			ns	
Input mux hold time	t_{MH}	50			ns	

NOTES

1 Maximum input voltage is 1 V less than V_{DD}.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Measured as the change in the bipolar zero error over temperature. This error does not include the error introduced by the external reference drift.
6 This error does not include the error introduced by the external reference drift.
7 INL is measured as a 7-bit +sign ADC with 8-bit resolution.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... 6 V
All Digital Inputs ..... V_{DD} +0.5 V to GND –0.5 V
Storage Temperature ..... –65 to 150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

ESD Rating ..... 2000 V
Package Power Dissipation Rating @ 75°C
SSOP, SOIC 1000mW
Derates above 75°C ..... 6mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

THEORY OF OPERATION

The defining feature of the MP8820 is that it digitizes a bipolar input signal centered around a given voltage, V_{MID}. The peak to peak swing of A_{IN} is defined by the two input reference voltages, $V_{REF(+)}$ and $V_{REF(-)}$.

The MP8820 takes in the center voltage and the two reference voltages and moves the resistor ladder endpoints V_{RT} and V_{RB} of the ADC around V_{MID} by $\pm(V_{REF(+)} - V_{REF(-)})$. In this way, a unipolar to bipolar translation can take place without having to use both a positive and negative supply. The center voltage acts as a bipolar zero and signals that moves below it are considered negative and signals that exceed it are taken to be positive. The block diagram is shown in *Figure 1.*

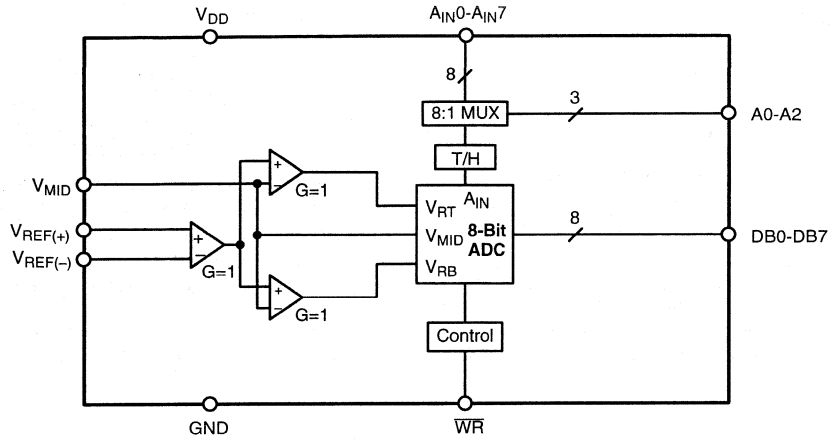


Figure 1. MP8820 Block Diagram

Unlike a unipolar system where one end of the ADC's resistor ladder is modulated above an offset voltage, both ends of the MP8820's reference chain expand or contract around a fixed V_{MID}. The maximum positive full scale voltage is $V_{RT} = V_{MID} + (V_{REF(+)} - V_{REF(-)})$. The maximum negative full scale voltage is $V_{RB} = V_{MID} - (V_{REF(+)} - V_{REF(-)})$. This type of translation is particularly useful in single supply applications where the input is centered about user specified V_{MID}.

The ideal transfer characteristic of the MP8820 is shown in *Figure 2.* An actual transfer characteristic with associated error terms is shown in *Figure 3.*

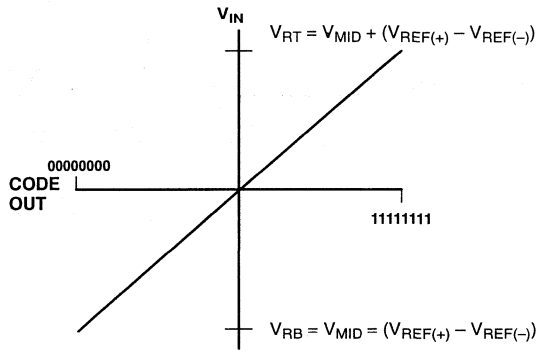


Figure 2. Ideal Transfer Characteristics

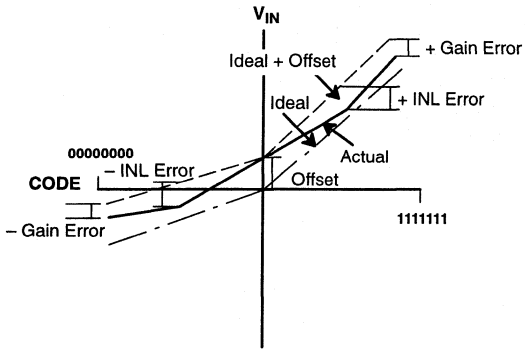


Figure 3. Transfer Characteristics with Error Terms

The sign of the digital output code is determined by whether the input voltage, A_{IN}, exceeds V_{MID}. If A_{IN} is greater than V_{MID}, then the seven bit conversion occurs in the positive half of the transfer function. If A_{IN} is less than V_{MID}, then the translation occurs in the negative half of the transfer function. *Table 1.* shows the digital codes that result from different input voltages.

CODE	A_{IN}
00000000	–FS
00000001	–FS + 1LSB
.	.
.	.
10000000	V_{MID} = BZ
.	.
.	.
11111110	FS – 2LSB
11111111	FS – 1LSB

Table 1. Digital Codes vs. Input Voltage

The MP8820 uses a stand alone µP interface. The user starts a conversion by taking $\overline{WR}$ low. While $\overline{WR}$ is low, the input track and hold follows the input voltage, A_{IN}. On the rising edge of $\overline{WR}$, the input is sampled. The rising edge of $\overline{WR}$ enables a state machine which steps the ADC through a conversion.

The output port is held in high impedance state during the conversion period. The operating timing diagrams are shown in *Figure 4.*

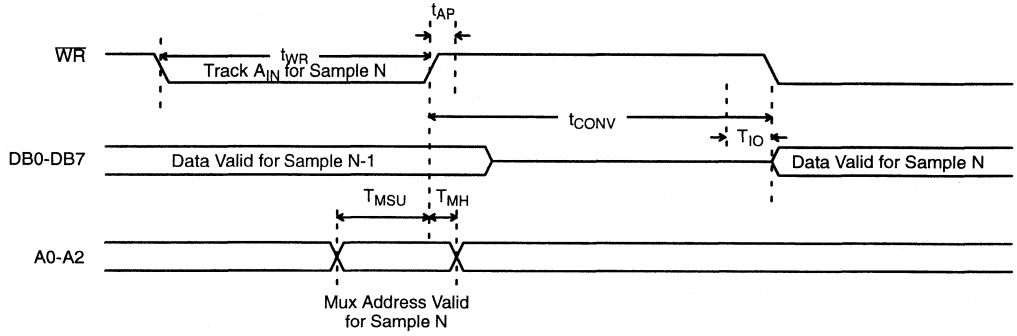


Figure 4. Operating Timing Diagrams

Analog To Digital Conversion

The MP8820 converts analog voltages into 256 digital codes by encoding the outputs of 15 coarse and 15 fine comparators. When $\overline{WR}$ goes low, the input sample and hold circuitry is enabled. The track and hold circuit will follow the output of the 8 channel mux. The channel that is to be converted does not need to be selected until a time equal to T_{MSU}, or 150 ns, before the rising edge of $\overline{WR}$. So, while $\overline{WR}$ is low, the track and hold circuit only has to follow the analog input to be converted for 150 ns.

The analog input is sampled at a time equal to the aperture delay, T_{AP}, after the rising edge of $\overline{WR}$. The aperture delay also accounts for internal propagation delays. The mux address lines may also select a new channel at a time equal to T_{AP} following the rising edge of $\overline{WR}$. For the analog timing diagram, see *Figure 5.*

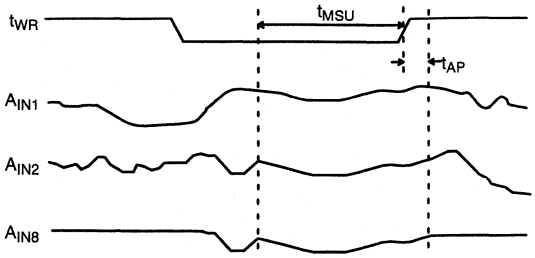


Figure 5. Analog Timing Diagram

clock phase ϕc. The voltage stored on the capacitor is then equal to $V_{BAL} + (V_{IN} - V_{TAP})$. This voltage will force the inverter high or low and the result is latched.

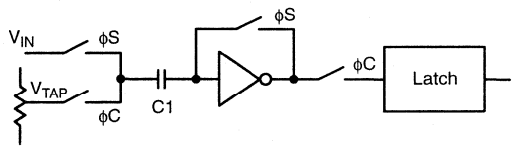


Figure 6. Comparator Block Diagram

Inside the ADC is a series of comparators that sample the analog input and compare it against a resistor tap voltage. A state machine generates the internal clocks necessary to control the comparators, ϕc (CLK high) and ϕs (CLK low = sample). See *Figure 6.* The rising edge of the CLK input marks the end of the sampling phase, ϕs. On ϕs, the analog input voltage is sampled and stored across capacitor C1. The switches controlled by ϕs are opened prior to the compare which is done on

The analog to digital conversion happens in four phases. During the first phase, the analog input is sampled. During the second phase, this input is compared against the reference ladder to determine the MSBs. After the MSBs are determined, a subrange is set for phase three, the conversion of the LSBs. Once all the bits have been derived, the MP8820 performs a correction. The valid data is then ready at the output. The timing diagram is shown in *Figure 7.*

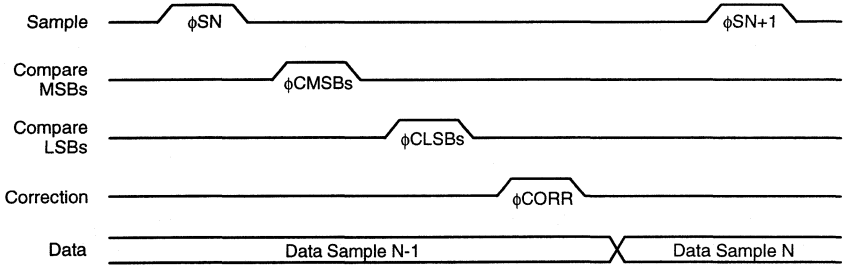
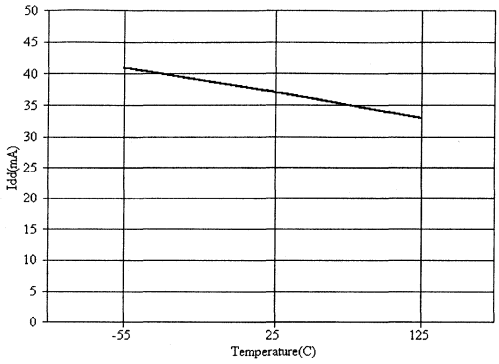


Figure 7. Internal ADC Timing Diagram

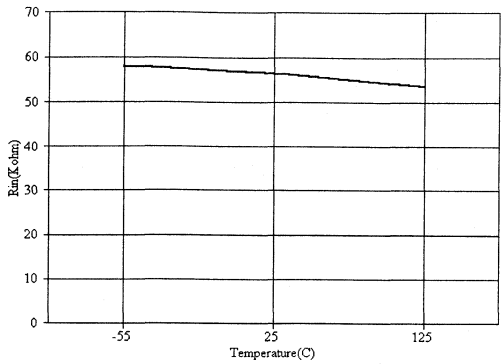
The input mux operates as a standard 8 to 1 decoder. One of eight analog inputs is selected depending on the condition of the address pins A0, A1, and A2. The mux can change address after a time equal to t_{AP} following the rising edge of $\overline{WR}$. The address should be held constant for at least 150 ns before the rising edge of $\overline{WR}$.

Function	$\overline{WR}$	XINT	A0	A1	A2
Start A_{IN} tracking	↓	1	X	X	X
Sample A_{IN}	↑	1	X	X	X
Start Convert	↑	1	X	X	X
Conversion Complete	1	↓	X	X	X
Enable Output Data	X	0	X	X	X
Select Input A_{IN1}	X	X	0	0	0
Select Input A_{IN2}	X	X	0	0	1
Select Input A_{IN3}	X	X	0	1	0
Select Input A_{IN4}	X	X	0	1	1
Select Input A_{IN5}	X	X	1	0	0
Select Input A_{IN6}	X	X	1	0	1
Select Input A_{IN7}	X	X	1	1	0
Select Input A_{IN8}	X	X	1	1	1

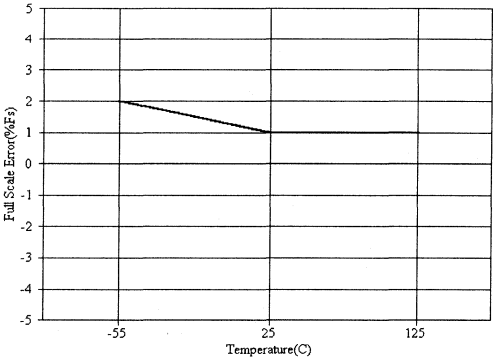
Table 2. Truth Table



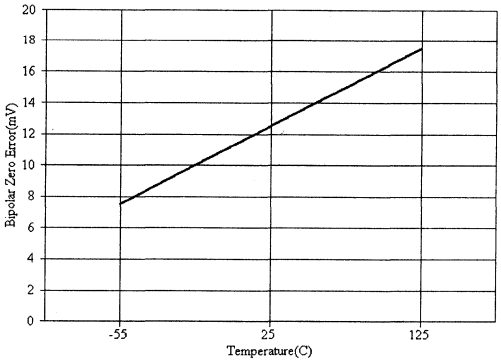
Graph 1. Supply Current vs. Temperature



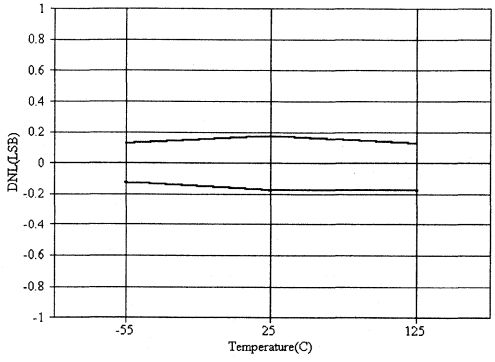
Graph 2. Input Resistance vs. Temperature



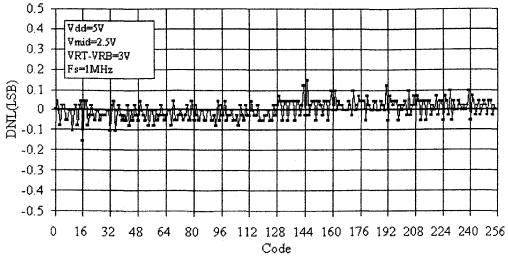
Graph 3. Full Scale Error vs. Temperature



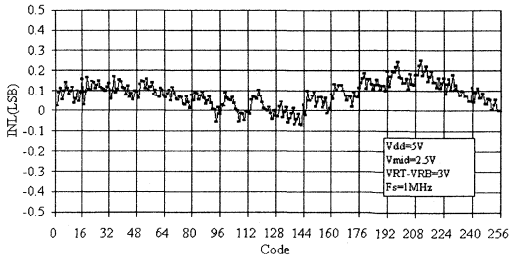
Graph 4. Bipolar Zero Error vs. Temperature



Graph 5. DNL vs. Temperature



Graph 6. DNL Error Plot



Graph 7. INL Error Plot for 7-Bit + Sign ADC

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MP8830

Triple 10-bit High Speed Analog-to-Digital Converter with Digitally Controlled References

FEATURES

- 3 Independent 10-bit ADCs
- Simultaneous Sampling @ 1.25 MSPS
- Independent Digitally Controlled References
- 9-bit Positive Reference and 6-bit Negative Reference Adjustment per Sample
- Low Power: 500mW (typ)
- Internal Track and Hold
- Single 5 V Supply
- Fast Mode for OCR
- A_{IN} Input Range: 1.3 V to 2.6 V p-p
- Black Level Clamp
- Latch-Up Free
- ESD Protection: 2000 V Minimum

BENEFITS

- Pixel-to-Pixel Correction
- Improves Effective Resolution over Software Correction Schemes
- Reduced DSP/Processor Demands
- Reduction of Parts Count and System Cost

APPLICATIONS

- Precision CCD Systems
- Color and B&W Scanners
- Digital Copiers
- IR Cameras

3

GENERAL DESCRIPTION

The MP8830 is a simultaneous sampling 1.25 MSPS triple 10-bit A/D Converter. It provides pixel-to-pixel correction of CCD or other inputs by updating gain and offset parameters supplied from an external correction memory. Each ADC has a 9-bit DAC driving its positive reference voltage and a 6-bit DAC driving its negative reference to independently adjust the gain and offset of each channel.

The MP8830 uses ADCs with a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance and performs an on-chip sample and hold function. The MP8830 uses proprietary high speed DACs to drive the ADC references which allows reference adjustment on every conversion at a 1.25 MHz rate. An internal clamp is available for DC restoration of A_{IN} black level.

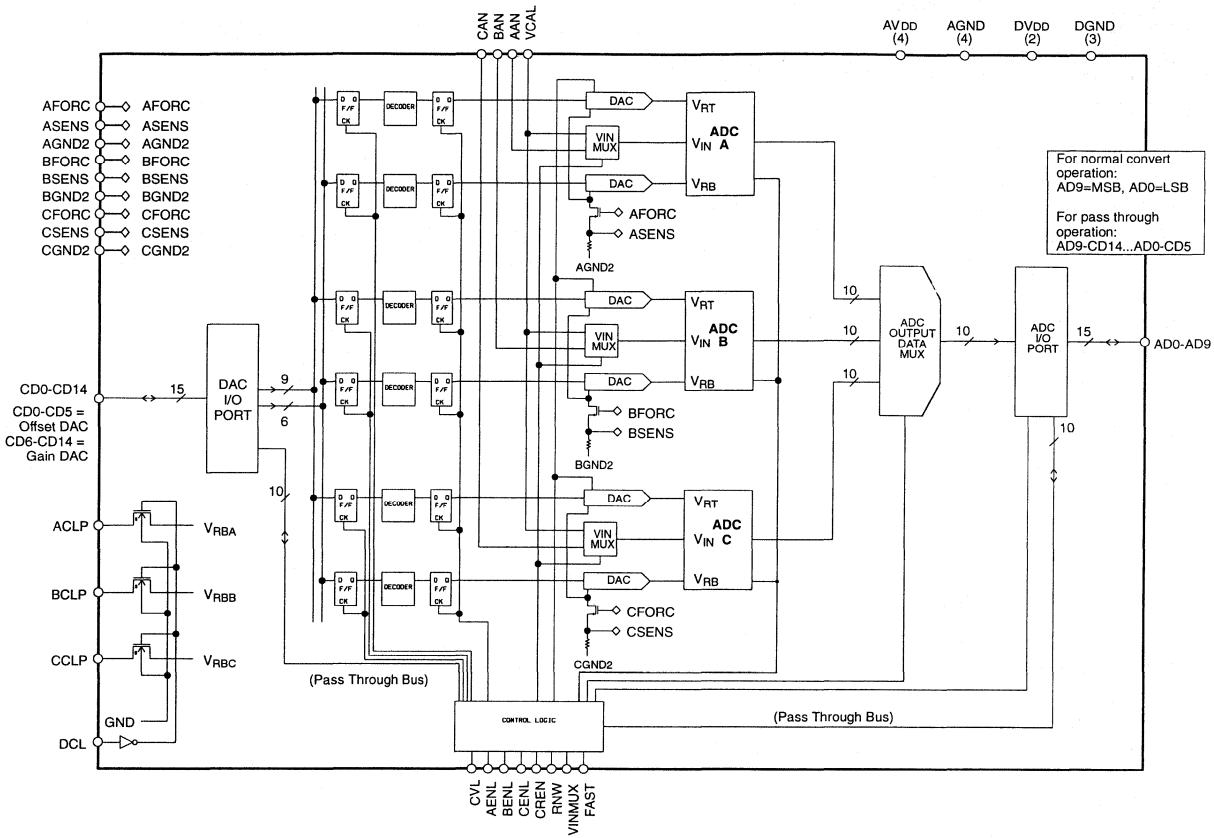
The MP8830 operates from a single 5 V supply and an external 1 V reference, and consumes only 500mW of power (typ).

Specified for operation over the temperature range 0 to 60°C, the MP8830 is available in a 64 lead Plastic Quad Flat Pack (PQFP) package.

ORDERING INFORMATION

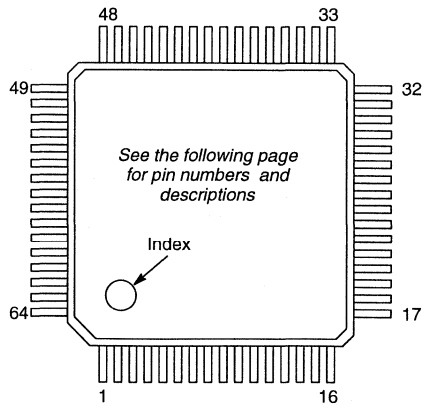
Package Type	Temperature Range	Part No.
PQFP	0 to +60°C	MP8830AE

BLOCK DIAGRAM



PIN CONFIGURATION

See Packaging Section for Package Dimensions



64 Pin PQFP
Q64

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DV_{DD}	Digital Positive Power Supply
2	CD14	DAC Input Pin 14
3	CD13	DAC Input Pin 13
4	CD12	DAC Input Pin 12
5	CD11	DAC Input Pin 11
6	CD10	DAC Input Pin 10
7	CD9	DAC Input Pin 9
8	CD8	DAC Input Pin 8
9	CD7	DAC Input Pin 7
10	CD6	DAC Input Pin 6
11	CD5	DAC Input Pin 5
12	CD4	DAC Input Pin 4
13	CD3	DAC Input Pin 3
14	CD2	DAC Input Pin 2
15	CD1	DAC Input Pin 1
16	CD0	DAC Input Pin 0
17	CV_{DD}	Analog Positive Power Supply
18	CSENS	Sensing Voltage for Biasing the C Channel
19	CFORC	Forcing Voltage for Biasing the C Channel
20	CAN	C Channel Analog Input
21	CGND2	Analog Ground Related to DAC Bias
22	CCLP	Clamp Voltage C
23	CGND1	Analog Negative Power Supply
24	BV_{DD}	Analog Positive Power Supply
25	BSENS	Sensing Voltage for Biasing the B Channel
26	BFORC	Forcing Voltage for Biasing the B Channel
27	BAN	B Channel Analog Input
28	BGND2	Analog Ground Related to DAC Bias
29	BCLP	Clamp Voltage B
30	BGND1	Analog Negative Power Supply
31	AV_{DD}	Analog Positive Power Supply
32	AGND2	Analog Ground Related to DAC Bias

PIN NO.	NAME	DESCRIPTION
33	ASENS	Sensing Voltage for Biasing the A Channel
34	AFORC	Forcing Voltage for Biasing the A Channel
35	AAN	A Channel Analog Input
36	AGND1	Analog Negative Power Supply
37	ACLP	Clamp Voltage A
38	VCAL	Calibration Input Voltage
39	VINMX	Analog Mux Control
40	DGND	Digital Negative Power Supply
41	DCL	Black Level Clamp Control (Active Low)
42	N/C	No Connection
43	DGND	Digital Negative Power Supply
44	DV_{DD}	Digital Positive Power Supply
45	FAST	FAST Mode Enable
46	GND3	Analog Negative Power Supply
47	V_{DD3}	Analog Positive Power Supply
48	CREN	Pass Through Mode Enable
49	RNW	READ not WRITE
50	CENL	Channel C Data Clock
51	BENL	Channel B Data Clock
52	AENL	Channel A Data Clock
53	CVL	Cycle Clock
54	AD9	ADC Data Output 9
55	AD8	ADC Data Output 8
56	AD7	ADC Data Output 7
57	AD6	ADC Data Output 6
58	AD5	ADC Data Output 5
59	AD4	ADC Data Output 4
60	AD3	ADC Data Output 3
61	AD2	ADC Data Output 2
62	AD1	ADC Data Output 1
63	AD0	ADC Data Output 0
64	DGND	Digital Negative Power Supply

Note: All digital signals are active high unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: $AV_{DD} = DV_{DD} = 5$ V, DGND = AGND = 0 V, $V_{REF} = AV_{DD} \times 0.2$ Temperature = 0 to 60°C[1]

A/D Converters						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions/Comments**
Resolution	N	10			Bits	
Differential Non-Linearity	DNL	–1	±0.75	2	LSB	Gain DAC = 000 (hex), offset DAC = 00 (hex). Monotonicity guaranteed.
Differential Non-Linearity	DNL	–1	±0.5	2	LSB	Gain DAC = 1FF (hex), offset DAC = 00 (hex). Monotonicity guaranteed.
Integral Non-Linearity	INL		2	2.75	LSB	Gain DAC = 000 (hex), offset DAC = 00 (hex), Best fit straight line.
Integral Non-Linearity	INL		1.5	2	LSB	Gain DAC = 1FF (hex), offset DAC = 00 (hex), Best fit straight line.
Zero Scale Error	ZSE	–15		9	mV	Measured with offset and gain DACs set to 000. Offset is defined as the difference between the clamp voltage and the analog input voltage which results in the transition of the ADC code from 004 to 005.
Zero Scale Drift[2]	ZSD		50		µV/°C	Measured as the change in the ZSE over temperature. This error does not include the error introduced by the external V_{REF} amplifier or external V_{REF} resistor divider.
DC Input Range	A_{IN}	VCLP –5mV		2.92 V + VCLP –5 mV	V	The digitizing range is set with the Gain DAC and offset DAC. Please note A_{IN} (min) is VCLP – 4 LSB = V_{RB} and A_{IN} (max) is GFS (max) + ZSR (max) + VCLP – 4 LSB.
Data Rate	FS	1.25			MSPS	The conversion rate is determined by the timing diagram and timing specifications. Set by the CVL period.
Analog Input Voltage Change from Sample to Sample[2]	ΔA_{IN}	0		±FS	V	Assuming A_{IN} voltage remains within the specified digitizing range based on the offset and gain DAC codes.
Input Capacitance[2]	C_{IN}			45	pF	Measured with A_{IN} DC = 2.5 V and AENL = low.
Gain DAC						
Resolution	N		9		Bits	
Differential Non-Linearity	DNL	–1		+2.25	LSB	
Integral Non-Linearity	INL			+2	LSB	
Gain DAC Full Scale ($V_{RT} - V_{RB}$)	GFS	2.6	2.68	2.76	V	Gain DAC = 1FF V_{RT} is the top of the ADC reference ladder. Refer to block diagram.
Gain DAC Zero Scale ($V_{RT} - V_{RB}$)	GZS	1.22	1.26	1.3	V	Gain DAC = 000 V_{RB} is the bottom of the ADC reference ladder. Refer to block diagram.
Maximum Gain Change per Cycle[2]	MGC			50	% FSR	After the specified maximum change in gain DAC setting, the ADC should output the same code ±1 LSB for all of the following conversions assuming the analog input remains fixed, i.e. DC.
Settling Time (MGC)[2]	ts-gd		200		ns	

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comments
Offset DAC						
Resolution	N		6		Bits	
Differential Non-Linearity	DNL	–0.5		0.5	LSB	
Integral Non-Linearity	INL			1	LSB	
V_{RB} Range	ZSR	152	158	164	mV	This is measured as the voltage difference at the clamp pin of the selected channel when the offset DAC changed from 000 (hex) to 3F (hex) with the gain DAC at 1FF (hex). Refer to V_{RT} and V_{RB} EQNs in the theory of operation section.
Maximum Offset Change per Cycle[2]	MOC			100	% FSR	After the specified maximum change in offset DAC setting, the ADC should output the same code ±1 LSB for all of the following conversions assuming the analog input remains fixed, i.e. DC.
Full Scale Settling Time[2]	ts-od		200		ns	For a 00 (hex) to 3F (hex) change of offset DAC code.
Black Level Clamp Switch						
On Resistance	R_{ON}		100	150	Ω	Effective R_{IN} at clamp pin.
Input Leakage	IL_{CLP}			25	nA	Offset DAC at 00 (hex) (worst case condition).
Clamp Switching Charge Injection[2]	Q_{CLP}			50	pC	Offset DAC at 00 (hex) (worst case condition).
Voltage at Clamp Pin	V_{CLP}	170	180	190	mV	Offset by 4 LSB from bottom tap of ADC ladder. Gain = 000 (H). Offset DAC = 00.
Reference Voltage Requirements (See Theory of Operation)						
Reference Voltage	V_{REF}	0.93	1	1.07	V	All linearity specifications assume the reference voltage = AV_{DD} X (0.2).
		0.5		1.15	V	Functional.
Calibration Voltage	VCAL	AGND		AV_{DD}	V	
Sense Pins Input Resistance (ASENS, BSENS, CSENS)	RINS		560		Ω	RINS is measured from the sense pin to AGND2, BGND2, CGND2 with the power turned off and test voltage less than 250 mV.
Power Supplies (Note: All GND pins are substrate)						
Analog Positive Supply	AV_{DD}	4.75	5	5.25	V	Bypass power supply pins.
Digital Positive Supply	DV_{DD}	AV_{DD}	AV_{DD}	AV_{DD}	V	Bypass power supply pins.
Analog Negative Supply	AGND	0	0	0	V	
Digital Negative Supply	DGND	0	0	0	V	
Power Supply Rejection	PSRR			–60	dB	f=1 KHz.
Supply Current	I_{DD}		100	130	mA	During specified operation.
Digital Characteristics						
Digital Input High Voltage for Control Pins	V_{IH}	3.5			V	All digital input pins other than DAC data inputs.
Digital Input Low Voltage for Control Pins	V_{IL}			1.5	V	All digital input pins other than DAC data inputs.
Digital Input High Voltage for DAC Input Pins	V_{IH}	2.4			V	DAC data inputs, CD0-CD14
Digital Input Low Voltage for DAC Input Pins	V_{IL}			0.4	V	DAC data inputs, CD0-CD14
V_{OL}	V_{OL}			0.5	V	@ I_{OL} = 4 mA
V_{OH}	V_{OH}	4.5				@ I_{OH} = 4 mA
Digital Input Leakage Current	I_{IN}	–10		10	µA	

3

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comments
3-State Leakage	I_{OZ}	–10		10	µA	In pass-through mode
Digital Timing Specifications[2]						For testing, rise time = fall time = 10 ns. Output loading = 60 pF except for AD0-AD9 for which loading is 40 pF. Rise and fall times faster than 5 ns should be avoided.
AENL, BENL, CENL Pulse Width	t_1	125			ns	
D/A Data Hold Time	t_2	20			ns	
BENL Rising Edge to CENL Rising Edge	t_3	270			ns	
AENL Rising Edge to CVL Falling Edge	t_4	30			ns	
D/A Data Setup Time	t_5	20			ns	
Analog Input Hold Time	t_6	20			ns	Measured as part of analog feedthrough test. Note, $t_{tapmax} < t_{4min} + t_{6min}$.
CVL Rising Edge to AENL Rising Edge	t_7	230			ns	
A/D Data Enable Time	t_8			40	ns	CVL to Channel A data. BENL to Channel B data. CENL to Channel C data.
CENL Rising Edge to CVL Rising Edge	t_9	40			ns	
Analog Input Settled to 0.1%	t_{10}	50			ns	Assumes the sample is taken at the rising edge of AENL.
A/D Data Hold Time	t_{11}	20			ns	
Aperture Delay	t_{AP}		20	40	ns	Analog sampling window delay from CVL rising (↑) edge (start) or AENL rising (↑) edge (end).
CVL Falling Edge to BENL Rising Edge	t_{12}	180			ns	
Delay from CD5-14 to AD0-9 with CREN=1	t_{13}			50	ns	
Delay from AD0-9 to CD5-14 with CREN = 1	t_{14}			50	ns	
Delay from DCL Falling Edge to Clamp on.	t_{15}			40	ns	External analog clamp voltage settling depends on external circuitry.
Delay from DCL Rising Edge to Clamp off.	t_{16}			40	ns	External analog clamp voltage settling depends on external circuitry.
Time for AD0-9 and CD5-14 to switch from normal operation to pass through mode or vise versa (i.e. bus contention).	t_{17}	0		40	ns	User should stop driving the bus before changing the mode and data will not be valid for 40 ns after a change of mode.
Digital Quiet Time	t_{18}	15			ns	This quiet time is necessary to reduce digital crosstalk during the critical sampling time. The accuracy of each conversion may be corrupted due to digital noise on the board during this period.
Digital Quiet Time	t_{19}	40			ns	This quiet time is necessary to reduce digital crosstalk during the critical sampling time. The accuracy of each conversion may be corrupted due to digital noise on the board during this period.

Notes
1 Production testing performanced at 25°C.
2 Not production tested.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted) [1, 2]

AV_{DD} to GND ..... 6 V
DV_{DD} to GND ..... 6 V
$AV_{DD} - DV_{DD}$ ..... 150 mV DC
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65°C to 150°C
Lead Temperature ..... 300°C

ESD Rating ..... 2000 V on all pins.

Package Power Dissipation Rating @ 75°C
PQFP ..... 1100 mW
Derates above 75°C ..... 15 mW/°C
T_{JMAX} ..... 150°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All logic inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

TRUTH TABLE

Function	CVL	AENL	BENL	CENL	CREN	RNW	VINMX	FAST	DCL
Start A_{IN} tracking	↑	1	1	1	0	X	0	X	X
Sample A_{IN}	1	↑	1	1	0	X	0	X	X
MSB convert	0	1	0	1	0	X	0	X	X
LSB convert	0	1	1	0	0	X	0	X	X
Output A ADC data from previous sample	↑	1	1	1	0	X	0	X	X
Output B ADC data from previous sample	X	1	↓	1	0	X	0	X	X
Output C ADC data from previous sample	X	1	1	↓	0	X	0	X	X
Load channel A data to first A DAC register	X	↓	1	1	0	X	0	X	X
Load channel B data to first B DAC register	X	1	↓	1	0	X	0	X	X
Load channel C data to first C DAC register	X	1	1	↓	0	X	0	X	X
Update second register for all DACs	↑	1	1	1	0	X	0	X	X
Turn on all black level clamp switches	X	X	X	X	X	X	X	X	0
Pass-through mode: ADC port in, DAC port out	X	X	X	X	1	0	X	X	X
Pass-through mode: DAC port in, ADC port out	X	X	X	X	1	1	X	X	X
ADC inputs connect to VCAL	X	X	X	X	X	X	1	X	X
Put ADCs in 4-bit mode	X	X	X	X	X	X	X	1	X

3

TIMING DIAGRAMS

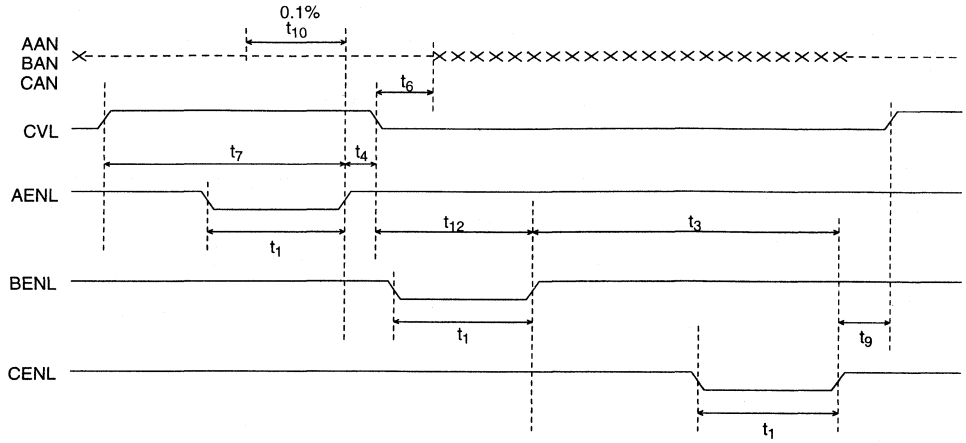


Figure 1. Clock Timing for Convert Mode

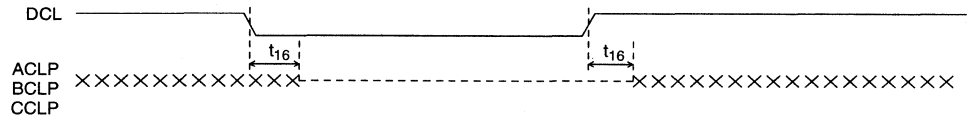


Figure 2. DC Clamp Operation

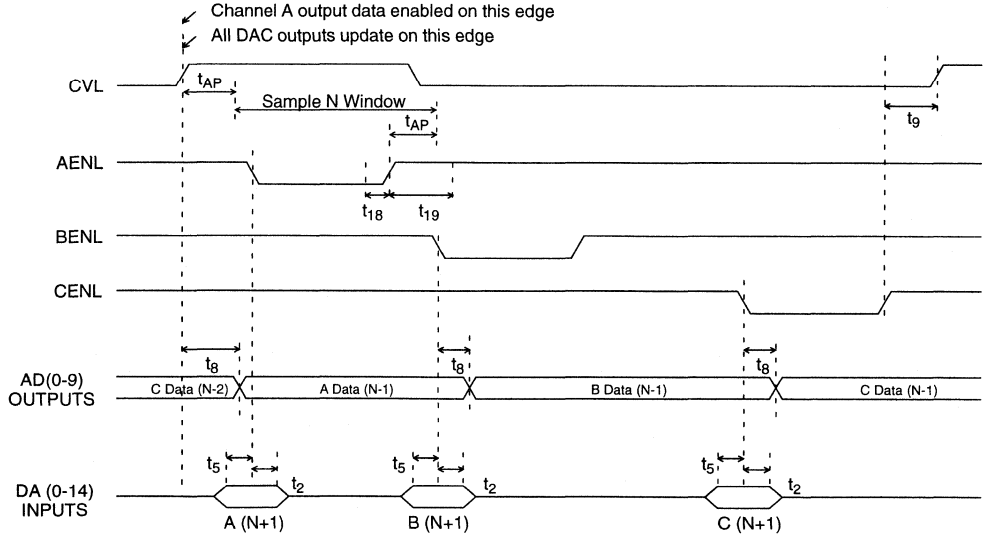
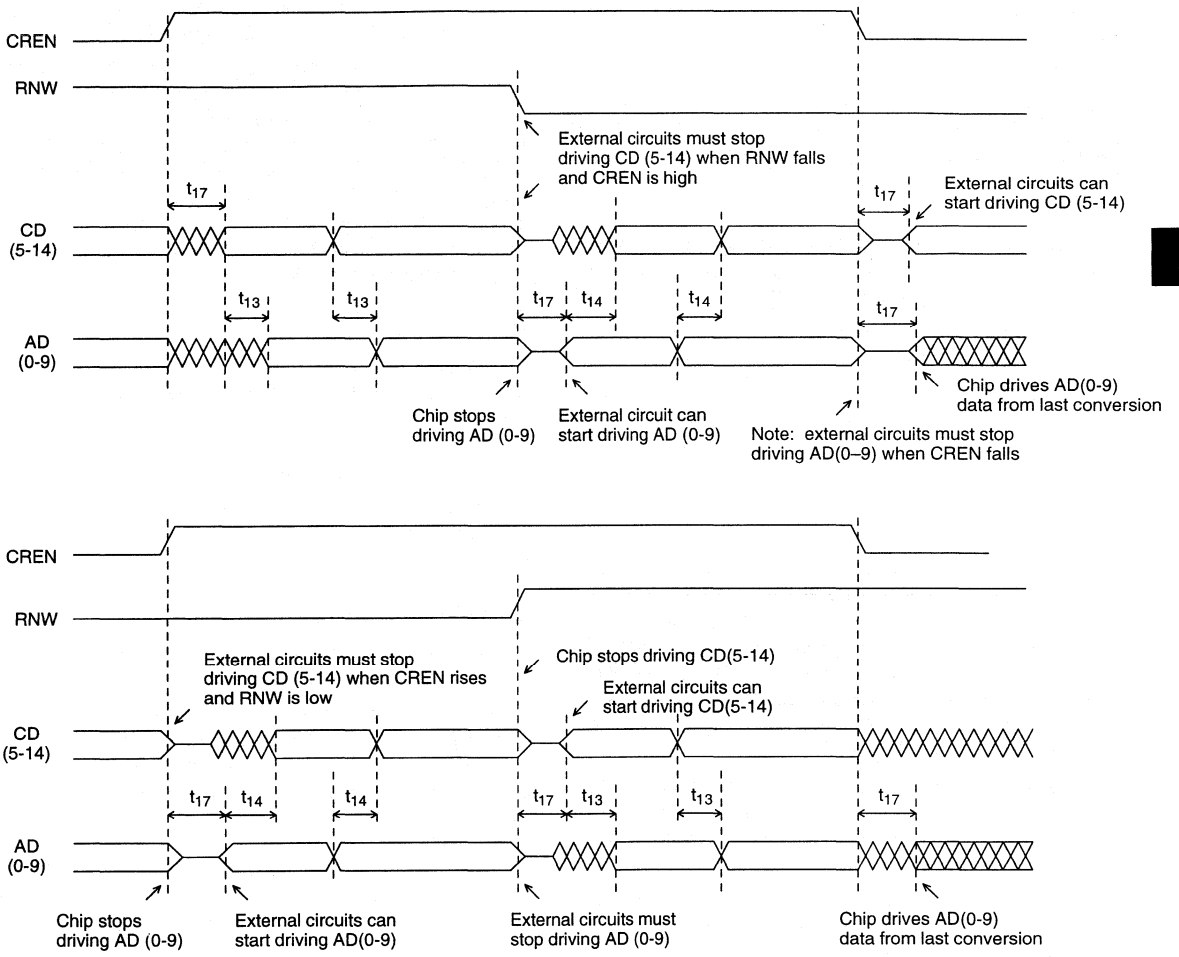


Figure 3. DAC Input and ADC Output Timing for Normal Convert Operation (CREN = 0)

Pass Through Mode

1. AENL, BENL & CENL should be held high during pass-through mode. ADCs and DACs will not work properly during pass-through.
2. Pass-through mode enable. When CREN is high, pass-through mode between the ADC and DAC ports is enabled. RNW controls the direction of pass-through operation.
3. READ not WRITE signal. RNW controls the direction of the pass-through operation when CREN is high, and has no impact when CREN is low. When RNW is high, data passes from the DAC port to the ADC port. When RNW is low, data passes from the ADC port to the DAC port. Note the port connections are: CD5; AD0; CD6; AD1;...;CD14; AD9.



T_{13} Pass through delay from CD(5-14) to AD(0-9)
T_{14} Pass through delay from AD(0-9) to CD(5-14)
T17 Pass through set up time

Figure 4. Timing for Pass Through Mode Operation

THEORY OF OPERATION

The MP8830 is composed of three ADC converters with dynamic gain and offset control along with their associated analog and digital support circuitry. The three converters are intended to be used in a simultaneous sampling configuration. The only external circuits required are a reference and reference buffer amp.

The ADC gain and offset DAC inputs, ADC output data, and the A_{IN} sampling time are related to the four clock inputs, CVL, AENL, BENL and CENL.

In applications which require rejecting a bias level from the analog input, a zero clamp is provided for each channel. With the addition of a buffer input amp and blocking capacitor, this function rejects the bias present during DCL = 0 time on the analog input.

ADC calibration or test can be performed using the built-in VCAL / A_{IN} MUX which will switch the ADC A_{IN} from the channel input voltage, AAN, BAN, CAN to VCAL.

A fast mode is provided, where only the four ADC MSBs are produced while the remaining data is set to 00(hex).

To simplify board layout, a data pass-through configuration is provided to allow bi-directional communication between the ADC data port and the 10 MSBs of the DAC I/O port.

ADC System Overall Sequence

The following section describes the events which take place during one conversion cycle (*Figures 1-4*). Assume at power up, or in the previous cycle, that the values for the gains and offsets needed for this sample set have been loaded into the first DAC registers. This data is loaded into the second registers for all three channels *on the rising edge of CVL*. A_{IN} tracking for all channels is also started after t_{AP} delay. Note that the AENL, BENL and CENL were at "1" states.

At the *falling edge of AENL*, the channel A gain and offset data for the next cycle is loaded into the channel A first DAC register. The analog input sample for all three channels is taken at the *rising edge of AENL* after t_{AP} delay.

At the *falling edge of BENL*, the channel B gain and offset data for the next cycle is loaded into the channel B first DAC register. The MSB comparators are also enabled at this time. At *the rising edge of BENL*, the MSB value is latched, and the range for the LSBs is selected. Note that the gain and offset DAC must be settled by this time in order for the MSB value to be correct ($t_7 + t_4 + t_1$ ensure this.)

At *the falling edge of CENL*, the channel C gain and offset data for the next cycle is loaded into the channel C first DAC register. The LSB comparators are also enabled at this time. At *the rising edge of CENL*, the LSB value is latched.

During the time (t_9) when CENL =1 and CVL = 0, the MSB data is corrected (if necessary) and then propagated along with the LSB data to the ADC outputs. On the rising edge of CVL, channel A data is enabled at the output port.

Since the actual ADC samples are taken at the rising edge of AENL after t_{AP} delay, this period of time is the most sensitive to transition noise from digital components. Keep all transitions outside of the t_{18}, t_{19} digital quiet time window around the AENL rising edge. Since the ADC output bus will change states at the rising edge of CVL, the time from CVL rising to AENL rising is important. The delay from CVL rising to channel A valid on the ADC bus is t_8. This requires that AENL rising edge must not occur until at least t_8 after CVL rising.

CVL Functions

CVL rising edge performs three functions. The first is to update the gain and offset DACs from their respective first registers simultaneously. The second function is to initiate the sample window. The third function is to latch the results of the previous conversions into the ADC output register.

The A channel ADC data is presented at the ADC data port after CVL rising edge. CVL falling edge does not change any internal state.

DAC Data Port Operation

DAC data is loaded first into an input register and then loaded into the DAC register.

The input register allows sequential loading of the next conversion settings for all the channels through the 15-bit DAC data bus while the ADC data is being clocked out of the ADC data port. The second register allows for simultaneous updating of all channels at the beginning of the analog sample period. This timing gives the ADC reference levels adequate time to settle before being used to convert the sampled A_{IN}. Note that the DAC data must be presented at each cycle, since there is no provision for holding DAC data after each cycle.

At power up, the DAC states should be set for the first sample's required gain and offset settings. This is accomplished by setting CVL = 1, and cycling each of the AENL, BENL, and CENL clocks from their 1 to 0 to 1 states sequentially with each channel's respective data present at the DAC data port.

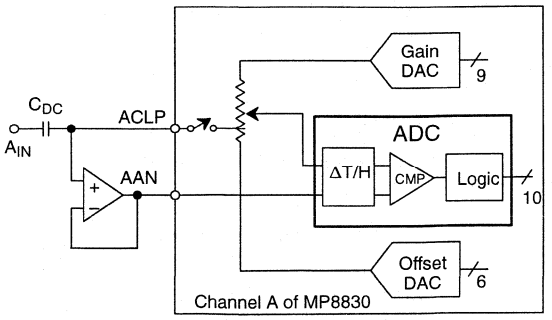


Figure 5. Simplified Diagram Channel A Example

Black Level Switch Operation

The MP8830 is equipped with a black level setting switch. The function of the black level setting switch is to store the DC offset value of the ADC as well as the common mode value of A_{IN} across the external C_{DC}-hold capacitor. This is a cost effective method to store the black level of A_{IN} or the offset of the system. Note that the ACLP, BCLP, and CCLP level is DC shifted to accommodate for the distribution of ADC offset.

One terminal of each clamp switch is connected at the ladder tap voltage which corresponds to +4 LSB from the ADC 000(hex) to 001(hex) transition. This 4 LSB offset allows the ADC to measure as low as –4 LSB of the analog input voltage relative to the clamp voltage. To increase the negative input detectable range, clamp with the offset DAC at a code higher than 00(hex).

The second terminal of the clamp switch is connected to a pin with its corresponding channel prefix. For channel A, the pin is named ACLP.

The control of the all the switches is provided by a separate unlatched logic input called DCL. The delay from DCL falling edge to switch on is specified as t_{16}. The actual time required to store the bias voltage depends on the external C value, and bias variation from sample to sample. The equivalent impedance of the clamp is 100Ω typical, spec name of R_{ON}, and must be included in the analysis of the zero sample time considerations.

The black level is a function of the offset DAC, and therefore requires that the value of the offset DAC be loaded into the offset DAC second register before the clamp is turned on. This value can be set from 00(hex) to 3F(hex) corresponding to a clamp level change of ZSR.

The voltage swing at the ACLP, BCLP, CCLP pin after clamp should be limited to the range of AV_{DD} to AGND. This will prevent the stored charge on the holding cap from being changed by the input protection devices.

A 50Ω to 100Ω resistor in series with the ACLP, BCLP, CCLP pin will limit the current induced in the protection and parasitic diodes due to over-voltages induced by the source. Limit this current with the use of external protection diodes.

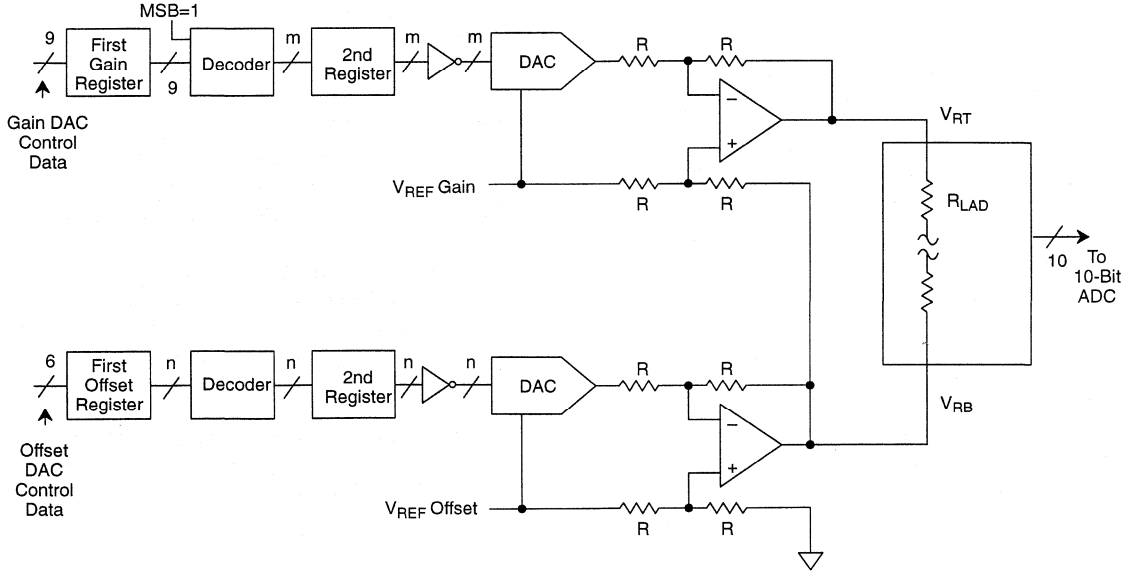


Figure 6. MP8830 Single-Channel Equivalent Circuit

ADC Gain and Offset Control

Each channel of the MP8830 contains a 10-bit ADC, a 10-bit DAC with MSB = 1 (9 active bits) driving the positive reference, and a 6-bit DAC driving the negative reference of the ADCs ladder network.

The relationship between the ADC gain and offset and the DAC data can be expressed mathematically.

Assign the terms V_{RT} and V_{RB} to represent the voltages for the ADC full scale and black levels. DgainA and DoffsetA represent the digital value for the gain and offset parameters set by the DACs for channel A.

V_{RT} and V_{RB} are defined by the equation:

$$V_{RT} = \left\{(1 + \frac{DgainA}{2^9}) * 1.3\right\} * V_{REF} + V_{RB}$$

$$V_{RB} = \left\{(1 + \frac{DoffsetA}{2^6}) * 0.16\right\} * V_{REF}$$

$$V_{RT} - V_{RB} = \left\{(1 + \frac{DgainA}{2^9}) * 1.3\right\} * V_{REF}$$

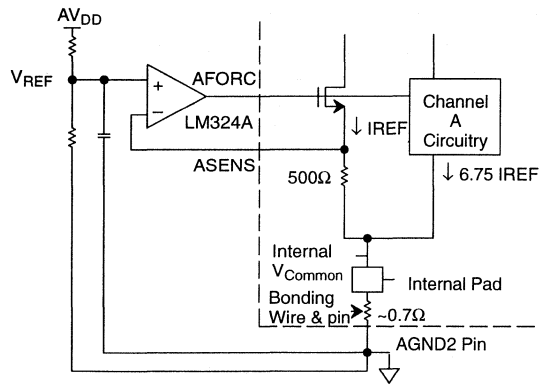


Figure 7. Driving the AFORC and ASENS Pins (Channel A Example)

Channel Bias Circuitry

The gain DAC and the offset DAC for each channel have a combined bias generator for setting their full scale range. An external op amp is required and is connected per *Figure 7.* The V_{REF} range for each channel can be either the same or differen depending on the application and nominal channel gain re quired. A higher V_{REF} provides lower channel gain.

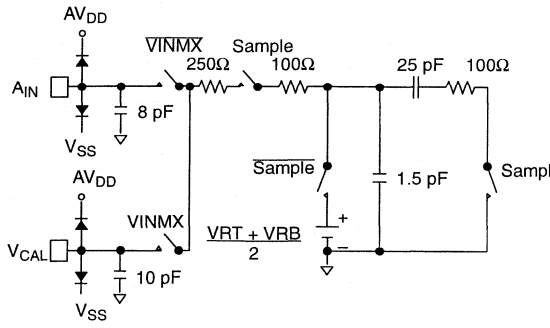


Figure 8. ADC Input Equivalent Circuit

ADC Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. *Figure 8.* shows an equivalent input circuit.

VCAL and VINMX

VCAL voltage is connected through an analog mux to all 3 channel inputs at VINMX=1. VCAL can then be used to normalize all three ADC input voltage to output states. It can be used for testing as well as building calibration tables for all three channels.

Supply and Grounds

AGND1, BGND1, CGND1, and GND3 should be connected under the package to make their common impedance as low as possible. AGND2, BGND2, CGND2 should also be connected to this ground.

Use a single supply to drive all of the V_{DD} pins. AV_{DD}, BV_{DD}, CV_{DD}, V_{DD3} should be connected to a common supply plane which forms a supply / ground plane with the analog ground plane. In addition, local decoupling (preferably 0.1 uFchip type) should be connected between each analog V_{DD} pin and its closest analog ground.

A decoupling capacitor (preferably 0.1 uFchip type) should be connected across pin 1 and 64 and between pin 44 and 43. A DV_{DD} to DGND supply/ground plane should also be provided.

PIN OUT DEFINITIONS

Pin #	Pin Name	Function
1, 44	DV_{DD}(2)	Digital positive power supplies. 5 V. Should be decoupled to digital GND plane. The two DV_{DD} pins both connect to the ESD ring as well as the control logic, data port logic, and the internal ADC output data bus drivers.
43, 64	DGND (2)	Digital negative power supplies. 0 V. The two DGND pins both connect to the ESD ring as well as the control logic and data port logic.
31 24 17 47	AV_{DD}, BV_{DD}, CV_{DD}, V_{DD3}	Analog positive power supplies. 5 V. Should be star connected to the analog supply post or direct connection to analog supply plane. Decouple to AGND, BGND, CGND. $V_{DD}3$ powers the ADC internal logic only.
36 30 23 46	AGND1, BGND1, CGND1, GND3	Analog negative power supplies. 0 V. Should be star connected to analog ground post or direct connection to the analog ground plane. These GNDs power the analog sections of the ADC and the circuitry in the DACs. GND3 pin connects to the internal ADC data bus and the ADC internal logic.
32 28 21	AGND2, BGND2, CGND2	Analog grounds related to DAC bias are the common voltage for the reference. The ADC ladder resistor terminates to this pin as well as the internal bias resistor used for setting the DAC reference. These pins should be used as the reference ground voltage for all analog measurements.
52	AENL	Channel A data clock, active low. A DAC data loaded into first register bank on the falling edge of AENL.
51	BENL	Channel B data clock, active low. B DAC data loaded into the first register on the falling edge of BENL. B ADC data loaded to the ADC output port on falling edge (and should be read on the rising edge).
50	CENL	Channel C data clock, active low. C DAC data loaded into the first register on the falling edge of CENL. C ADC data loaded to the ADC output port on falling edge (and should be read on the rising edge).
53	CVL	Cycle clock. All DACs loaded on rising edge. Begin sample of analog input on rising edge. A ADC data is loaded to the ADC output port on the rising edge of CVL (and should be read on the rising edge of AENL).
48	CREN	Pass through mode enable. When CREN is high, passthrough mode between the ADC and DAC ports is enabled. RNW controls the direction of pass through operation.
49	RNW	READ not WRITE signal. RNW controls the direction of the pass through operation when CREN is high and has no impact when CREN is low. When RNW is high data passes from the DAC port to the ADC port. When RNW is low, data passes from the ADC port to the DAC port. Note, the port connections are: CD5; AD0; CD6; AD1;.....;CD14; AD9.
39	V_{IN}MX	Analog mux control. V_{IN}MX controls the analog mux on the input of all three ADCs. When V_{IN}MX is high, all ADC inputs are connected to VCAL. When low, each ADC is connected to its particular analog input pin.
45	FAST	Fast mode enable. The FAST pin controls the mode of the ADCs. When low, the part functions as specified for 10-bit resolution. When high, the ADC's resolution becomes 4-bit and the LSBs are forced low. The clock rate can be increased in this mode to 3 MHz.
37	ACLP	Clamp voltage A. Black level clamp pin for the A channel.
29	BCLP	Clamp voltage B. Black level clamp pin for the B channel.
22	CCLP	Clamp voltage C. Black level clamp pin for the C channel.
41	DCL	Black level clamp control (active low). Black level clamp enable for all pins. All Black level clamps are turned on when DCL is low.
35	AAN	A channel analog input.
27	BAN	B channel analog input.
20	CAN	C channel analog input.
38	VCAL	Calibration input voltage.

34	AFORC	Forcing voltage for biasing the internal DACs. This is the gate of the N-Channel biasing transistor for the A channel.
33	ASENS	Sensing voltage for biasing the internal DACs. This is the source of the N-channel biasing transistor and the top terminal of the internal biasing resistor for the A channel.
26	BFORC	Forcing voltage for biasing the internal DACs. This is the gate of the N-Channel biasing transistor for the B channel.
25	BSENS	Sensing voltage for biasing the internal DACs. This is the source of the N-Channel biasing transistor and the top terminal of the internal biasing resistor for the B channel.
19	CFORC	Forcing voltage for biasing the internal DACs. This is the gate of the N-Channel biasing transistor for the C channel.
18	CSENS	Sensing voltage for biasing the internal DACs. This is the source of the N-Channel biasing transistor and the top terminal of the internal biasing resistor for the C channel.
54-63	AD9-AD0	ADC data output pins. AD9 is the MSB.
2-16	CD14-CD0	DAC input pins. CD14-CD6 are the Gain DAC MSB to LSB. CD5-CD0 are the offset DAC MSB to LSB.
42	N/C	No connection.
40	DGND	Digital Ground.

Note: All digital signals are active high unless otherwise noted.

APPLICATION NOTES FOR CCD SYSTEMS

A typical CCD digitizing configuration is shown in *Figure 9.*, which incorporates global gain and offset adjustment as well as pixel-to-pixel variation correction. The MP8830 can greatly simplify this type of system by replacing the ADCs, the pixel correction DACs, and the global offset DACs as shown in *Figure 10.* One main advantage of the MP8830 is the way the offset and span for each pixel are controlled. In the traditional application, the offset and span settings interact requiring addtional computations for each pixel adjustment. With the MP8830, the offset and span settings can be calibrated separately simplifying the computations necessary.

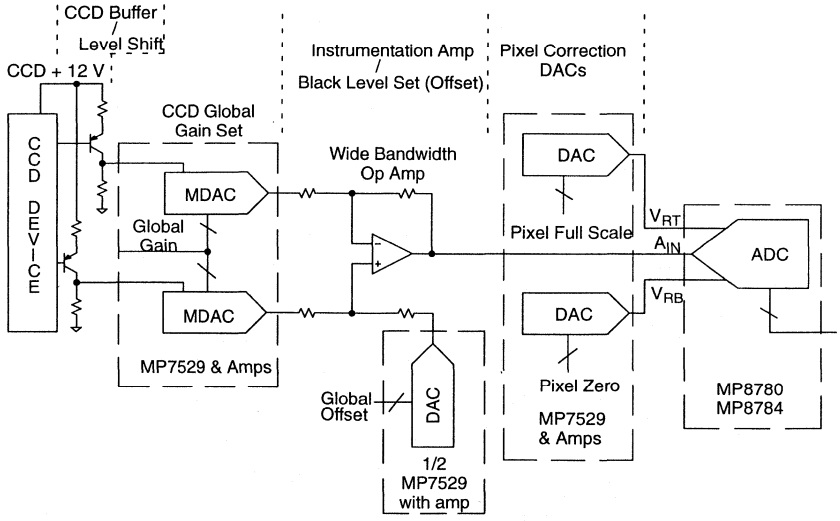


Figure 9. Common Configuration for CCD Digitizer 1 Channel Shown

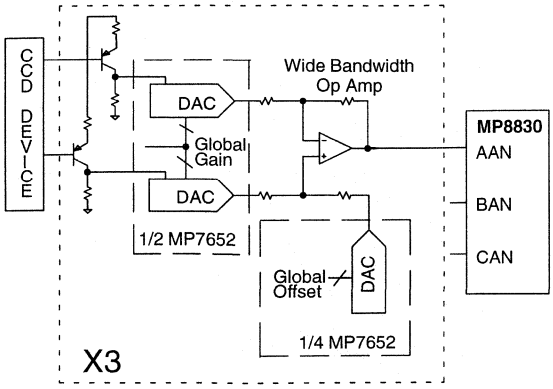


Figure 10. Common Configuration for CCD Digitizer with MP8830 1 Channel Shown

The configuration shown in *Figure 10.* incorporates all of the building blocks present in previous generations. As shown, the MP7652 allows for a serial data path for the global adjustment DACs. The MP7643 allows for a parallel data path. The clamp function would not normally be used in this configuration.

As shown in *Figure 11.*, by using the clamp pin, the global offset (black level) can be AC coupled to the ADC in order to simplify the offset calibration and eliminate thermal and power supply induced errors.

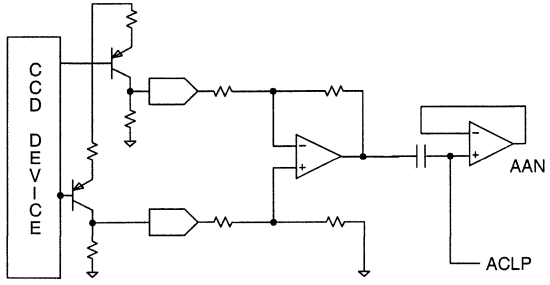


Figure 11. Configuration for CCD Digitizer using Black Level Clamp Channel A Shown

The amount of adjustment range available with the standard configuration may allow for the use of only one V_{REF} buffer amp by connecting the A, B, CFRC pins together on the MP8830 and using the ASENS pin as the feedback point to the buffer. BSENS and CSENS are open in this case. See *Figure 12.*

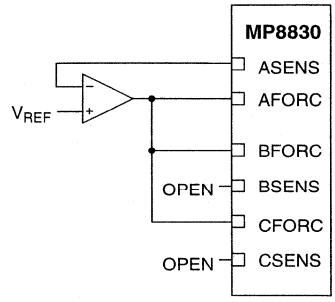


Figure 12. Simplified Reference Buffer Amp Configuration

Additional gain adjustment is possible by varying the channel V_{REF} voltage during calibration. *Figure 13.* shows a general drawing for this approach. By using the MP7643, the buffer amplifiers can be eliminated as shown in *Figure 14.*

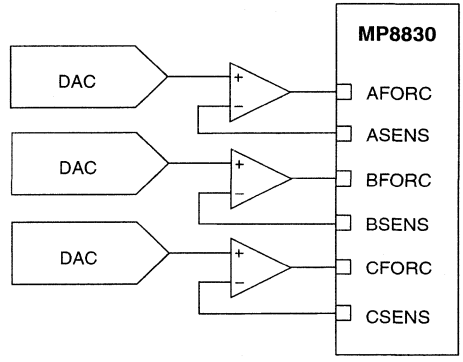


Figure 13. 3/8 of MP7670

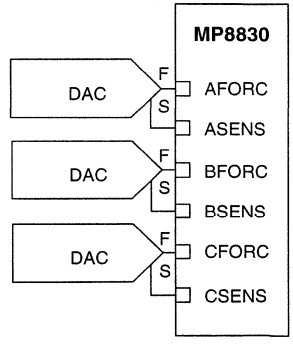
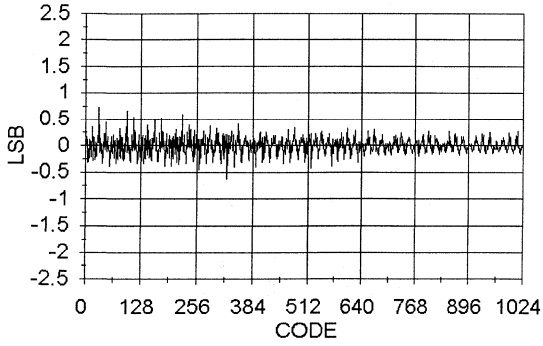
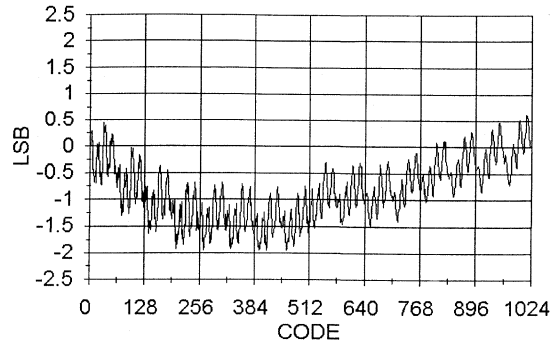


Figure 14. 3/4 of MP7643

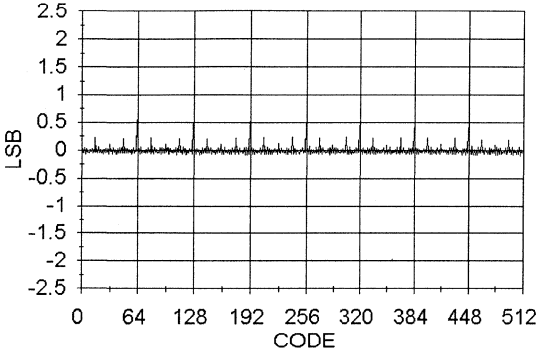
PERFORMANCE CHARACTERISTICS



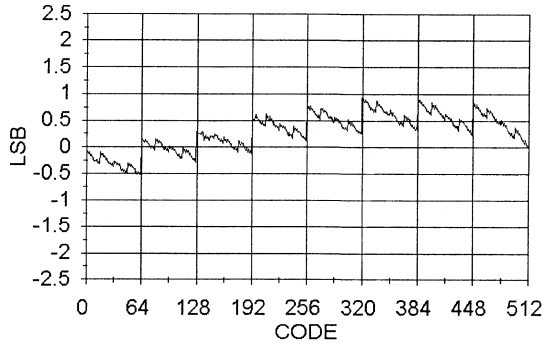
Graph 1. ADC DNL Error Plot Channel A



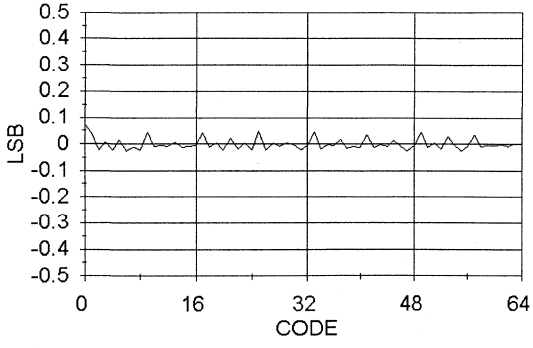
Graph 2. ADC INL Error Plot Channel A



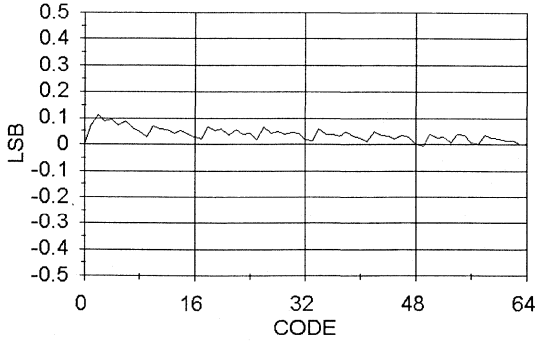
Graph 3. Gain DAC DNL Error Plot Channel A



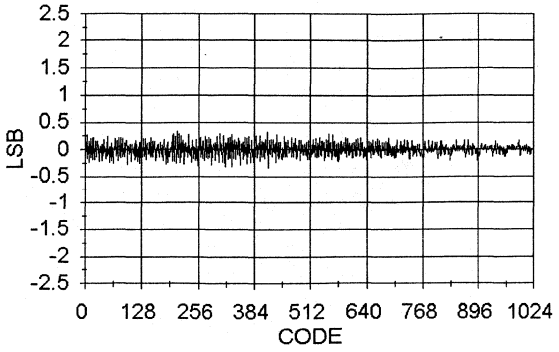
Graph 4. Gain DAC INL Error Plot Channel A



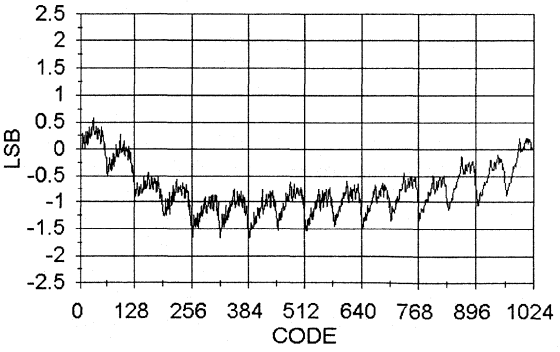
Graph 5. Offset DAC DNL Error Plot Channel A



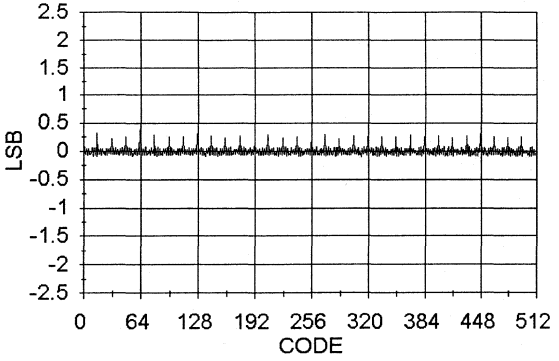
Graph 6. Offset DAC INL Error Plot Channel A



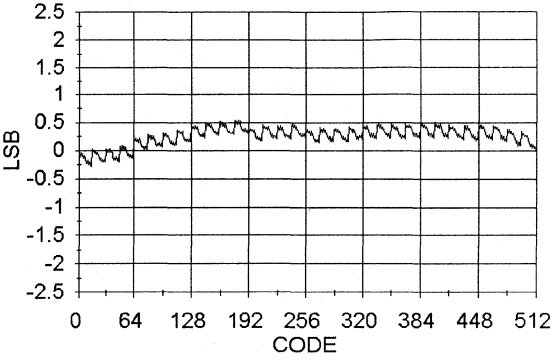
Graph 7. ADC DNL Error Plot
Channel B



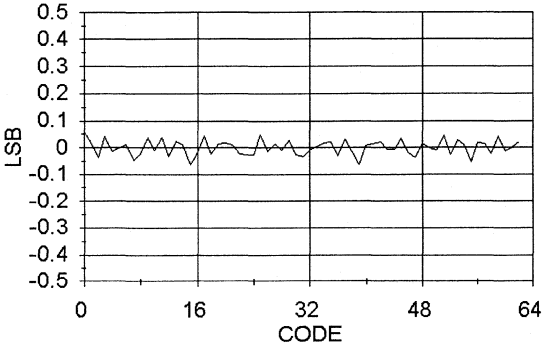
Graph 8. ADC INL Error Plot
Channel B



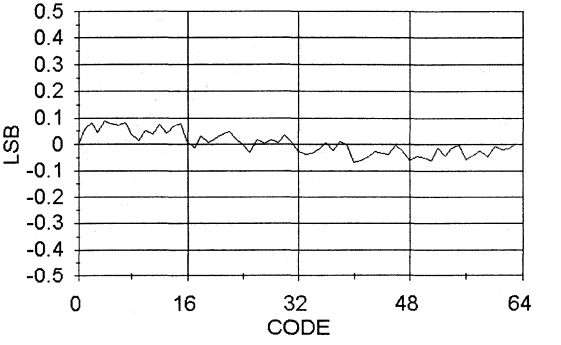
Graph 9. Gain DAC DNL Error Plot
Channel B



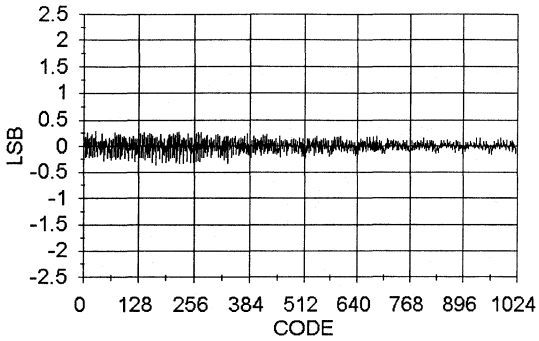
Graph 10. Gain DAC INL Error Plot
Channel B



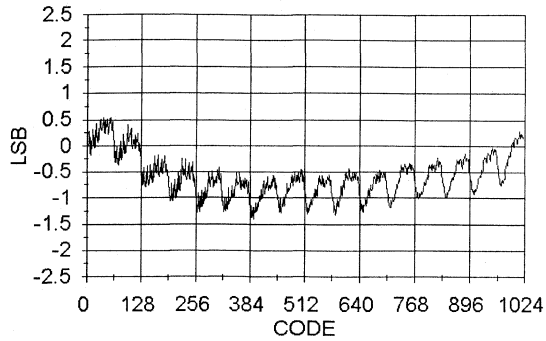
Graph 11. Offset DAC DNL Error Plot
Channel B



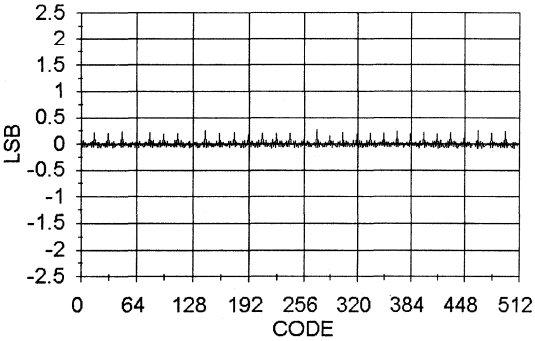
Graph 12. Offset DAC INL Error Plot
Channel B



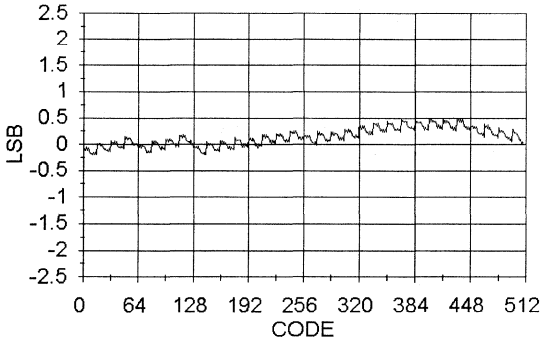
Graph 13. ADC DNL Error Plot Channel C



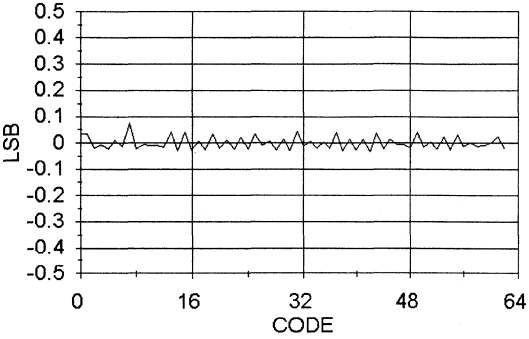
Graph 14. ADC INL Error Plot Channel C



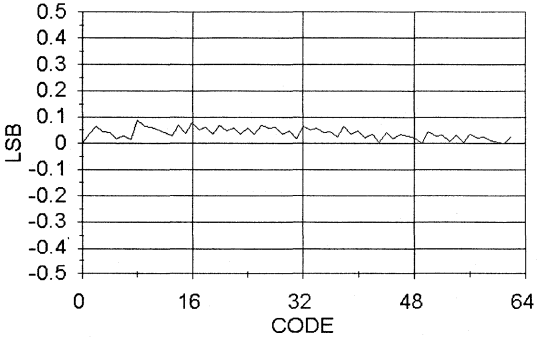
Graph 15. Gain DAC DNL Error Plot Channel C



Graph 16. Gain DAC INL Error Plot Channel C



Graph 17. Offset DAC DNL Error Plot Channel C



Graph 18. Offset DAC INL Error Plot Channel C

MP8831

10-Bit, High Speed Analog-to-Digital Converter with Digitally Controlled References

FEATURES

- **10-bit ADC with DNL < ±0.75 LSB**
- **1.25 MHz Sampling Rate**
- **Independent, Digitally Controlled ADC Offset & Full Scale Adjust**
  - **ADC Full Scale Range: 1.300V to 2.600V, with 9-bit Resolution**
  - **ADC Offset Range: 0.162V to 0.324V, with 6-bit Resolution**
  - **Update Rate: Pixel by Pixel**
- **Single 5 V Supply**
- **Low Power CMOS: 180 mW (typical)**
- **Power Down Mode (less than 100 μA)**
- **Latch-Up Free**
- **ESD Protection to over 2000V**

APPLICATIONS

- **Precision B/W & color CCD Scanners & Cameras**
- **Digital Copiers**
- **Infra-Red Image Digitizers**

BENEFITS

- **Improved Resolution Compared to Software Corrections**
- **Reduced Part Count & System Cost**
- **Lower Power Consumption & Power Down for Battery Applications**

3

GENERAL DESCRIPTION

The MP8831 is a 1.25 MSPS image digitizing chip that includes a 10-bit Analog-to-Digital Converter with Digital-to-Analog Converters that allow sample-to-sample corrections of the offset and full scale voltages. This allows imaging systems to calibrate and compensate for individual pixel offset and gain errors. The offset can be adjusted from 0.162V to 0.324V in 64 steps (6-bit resolution), while the full scale range (i.e. peak to peak input range) is adjustable from 1.3V to 2.6V in 512 steps (9-bit resolution).

The A/D converter uses a subranging architecture to achieve high sample rates and low power consumption. Our patented comparator design performs an on-chip track & hold function with a low analog input capacitance. Our proprietary high speed DAC design is used to drive and update the ADC reference ladder at a 5 MHz rate.

The MP8831 operates from a single +5 volt supply and an external 1V reference. Power consumption is typically only 180mW during conversion operation, and less that 500mW in power down mode.

Specified for operation over the industrial temperature range (0 to +70°C), the MP8831 is available in a Surface Mount (SOIC) package.

ORDERING INFORMATION

Package Type	Temperature Range	Part No.
SOIC	0 to +70°C	MP8831AS

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Section 4

Digital-to-Analog Converters

Listed Alpha-Numerically

Digital-to-Analog Converters

Fixed Voltage Output DACs

Resolution	14-Bit	12-Bit	8-Bit
Serial	MP7610	MP7612	
Parallel	MP7611	MP7613	MP7228 MP7226 (Quad)
# of Channels	Octal		

8-Bit Multiplying Voltage Output DACs

Input Bandwidth	≤5 MHz	≤10 MHz	≤15 MHz
Serial	MP7670 MP8840	MP7641 MP7651	MP7652
Parallel			MP7643
# of Channels	Octal		Quad

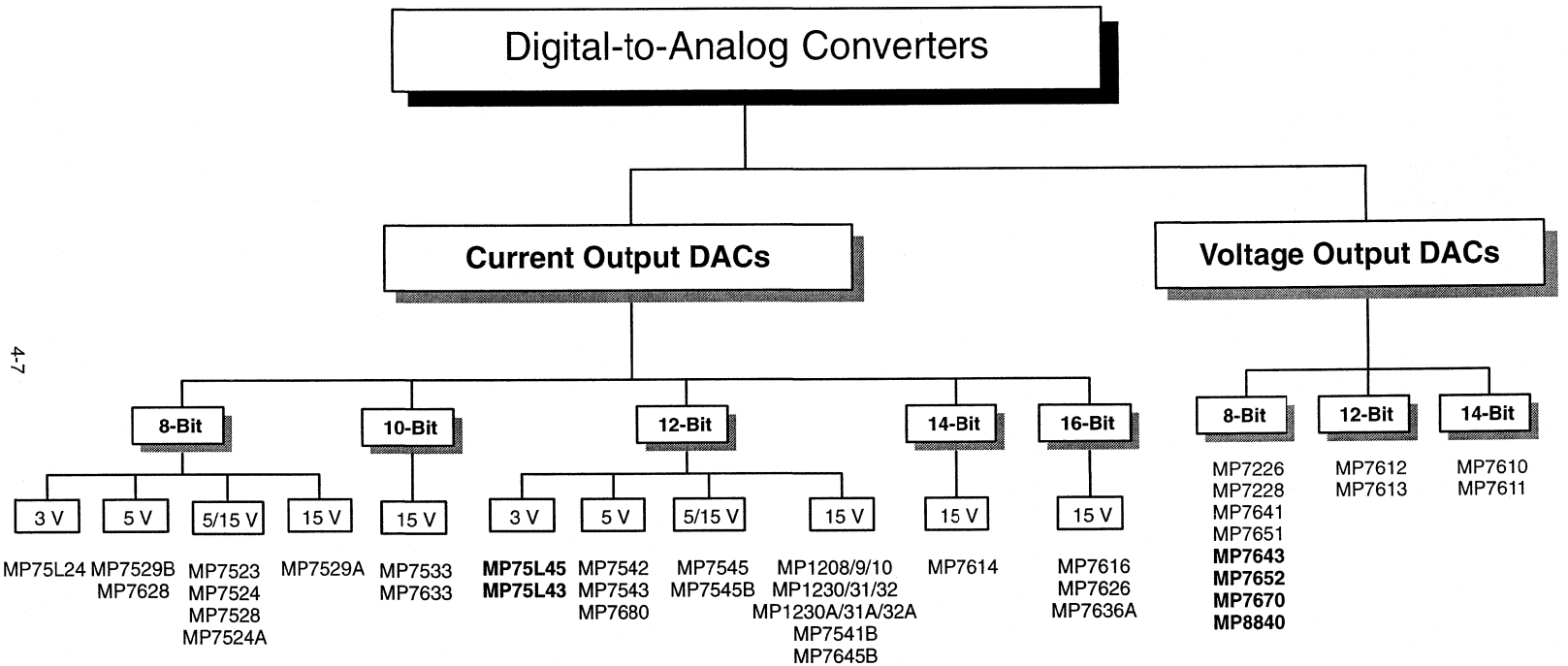
EXAR Corporation

Digital-to-Analog Converter Overview

Part #	Resolution (Bits)	# DACs	I or V/ FIX or MUL	Buffered or Double Buffered	Parallel or Serial	Operating Voltage Range	Pkg
MP7616	16	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7626	16	1	I/M 4Q	B	P	4.5 to 16.5 V	PDIP, CDIP, PLCC
MP7636A	16	1	I/M 4Q	DB	P	4.5 to 16.5 V	SOIC
MP7610	14	8	V/F	DB	S	+12/–12 V	PDIP, SOIC
MP7611	14	8	V/F	DB	P	+12/–12 V	PQFP, PGA, PLCC
MP7614	14	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7612	12	8	V/F	DB	S	+12/–12 V	PDIP, SOIC
MP7613	12	8	V/F	DB	P	+12/–12 V	PQFP, PGA, PLCC
MP7680	12	4	I/M 4Q	DB	P	4.5 to 5.5 V	PDIP, CDIP, PQFP
MP1208	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1209	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1210	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1230	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1230A	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP1231	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP1231A	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP1232	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP
MP1232A	12	1	I/M 4Q	DB	P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7541	12	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7541B	12	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7542	12	1	I/M 4Q	DB	P	4.5 to 5.5 V	PDIP, CDIP, SOIC
MP7543	12	1	I/M 4Q		S	4.5 to 5.5 V	PDIP, CDIP, SOIC, PLCC
MP7545	12	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7545B	12	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, SOIC, PLCC
MP7623	12	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7645B	12	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP
MP7533	10	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7633	10	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7641	8	8	V/M 2Q	B	S	±5, +5, +10 V	PDIP, SOIC
MP7651	8	8	V/M 2Q	B	S	±5 V	PDIP, SOIC
MP7670	8	8	V/M 4Q	B	S	–5, +5 V	PDIP, SOIC
MP8840	8	8	V/M 4Q	B	S	–5, +5 V	PDIP, SOIC
MP7643	8	4	V/M 2Q	B	P	±5, +5, +10 V	PDIP, SOIC
MP7652	8	4	V/M 2Q	B	S	±5, +5, +10 V	PDIP, SOIC
MP7226	8	4	V/F	DB	P	±5/15 V	PDIP, SOIC, PLCC
MP7628	8	4	I/M 4Q	B	P	4.5 to 5.5 V	PDIP, CDIP, SOIC, PLCC
MP7528	8	2	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7529A	8	2	I/M 4Q	B	P	4.5 to 16 V	PDIP, SOIC, PLCC
MP7529B	8	2	I/M 4Q	B	P	4.5 to 5.5 V	PDIP, SOIC, PLCC
MP7228	8	8	V/F	DB	P	±5/15 V	PDIP, CDIP, PLCC, SOIC
MP7523	8	1	I/M 4Q		P	4.5 to 16 V	PDIP, CDIP, SOIC
MP7524	8	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, CDIP, SOIC, PLCC
MP7524A	8	1	I/M 4Q	B	P	4.5 to 16 V	PDIP, SOIC

Definitions

I = Current Output, V = Voltage Output, F = Fixed Reference, M 2Q = Two Quadrant Multiplying, M 4Q = Four Quadrant Multiplying



Bold: New Product

New Product Highlights

Digital-to-Analog Converters

MP7643

4-Channel, Programmable Gain Voltage Output, 15 MHz Input Bandwidth 8-Bit DACs with Multiplying Parallel Digital Data Port

- Programmable Gain
- 4 Independent 2-Quadrant Multiplying 8-Bit DACs with Output Amplifiers
- Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability
- High Speed:
  - 12.5 MHz Digital Clock Rate
  - $V_{REF\ to}\ V_{OUT}$ Settling Time: 150ns to 8-bit (typ)
  - Voltage Reference Input Bandwidth: 15 MHz
- Very Low Noise Gain Control
- Low Power: 80mW
- Low AC Voltage Reference Feedthrough
- Excellent Channel-to-Channel Isolation
- DNL = ±0.5 LSB, INL = ±1 LSB (typ)
- DACs Matched to ±0.5% (typ)
- Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz
- Latch-Up Free
- ESD Protection: 2000 V Minimum

MP7652

4-Channel Voltage Output 15 MHz, Input Bandwidth, 8-Bit Multiplying DACs with 3-Wire Serial Digital Port and Independent References

- Independent References
- 4 Independent 2-Quadrant Multiplying 8-Bit DACs
- Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability
- High Speed:
  - 12.5 MHz Digital Clock Rate
  - $V_{REF\ to}\ V_{OUT}$ Settling Time: 150ns to 8–bit (typ)
  - Voltage Reference Input Bandwidth: 15 MHz
- Low Power: 80mW
- Low AC Voltage Reference Feedthrough
- Excellent Channel-to-Channel Isolation
- DNL = ±0.5 LSB, INL = ±1 LSB (typ)
- DACs Matched to ±0.5% (typ)
- Very Low Noise
- Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz
- $V_{REF}/2$ Output Preset Level
- Latch-Up Free
- ESD Protection: 2000 V Minimum

MP7670

8-Channel, Voltage Output, 5 MHz, 4 Quadrant Multiplying 8-Bit D/A Converter with Serial Digital Data Port

- 8 Independent 4-Quadrant Multiplying 8-Bit DACs
- High Speed:
  - Settling Time: 2.5 µs to ±1 LSB (typ)
  - Slew Rate: 5 V/µs (typ)
  - Voltage Reference Input Bandwidth: 5 MHz (V_{IN} = 100 mV p-p)
- Low Power: 80 mW (typ)
- DACs Matched to ±0.5% (typ)
- Power on Preset to Zero Volts for All Outputs
- Midscale Preset, all DAC Outputs are Zero Volts
- Latch-Up Free
- Greater than 2000 V ESD Protection

MP8840

8-Channel, Voltage Output, 2 MHz, 4 Quadrant Multiplying, 8-Bit DAC with Serial Digital Data Port

- 8 Independent 4-Quadrant Multiplying 8-Bit DACs
- High Speed:
  - Settling Time: 3.5 µs to ±1 LSB
  - Slew Rate: 4 V/µs
  - Voltage Reference Input Bandwidth: 2.5 MHz (V_{IN} = 100 mV p-p)
- Low Power: 80 mW (typ)
- DACs Matched to ±0.5% (typ)
- Midscale Preset, All DAC Outputs are Zero Volts
- Latch-Up Free
- Greater than 2000 V ESD Protection
- 5 MHz Version: MP7670

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MP1208/9/10

Microprocessor Compatible
Double-Buffered, 12-Bit
Digital-to-Analog Converter

FEATURES

- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **Stable, More Accurate Segmented DAC Approach**
- **Ultra Stable**
  - **0.2 ppm/°C Linearity Tempco**
  - **2 ppm/°C Max Gain Error Tempco**
- **Low Sensitivity to Amplifier V_{OS}**
- **Low Output Capacitance**
- **C_{OUT1} = 80 pF at Full Scale, Gives Fastest Settling Times, and Larger Stable Bandwidth capability**
- **Lower Glitch Energy**
- **Four Quadrant Multiplication**
- **All Parts guaranteed 12-Bit Monotonic**
- **Low Feedthrough Error**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Latch-Up Free**
- **–55°C to +125°C Operation**
- **8-Bit Bus Version: MP1230A/1231A/1232A**

4

GENERAL DESCRIPTION

The MP1208/09/10 series are 12-bit Digital-to-Analog Converters with an 8/4 bit latched input interface that provide maximum flexibility in interfacing to µP data bus. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP1208 series use a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$ = 1.

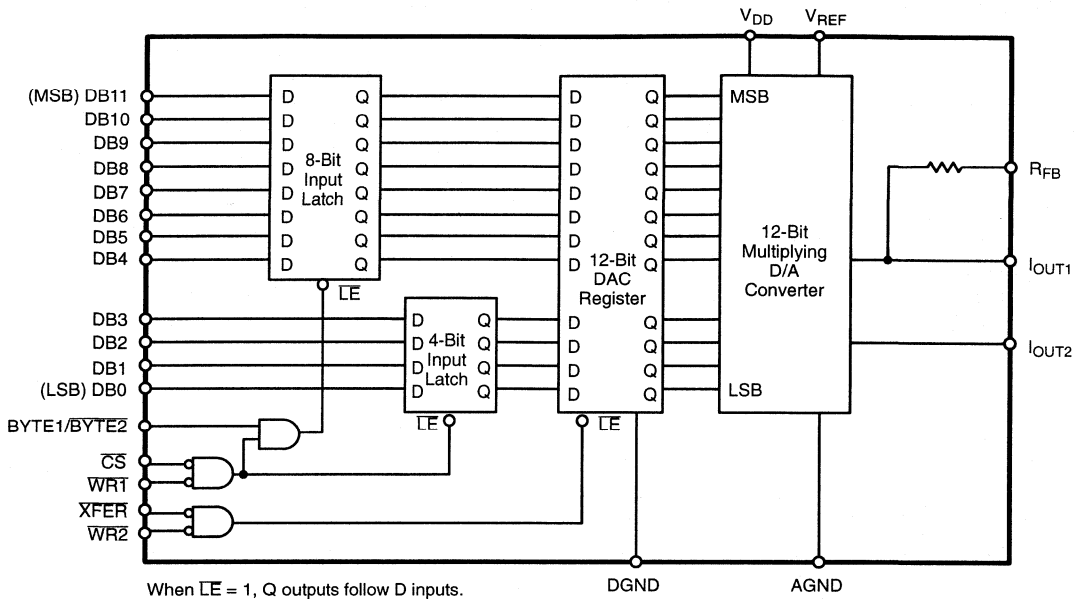
The MP1208 series are manufactured using advanced thin film resistors on a double metal CMOS process. The MP1208 series incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal trimming. Outstanding features include:

– Stability: Both integral and differential linearity are rated at 0.2 ppm/°C typical, and monotonicity is guaranteed over the entire temperature range including the industrial (–40 to +85°C) and military ranges. Scale factor is a low 2 ppm/°C maximum.

– Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} and I_{OUT2} are a low 80pF / 40pF and 25pF / 65 pF for the conditions of full/zero scale. This is over two times less than the National DAC 1208 Series. Lower capacitance allows the MP1208 series to achieve faster CMOS DAC settling times; less than 1 µsec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available, for a given amplifier loop gain, because a smaller feedback "zero" compensating capacitor is required to offset the smaller I_{OUT} capacitance.

– Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP1208 series over conventional R-2R DACs, to 330µV per millivolt of offset.

SIMPLIFIED BLOCK DIAGRAM



When $\overline{LE}$ = 1, Q outputs follow D inputs.

When $\overline{LE}$ = 0, Q outputs are latched.

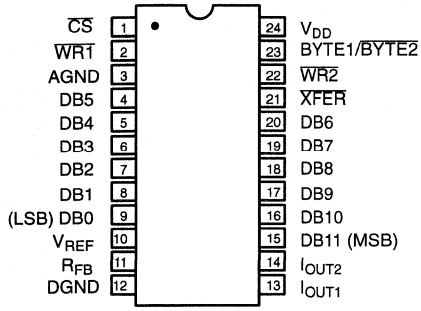
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP1210HN	±2	±2	±0.4
Plastic Dip	–40 to +85°C	MP1209JN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP1208KN	±1/2	±3/4	±0.4
Ceramic Dip	–40 to +85°C	MP1208BD	±1/2	±3/4	±0.4
Ceramic Dip	–55 to +125°C	MP1208TD*	±1/2	±3/4	±0.4
Ceramic Dip	–40 to +85°C	MP1209AD	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP1209SD*	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP1210RD*	±2	±2	±0.4

*Contact factory for non-compliant military processing

PIN CONFIGURATION

See Packaging Section for Package Dimensions



24 Pin CDIP, PDIP (0.600")
D24, N24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{CS}$	Chip Select (Active Low)
2	$\overline{WR1}$	Write1 (Active Low)
3	AGND	Analog Ground
4	DB5	Data Input Bit 5
5	DB4	Data Input Bit 4
6	DB3	Data Input Bit 3
7	DB2	Data Input Bit 2
8	DB1	Data Input Bit 1
9	DB0	Data Input Bit 0 (LSB)
10	V_{REF}	Reference Input Voltage
11	R_{FB}	Internal Feedback Resistor
12	DGND	Digital Ground
13	I_{OUT1}	Current Output 1
14	I_{OUT2}	Current Output 2
15	DB11	Data Input Bit 11 (MSB)
16	DB10	Data Input Bit 10
17	DB9	Data Input Bit 9
18	DB8	Data Input Bit 8
19	DB7	Data Input Bit 7
20	DB6	Data Input Bit 6
21	$\overline{XFER}$	Transfer Control Signal (Active Low)
22	$\overline{WR2}$	Write 2 (Active Low)
23	BYTE1/ $\overline{BYTE2}$	Byte Sequence Control
24	V_{DD}	Positive Power Supply

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
MP1208				±1/2		±1/2		
MP1209				±1		±1		
MP1210				±2		±2		
Differential Non-Linearity	DNL						LSB	
MP1208				±3/4		±3/4		
MP1209				±1		±1		
MP1210				±2		±2		
Gain Error	GE		±0.1	±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ±5%
Output Leakage Current	I_{OUT}	–10	1	10		±200	nA	
DYNAMIC PERFORMANCE[2]								RL=100Ω, CL=13pF
Current Settling Time	t_S		1				µs	Full Scale Change to 1/2 LSB R_L = 100Ω
AC Feedthrough at I_{OUT1}	FT		1				mV p-p	V_{REF}=100kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
V_{IN}[2]			±10	±25			V	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}	–1	0.1	1		±1	µA	V_{IN} = 0 or V_{DD}
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT1}		80	100			pF	DAC Inputs all 1's
	C_{OUT1}		40	60			pF	DAC Inputs all 0's
	C_{OUT2}		65	85			pF	DAC Inputs all 0's
	C_{OUT2}		25	45			pF	DAC Inputs all 1's
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}		1.2	2.0		2.0	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Write and $\overline{XFER}$ Pulse Width	t_{WR}	100	50				ns	
Data Set-Up Time	t_{DS}	100	50				ns	
Data Hold Time	t_{DH}	90	70				ns	
Control Set-Up Time	t_{CS}	200	100				ns	
Control Hold Time	t_{CH}	10	0				ns	

NOTES:

1 Full Scale Range (FSR) is 10V.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

4

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP 1150mW
Derates above 75°C ..... 15mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

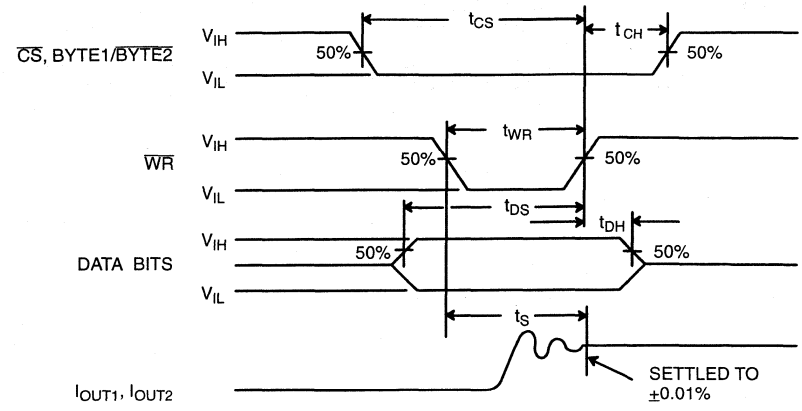


Figure 1. Timing Diagram

APPLICATION NOTES
Refer to Section 8 for Applications Information

The MP1208 series allows direct interface to microprocessor system buses without the need for additional interface circuitry. They also provide all 12 data input lines in parallel for optimum interface to a 16-bit data bus, but can be mapped onto an 8-bit bus by tying lines DB0 through DB3 to lines DB8 through DB11, respectively.

All digital inputs maintain TTL compatibility over the entire range of V_{DD}. The internal latches are lever-triggered, and therefore can be hardwired for transparent operation. The MP1208 series can be wired for a single layer of buffering by tying the 12 bit DAC register transparent (ground $\overline{XFER}$ and $\overline{WR2}$) or by tying the 8-bit and 4-bit latch transparent (ground $\overline{CS}$, $\overline{WR1}$, BYTE1/$\overline{BYTE2}$ = V_{DD}). In non-microprocessor applications, the MP1208 series can be wired for flow-through operation. The analog output will continuously reflect the state of the digital inputs by tying the 8-bit latch, 4-bit latch, and 12-bit DAC register transparent.

Double-buffering provides the user with the capability of refreshing simultaneously all 12 data bits to the DAC from an 8-bit data bus. Double-buffering also allows a single DAC or several DACs to be updated from the same data bus at the same time. This will be done asynchronously by an external monitoring device (such as a voltage comparator) or by a system interrupt. In this example, tie $\overline{WR2}$ low and use the $\overline{XFER}$ to update the 12-bit register.

For a two byte load, tie BYTE1/$\overline{BYTE2}$ and $\overline{XFER}$ together and $\overline{WR1}$ and $\overline{WR2}$ together. The first write will update the 8-bit input latch (the 4-bit latch is also changed). The second write will overwrite the 4-bit latch and transfer all 12 bits to the 12-bit DAC register, updating the D/A converter. (See *Typical Application.*)

MP1230/31/32

Microprocessor Compatible
Double-Buffered 12-Bit
Digital-to-Analog Converter

FEATURES

- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **Stable, More Accurate Segmented DAC Approach**
- **Ultra Stable**
  - **0.2 ppm/°C Linearity Tempco**
  - **2 ppm/°C Max. Gain Error Tempco**
- **Low Sensitivity to Amplifier V_{OS}**
- **C_{OUT1} = 80 pF at Full Scale, Gives Fastest Settling Times and Larger, Stable Bandwidth**
- **Lower Glitch Energy**
- **Four Quadrant Multiplication**
- **Low Feedthrough Error**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Latch-Up Free**
- **Use MP1230A/1231A/1232A for New Designs**

4

GENERAL DESCRIPTION

The MP1230/31/32 are 12-bit Digital-to-Analog Converters with 8/4 bit latched inputs for direct interface to the 8-bit data bus. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP1230 series uses a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$= 1.

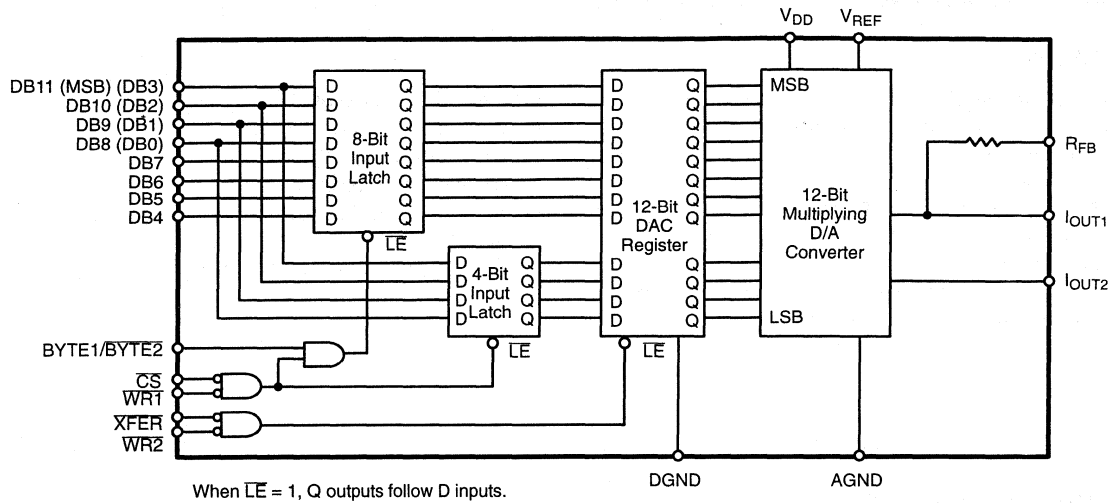
The MP1230 series is manufactured using advanced thin film resistors on a double metal CMOS process. The MP1230 series incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal trimming. Outstanding features include:

- Stability: Both integral and differential linearity are rated at 0.2 ppm/°C typical, and monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. Scale factor is a low 2 ppm/°C maximum.

- Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} is a low 80pF / 40pF and 25pF / 65 pF at I_{OUT2} for the conditions of full scale/zero . This is over twice less than the National DAC1230 Series. Lower capacitance allows the MP1230 series to achieve faster CMOS DAC settling times; less than 1 µsec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available for a given amplifier loop gain because a smaller feedback "zero" compensating capacitor is required to offset the smaller I_{OUT} capacitance.

- Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP1208/1230 series over conventional R-2R DACs, to 330µV per millivolt of offset.

SIMPLIFIED BLOCK DIAGRAM



When $\overline{LE}$ = 1, Q outputs follow D inputs.
When $\overline{LE}$ = 0, Q outputs are latched.

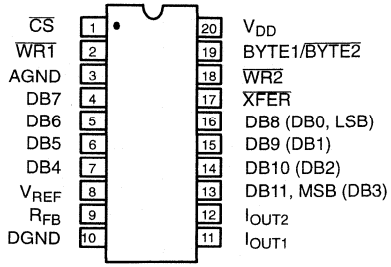
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP1231JN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP1230KN	±1/2	±3/4	±0.4
Plastic Dip	–40 to +85°C	MP1232HN	±2	±2	±0.4
SOIC	–40 to +85°C	MP1231JS	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP1231AD	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP1230BD	±1/2	±3/4	±0.4
Ceramic Dip	–40 to +85°C	MP1232ZD	±2	±2	±0.4
Ceramic Dip	–55 to +125°C	MP1231SD*	±1	±1	±0.4

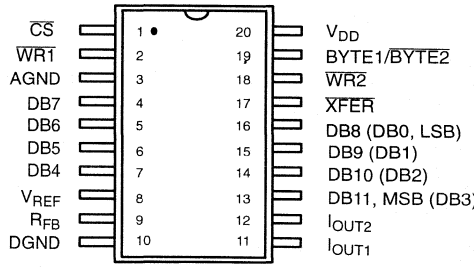
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{CS}$	Chip Select (Active Low)
2	$\overline{WR1}$	Write 1 (Active Low)
3	AGND	Analog Ground
4	DB7	Data Input Bit 7
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	V_{REF}	Reference Input Voltage
9	R_{FB}	Internal Feedback Resistor
10	DGND	Digital Ground
11	I_{OUT1}	Current Output 1
12	I_{OUT2}	Current Output 2
13	DB11 (DB3)	Data Input Bit 9 (MSB)
14	DB10 (DB2)	Current Output 10
15	DB9 (DB1)	Data Input Bit 9
16	DB8 (DB0)	Data Input Bit 8 (LSB)
17	$\overline{XFER}$	Transfer Control Signal (Active Low)
18	$\overline{WR2}$	Write 2 (Active Low)
19	BYTE1/ $\overline{BYTE2}$	Byte Sequence Control
20	V_{DD}	Positive Power Supply

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12			Bits
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
MP1230				±1/2		±1/2		
MP1231				±1		±1		
MP1232				±2		±2		
Differential Non-Linearity	DNL						LSB	
MP1230				±3/4		±3/4		
MP1231				±1		±1		
MP1232				±2		±2		
Gain Error	GE		±0.1	±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		1			±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		5	±20		±20	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}		1	±10		±200	nA	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S		1.0				µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T		1.0				mV p-p	V_{REF}=100kHz, 20Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}		0.1	±1		±1	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		80	100			pF	DAC Inputs all 1's
	C_{OUT1}		40	60			pF	DAC Inputs all 0's
	C_{OUT2}		65	85			pF	DAC Inputs all 1's
	C_{OUT2}		25	45			pF	DAC Inputs all 0's
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	4.5	15	16			V	
Supply Current	I_{DD}		1.2	2		2	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
$\overline{WR}$, $\overline{XFER}$ Pulse Width	t_{WR}	100	50				ns	
Data Set-Up Time	t_{DS}	100	50				ns	
Data Hold Time	t_{DH}	90	70				ns	
$\overline{CS}$ Set-Up Time	t_{CS}	200	100				ns	
$\overline{CS}$ Hold Time	t_{CH}	10	0				ns	

NOTES:

1 Full Scale Range (FSR) is 10V.
2 Guaranteed but not production tested
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See switching waveforms
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

4

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

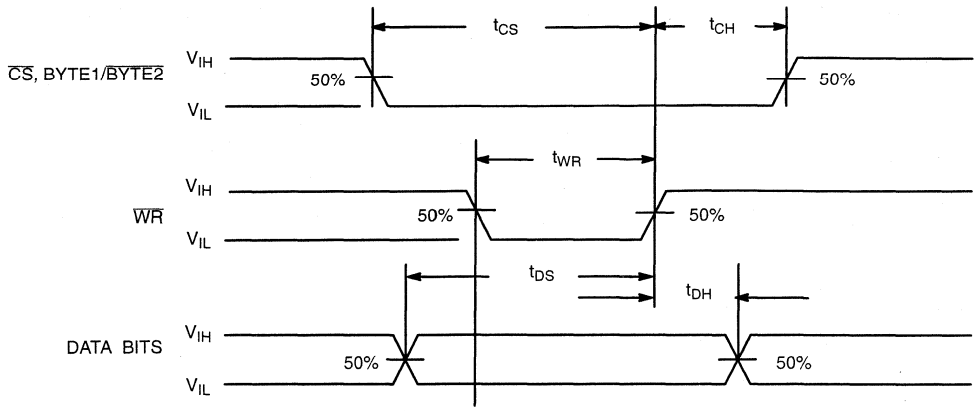
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

SWITCHING WAVEFORMS



DEFINITION OF CONTROL SIGNALS:

$\overline{CS}$: Chip Select.(Active low)
It will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1 (Active low)
The $\overline{WR1}$ is used to load the digital data bits (DB) into the input latch.

BYTE1/$\overline{BYTE2}$: Byte sequence control.
The BYTE1/$\overline{BYTE2}$ control pin is used to select both MSB and LSB input latches.

$\overline{WR2}$: Write 2 (Active low)
It will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer control signal (Active low)
This signal in combination with $\overline{WR2}$ causes the 16-bit data which is available in the input latches to transfer to the DAC register

DB0 to DB11: Digital Inputs.
DB0 is the least significant digital input (LSB) and DB11 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1 Bus.
I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in the DAC register.

I_{OUT2}: DAC Current Output 2 Bus.
I_{OUT2} is a complement of I_{OUT1}.

R_{FB}: Feedback Resistor.
This internal feedback resistor should always be used (not an external resistor) since it matches the resistors in the DAC and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input.
This input connects an external precision voltage source to the internal DAC. The V_{REF} can be selected over the range of +25V to –25V or the analog signal for a 4-quadrant multiplying mode application.

V_{DD}: Power Supply Voltage.
This is the power supply pin for the part. The V_{DD} can be from +5 V DC to +15 V DC, however optimum voltage is +12 to +15 V DC.

AGND: Analog Ground
Back gate of the DAC N-channel current steering switches.

DGND: Digital Ground

APPLICATION NOTES

Refer to Section 8 for Applications Information

The MP1230 series allows direct interface to microprocessor system buses without the need for additional interface circuitry. They provide 8 data input lines in parallel for optimum interface to a 16-bit data bus, but can be mapped onto an 8-bit bus by tying lines DB0 through DB3 to lines DB8 through DB11, respectively.

All digital inputs maintain TTL compatibility over the entire range of V_{DD}. The internal latches are level-triggered, and therefore can be hardwired for transparent operation. The MP1208 series can be wired for a single layer of buffering by tying the 12-bit DAC register transparent (ground $\overline{XFER}$ and $\overline{WR2}$) or by tying the 8-bit and 4-bit latch transparent (ground $\overline{CS}$, $\overline{WR1}$, BYTE1/$\overline{BYTE2}$ = V_{DD}). In non-microprocessor applications, the MP1230 series can be wired for flow-through operation. The analog output will continuously reflect the state of the digital inputs by tying the 8-bit latch, 4-bit latch, and 12-bit DAC register transparent.

Double-buffering provides the user with the capability of refreshing simultaneously all 12 data bits to the DAC from an 8-bit data bus. Double-buffering also allows a single DAC or several DACs to be updated from the same data bus at the same time. This will be done asynchronously by an external monitoring device (such as a voltage comparator) or by a system interrupt. In this example, tie $\overline{WR2}$ low and use the $\overline{XFER}$ to update the 12-bit register.

For a two byte load, tie BYTE1/$\overline{BYTE2}$ and $\overline{XFER}$ together and $\overline{WR1}$ and $\overline{WR2}$ together. The first write will update the 8-bit input latch (the 4-bit latch is also changed). The second write will overwrite the 4-bit latch and transfer all 12 bits to the 12-bit DAC register, updating the DAC. (*See Typical Application.*)

Use the high order address lines for the device select ($\overline{CS}$). Normally the low order address lines (A0, A1) will be decoded for BYTE1/$\overline{BYTE2}$ and $\overline{XFER}$. The $\overline{XFER}$ input can be decoded independently (3 write loads) when independent control is desired.

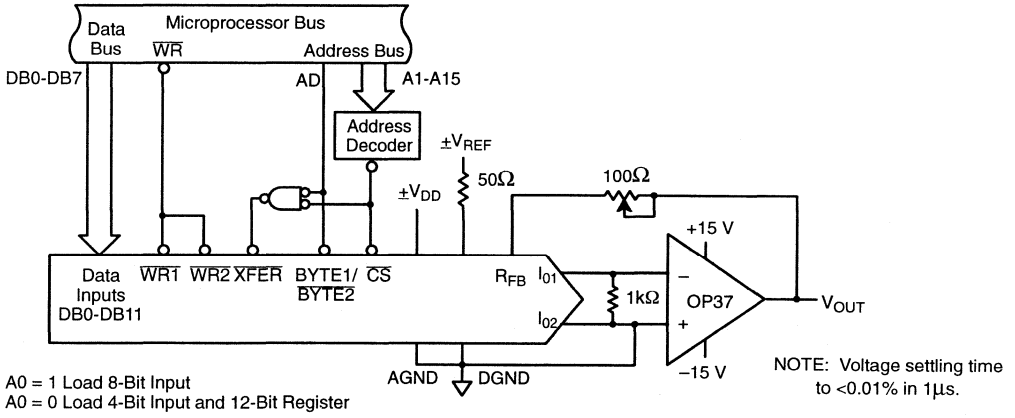


Figure 1. Two Write Load / Unipolar Configuration

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MP1230A/31A/32A

CMOS Microprocessor Compatible
Double-Buffered 12-Bit
Digital-to-Analog Converter

FEATURES

- **Superior Ruggedized 1230 Series: 2 KV ESD**
- **Four Quadrant Multiplication**
- **Stable, More Accurate Segmented DAC Approach**
  - **0.2 ppm/°C Linearity Tempco**
  - **2 ppm/°C Max Gain Error Tempco**
  - **Lowest Sensitivity to Amplifier Offset**
  - **Lowest Output Capacitance (C_{OUT} = 80pF)**
  - **Lower Glitch Energy**
- **Monotonic over Temperature Range**
- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **V_{DD} from +11 V to +16 V**
- **Latch-Up Free CMOS Technology**
- **12-Bit Bus Version: MP1208/1209/1210**
- **16-Bit Upgrade: MP7636A**

GENERAL DESCRIPTION

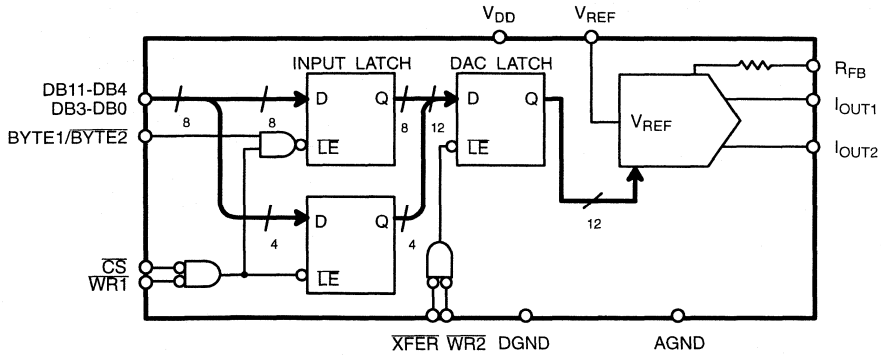
The MP1230A series are superior pin for pin replacements for the 1230 series. The MP1230A series is manufactured using advanced thin film resistors on a double metal CMOS process which promotes significant improvements in reliability, latch-up free performance and ESD protection.

The MP1230A series incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved without trimming. Outstanding features include:

- Stability: integral and differential linearity tempcos are rated at 0.2 ppm/°C typical. Monotonicity is guaranteed over all temperature ranges. Scale factor tempco is a low 2 ppm/°C maximum.
- Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} and I_{OUT2} is a low 80pF / 40pF and 25pF / 65 pF. This less than half the competitive DAC 1230 series. Lower capacitance allows the MP1230A series to achieve settling times faster than 1 µs for a 10 V step.
- Low Sensitivity to Output Amplifier Offset: The linearity error caused by amplifier offset is reduced by a factor of 2 in the MP1230A series over conventional R-2R DACs.

The MP1230A series uses a circuit which reduces transients in the supplies caused by DATA bus transitions at $\overline{CS}$ = 1.

SIMPLIFIED BLOCK DIAGRAM

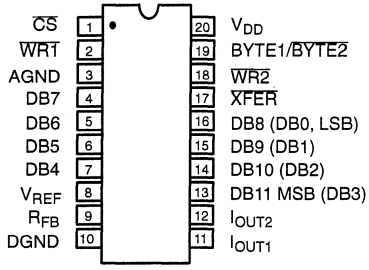


ORDERING INFORMATION

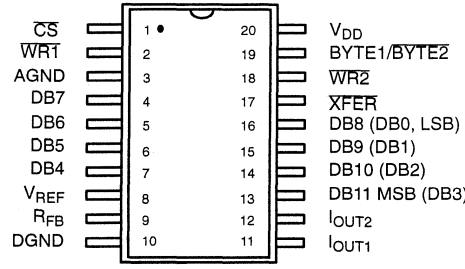
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP1230ABN	±1/2	±3/4	±0.4
Plastic Dip	–40 to +85°C	MP1231ABN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP1232ABN	±2	±2	±0.4
SOIC	–40 to +85°C	MP1230ABS	±1/2	±3/4	±0.4
SOIC	–40 to +85°C	MP1231ABS	±1	±1	±0.4
SOIC	–40 to +85°C	MP1232ABS	±2	±2	±0.4

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{CS}$	Chip Select (Active Low)
2	$\overline{WR1}$	Write 1 (Active Low)
3	AGND	Analog Ground
4	DB7	Data Input Bit 7
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	V_{REF}	Reference Input Voltage
9	R_{FB}	Feedback Resistor
10	DGND	Digital Ground
11	I_{OUT1}	Current Output 1

PIN NO.	NAME	DESCRIPTION
12	I_{OUT2}	Current Output 2
13	DB11 (DB3)	Data Input Bit 11 (MSB) Data Input Bit 3
14	DB10 (DB2)	Data Input Bit 10 Data Input Bit 2
15	DB9 (DB1)	Data Input Bit 9 Data Input Bit 1
16	DB8 (DB0)	Data Input Bit 8 Data Input Bit 0 (LSB)
17	$\overline{XFER}$	Transfer Control Signal (Active Low)
18	$\overline{WR2}$	Write 2 (Active Low)
19	BYTE1/ $\overline{BYTE2}$	Byte Sequence Control
20	V_{DD}	Positive Power Supply

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
MP1230ABN/ATD/ABS				±1/2		±1/2		
MP1231ABN/ATD/ABS				±1		±1		
MP1232ABN/ATD/ABS				±2		±2		
Differential Non-Linearity	DNL						LSB	
MP1230ABN/ATD/ABS				±3/4		±3/4		
MP1231ABN/ATD/ABS				±1		±1		
MP1232ABN/ATD/ABS				±2		±2		
Gain Error	GE			±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		0.5			±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		5	±20		±20	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 0.25V
Output Leakage Current	I_{OUT}		1	±10		±200	nA	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S		1.0				µsec	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T		1.0				mV p-p	V_{REF}=100kHz, 20Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0, 5 V
Input Capacitance[2]			10				pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		80	100		100	pF	DAC Inputs all 1's
	C_{OUT1}		40	60		60	pF	DAC Inputs all 0's
	C_{OUT2}		65	85		85	pF	DAC Inputs all 1's
	C_{OUT2}		25	45		45	pF	DAC Inputs all 0's
POWER SUPPLY								
Functional Voltage Range[4]	V_{DD}	+4.5		+16	+4.5	+16	V	
Supply Current	I_{DD}		1.2	2.0		2.0	mA	All digital inputs = 0 V or all = 5 V

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 3]								
Chip Select to Write Set-Up Time	t_{CS}	200	100				ns	
Chip Select to Write Hold Time	t_{CH}	10	0				ns	
Data Valid to Write Set-Up Time	t_{DS}	100	50				ns	
Data Valid to Write Hold Time	t_{DH}	90	70				ns	
Write Pulse Width,	t_{WR}	100	50				ns	

NOTES:

1 Full Scale Range (FSR) is 10V.
2 Guaranteed but not production tested.
3 See timing diagram.
4 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to +6.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

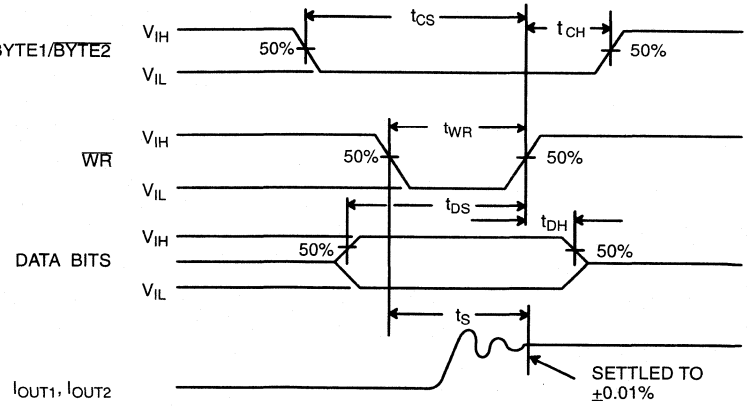
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

TIMING DIAGRAM



DEFINITION OF CONTROL SIGNALS:

$\overline{CS}$: Chip Select.(Active low)
It will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1 (Active low)
The $\overline{WR1}$ is used to load the digital data bits (DB) into the input latch.

BYTE1/$\overline{BYTE2}$: Byte sequence control.
The BYTE1/$\overline{BYTE2}$ control pin is used to select both MSB and LSB input latches.

$\overline{WR2}$: Write 2 (Active low)
It will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer control signal (Active low)
This signal in combination with $\overline{WR2}$ causes the 16-bit data which is available in the input latches to transfer to the DAC register

DB0 to DB11: Digital Inputs.
DB0 is the least significant digital input (LSB) and DB11 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1 Bus.
I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in the DAC register.

I_{OUT2}: DAC Current Output 2 Bus.
I_{OUT2} is a complement of I_{OUT1}.

R_{FB}: Feedback Resistor.
This internal feedback resistor should always be used (not an external resistor) since it matches the resistors in the DAC and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input.
This input connects an external precision voltage source to the internal DAC. The V_{REF} can be selected over the range of +25V to –25V or the analog signal for a 4-quadrant multiplying mode application.

V_{DD}: Power Supply Voltage.
This is the power supply pin for the part. The V_{DD} can be from +5 V DC to +15 V DC, however optimum voltage is +12 to +15 V DC.

AGND: Analog Ground
Back gate of the DAC N-channel current steering switches.

DGND: Digital Ground

4

THEORY OF OPERATION

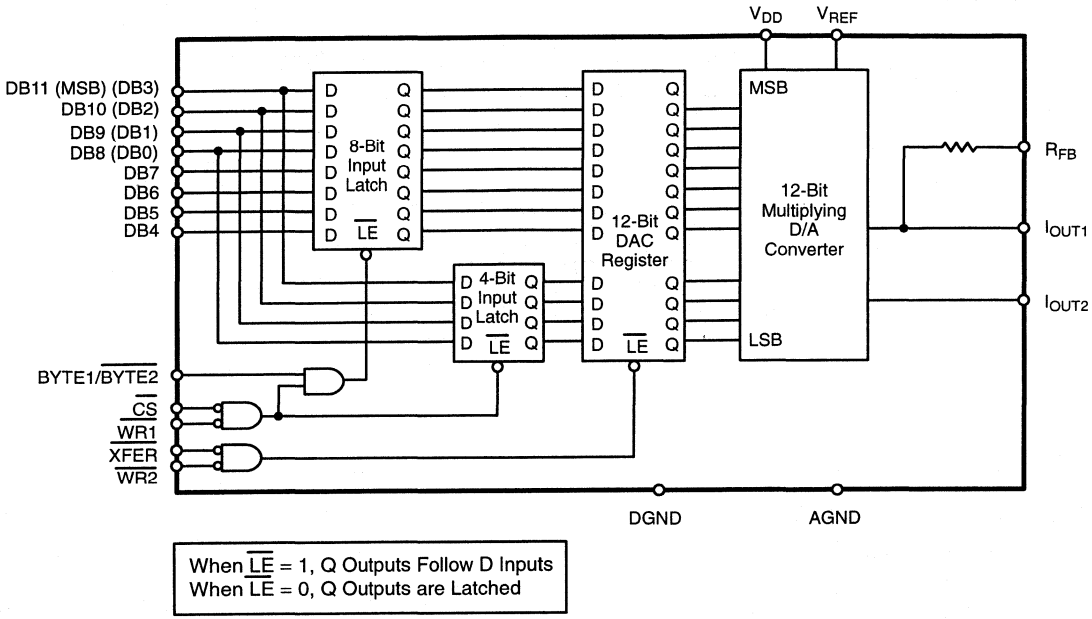


Figure 1. Functional Diagram

Digital Interface

Figure 1. shows the internal control logic that controls the writing of the input latches. It is easy to understand how the MP1230A/31A/32A works by understanding each basic operation.

Writing to Input Latches

The condition BYTE1/$\overline{\text{BYTE2}}$= high, $\overline{\text{CS}}$ = $\overline{\text{WR1}}$ = 0 loads the data bus DB11-DB4 into both input latches.

A second cycle with BYTE1/$\overline{\text{BYTE2}}$ = low (*Figure 2.*) loads the pins DB11-DB8 (DB3-DB0) into the 4-bit input latch.

Timing diagrams show the inputs $\overline{\text{CS}}$ and DB11-DB0 to be stable during the entire writing cycle. In reality all the above signals can change (*Figure 2.*) as long as they meet the timing conditions specified in the Electrical Characteristic Table.

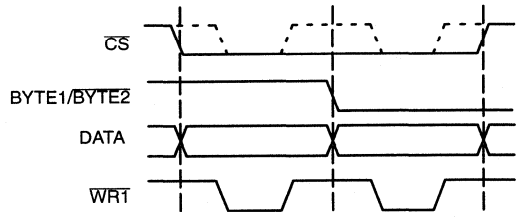


Figure 2. Write Cycles to Input Latches

Transferring Data to the DAC Latches

Once one or all the input latches have been loaded, the condition $\overline{\text{XFER}}$= $\overline{\text{WR2}}$= low transfers the content of the input latches in the DAC latch. The outputs of the DAC latch change and the DAC current (I_{OUT}) will reach a new stable value within the settling time t_S (*Figure 3.*).

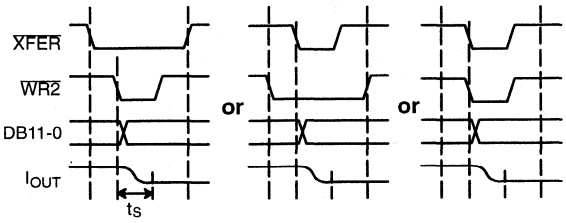
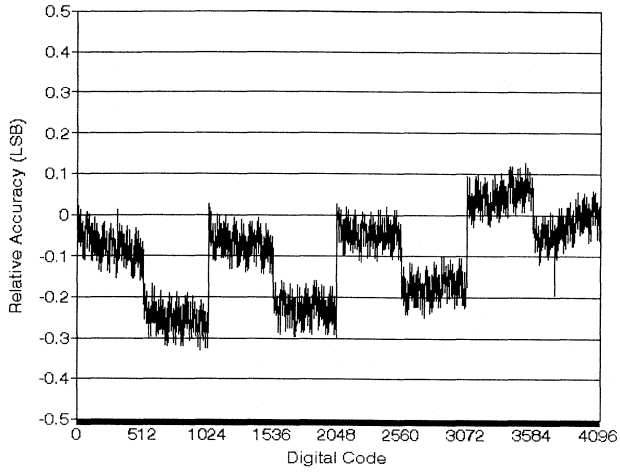


Figure 3. Transfer Cycles from Input Latches to DAC Latches

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information

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MP7226

BiCMOS
Fixed, Quad, Voltage Output, Single or Dual Supply 8-Bit Digital-to-Analog Converter

FEATURES

- MPS Pioneered Segmented DAC Approach
- Four 8-Bit DACs with Buffer Amplifiers
- Bipolar Amplifier Inputs for Low Noise and Drift
- Operates with Single or Dual Supplies
- µP Compatible (95ns $\overline{WR}$)
- No External Adjustments Required
- Power-on-Reset Function
- Specified for 5 to 15 V Operation
- ESD Protection: 2000 Volts Minimum
- Latch-Up Proof
- Octal Available: MP7228

APPLICATIONS

- Function Generators
- Automatic Test Equipment
- Process Controls

BENEFITS

- Reduced Board Space; Lower System Cost
- Reduced System Errors due to Excellent DAC-to-DAC Matching and Tracking
- Easy to Design with Microprocessors
- Stable, High Reliability through Advanced Processing
- Lower 1/f Noise Increases Useful Dynamic Range

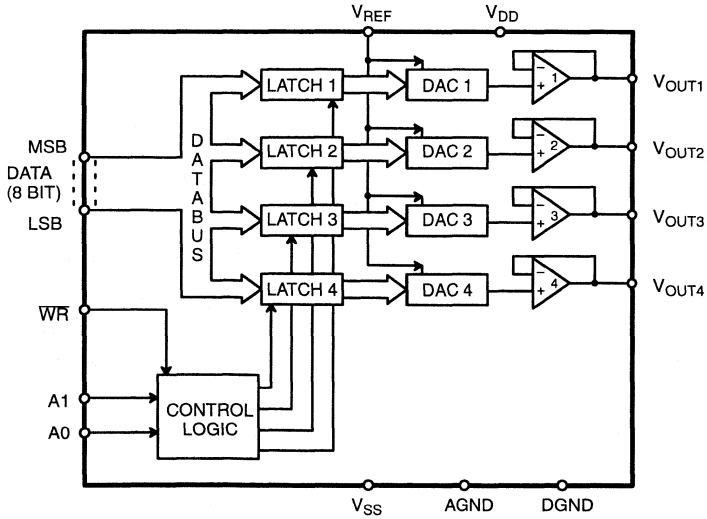
4

GENERAL DESCRIPTION

The MP7226 contains four 8-bit voltage-output Digital-to-Analog Converters, with BiCMOS output buffer amplifiers and interface logic on a monolithic chip. Separate on-chip latches are provided for each of the four D/A converters. The control logic is speed compatible with most 8-bit microprocessors. All digital inputs are TTL/CMOS(5V) compatible.

The MP7226 is manufactured using advanced thin film resistors on a double metal BiCMOS process. The MP7226 incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7226 maintains 8-Bit accuracy over the full operating temperature range without laser trim or external adjustments.

SIMPLIFIED BLOCK DIAGRAM



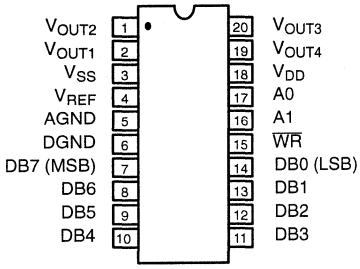
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Full Scale Error (LSB)
Plastic Dip	–40 to +85°C	MP7226KN	1	±1/2	±1
Plastic Dip	–40 to +85°C	MP7226LN*	1/2	±1/2	±1/2
PLCC	–40 to +85°C	MP7226KP	1	±1/2	±1
PLCC	–40 to +85°C	MP7226LP*	1/2	±1/2	±1/2
SOIC	–40 to +85°C	MP7226KS	1	±1/2	±1
SOIC	–40 to +85°C	MP7226LS*	1/2	±1/2	±1/2

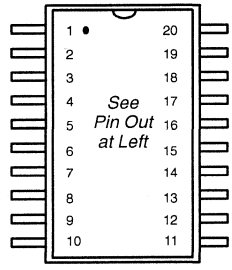
*Contact factory for availability.

PIN CONFIGURATIONS

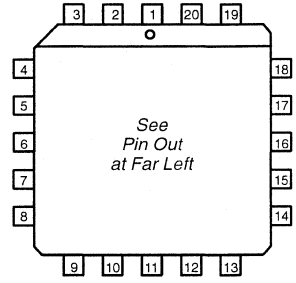
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{OUT2}	DAC 2 Voltage Output
2	V_{OUT1}	DAC 1 Voltage Output
3	V_{SS}	Negative Power Supply (0 V to –5 V)
4	V_{REF}	Reference Input Voltage
5	AGND	Analog Ground
6	DGND	Digital Ground
7	DB7	Data Input Bit 7 (MSB)
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4

PIN NO.	NAME	DESCRIPTION
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0	Data Input Bit 0 (LSB)
15	$\overline{WR}$	Write (Active Low)
16	A1	DAC Address Bit 1
17	A0	DAC Address Bit 0
18	V_{DD}	Positive Power Supply (+5 to +15 V)
19	V_{OUT4}	DAC 4 Voltage Output
20	V_{OUT3}	DAC 3 Voltage Output

ELECTRICAL CHARACTERISTICS

Single or Dual Supply Operation (V_{DD} = +10.8 V to 16.5 V, V_{SS} = 0 V or –5 V ±10%, AGND = 0 V, DGND = 0 V, V_{REF} = +2 V to +10 V, R_L = 2kΩ, C_L = 100pF unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	
K				1		1		End Point Linearity Spec
L				1/2		1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
K				±1/2		±3/4		
L				±1/2		±3/4		
Total Unadjusted Error[2]							LSB	V_{DD} = 15 V ±10%, V_{REF} = +10 V
K				±2		±2		
L				±1		±1		
Full Scale Error[3]							LSB	V_{REF} = +10 V typ. Tempco is 5 ppm/°C
K				±1		±1		
L				±1/2		±1/2		
Zero Code Error							mV	TA = 25°C typ. Tempco is 30µV/°C
K				±20		±30		
L				±15		±20		
Output Load Resistance		2			2		kΩ	V_{OUT} = +10 V
DYNAMIC PERFORMANCE[4]								
Voltage Output Slew Rate		2	4		2		V/µs	
Voltage Output Settling Time				4		5	µs	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough			25				nVs	Code transition all 0s to all 1s V_{REF} = 0 V, $\overline{WR}$ = V_{DD}
Digital Crosstalk[5]			25				nVs	Code transition all 0s to all 1s V_{REF} = +10 V, $\overline{WR}$ = 0 V
REFERENCE INPUT								
Reference Input Range[1]		1		10	1	10	V	Limitation: $V_{REF} - V_{SS} < 11$ V
Reference Input Resistance	R_{IN}	2			2		kΩ	Min R_{IN} at Code 149_{10}
Reference Input Capacitance[4]			500				pF	Occurs when all DACs are loaded with all 1s
AC Feedthrough			–70				dB	V_{REF} = 10 kHz, 5 V p-p sinewave
DIGITAL INPUTS								
Input High Voltage	V_{INH}	2.4			2.4		V	
Input Low Voltage	V_{INL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance[4]				8		8	pF	
Input Coding								Binary

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
V_{DD} Range		10.8		16.5	10.8	16.5	V	For specified performance
V_{SS} Range (Dual Supplies)[8]		0		–5.5	0	–5.5	V	For specified performance
I_{DD}				12		14	mA	Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
I_{SS} (Dual Supplies)				10		12		Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4, 6, 7]								
Address to $\overline{WR}$ Setup Time, t1	t_{AS}	0			0		ns	
Address to $\overline{WR}$ Hold Time, t2	t_{AH}	0			0		ns	
Data Valid to $\overline{WR}$ Setup Time, t3	t_{DS}	70			95		ns	
Data Valid to $\overline{WR}$ Hold Time, t4	t_{DH}	10			10			
$\overline{WR}$ Pulse Width, t5	t_{WR}	95			120		ns	

NOTES:

1 V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.
2 Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
3 Calculated after zero code error has been adjusted out.
4 Sample tested at 25°C to ensure compliance.
5 The glitch impulse transferred to the output of one converter (not adjusted) due to a change in the digital input code to another addressed converter.
6 All input rise and fall times are measured from 10% to 90% of +5 V, $t_R = t_F = 5$ ns.
7 Timing measurement reference level is $(V_{INH} + V_{INL})/2$.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS

Single & Dual ±5 V Supply Operation (V_{DD} = +5 V ±5%, V_{SS} = 0 V to –5 V ±10%, V_{REF} = +1.25 V, AGND = 0 V, DGND = 0 V, R_L = 2kΩ, C_L = 100pF unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	
K				2		2		End Point Linearity Spec
L				1		1		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
K				±1		±1		
L				±1		±1		
Total Unadjusted Error[2]				±4			LSB	V_{DD} = 5 V ±5%, V_{REF} = 1.25 V
Full Scale Error[3]							LSB	V_{REF} = +1.25 V
K				±4		±4		
L				±2		±2		
Zero Code Error				±20			mV	
Output Load Resistance		2					kΩ	V_{OUT} = +10 V
DYNAMIC PERFORMANCE[4]								
Voltage Output Slew Rate		2	4				V/µs	
Voltage Output Settling Time				4			µs	V_{REF} = +1.25 V; Settling Time to ±1/2 LSB
Digital Feedthrough			25				nVs	Code transition all 0s to all 1s V_{REF} = 0 V, $\overline{WR}$ = V_{DD}
Digital Crosstalk[5]			25				nVs	Code transition all 0s to all 1s V_{REF} = +1.25 V, $\overline{WR}$ = 0 V
REFERENCE INPUT								
Reference Input Range		1		1.6	1	1.6	V	V_{OUT} must be < V_{DD} by 3.2V
Reference Input Resistance	R_{IN}	2			2		kΩ	
Reference Input Capacitance[4]			500				pF	Occurs when all DACs are loaded with all 1s
AC Feedthrough			–70				dB	V_{REF} = 10 kHz, 1/2 V p-p sinewave
DIGITAL INPUTS								
Input High Voltage	V_{INH}	2.4			2.4		V	
Input Low Voltage	V_{INL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance[4]				8		8	pF	
Input Coding								Binary

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
V_{DD} Range		4.75		5.25	4.75	5.25	V	For specified performance
I_{DD}				8		8	mA	Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
I_{SS} (Dual Supplies)				6		6		Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4, 6, 7]								
Address to $\overline{WR}$ Setup Time, t1	t_{AS}	0			0		ns	
Address to $\overline{WR}$ Hold Time, t2	t_{AH}	0			0		ns	
Data Valid to $\overline{WR}$ Setup Time, t3	t_{DS}	70			95		ns	
Data Valid to $\overline{WR}$ Hold Time, t4	t_{DH}	0						
WR Pulse Width, t5	t_{WR}	95			120		ns	

NOTES:

1 V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.
2 Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
3 Calculated after zero code error has been adjusted out.
4 Sample tested at 25°C to ensure compliance.
5 The glitch impulse transferred to the output of one converter (not adjusted) due to a change in the digital input code to another addressed converter.
6 All input rise and fall times are measured from 10% to 90% of +5 V, $t_R = t_F = 5$ ns.
7 Timing measurement reference level is $(V_{INH} + V_{INL})/2$.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to AGND, DGND ..... 0 to +17 V
Digital Input Voltage to DGND ..... –0.5 to V_{DD} +0.5 V
V_{REF} to AGND, DGND ..... –0.5 to V_{DD} +0.5 V
V_{SS} to AGND, DGND ..... +0.5 to –7 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC, PLCC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

D/A CONVERTER SECTION

The MP7226 contains four matched, 8-bit, voltage-mode Digital-to-Analog Converters (DACs) which incorporate an MPS pioneered unique bit decoding technique. This decoding scheme reduces the maximum binary weight carried by any resistor switch, reducing the accuracy required of the switches and resistor network.

In the MP7226, the first three MSBs are decoded into three equal current sources, each contributing 25% of the full scale output current.

Decoding two bits to three, a 1% change in any one of the converter's three decoded current sources affects the output by no more than 0.25% of full scale, compared with 0.5% in a conventional R-2R type CMOS DAC.

The output voltages have the same polarity as the reference voltage, allowing single supply operation. The voltage reference range is from +2V to +10V. Each DAC uses a highly-stable, thin-film, ladder network and high-speed NMOS switches. *Figure 1.* shows a simplified circuit diagram for one channel.

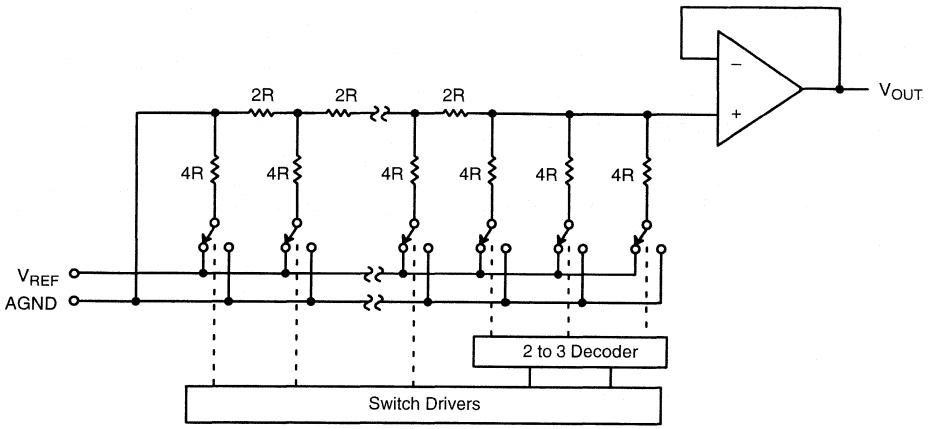


Figure 1. Simplified D/A Circuit Diagram

V_{REF} Input

The V_{REF} and AGND are common to all four DACs and set the full-scale output. The input impedance of the V_{REF} pin is the parallel combination of the four individual DAC reference impedances and is code dependent. This impedance varies from 2kΩ to 500kΩ. Therefore, it is very important that the external reference source output impedance is low enough so that its output voltage will not be affected by the varying digital code. Due to transient currents at the V_{REF} input during digital code changes, a 0.1μF or greater decoupling capacitor on that V_{REF} input is recommended. The input capacitance at the V_{REF} pin is also code dependent and typically varies from less than 120pF to 350pF.

Each V_{OUT} voltage can be represented by a digitally programmable voltage source using the following expression :

$$V_{OUT} = Dn \times V_{REF}/256$$

where Dn is the decimal equivalent to the digital input code and can vary from 0 to 255.

Output Buffer Amp

Each D/A converter output is buffered by a unity gain noninverting BiCMOS amplifier which has slew rate greater than 2 V/μs . The output buffer settles to ±1/2 LSB in less than 4μs when driving a load of 2kΩ in parallel with 100pF with a full scale transition from 0V to +10V or from +10V to 0V . The buffers can drive 2kΩ and 500pF to 10V levels without oscillation.

A simplified circuit diagram of the output buffer is shown in *Figure 2.* The Input stage is provided by BiCMOS PNP transistors with resulting lower input offset voltage, offset voltage drift over time and noise when compared to MOS process . The amplifier output stage uses a substrate NPN bipolar device to provide a low output impedance, high-output current capability.

The MP7226 is specified for single or dual power supply operation, with only the buffer amplifier outputs using V_{SS} supply current . Operating the MP7226 from dual supplies will improve the negative going output settling time near ground. In dual supply voltage operation , the output amplifier can sink 500μA when V_{OUT} = 0 V.

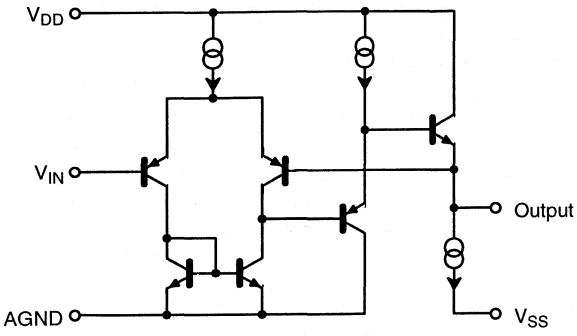


Figure 2. Simplified Output Buffer Amplifiers

The amplifiers outputs may be shorted to ground. However, the power dissipation of the package should not exceed the maximum limit.

Digital Inputs

All of the digital inputs to this DAC maintain TTL level interface compatibility and can also be driven directly with 5V CMOS logic inputs. The digital inputs are ESD protected to a rating of 2000 volts.

Digital Interface Logic

The MP7226 allows direct interface to most microprocessor buses without additional interface circuitry.

Figure 3. shows the input control logic circuit diagram and *Table 1.* shows the control logic truth table and operation for $\overline{WR}$, A1, A0. The address lines A0, and A1 determine which DAC will accept the input data. The $\overline{WR}$ input determines whether the selected DAC is transparent (output follows the input), latched, or no operation. The $\overline{WR}$ input will also inhibit power on reset of the DAC latches to 0, if its initial state = 0 after 5 µs of power.

Figure 4. shows the write cycle timing diagram. When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent, and the DAC's output corresponds to the value present on the data bus. On some data buses, data is not always valid for the entire period that the $\overline{WR}$ signal is low and can cause unwanted data at the output. Ensuring that the write pulse ($\overline{WR}$) conforms to the data hold time, (t4) spec will prevent this problem.

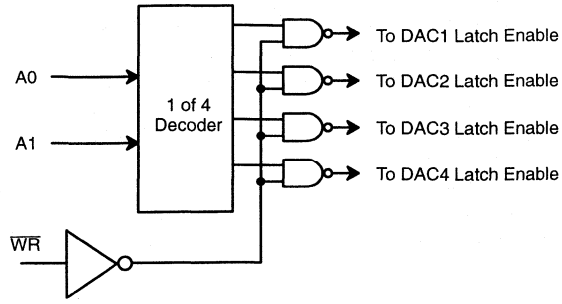
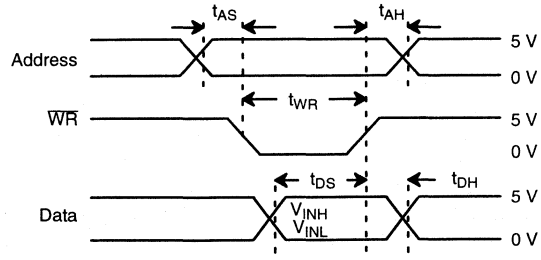


Figure 3. Input Control Logic

$\overline{WR}$	A1	A0	Operation
H	X	X	No Operation; Device Not Selected
L	L	L	DAC 1 Transparent
↑	L	L	DAC 1 Latched
L	L	H	DAC 2 Transparent
L	H	L	DAC 3 Transparent
L	H	H	DAC 4 Transparent

Table 1. Truth Table



NOTE: When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent and any invalid data at this time will cause erroneous output.

Figure 4. Write Cycle Timing Diagram

APPLICATIONS INFORMATION

Power On Reset

At power up, all inputs are reset to 0 V if $\overline{WR} = 1$. For $\overline{WR} = 0$, the addressed DAC will receive input data.

Power Supply

The MP7226 can operate with either a single or dual power supply. Improved zero-code settling error can be obtained by using dual power supplies. The dual power supply specifications are a positive supply (V_{DD}) range of +10.5V to +16.5V, and a –5V supply (V_{SS}) . The single power supply specifications are a positive supply (V_{DD}) range of +10.5V to +16.5V, or range of +4.75V to 5.5V . The specified reference voltage (V_{REF}) range under these conditions is from +2V to V_{DD} –4V. For those applications requiring +10V at the output (V_{REF} = +10V), V_{DD} must be +14V minimum to meet data sheet limits . 8-bit performance is guaranteed for single supply operation (V_{SS} = 0V); however, zero code output sink capability is improved with V_{SS} = –5V. For adequate DAC and Buffer operation, V_{REF} must always be below V_{DD} by at least 3.5V.

Power Supply Decoupling

The Power Supplies used with the MP7226 should be well regulated and filtered. Local power supply decoupling consisting of a 10µF tantalum capacitor in parallel with a 0.01µF ceramic is recommended. The decoupling capacitors should be connected between the V_{DD} and AGND, and between V_{SS} and AGND if V_{SS} = –5V.

Unipolar Output Operation

In this configuration, the reference voltage is the same polarity as the output voltage. Since the reference voltage must always be positive with respect to GND, the output can only be 0 or positive.

Table 2. shows the code relationship for the part in unipolar operation

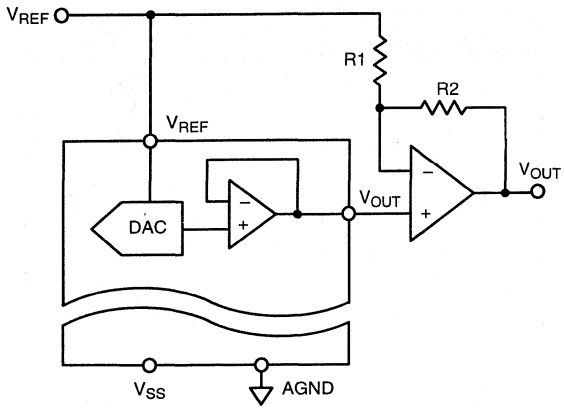
Digital Input	Analog Output, V_{OUT}
1 1 1 1 1 1 1 1	$+ V_{REF} (\frac{255}{256})$
1 0 0 0 0 0 0 1	$+ V_{REF} (\frac{129}{256})$
1 0 0 0 0 0 0 0	$+ V_{REF} (\frac{128}{256}) = + \frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$+ V_{REF} (\frac{127}{256})$
0 0 0 0 0 0 0 1	$+ V_{REF} (\frac{1}{256})$
0 0 0 0 0 0 0 0	0 V

Note : $1\ LSB = (2^{-8})\ (V_{REF}) = \frac{1}{256}\ (V_{REF})$

Table 2. Unipolar Code Table

Digital Input	Analog Output
1 1 1 1 1 1 1 1	$+ V_{REF} (\frac{127}{128})$
1 0 0 0 0 0 0 1	$+ V_{REF} (\frac{1}{128})$
1 0 0 0 0 0 0 0	0 V
0 1 1 1 1 1 1 1	$- V_{REF} (\frac{1}{128})$
0 0 0 0 0 0 0 1	$- V_{REF} (\frac{127}{128})$
0 0 0 0 0 0 0 0	$- V_{REF} (\frac{128}{128}) = - V_{REF}$

Table 3. Bipolar Code Table



$V_{OUT} = D_n \times V_{REF} \times (1+R2/R1) - V_{REF} \times R2/R1$
if R1 = R2
$V_{OUT} = V_{REF} \times (2D_n - 1)$
Where D_n is the digital input code and can vary from 0 to 255

Figure 5. Bipolar Output Circuit

Bipolar Binary Operation

The Bipolar Mode configuration for each DAC requires one external op-amp and two resistors per channel.

Figure 5. shows a typical Bipolar Operation circuit using the MP7226. *Table 3.* shows the code relationship for the circuit of *Figure 5.* assuming R1 = R2 .

AC Reference Signal

An AC signal can be applied to the reference of the MP7226 for multiplying capability within the upper (+10V) and lower (+2V) limits of the reference voltage input, with either single or dual supplies . This signal must be level shifted or AC coupled with proper bias level before being applied to the reference input. *Figure 6.* shows techniques for applying an AC signal to the MP7226. Since all four DACs share a common reference, they will all share this AC modulated reference. Input frequencies up to 50kHz will typically be distorted less than 0.1% .

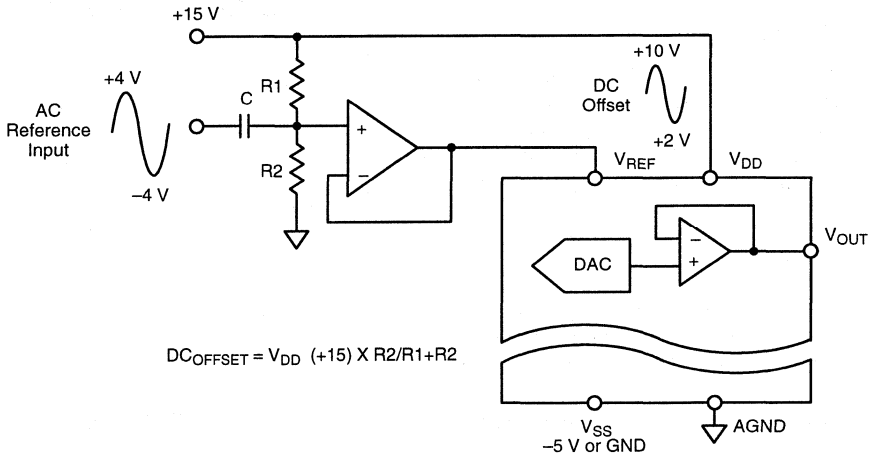


Figure 6. AC Reference Input Signal Circuit (AC Couple)

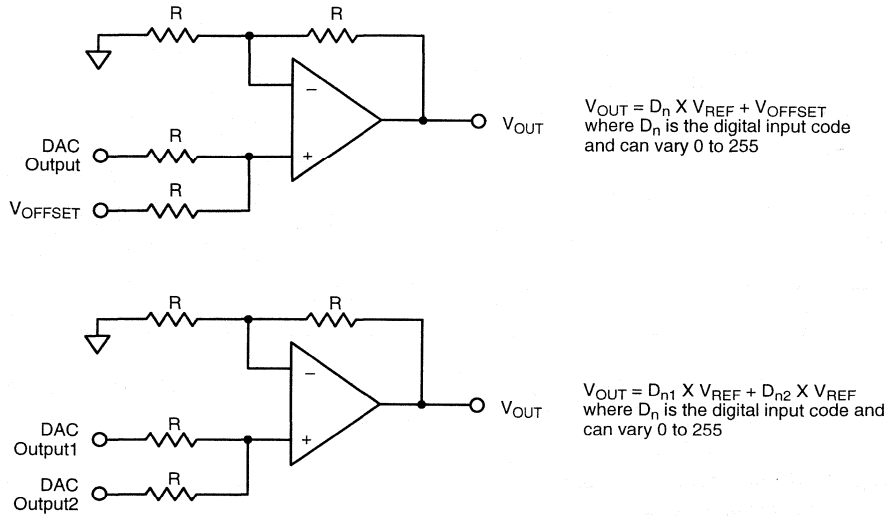


Figure 7. Digitally Programmable Offset Adjustment Circuits

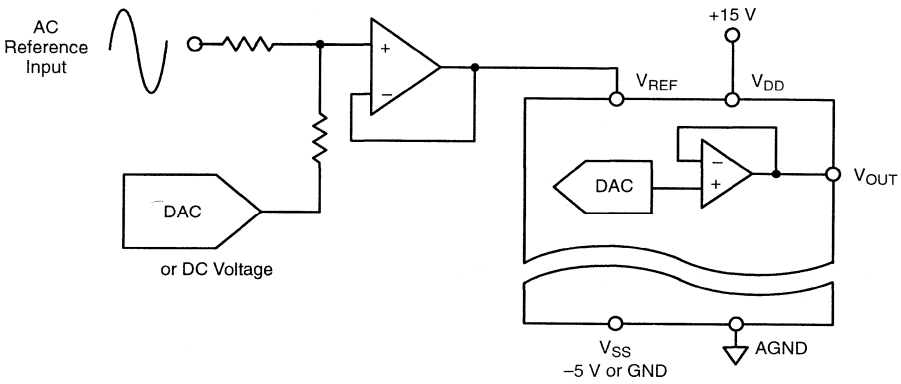


Figure 8. Digitally Programmable AC Reference Input Signal Circuit (DC Couple)

Offsetting DAC Outputs

Figure 7. shows examples of offset circuits.

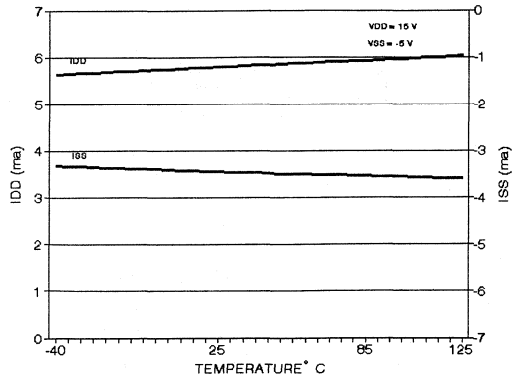
DAC offset effects

When using the device in single supply applications, and minimum reference voltage, there is a possibility that the DAC output will not change when the code is incremented from 0. Once the DAC has reached the offset voltage of the output buffer, the DAC output will begin to increment in a normal operation.

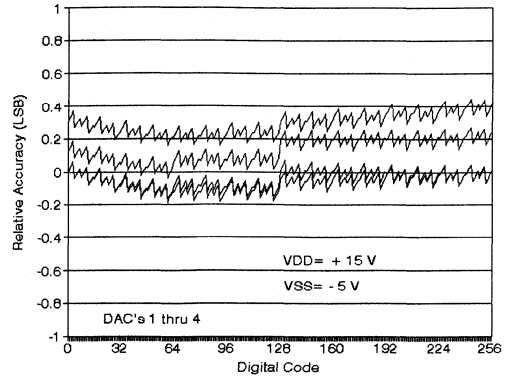
5V Operation

The MP7226 can be operated with a single power supply (V_{DD} = +5V) or dual power supplies (V_{DD} = +5V and V_{SS} = –5V) . The reference voltage range is reduced along with Some performance parameter degradation. However the DNL of each DAC remains at ±1 LSB guaranteeing monotonicity.

PERFORMANCE CHARACTERISTICS



Graph 1. Power Supply Current vs. Temperature



Graph 2. Relative Accuracy vs. Digital Code

MP7228

BiCMOS

Fixed, Octal, Voltage Output, Single or Dual Supply, 8-Bit Digital-to-Analog Converter

FEATURES

- MPS Pioneered Segmented DAC Approach
- Eight 8-Bit DACs with Buffer Amplifiers
- Bipolar Amplifier Inputs for Low Noise and Drift
- Operates with Single or Dual Supplies
- µP Compatible (95ns $\overline{WR}$)
- No External Adjustments Required
- Power-on-Reset Function
- Specified for 5 to 15 V Operation
- ESD Protection: 2000 Volts Minimum
- Latch-Up Proof
- Quad Available: MP7226

APPLICATIONS

- Function Generators
- Automatic Test Equipment
- Process Controls

BENEFITS

- Reduced Board Space; Lower System Cost
- Reduced System Errors due to Excellent DAC-to-DAC Matching and Tracking
- Easy to Design with Microprocessors
- Stable, High Reliability through Advanced Processing
- Lower 1/f Noise Increases Useful Dynamic Range

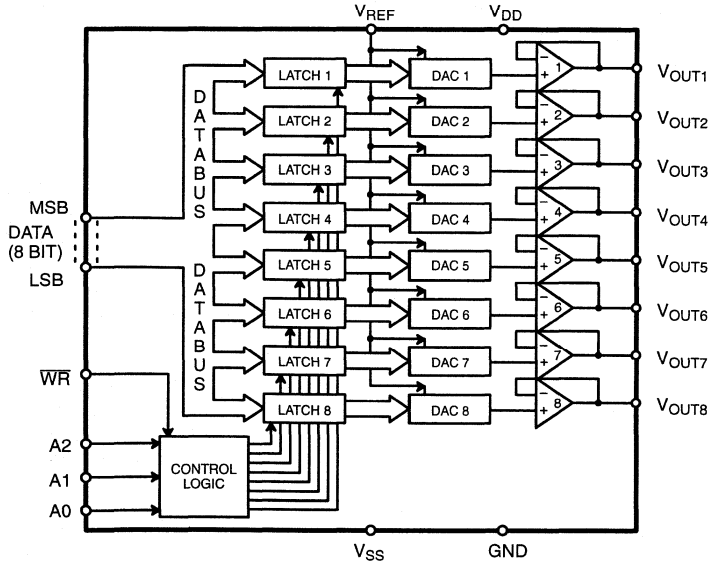
4

GENERAL DESCRIPTION

The MP7228 contains eight 8-bit voltage-output Digital-to-Analog Converters, with BiCMOS output buffer amplifiers and interface logic on a monolithic chip. Separate on-chip latches are provided for each of the eight D/A converters. The control logic is speed compatible with most 8-bit microprocessors. All digital inputs are TTL/CMOS(5V) compatible.

The MP7228 is manufactured using EXAR's advanced thin film resistors on a double metal BiCMOS process. The MP7228 incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7228 maintains 8-Bit accuracy over the full operating temperature range without laser trim or external adjustments.

SIMPLIFIED BLOCK DIAGRAM

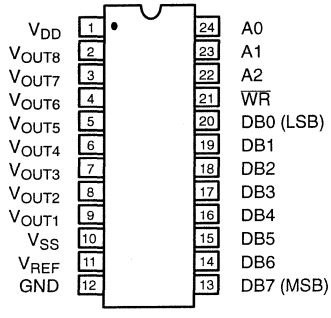


ORDERING INFORMATION

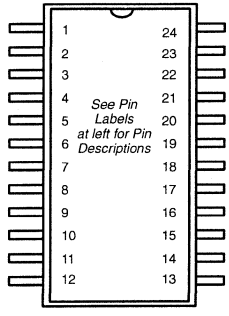
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Full Scale Error (LSB)
Plastic Dip	–40 to +85°C	MP7228KN	1	±1/2	±1
Plastic Dip	–40 to +85°C	MP7228LN	1/2	±1/2	±1/2
PLCC	–40 to +85°C	MP7228KP	1	±1/2	±1
PLCC	–40 to +85°C	MP7228LP	1/2	±1/2	±1/2
SOIC	–40 to +85°C	MP7228KS	1	±1/2	±1
SOIC	–40 to +85°C	MP7228LS	1/2	±1/2	±1/2
Ceramic Dip	–55 to +125°C	MP7228TD*	±1	±1/2	±1
Ceramic Dip	–55 to +125°C	MP7228UD*	±1/2	±1/2	±1/2

*Contact factory for availability.

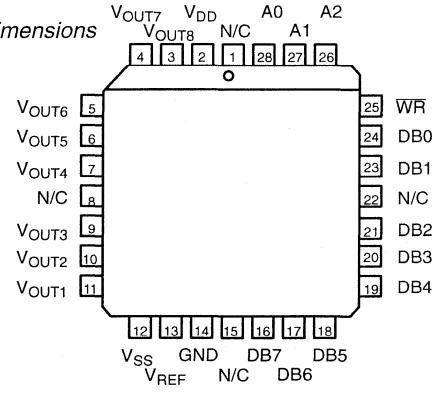
PIN CONFIGURATIONS *See Packaging Section for Package Dimensions*



24 Pin CDIP, PDIP (0.300")
DN24, NN24



24 Pin SOIC (Jedec, 0.300")
S24



28 Pin PLCC
P28

PIN OUT DEFINITIONS

DIP	PLCC	NAME	DESCRIPTION
	1	N/C	No Connection
1	2	V_{DD}	Positive Power Supply (+5V to +15V)
2	3	V_{OUT8}	DAC 8 Voltage Output
3	4	V_{OUT7}	DAC 7 Voltage Output
4	5	V_{OUT6}	DAC 6 Voltage Output
5	6	V_{OUT5}	DAC 5 Voltage Output
6	7	V_{OUT4}	DAC 4 Voltage Output
	8	N/C	No Connection
7	9	V_{OUT3}	DAC 3 Voltage Output
8	10	V_{OUT2}	DAC 2 Voltage Output
9	11	V_{OUT1}	DAC 1 Voltage Output
10	12	V_{SS}	Negative Power Supply (0V to –5V)
11	13	V_{REF}	Reference Input Voltage
12	14	GND	Ground

DIP	PLCC	NAME	DESCRIPTION
	15	N/C	No Connection
13	16	DB7	Data Input Bit 7 (MSB)
14	17	DB6	Data Input Bit 6
15	18	DB5	Data Input Bit 5
16	19	DB4	Data Input Bit 4
17	20	DB3	Data Input Bit 3
18	21	DB2	Data Input Bit 2
	22	N/C	No Connection
19	23	DB1	Data Input Bit 1
20	24	DB0	Data Input Bit 0 (LSB)
21	25	$\overline{WR}$	Write (Active Low)
22	26	A2	DAC address Bit 2
23	27	A1	DAC address Bit 1
24	28	A0	DAC address Bit 0

ELECTRICAL CHARACTERISTICS

Single or Dual Supply Operation (V_{DD} = +10.8 V to 16.5 V, V_{SS} = 0 V or –5 V ±10%, GND = 0 V, V_{REF} = +2 V to +10 V, R_L = 2kΩ, C_L = 100pF unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	
K, T				1		1		End Point Linearity Spec
L, U				1/2		1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
K, T				±1/2		±3/4		
L, U				±1/2		±3/4		
Total Unadjusted Error[2]							LSB	V_{DD} = 15 V ±10%, V_{REF} = +10 V
K, T				±2		±2		
L, U				±1		±1		
Full Scale Error[3]							LSB	V_{REF} = +10 V typ. Tempco is 5 ppm/°C
K, T				±1		±1		
L, U				±1/2		±1/2		
Zero Code Error							mV	TA = 25°C typ. Tempco is 10µV/°C
K, T				±20		±30		
L, U				±15		±20		
Output Load Resistance		2			2		kΩ	V_{OUT} = +10 V
DYNAMIC PERFORMANCE[4]								
Voltage Output Slew Rate		2	4		2		V/µs	
Voltage Output Settling Time				4		5	µs	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough			25				nVs	Code transition all 0s to all 1s V_{REF} = 0 V, $\overline{WR}$ = V_{DD}
Digital Crosstalk[5]			25				nVs	Code transition all 0s to all 1s V_{REF} = +10 V, $\overline{WR}$ = 0 V
REFERENCE INPUT								
Reference Input Range[1]		1		10	1	10	V	*Limitation: $V_{REF} - V_{SS} < 11$ V
Reference Input Resistance	R_{IN}	2			2		kΩ	Min R_{IN} at code 149_{10}
Reference Input Capacitance[4]			500				pF	Occurs when all DACS are loaded with all 1s
AC Feedthrough			–70				dB	V_{REF} = 10 kHz, 5 V p-p sinewave
DIGITAL INPUTS								
Input High Voltage	V_{INH}	2.4			2.4		V	
Input Low Voltage	V_{INL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance[4]				8		8	pF	
Input Coding								Binary

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
V_{DD} Range		10.8		16.5	10.8	16.5	V	For specified performance
V_{SS} Range (Dual Supplies)[8]		0		–5.5	0	–5.5	V	For specified performance
I_{DD}				16		20	mA	Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
I_{SS} (Dual Supplies) TA = 25°C				14		18		Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4, 6, 7]								
Address to $\overline{WR}$ Setup Time	t_{AS}	0			0		ns	
Address to $\overline{WR}$ Hold Time	t_{AH}	0			0		ns	
Data Valid to $\overline{WR}$ Setup Time	t_{DS}	70			95		ns	
Data Valid to $\overline{WR}$ Hold Time	t_{DH}	10			10		ns	
$\overline{WR}$ Pulse Width	t_{WR}	95			120		ns	

NOTES:

1 V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.
2 Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
3 Calculated after zero code error has been adjusted out.
4 Sample tested at 25°C to ensure compliance.
5 The glitch impulse transferred to the output of one converter (not adjusted) due to a change in the digital input code to another addressed converter.
6 All input rise and fall times are measured from 10% to 90% of +5 V, $t_R = t_F = 5$ ns.
7 Timing measurement reference level is $(V_{INH} + V_{INL})/2$.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS

Single & Dual ±5 V Supply Operation (V_{DD} = +5 V ±5%, V_{SS} = 0 V to –5 V ±10%, V_{REF} = +1.25 V, R_L = 2kΩ, C_L = 100pF, GND = 0 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	
K, T				2		2		End Point Linearity Spec
L, U				1		1		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
K, T				±1		±1		
L, U				±1		±1		
Total Unadjusted Error[2]				±4			LSB	V_{DD} = 5 V ±5%, V_{REF} = 1.25 V
Full Scale Error[3]							LSB	V_{REF} = +1.25 V
K, T				±4		±4		
L, U				±2		±2		
Zero Code Error				±20			mV	
Output Load Resistance		2					kΩ	V_{OUT} = +10 V
DYNAMIC PERFORMANCE[4]								R_L=100Ω, C_L=13pF
Voltage Output Slew Rate		2	4				V/µs	
Voltage Output Settling Time				4			µs	V_{REF} = +1.25 V; Settling Time to ±1/2 LSB
Digital Feedthrough			25				nVs	Code transition all 0s to all 1s V_{REF} = 0 V, $\overline{WR}$ = V_{DD}
Digital Crosstalk[5]			25				nVs	Code transition all 0s to all 1s V_{REF} = +1.25 V, $\overline{WR}$ = 0 V
REFERENCE INPUT								
Reference Input Range		1		1.6	1	1.6	V	V_{OUT} must be < V_{DD} by 3.2V
Reference Input Resistance	R_{IN}	2			2		kΩ	Min R_{IN} at code 149_{10}
Reference Input Capacitance[4]			500				pF	Occurs when all DACs are loaded with all 1s
AC Feedthrough			–70				dB	V_{REF} = 10 kHz, 1/2 V p-p sinewave
DIGITAL INPUTS								
Input High Voltage	V_{INH}	2.4			2.4		V	
Input Low Voltage	V_{INL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance[4]				8		8	pF	
Input Coding								Binary

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
V_{DD} Range		4.75		5.25	4.75	5.25	V	For specified performance
I_{DD}				10		10	mA	Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
I_{SS} (Dual Supplies)				8		8		Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4, 6, 7]								
Address to $\overline{WR}$ Setup Time	t_{AS}	0			0		ns	
Address to $\overline{WR}$ Hold Time	t_{AH}	0			0		ns	
Data Valid to $\overline{WR}$ Setup Time	t_{DS}	70			95		ns	
Data Valid to $\overline{WR}$ Hold Time	t_{DH}	0						
WR Pulse Width	t_{WR}	95			120		ns	

NOTES:

1 V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.
2 Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
3 Calculated after zero code error has been adjusted out.
4 Sample tested at 25°C to ensure compliance.
5 The glitch impulse transferred to the output of one converter (not adjusted) due to a change in the digital input code to another addressed converter.
6 All input rise and fall times are measured from 10% to 90% of +5 V, $t_R = t_F = 5$ ns.
7 Timing measurement reference level is $(V_{INH} + V_{INL})/2$.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND ..... –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... –0.5 to V_{DD} +0.5 V
V_{SS} to GND ..... +0.5 to –7 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, PLCC, SOIC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

D/A CONVERTER SECTION

The MP7228 contains eight matched, 8-bit, voltage-mode digital-to-analog converters (DACs) which incorporate an MPS pioneered unique bit decoding technique. This decoding scheme reduces the maximum binary weight carried by any resistor switch, reducing the accuracy required of the switches and resistor network.

In the MP7228, the first three MSBs are decoded into three equal current sources, each contributing 25% of the full scale output current.

Decoding two bits to three, a 1% change in any one of the converter's three decoded current sources affects the output by no more than 0.25% of full scale, compared with 0.5% in a conventional R-2R type CMOS DAC.

The output voltages have the same polarity as the reference voltage, allowing single supply operation. The voltage reference range is from +2V to +10V. Each DAC uses a highly-stable, thin-film, ladder network and high-speed NMOS switches. *Figure 1.* shows a simplified circuit diagram for one channel.

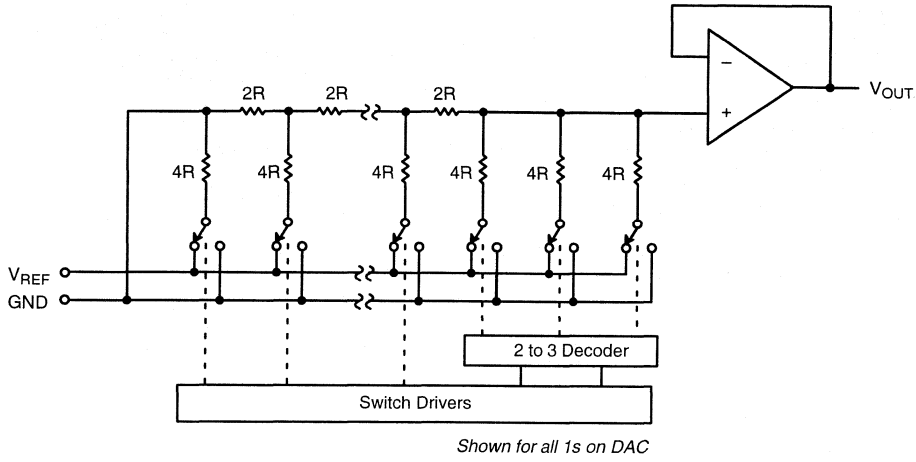


Figure 1. Simplified D/A Circuit Diagram

V_{REF} Input

The V_{REF} and GND are common to all eight DACs and set the full-scale output. The input impedance of the V_{REF} pin is the parallel combination of the eight individual DAC reference impedances and is code dependent. This impedance varies from 2kΩ to 500kΩ. Therefore, it is very important that the external reference source output impedance is low enough so that its output voltage will not be affected by the varying digital code. Due to transient currents at the V_{REF} input during digital code changes, a 0.1µF or greater decoupling capacitor on that V_{REF} input is recommended. The input capacitance at the V_{REF} pin is also code dependent and typically varies from less than 120pF to less than 350pF.

Each V_{OUT} voltage can be represented by a digitally programmable voltage source using the following expression :

$$V_{OUT} = Dn \times V_{REF}/256$$

where Dn is the decimal equivalent to the digital input code and can vary from 0 to 255.

Output Buffer Amp

Each D/A converter output is buffered by a unity gain noninverting BiCMOS amplifier which has slew rate greater than 4 V/µs. The output buffer settles to ±1/2 LSB in less than 4µs when driving a load of 2kΩ in parallel with 100pF with a full scale transition from 0V to +10V or from +10V to 0V . The buffers can drive 2kΩ and 500pF to 10V levels without oscillation.

A simplified circuit diagram of the output buffer is shown in *Figure 2.* The Input stage is provided by BiCMOS PNP transistors with resulting lower input offset voltage, offset voltage drift over time and noise when compared to MOS process . The amplifier output stage uses a substrate NPN bipolar device to provide a low output impedance, high-output current capability.

The MP7228 is specified for single or dual power supply operation, with only the buffer amplifier outputs using V_{SS} supply current . Operating the MP7228 from dual supplies will improve the negative going output settling time near ground. In dual supply voltage operation, the output amplifier can sink 500µA when V_{OUT} = 0 V.

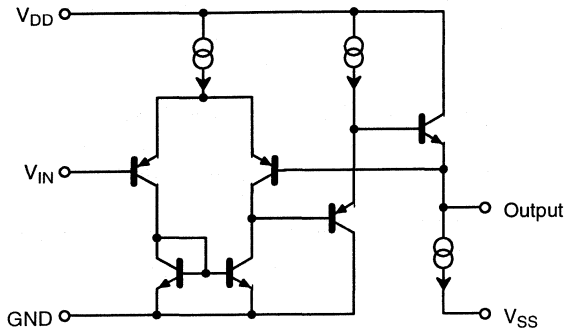


Figure 2. Simplified Output Buffer Amplifiers

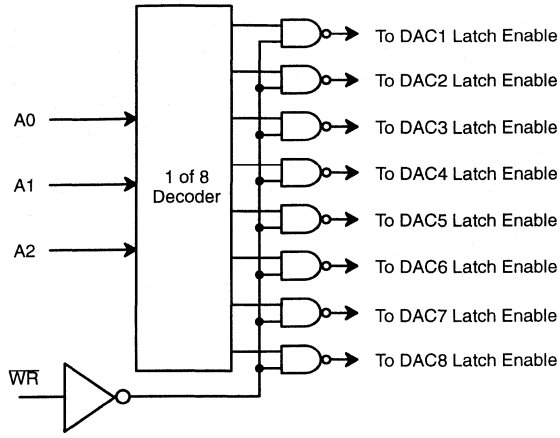


Figure 3. Input Control Logic

The amplifiers outputs may be shorted to ground. However, the power dissipation of the package should not exceed the maximum limit.

Digital Inputs

All of the digital inputs to this DAC maintain TTL level interface compatibility and can also be driven directly with 5V CMOS logic inputs. The digital inputs are static protected to a rating of 2000 volts .

Digital Interface Logic

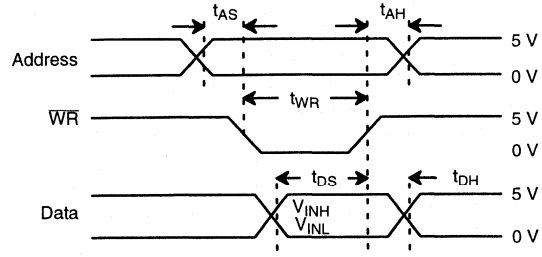
The MP7228 allows direct interface to most microprocessor buses without additional interface circuitry.

Figure 3. shows the input control logic circuit diagram and *Table 1.* shows the control logic truth table and operation for $\overline{WR}$, A2, A1, A0. The address lines A0, A1 and A2 determines which DAC will accept the input data. The $\overline{WR}$ input determines whether the selected DAC is transparent (output follows the input), latched, or no operation. The $\overline{WR}$ input will also inhibit power on reset of the DAC latches to 0, if its initial state = 0 after 5 µs of power.

Figure 4. shows the write cycle timing diagram. When $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent , and the DAC's output corresponds to the value present on the data bus.

$\overline{WR}$	A2	A1	A0	Operation
H	X	X	X	No Operation; Device Not Selected
L	L	L	L	DAC 1 Transparent
↑	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

Table 1. Truth Table



NOTE: When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent and any invalid data at this time will cause erroneous output.

Figure 4. Write Cycle Timing Diagram

APPLICATIONS INFORMATION

Power On Reset

At power up, all inputs are reset to 0 V if $\overline{WR} = 1$. If $\overline{WR} = 0$, the addressed DAC will receive input data.

Power Supply

The MP7228 can operate with either a single or dual power supply. Improved zero-code settling error can be obtained by using dual power supplies. The dual power supply specifications are a positive supply (V_{DD}) range of +10.5V to +16.5V, and a –5V supply (V_{SS}) . The single power supply specifications are a positive supply (V_{DD}) range of +10.5V to +16.5V, or range of +4.75V to 5.5V . The specified reference voltage (V_{REF}) range under these conditions is from +2V to V_{DD}–4V. For those applications requiring +10V at the output (V_{REF} = +10V), V_{DD} must be +14V minimum to meet data sheet limits. 8-bit performance is guaranteed for single supply operation (V_{SS} = 0V); however, zero code output sink capability is improved with V_{SS} = –5V. For adequate DAC and Buffer operation, V_{REF} must always be below V_{DD} by at least 3.5V.

Power Supply Decoupling

The Power Supplies used with the MP7228 should be well regulated and filtered. Local power supply decoupling consisting of a 10µF tantalum capacitor in parallel with a 0.01µF ceramic is recommended. The decoupling capacitors should be connected between the V_{DD} and GND also between V_{SS} and GND if V_{SS} = –5V.

Unipolar Output Operation

In this configuration, the reference voltage is the same polarity as the output voltage. Since the reference voltage must always be positive with respect to GND, the output can only be 0 or positive.

Table 2. shows the code relationship for the part in unipolar operation.

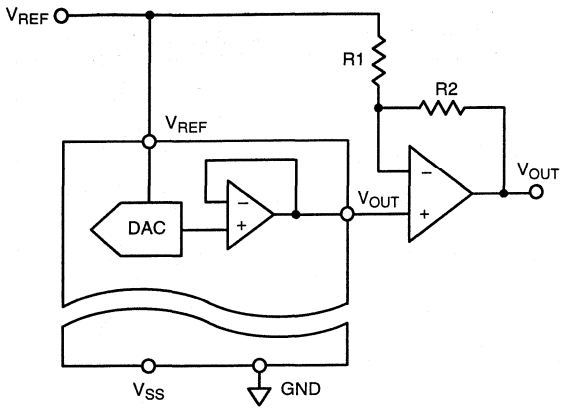
Digital Input	Analog Output, V_{OUT}
1 1 1 1 1 1 1 1	$+ V_{REF} (\frac{255}{256})$
1 0 0 0 0 0 0 1	$+ V_{REF} (\frac{129}{256})$
1 0 0 0 0 0 0 0	$+ V_{REF} (\frac{128}{256}) = + \frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$+ V_{REF} (\frac{127}{256})$
0 0 0 0 0 0 0 1	$+ V_{REF} (\frac{1}{256})$
0 0 0 0 0 0 0 0	0 V

Note : $1\ LSB = (2^{-8})\ (V_{REF}) = \frac{1}{256}\ (V_{REF})$

Table 2. Unipolar Code Table

Digital Input	Analog Output
1 1 1 1 1 1 1 1	$+ V_{REF} (\frac{127}{128})$
1 0 0 0 0 0 0 1	$+ V_{REF} (\frac{1}{128})$
1 0 0 0 0 0 0 0	0 V
0 1 1 1 1 1 1 1	$- V_{REF} (\frac{1}{128})$
0 0 0 0 0 0 0 1	$- V_{REF} (\frac{127}{128})$
0 0 0 0 0 0 0 0	$- V_{REF} (\frac{128}{128}) = - V_{REF}$

Table 3. Bipolar Code Table



$V_{OUT} = D_n \times V_{REF} \times (1+R2/R1) - V_{REF} \times R2/R1$
if R1 = R2
$V_{OUT} = V_{REF} \times (2D_n - 1)$
Where D_n is the digital input code and can vary from 0 to 255

Figure 5. Bipolar Output Circuit

Bipolar Binary Operation

The Bipolar Mode configuration for each DAC requires one external op-amp and two resistors per channel.

Figure 5. shows a typical Bipolar Operation circuit using the MP7228. *Table 3.* shows the code relationship for the circuit of *Figure 5.* assuming R1 = R2 .

AC Reference Signal

An AC signal can be applied to the reference of the MP7228 for multiplying capability within the upper (+10V) and lower (+2V) limits of the reference voltage input, with either single or dual supplies. This signal must be level shifted or AC coupled with proper bias level before being applied to the reference input. *Figure 6.* shows techniques for applying an AC signal to the MP7228. Since all eight DACs share a common reference, they will all share this AC modulated reference. Input frequencies up to 50kHz will typically be distorted less than 0.1% .

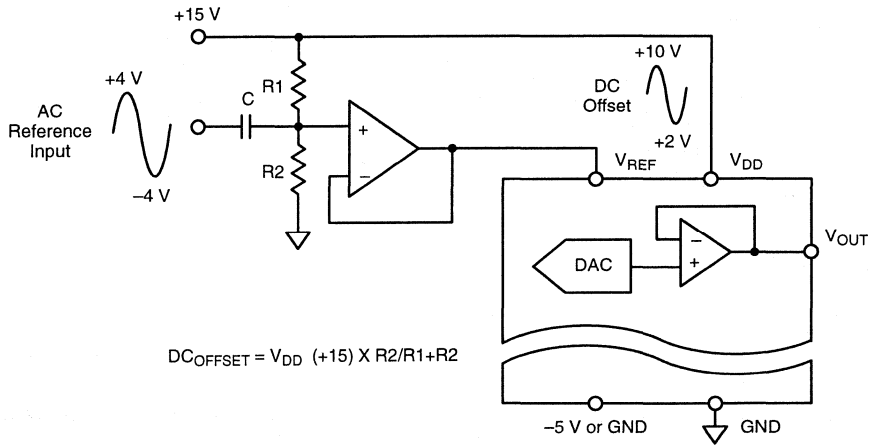


Figure 6. AC Reference Input Signal Circuit (AC Couple)

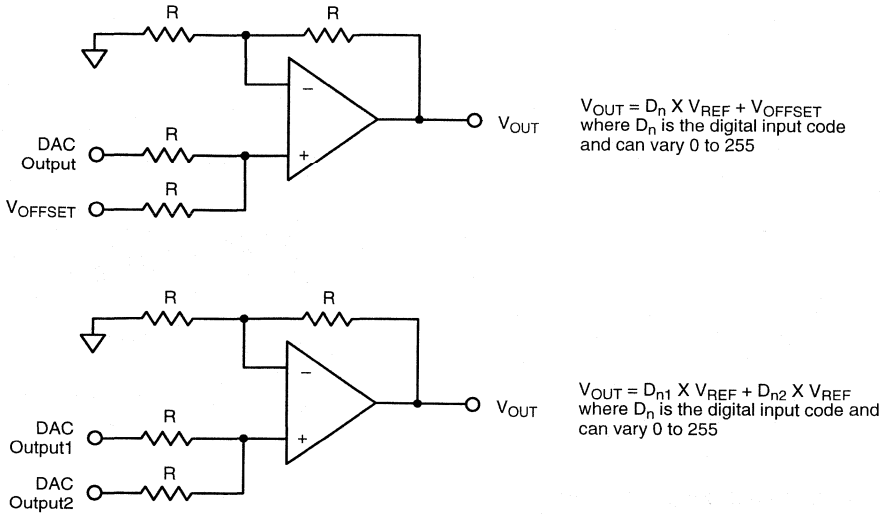


Figure 7. Offset Circuits

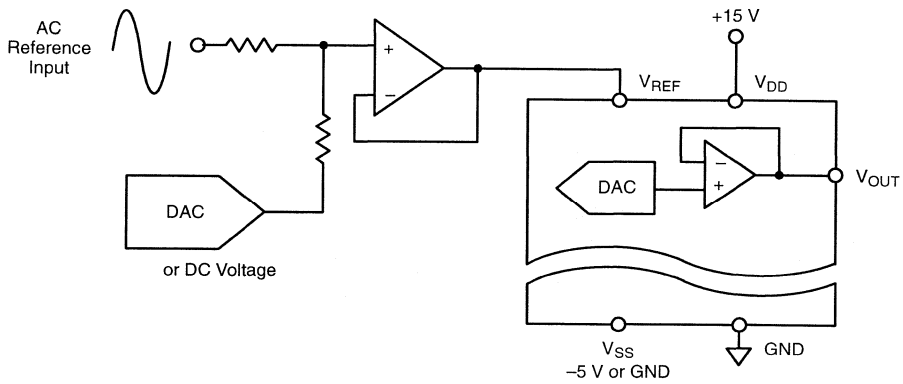


Figure 8. AC Reference Input Signal Circuit (DC Couple)

Offsetting DAC Outputs

Figure 7. shows examples of offset circuits.

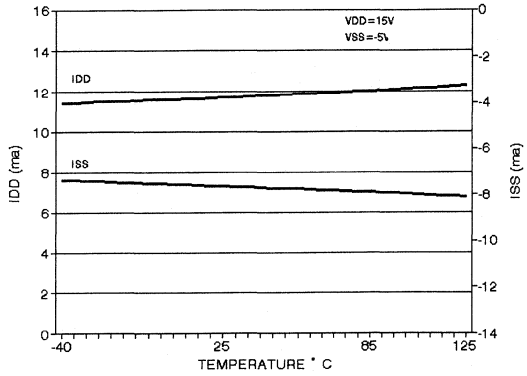
DAC Offset Effects

When using the device in single supply applications, and minimum reference voltage, there is a possibility that the DAC output will not change when the code is incremented from 0. Once the DAC has reached the offset voltage of the output buffer, the DAC output will begin to increment in a normal operation.

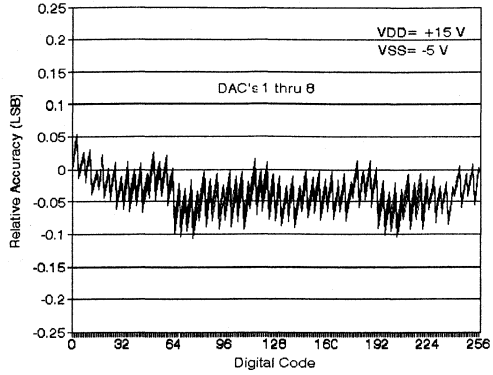
5V Operation

The MP7228 can be operated with a single power supply (V_{DD} = +5V) or dual power supplies (V_{DD} = +5V and V_{SS} = –5V). The reference voltage range is reduced. However, the DNL of each DAC remains at ±3/4 LSB guaranteeing monotonicity.

PERFORMANCE CHARACTERISTICS



Graph 1. Power Supply Current vs. Temperature



Graph 2. Relative Accuracy vs. Digital Code

MP7523

15 V CMOS
Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four-Quadrant Multiplying**
- **Low Feedthrough: 1/2 LSB @ 200 kHz**
- **Fast Settling: 100 ns (typ.)**
- **Low Power Dissipation**
- **Low Cost**
- **5 V/15 V Operation**
- **Buffered Version: MP7524**

APPLICATIONS

- **Battery Operated Equipment**
- **Low Power, Ratiometric A/D Converters**
- **Digitally Controlled Gain Circuits**
- **Digitally Controlled Attenuators**
- **CRT Character Generation**
- **Low Noise Audio Gain Control**

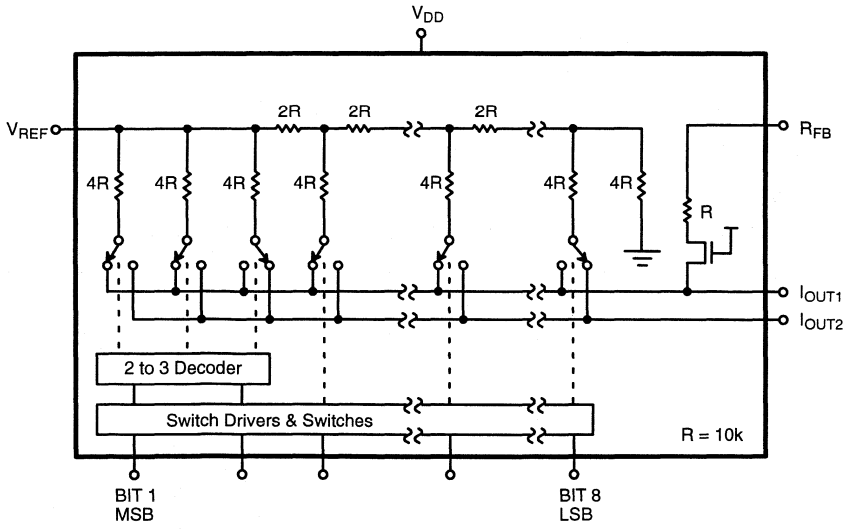
GENERAL DESCRIPTION

The MP7523 is a low cost multiplying Digital-to-Analog Converter. The device uses an advanced thin-film-on-CMOS technology to provide 8-bit resolution with accuracy to 10-bits and very low power dissipation.

The MP7523's excellent multiplying characteristics and low cost allow it to be used in a wide ranging field of applications such as: low noise audio gain control, CRT character generation, motor speed control, digitally controlled attenuators, etc.

4

SIMPLIFIED BLOCK DIAGRAM



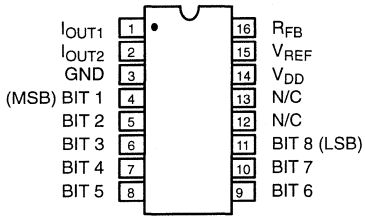
3 Segment D/A Converter with Termination to DGND
Logical "1" at Digital Input Steers Current to I_{OUT1}

ORDERING INFORMATION

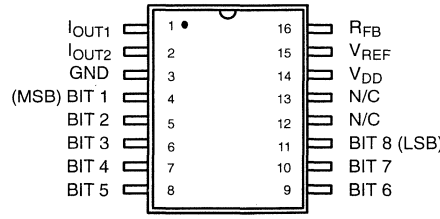
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7523JN	±1/2	±1	±1.8
Plastic Dip	–40 to +85°C	MP7523KN	±1/4	±1	±1.8
SOIC	–40 to +85°C	MP7523JS	±1/2	±1	±1.8
SOIC	–40 to +85°C	MP7523KS	±1/4	±1	±1.8

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



16 Pin PDIP (0.300")
N16



16 pin SOIC (Jedec, 0.300")
S16

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Bit 1 (MSB)
5	BIT 2	Bit 2
6	BIT 3	Bit 3
7	BIT 4	Bit 4
8	BIT 5	Bit 5

PIN NO.	NAME	DESCRIPTION
9	BIT 6	Bit 6
10	BIT 7	Bit 7
11	BIT 8	Bit 8
12	N/C	No Connection
13	N/C	No Connection
14	V_{DD}	Positive Power Supply
15	V_{REF}	Reference Input Voltage
16	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line (Max INL – Min INL) / 2
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
Monotonicity								Guaranteed over temp
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
Gain Error	GE			±1.5		±1.8	%	Using Internal R_{FB}
J, A, S								Digital Inputs = V_{INH}
K, B, T								
Power Supply Rejection Ratio	PSRR			±200		±300	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
J, A, S								Digital Inputs = V_{INH}
K, B, T								
Output Leakage Current (Pin 1)	I_{OUT1}			±50nA		±200nA	nA	Digital Inputs = V_{INL}
J, A, S								
K, B, T								
Output Leakage Current (Pin 2)	I_{OUT2}			±50nA		±200nA	nA	Digital Inputs = V_{INH}
J, A, S								
K, B, T								
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	kΩ	V_{OUT1} = V_{OUT2} = 0 V
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	14.5			14.5		V	
Logical "0" Voltage	V_{IL}			0.5		0.5	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT1}			100		100	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			30		30	pF	DAC Inputs all 1's
	C_{OUT2}			100		100	pF	DAC Inputs all 0's

4

ELECTRICAL CHARACTERISTICS (CON'T)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
Functional Voltage Range[2]	V_{DD}	5		16	5	16	V	
Supply Current	I_{DD}			1.6		1.6	mA	All digital inputs = 0 V or all = 15 V

NOTES:

1 Full Scale Range (FSR) is 10V.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... –0.5 to 6.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 800mW
Derates above 75°C ..... 11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

Refer to Section 8 for Applications Information

MP7524

CMOS
Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four-Quadrant Multiplication**
- **On-chip Bus Interface Logic**
- **+5 V to +15 V Operation**
- **Low Power Consumption**
- **Monotonicity Guranteed (Full Temperature Range)**
- **TTL/15 V CMOS Compatible**

APPLICATIONS

- **Microprocessor Controlled Gain Circuits**
- **Microprocessor Controlled Attenuator Circuits**
- **Microprocessor Controlled Function Generation**
- **Precision AGC Circuits**
- **Bus Structured Instruments**

GENERAL DESCRIPTION

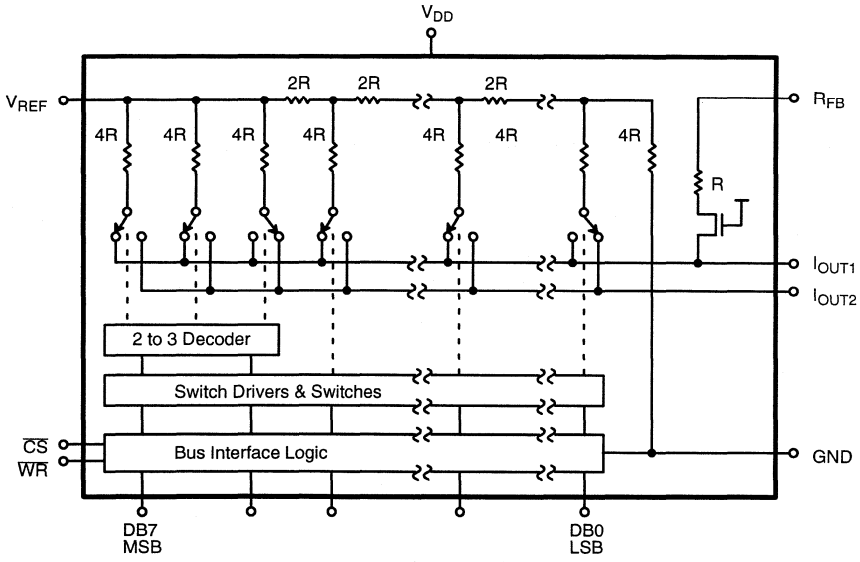
The MP7524 is a low cost, 8-bit CMOS Digital-to-Analog Converter designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the MP7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the MP7524 provides accuracy to 1/8 LSB with power dissipation of only 10mW.

Featuring operation from +5 V to +15 V, the MP7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the MP7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

4

SIMPLIFIED BLOCK DIAGRAM



3 Segment D/A Converter with Termination to GND
Logical "1" at Digital Input Steers Current to IOUT1

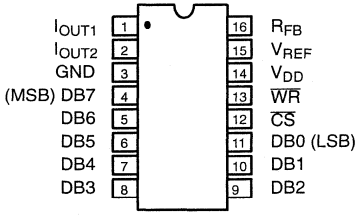
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7524JN	±1/2	±1	±1.4%
Plastic Dip	–40 to +85°C	MP7524KN	±1/4	±1	±1.4%
Plastic Dip	–40 to +85°C	MP7524LN	±1/8	±1	±1.4%
SOIC (0.150")	–40 to +85°C	MP7524JR	±1/2	±1	±1.4%
SOIC (0.150")	–40 to +85°C	MP7524KR	±1/4	±1	±1.4%
SOIC (0.300")	–40 to +85°C	MP7524JS	±1/2	±1	±1.4%
SOIC (0.300")	–40 to +85°C	MP7524KS	±1/4	±1	±1.4%
SOIC (0.300")	–40 to +85°C	MP7524LS	±1/8	±1	±1.4%
PLCC	–40 to +85°C	MP7524JP	±1/2	±1	±1.4%
PLCC	–40 to +85°C	MP7524KP	±1/4	±1	±1.4%
PLCC	–40 to +85°C	MP7524LP	±1/8	±1	±1.4%
Ceramic Dip	–40 to +85°C	MP7524AD	±1/2	±1	±1.4%
Ceramic Dip	–40 to +85°C	MP7524BD	±1/4	±1	±1.4%
Ceramic Dip	–40 to +85°C	MP7524CD	±1/8	±1	±1.4%
Ceramic Dip	–55 to +125°C	MP7524SD*	±1/2	±1	±1.4%
Ceramic Dip	–55 to +125°C	MP7524TD*	±1/4	±1	±1.4%
Ceramic Dip	–55 to +125°C	MP7524UD*	±1/8	±1	±1.4%

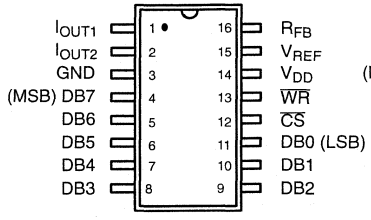
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

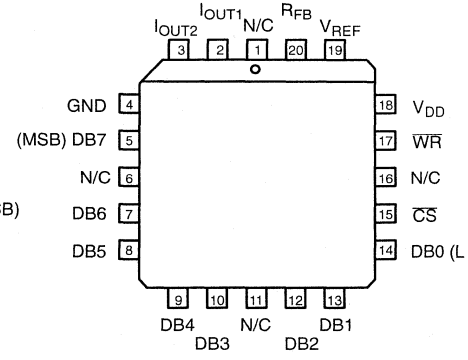
See Packaging Section for Package Dimensions



16 Pin CDIP, PDIP (0.300")
D16, N16



16 Pin SOIC
(Jedec, 0.150" & 0.300")
SN16, S16



20 Pin PLCC
P20

PIN OUT DEFINITIONS

CDIP, PDIP and SOIC

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	DB7	Data Input Bit 7 (MSB)
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	DB3	Data Input Bit 3
9	DB2	Data Input Bit 2
10	DB1	Data Input Bit 1
11	DB0	Data Input Bit 0 (LSB)
12	$\overline{CS}$	Chip Select
13	$\overline{WR}$	Write
14	V_{DD}	Power Supply
15	V_{REF}	Reference Input
16	R_{FB}	Feedback Resistance

PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	I_{OUT1}	Current Output 1
3	I_{OUT2}	Current Output 2
4	GND	Ground
5	DB7	Data Input Bit 7 (MSB)
6	N/C	No Connection
7	DB6	Data Input Bit 6
8	DB5	Data Input Bit 5
9	DB4	Data Input Bit 4
10	DB3	Data Input Bit 3
11	N/C	No Connection
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0	Data Input Bit 0 (LSB)
15	$\overline{CS}$	Chip Select
16	N/C	No Connection
17	$\overline{WR}$	Write
18	V_{DD}	Power Supply
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistance

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1/2		±1/2		
K, B, T				±1/2		±1/2		
L, C, U				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
L, C, U				±1		±1		
Gain Error	GE			±1.0		±1.4	% FSR	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR			±800		±1600	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current (Pin 1)	I_{OUT1}			±50nA		±400nA	nA	Digital Inputs = V_{INL}
DYNAMIC PERFORMANCE								RL = 100Ω, C_L = 10pF
Current Settling Time[2]	t_S			100		150	ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}[2]	F_T			±1/2		±1	LSB	V_{REF}=100kHz, 20 Vp-p, sinewave
at I_{OUT2}				±1/2		±1	LSB	DB0-DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]	C_{IN}			20		20	pF	V_{IN} = 0 V
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			70		70	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			20		20	pF	DAC Inputs all 1's
	C_{OUT2}			60		60	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Supply Current	I_{DD}		1	2		2	mA	All digital inputs = 0 V or all = 5 V
			1	2		2	mA	All digital inputs = V_{IL} or all = V_{IH}

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}						ns	
J, K, L, A, B, C		170			220			
S, T, U		170			240			
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}	135			170		ns	
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}						ns	
J, K, L, A, B, C		170			220			
S, T, U		170			240			

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested .
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

4

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
L, C, U				±1/8		±1/8		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
L, C, U				±1		±1		
Gain Error	GE			±0.5		±0.6	% FSR	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR			±200		±400	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current (Pin 1)	I_{OUT1}			±50nA		±200nA	nA	Digital Inputs = V_{INL}
DYNAMIC PERFORMANCE								RL=100Ω, CL=13pF
Current Settling Time[2]	t_S			50		100	ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}[2]	FT			±1/2		±1	LSB	V_{REF}=100kHz, 20Vp-p, sinewave
at I_{OUT2}				±1/2		±1	LSB	DB0 - DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	13.5			13.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]	C_{IN}			20		20	pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			70		70	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			20		20	pF	DAC Inputs all 1's
	C_{OUT2}			60		60	pF	DAC Inputs all 0's
POWER SUPPLY								
Supply Current	I_{DD}		1	2		2	mA	All digital inputs = 0 V or all = 15 V
			1	2		2	mA	All digital inputs = V_{IL} or all = V_{IH}

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}						ns	
J, K, L, A, B, C		100			130			
S, T, U		100			150			
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}						ns	
J, K, L, A, B, C		60			80			
S, T, U		60			100			
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}						ns	
J, K, L, A, B, C		100			130			
S, T, U		100			150			

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

4

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... –0.5, +17 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... –0.5 to 7 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 700mW
Derates above 75°C ..... 10mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

Refer to Section 8 for Applications Information

INTERFACE LOGIC INFORMATION

Mode Selection

MP7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the MP7524 is in the WRITE mode, and the MP7524 analog circuit responds to data activity at the DB0-DB7 data bus inputs. In this mode, the MP7524 acts like a non-latched input D/A converter.

Hold Mode

When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the MP7524 is in the HOLD mode. The MP7524 analog output holds the value corresponding to the last digital input present at DB0-DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the high state.

$\overline{CS}$	$\overline{WR}$	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0-DB7) inputs
H	X	Hold	Data Bus (DB0-DB7) is locked out
X	H	Hold	DAC holds last data present when $\overline{WR}$ assumed HIGH state

L = LOW state, H = HIGH state, X = Don't care state

Table 1. Mode Selection Table

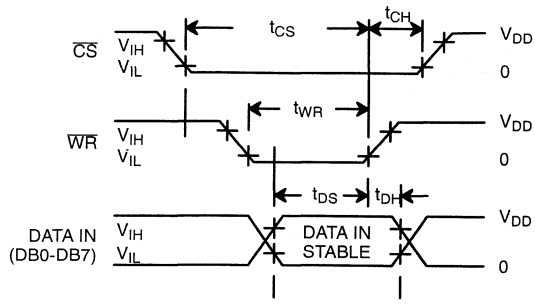
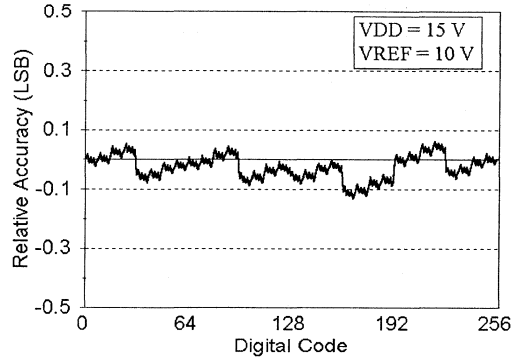


Figure 1. Write Cycle Timing Diagram



Graph 1. Relative Accuracy vs. Digital Code

MICROPROCESSOR INTERFACE

MP7524/8080A Interface

Figure 2. shows the MP7524 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080A CPU, 8224 clock generator and 8228 system controller/bus driver. The MP7524 $\overline{WR}$ input is connected to the 8228 system data bus outputs. The $\overline{CS}$ input is connected to the system address decoding logic. Note that pull-up resistors R3 and R4 are required to ensure that the $\overline{CS}$ and $\overline{WR}$ input HIGH states reach 3.0V min. Pull-ups are not required on the system data bus since the 8228 VOH is 3.6 V min for DB0-DB7.

System timing is shown in *Figure 3.* Data is loaded into the MP7524 when the $\overline{WR}$ and $\overline{CS}$ inputs are both LOW. The data is latched into the MP7524 when $\overline{WR}$ returns HIGH. MP7524 updating is accomplished by using any of the 8080A memory write instructions (such as MOV M, r).

The MP7524 can also be addressed and loaded as an isolated Output Device by connecting the MP7524 $\overline{WR}$ input to the 8228 $\overline{I/O\ W}$ terminal (instead of $\overline{MEMW}$).

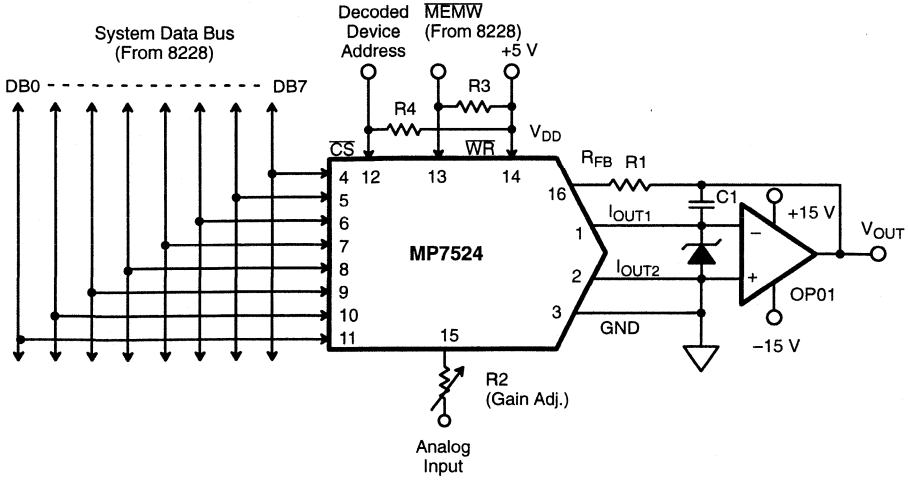
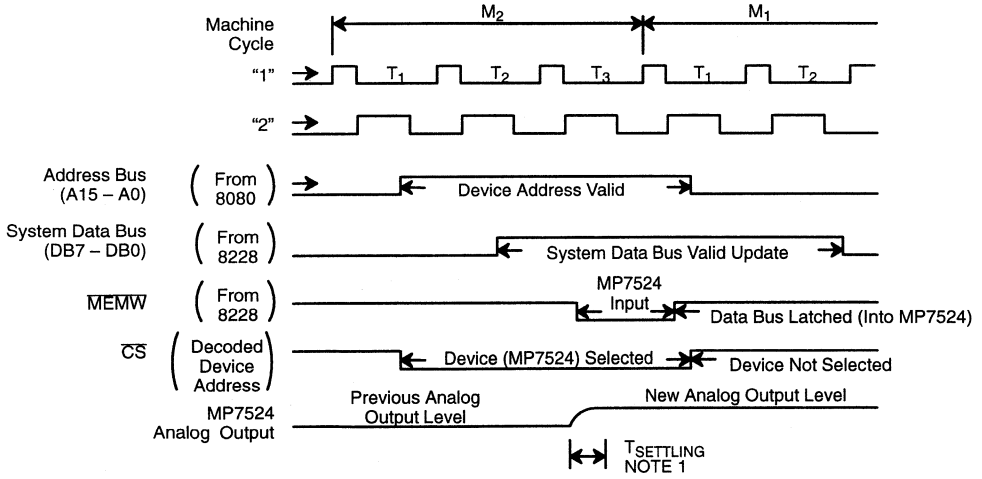


Figure 2. MP7524/8080A Interface



NOTE:
1. Settling Time Is Dependent Primarily Upon Output Amplifier Slewing And Settling Characteristics. Waveform Shown Is Not Representative Of Any Specific Amplifier

Figure 3. Timing Diagram

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MP7524A

CMOS
Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- I_{OUT} Pin Voltages are User Definable
- Improved Isolation of Analog from Digital Ground
- Full Four-Quadrant Multiplication
- On-chip Bus Interface Logic
- +5 V to +15 V V_{DD} Operation
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Use in Single Supply Design Designs
- 3 V Version: MP75L24

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments
- Disk Drives

GENERAL DESCRIPTION

The MP7524A is a low cost, 8-bit CMOS Digital-to-Analog Converter designed for direct interface to most microprocessors.

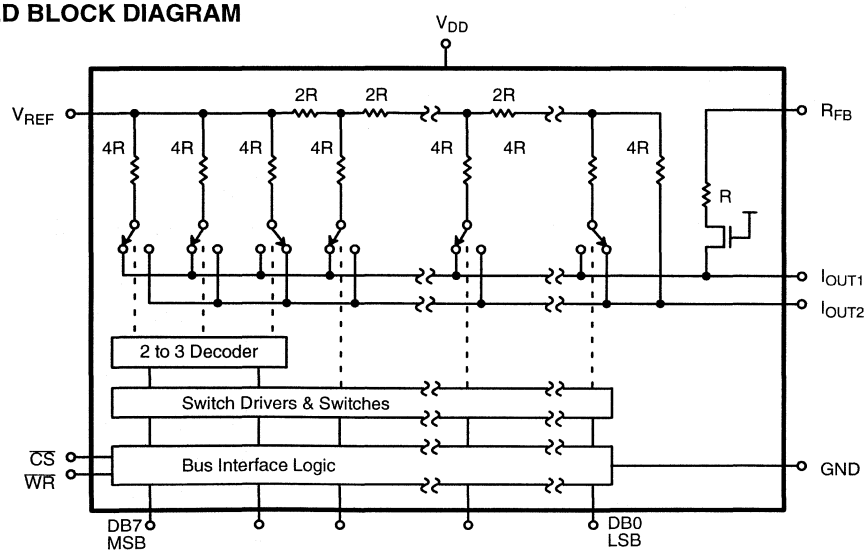
The MP7524A is pin-to-pin compatible to the MP7524. In addition, the $I_{OUT1,2}$ pins may be taken to a non-ground voltage. This allows its use in single supply circuits. The I_{OUT2} current is 1 LSB higher than that of the MP7524.

Basically an 8-bit DAC with input latches, the MP7524A's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the MP7524A provides accuracy to 1/8 LSB with power dissipation of only 10mW.

Featuring operation from +5 V to +15 V, the MP7524A interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the MP7524A an ideal choice for many microprocessor controlled gain setting and signal control applications.

4

SIMPLIFIED BLOCK DIAGRAM



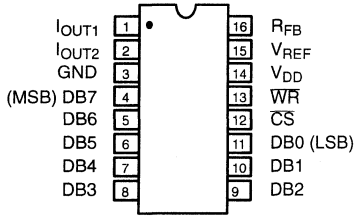
3 Segment D/A Converter with Termination to I_{OUT2}
Logical "1" at Digital Input Steers Current to IOUT1

ORDERING INFORMATION

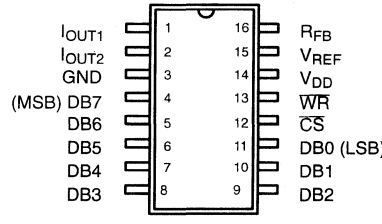
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7524AAN	±1/2	±1	±0.6
Plastic Dip	–40 to +85°C	MP7524ABN	±1/4	±1	±0.6
Plastic Dip	–40 to +85°C	MP7524ACN	±1/8	±1	±0.6
SOIC	–40 to +85°C	MP7524AAR	±1/2	±1	±0.6
SOIC	–40 to +85°C	MP7524ABR	±1/4	±1	±0.6
SOIC	–40 to +85°C	MP7524ACR	±1/8	±1	±0.6

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



16 Pin PDIP (0.300")
N16



16 Pin SOIC (Jedec, 0.150")
SN16

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	DB7	Data Input Bit 7 (MSB)
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	DB3	Data Input Bit 3

PIN NO.	NAME	DESCRIPTION
9	DB2	Data Input Bit 2
10	DB1	Data Input Bit 1
11	DB0	Data Input Bit 0 (LSB)
12	$\overline{CS}$	Chip Select
13	$\overline{WR}$	Write
14	V_{DD}	Power Supply
15	V_{REF}	Reference Input
16	R_{FB}	Feedback Resistance

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
A				±1/2		±1/2		
B				±1/2		±1/2		
C				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
A				±1		±1		
B				±1		±1		
C				±1		±1		
Gain Error	GE			±1.0		±1.4	% FSR	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR			±800		±1600	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current (Pin 1)	I_{OUT1}			±50nA		±400nA	nA	Digital Inputs = V_{INL}
DYNAMIC PERFORMANCE								RL = 100Ω, C_L = 10pF
Current Settling Time[2]	t_S			100		150	ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}[2]	F_T			±1/2		±1	LSB	V_{REF}=100kHz, 20 Vp-p, sinewave
at I_{OUT2}				±1/2		±1	LSB	DB0-DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	+2.4			+2.4		V	
Logical "0" Voltage	V_{IL}			+0.8		+0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]	C_{IN}			20		20	pF	V_{IN} = 0 V
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			70		70	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			20		20	pF	DAC Inputs all 1's
	C_{OUT2}			60		60	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Supply Current	I_{DD}		1	2		2	mA	All digital inputs = 0 V or all = 5 V
			1	2		2	mA	All digital inputs = V_{IL} or all = V_{IH}

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}						ns	
A, B, C		170			220			
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}	135			170		ns	
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}						ns	
A, B, C		170			220			
VOLTAGE MODE OPERATION[2, 6]								
Integral Nonlinearity Error @ V_{REF}	INL			1			LSB	I_{OUT1} = 2.5 V I_{OUT2} = 0 V

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode and ±10V for bipolar.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.
6 Refer to *Figure 7*.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	.End Point Linearity
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
L, C, U				±1/8		±1/8		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
L, C, U				±1		±1		
Gain Error	GE			±0.5		±0.6	% FSR	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR			±200		±400	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current (Pin 1)	I_{OUT1}			±50nA		±400nA	nA	Digital Inputs = V_{INL}
DYNAMIC PERFORMANCE								RL=100Ω, CL=13pF
Current Settling Time[2]	t_S			50		100	ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}[2]	FT			±0.50		±1.00	LSB	V_{REF} = 10kHz, 20 Vp-p, sinewave
at I_{OUT2}				±0.50		±1.00	LSB	DB0 - DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	+13.5			+13.5		V	
Logical "0" Voltage	V_{IL}			+1.5		+1.5	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]	C_{IN}			20		20	pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			70		70	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			20		20	pF	DAC Inputs all 1's
	C_{OUT2}			60		60	pF	DAC Inputs all 0's
POWER SUPPLY								
Supply Current	I_{DD}		1	2		2	mA	All digital inputs = 0 V or all = 15 V
			1	2		2	mA	All digital inputs = V_{IL} or all = V_{IH}

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}						ns	
A, B, C		100			130			
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}						ns	
A, B, C		60			80			
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}						ns	
A, B, C		100			130			
VOLTAGE MODE OPERATION[2, 6]								
Integral Nonlinearity Error @ V_{REF}	INL			1			LSB	I_{OUT1} = 5 V I_{OUT2} = 0 V

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode and ±10V for bipolar.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 See timing diagram.

5 Specified values guarantee functionality. Refer to other parameters for accuracy.

6 Refer to *Figure 7.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... –0.5, +17 V

Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V

I_{OUT1}, I_{OUT2} to GND ..... –0.5 to 7 V

V_{REF} to GND ..... ±25 V

V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC 700mW

Derates above 75°C ..... 10mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES
Refer to Section 8 for Applications Information

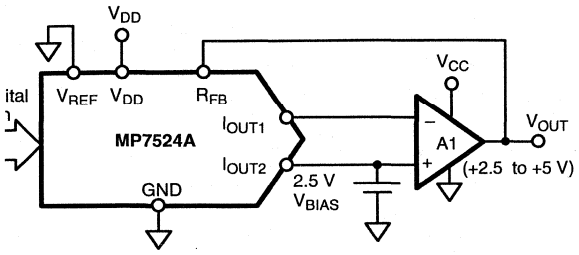


Figure 1. Single Supply Operation with 2.5 V to 5 V Swing

The R-2R ladder termination resistor on the MP7524A is internally connected to I_{OUT2} instead of ground as in the MP7524. This configuration allows the use of the DAC in the single supply current steering mode, where I_{OUT2} is biased above ground level.

Figure 2. shows the generalized configuration.

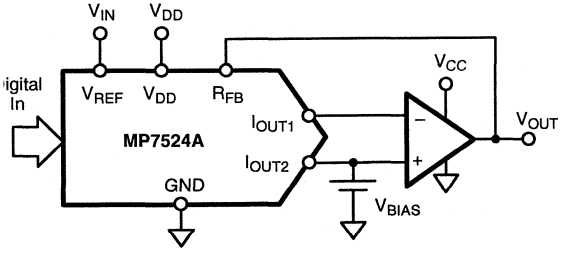


Figure 2. Single Supply Operation in Current Switching Mode

The advantage of this single supply configuration over the voltage switching mode is the greater flexibility with which the output voltage swing can be defined. A low impedance reference bias voltage is needed. Unlike the voltage switching mode which has a minimum output voltage of 0V, the current steering mode allows for output swings that do not have to approach the rail voltages. The describing equation for this configuration is:

$$V_{OUT} = \frac{D}{256}(V_{BIAS} - V_{IN}) + V_{BIAS}$$

where D=decimal equivalent of the DAC digital input code
V_{BIAS} is a voltage reference: $0\ V \leq V_{BIAS} \leq 2.5V$ for best linearity.
V_{IN} is a bipolar input voltage

By choosing the proper V_{BIAS} and V_{IN}, the output voltage can be set in the range between V_{BIAS} and $2V_{BIAS} - V_{IN}$. For example, for $V_{DD} = 5\ V$ & $V_{CC} = 15\ V$, select $V_{IN} = 0\ V$ and $V_{BIAS} = 2.5\ V$. This will result in a swing of 2.5 V to 5 V.

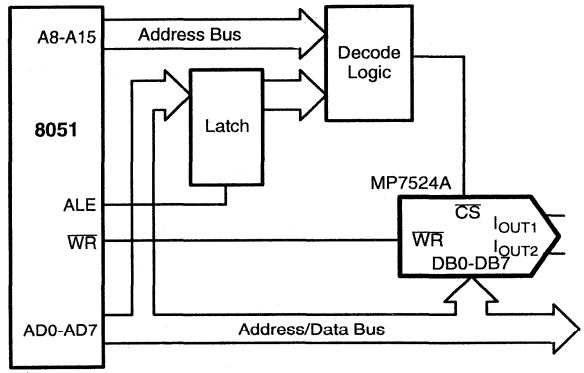


Figure 3. Microcontroller Interface

4

INTERFACE LOGIC INFORMATION

Mode Selection

MP7524A mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the MP7524A is in the WRITE mode, and the MP7524A analog circuit responds to data activity at the DB0-DB7 data bus inputs. In this mode, the MP7524A acts like a non-latched input D/A converter.

Hold Mode

When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the MP7524A is in the HOLD mode. The MP7524A analog output holds the value corresponding to the last digital input present at DB0-DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the high state.

$\overline{CS}$	$\overline{WR}$	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0-DB7) inputs
H	X	Hold	Data Bus (DB0-DB7) is locked out
X	H	Hold	DAC holds last data present when $\overline{WR}$ assumed HIGH state

L = LOW state, H = HIGH state, X = Don't care state

Table 1. Mode Selection Table

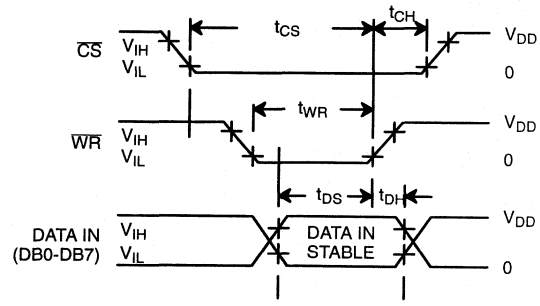


Figure 4. Write Cycle Timing Diagram

MICROPROCESSOR INTERFACE

MP7524A/8080A Interface

Figure 5. shows the MP7524A used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080A CPU, 8224 clock generator and 8228 system controller/bus driver. The MP7524A $\overline{WR}$ input is connected to the 8228 system data bus outputs. The $\overline{CS}$ input is connected to the system address decoding logic. Note that pull-up resistors R3 and R4 are required to ensure that the $\overline{CS}$ and $\overline{WR}$ input HIGH states reach 3.0V min. Pull-ups are not required on the system data bus since the 8228 V_{OH} is 3.6 V min for DB0-DB7.

System timing is shown in *Figure 6.* Data is loaded into the MP7524A when the $\overline{WR}$ and $\overline{CS}$ inputs are both LOW. The data is latched into the MP7524A when $\overline{WR}$ returns HIGH. MP7524A updating is accomplished by using any of the 8080A memory write instructions.

The MP7524A can also be addressed and loaded as an isolated Output Device by connecting the MP7524A $\overline{WR}$ input to the 8228 $\overline{I/O\ W}$ terminal (instead of $\overline{MEMW}$).

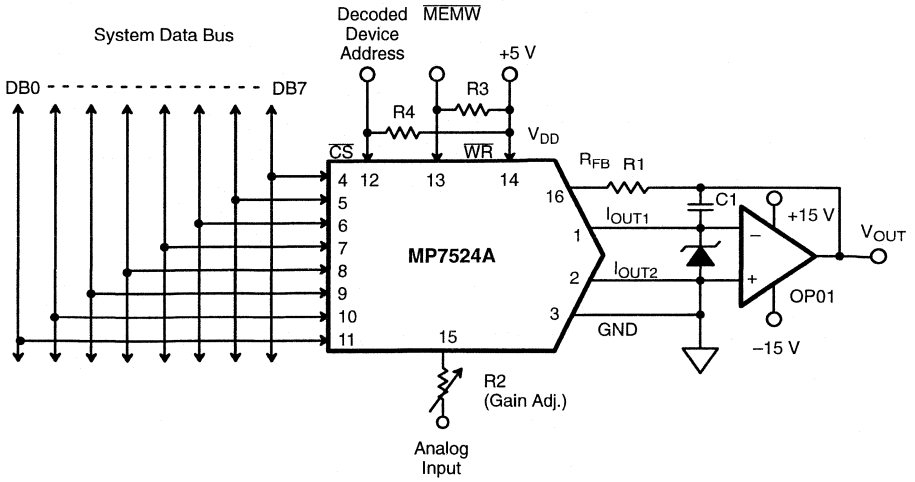


Figure 5. MP7524A/8080A Interface

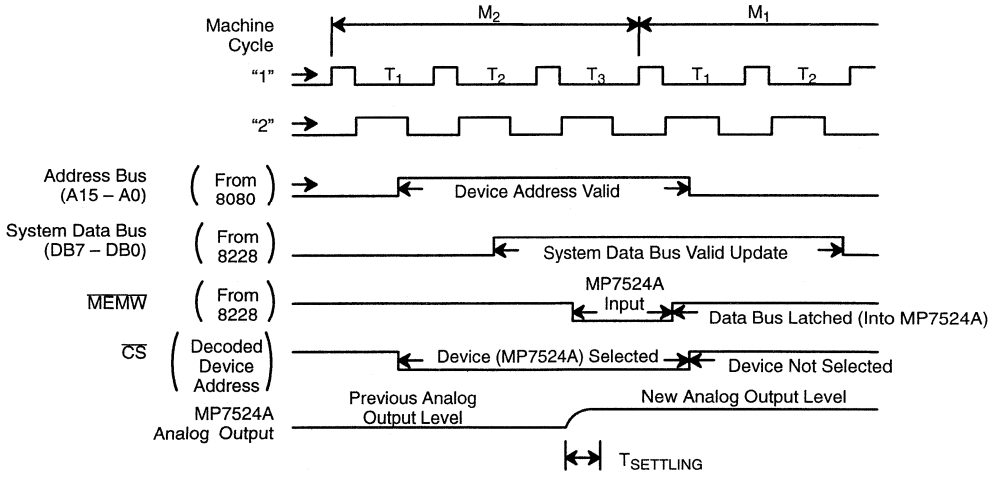


Figure 6. Timing Diagram

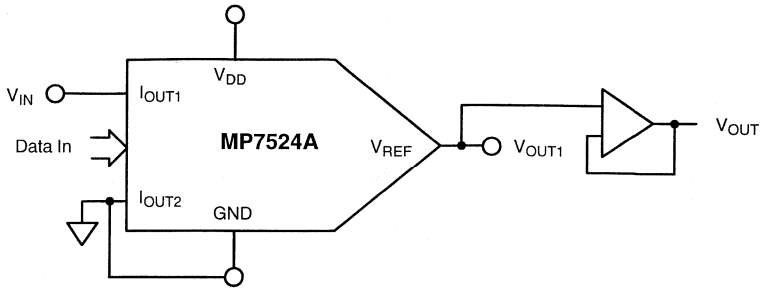


Figure 7. Voltage Mode Operation

MP7528

CMOS
Dual Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **On-Chip Latches for Both DACs**
- **+5 V to +15 V Operation**
- **DACs Matched to 1%**
- **Four Quadrant Multiplication**
- **15 V CMOS Compatible**
- **See MP7529A or MP7529B for Improved Performance**

APPLICATIONS

- **Microprocessor Controlled Gain Circuits**
- **Microprocessor Controlled Attenuator Circuits**
- **Microprocessor Controlled Function Generation**
- **Precision AGC Circuits**
- **Bus Structured Instruments**

GENERAL DESCRIPTION

The MP7528 is a dual 8-bit digital/analog converter designed using EXAR's proven decoded DAC architecture. It features excellent DAC-to-DAC matching and guaranteed monotonicity.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

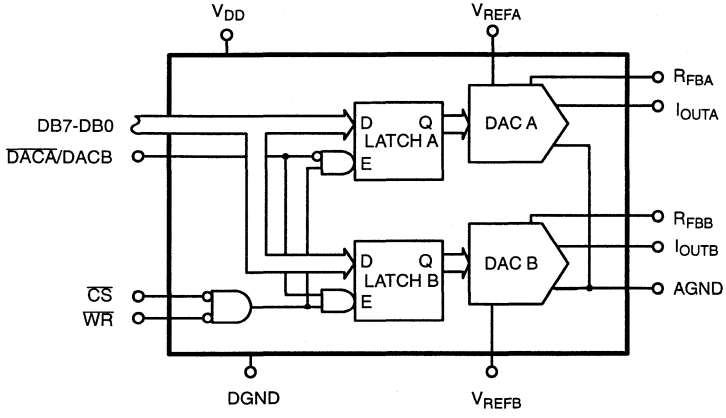
Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{DACA}$/DACB determines which DAC is to be loaded. The MP7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors.

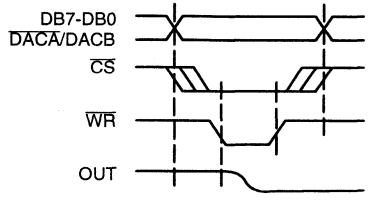
The device operates from a +5V to +15V power supply with only 2 mA of current (maximum).

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

4

SIMPLIFIED BLOCK AND TIMING DIAGRAM





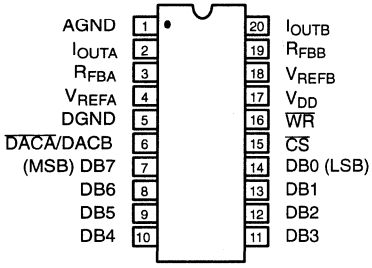
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7528JN	±1	±1	±6
Plastic Dip	–40 to +85°C	MP7528KN	±1/2	±1	±4
Plastic Dip	–40 to +85°C	MP7528LN	±1/4	±1	±3
SOIC	–40 to +85°C	MP7528JS	±1	±1	±6
SOIC	–40 to +85°C	MP7528KS	±1/2	±1	±4
SOIC	–40 to +85°C	MP7528LS	±1/4	±1	±3
PLCC	–40 to +85°C	MP7528JP	±1	±1	±6
PLCC	–40 to +85°C	MP7528KP	±1/2	±1	±4
PLCC	–40 to +85°C	MP7528LP	±1/4	±1	±3
Ceramic Dip	–40 to +85°C	MP7528AD	±1	±1	±6
Ceramic Dip	–40 to +85°C	MP7528BD	±1/2	±1	±4
Ceramic Dip	–40 to +85°C	MP7528CD	±1/4	±1	±3
Ceramic Dip	–55 to +125°C	MP7528SD*	±1	±1	±6
Ceramic Dip	–55 to +125°C	MP7528TD*	±1/2	±1	±4

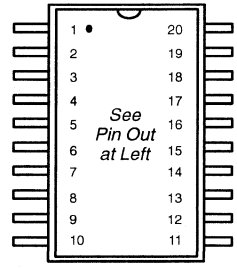
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions

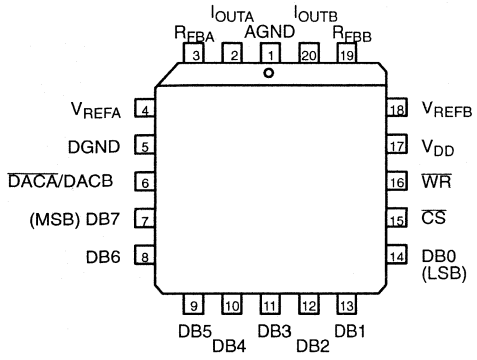


20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300")
S20

PIN CONFIGURATIONS (CONT'D)



20 Pin PLCC
P20

4

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	I_{OUTA}	Current Out DAC A
3	R_{FBA}	Feedback Resistor for DAC A
4	V_{REFA}	Reference Input for DAC A
5	DGND	Digital Ground
6	$\overline{DAC A}$/ DAC B	DAC Select
7	DB7 (MSB)	Data Input Bit 7
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0 (LSB)	Data Input Bit 0
15	$\overline{CS}$	Chip Select
16	$\overline{WR}$	Write
17	V_{DD}	Power Supply
18	V_{REFB}	Reference Input for DAC B
19	R_{FBB}	Feedback Resistor for DAC B
20	I_{OUTB}	Current Out DAC B

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8			Bits
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J, A, S				±1		±1		
K, B, T				±1/2		±1/2		
L, C				±1/4		±1/4		
Monotonicity								Guaranteed over temp
Differential Non-Linearity	DNL			±1		±1	LSB	All grades monotonic over full temperature range.
J, A, S								
K, B, T								
L, C								
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±4		±6		Digital Inputs = V_{INH}
K, B, T				±2		±4		
L, C				±1		±3		
Gain Temperature Coefficient[2]	TC_{GE}					±70	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±200		±400	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5% Digital Inputs = V_{INH}
Output Leakage Current (Pin 2)	I_{OUT1}			±50nA		±400nA	nA	Digital Inputs = V_{INL}
Output Leakage Current (Pin 20)	I_{OUT2}			±50nA		±400nA	nA	Digital Inputs = V_{INH}
Input Resistance	V_{REFA}	8		15	8	15	kΩ	TC = –300 ppm/°C max.
	V_{REFB}	8		15	8	15	kΩ	11 kΩ typical
Input Resistance Matching				±1		±1	%	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Harmonic Distortion	THD		–85				dB	V_{IN} = $6V_{RMS}$ @ 1 KHz
Digital Crosstalk	Q		30				nVs	Measured for code transition Z_S to F_{SS}
Channel-to-Channel Isolation	CCI		–77				dB	
AC Feedthrough at I_{OUT1}	F_T		–70		–65		dB	V_{REF} = 10kHz, 20 Vp-p, sinewave
Glitch Energy	Egl		160				nVs	Z_S to F_S Input Change
Propagation Delay	t_{PD}		220		270		ns	From digital input to 90% of final analog output current

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			10		10	pF	
Control	C_{IN}			15		15	pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUTA}			120		120	pF	DAC Inputs all 1's
	C_{OUTA}			50		50	pF	DAC Inputs all 0's
	C_{OUTB}			120		120	pF	DAC Inputs all 1's
	C_{OUTB}			50		50	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range[2]	V_{DD}	4.5		15.75	4.5	15.75	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or all = 5 V
				2		2	mA	All digital inputs = V_{IL} or all = V_{IH}
SWITCHING CHARACTERISTICS[4]								
Chip Select to Write Set-Up Time	t_{CS}	200			230		ns	
Chip Select to Write Hold Time	t_{CH}	20			30		ns	
DAC Select to Write Set-Up Time	t_{AS}	200			230		ns	
DAC Select to Write Hold Time	t_{AH}	20			30			
Data Valid to Write Set-Up Time	t_{DS}	110			130		ns	
Data Valid to Write Hold Time	t_{DH}	0			0		ns	
Write Pulse Width	t_{WR}	180			200		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8			Bits
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J, A, S				±1		±1		
K, B, T				±1/2		±1/2		
L, C				±1/4		±1/4		
Monotonicity								Guaranteed over temp
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
L, C				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±4		±5		Digital Inputs = V_{INH}
K, B, T				±2		±3		
L, C				±1		±1		
Gain Temperature Coefficient[2]	TC_{GE}					±35	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±100		±200	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5% Digital Inputs = V_{INH}
Output Leakage Current (Pin 2)	I_{OUT1}			±50nA		±200nA	nA	Digital Inputs = V_{INL}
Output Leakage Current (Pin 20)	I_{OUT2}			±50nA		±200nA	nA	Digital Inputs = V_{INH}
Input Resistance	V_{REFA}	8		15	8	15	kΩ	TC = –300 ppm/°C max.
	V_{REFB}	8		15	8	15	kΩ	11 kΩ typical
Input Resistance Matching				±1		±1	%	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Harmonic Distortion	THD		–85				dB	V_{IN} = $6V_{RMS}$ @ 1 KHz
Digital Crosstalk	Q		60				nVs	Measured for code transition ZS to F_S
Channel-to-Channel Isolation	CCI		–77				dB	
AC Feedthrough at I_{OUT1}	F_T		–70		–65		dB	V_{REF} = 10kHz, 20 Vp-p, sinewave
Glitch Energy	EgI		440				nVs	ZS to F_S Input Change
Propagation Delay	t_{PD}			80		100	ns	From 50% of digital input to 90% of final analog output current
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	13.5			13.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Input Leakage Current	I_{ILKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			10		10	pF	
Control	C_{IN}			15		15	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUTA}			120		120	pF	DAC Inputs all 1's
	C_{OUTA}			50		50	pF	DAC Inputs all 0's
	C_{OUTB}			120		120	pF	DAC Inputs all 1's
	C_{OUTB}			50		50	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range[2]	V_{DD}	4.5		15.75	4.5	15.75	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or all = 5 V
				2		2	mA	All digital inputs = V_{IL} or all = V_{IH}
SWITCHING CHARACTERISTICS								
Chip Select to Write Set-Up Time	t_{CS}	60			80		ns	
Chip Select to Write Hold Time	t_{CH}	10			15		ns	
DAC Select to Write Set-Up Time	t_{AS}	60			80		ns	
DAC Select to Write Hold Time	t_{AH}	10			15		ns	
Data Valid to Write Set-Up Time	t_{DS}	30			40		ns	
Data Valid to Write Hold Time	t_{DH}	0			0		ns	
Write Pulse Width	t_{WR}	60			80		ns	

4

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +17 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)
Digital Input Voltage to DGND ..... –0.5 V, +17 V
V_{PIN2}, V_{PIN20} to GND ..... –0.5 V, +17 V
V_{REFA}, V_{REFB} to GND ..... ±25
V_{RFBA}, V_{RFBB} to GND ..... ±25 V
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs.) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.
3 GND refers to AGND and DGND.

INTERFACE LOGIC INFORMATION

DAC Selection: Both DAC latches share a common 8-bit input port. The control input $\overline{DACA}$/DACB selects which DAC can accept data from the input port.

Mode Selection: Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below:

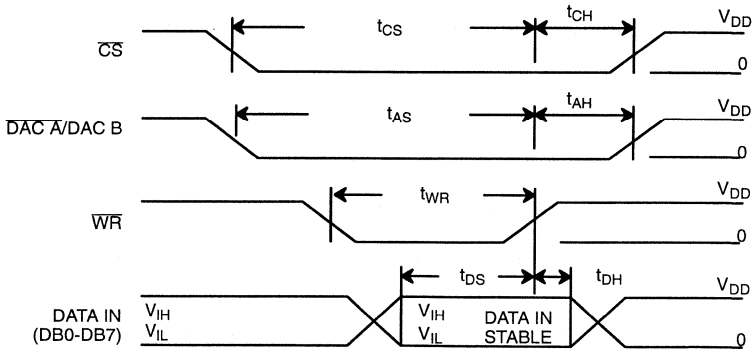
Write Mode: When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7.

Hold Mode: The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{CS}$ and $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{DAC\ A}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = LOW state, H = HIGH state, X = Don't care state

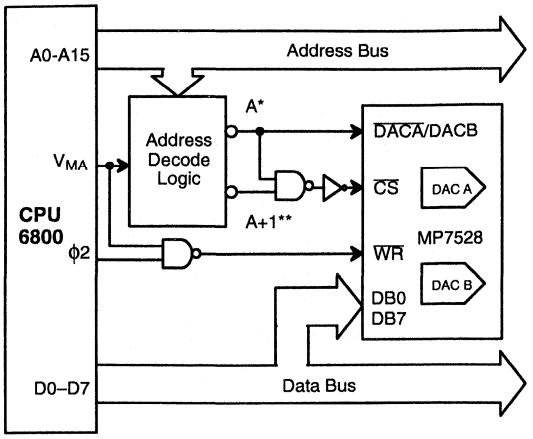
Table 1. Mode Selection Table



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD}.
   V_{DD} = +5 V, $t_r = t_f$ = 20 ns
   V_{DD} = +15 V, $t_r = t_f$ = 40 ns
2. Timing measurement reference level is $V_{IH} + V_{IL} / 2$

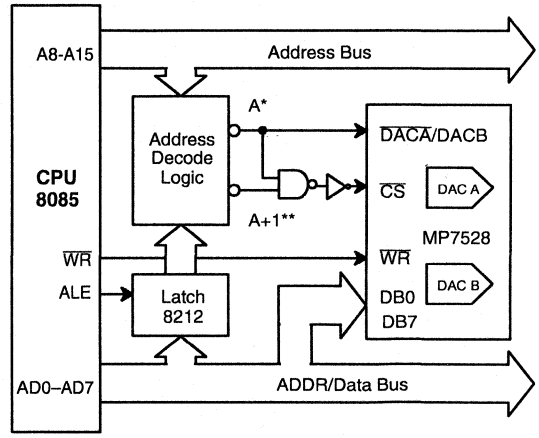
Figure 1. Write Cycle Timing Diagram

MICROPROCESSOR INTERFACE



Analog circuitry has been omitted for clarity
*A = Decoded 7528 DAC A Address
**A + 1 = Decoded 7528 DAC B Address

Figure 2. MP7528 Dual DAC to 6800 CPU Interface



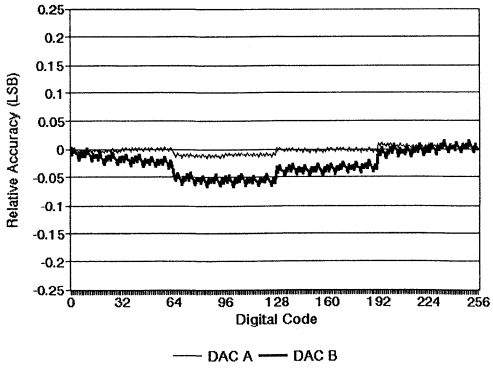
Analog circuitry has been omitted for clarity
*A = Decoded 7528 DAC A Address
**A + 1 = Decoded 7528 DAC B Address

NOTE:
8085 instruction SHLD (store H & L direct) can update both DACS with data from H and L registers

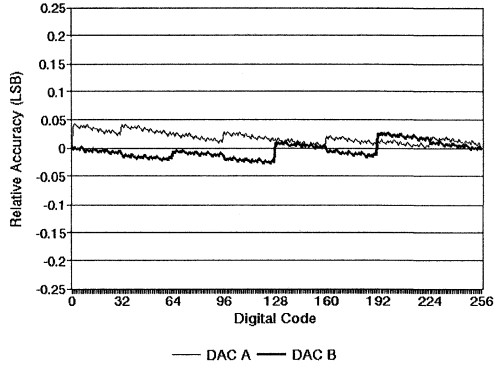
Figure 3. MP7528 Dual DAC to 8085 CPU Interface

4

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code 5 V



Graph 2. Relative Accuracy vs. Digital Code 15 V

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MP7529A

15 V CMOS
Dual Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **Very Low Total Harmonic Distortion**
- **Lower Glitch Energy**
- **Four Quadrant Multiplication**
- **On-Chip Latches for Both DACs**
- **+10.8 V to +15.75 V Operation**
- **Low Power Consumption**
- **TTL/5V CMOS Compatible**
- **Latch-Up Free**
- **Second Source to AD7628**
- **5 V Operation: MP7529B**

BENEFITS

- **Quiet Operation in Audio Applications**
- **Easy Interface to Microprocessors**

4

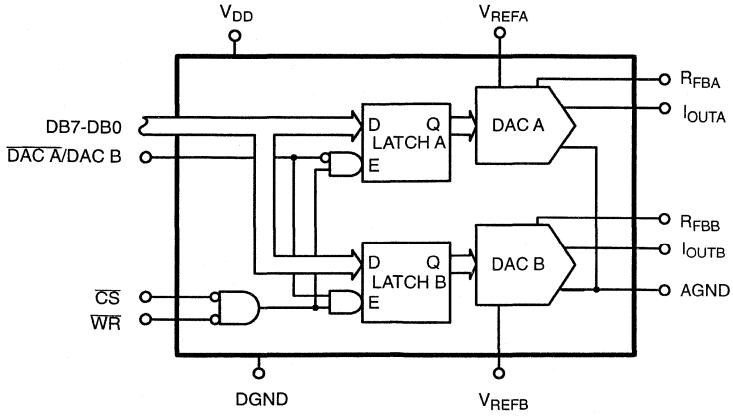
GENERAL DESCRIPTION

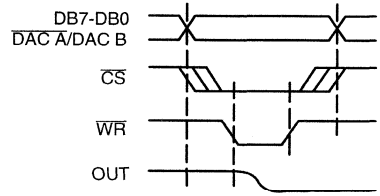
The MP7529A is a dual 8-bit Digital-to-Analog Converter featuring excellent DAC-to-DAC matching, tracking and specifically optimized for applications requiring low total harmonic distortion. The MP7529A is manufactured using advanced thin film resistors on a double metal CMOS process. The MP7529A incorporates a unique decoding technique yielding lower glitch energy, higher speed and excellent accuracy over temperature and time.

Data is transferred to either of the two D/A Converter latches via a common 8-bit TTL/5 V CMOS compatible input port. The control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded.

The device is specified for operation from +10.8 V to +15.75 V power supply, and is TTL-compatible over this range. Power dissipation is only 20 mW. Both DACs offer excellent four quadrant multiplication characteristics, and include separate reference inputs and feedback resistors. An improved latch-up resistant design eliminates the need for external protective Schottky diodes in most applications.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



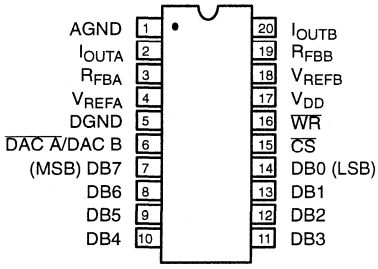


ORDERING INFORMATION

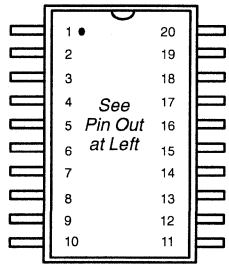
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7529AJN	±1	±1	±5
Plastic Dip	–40 to +85°C	MP7529AKN	±1/2	±1	±3
SOIC	–40 to +85°C	MP7529AJS	±1	±1	±5
SOIC	–40 to +85°C	MP7529AKS	±1/2	±1	±3
PLCC	–40 to +85°C	MP7529AJP	±1	±1	±5
PLCC	–40 to +85°C	MP7529AKP	±1/2	±1	±3

PIN CONFIGURATIONS

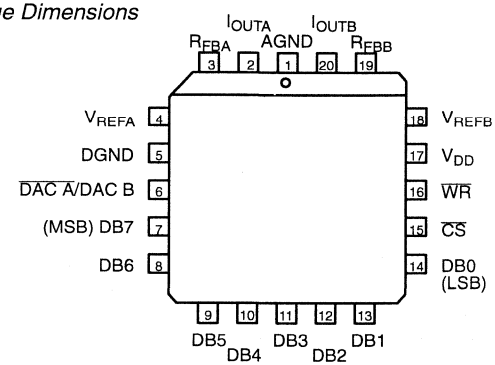
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	I_{OUTA}	Current Output of DAC A
3	R_{FBA}	Internal Feedback Resistor of DAC A
4	V_{REFA}	Reference Input Voltage of DAC A
5	DGND	Digital Ground
6	$\overline{DAC\ A}$/ DAC B	DAC selection control
7	DB7	Data Input Input Bit 7 (MSB)
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4

PIN NO.	NAME	DESCRIPTION
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0	Data Input Bit 0 (LSB)
15	$\overline{CS}$	Chip Select (Active Low)
16	$\overline{WR}$	Write Enable (Active Low)
17	V_{DD}	Power Supply
18	V_{REFB}	Reference Input Voltage of DAC B
19	R_{FBB}	Internal Feedback Resistor of DAC B
20	I_{OUTB}	Current Output of DAC B

ELECTRICAL CHARACTERISTICS

(V_{DD} = +10.8 V to +15.75, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J				±1		±1		
K				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J				±1		±1		
K				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J				±4		±5		
K				±2		±3		
Gain Temperature Coefficient[2]	TC_{GE}		±15			±35	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±100		±200	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$, ΔV_{DD} = ± 5% V_{DD} = 10.8 V, ±5%, & 15.75 V ±5%
Output Leakage Current	I_{LKG}			±50		±200	nA	
DYNAMIC PERFORMANCE[2]								
Harmonic Distortion	THD		–95				dB	V_{IN} = 6V_{RMS} @ 1 kHz
Digital Crosstalk	Q		30				nVs	
AC Feedthrough	F_T						dB	
V_{REFA} to I_{OUTA}	F_{TA}		–70			–65	dB	
V_{REFB} to I_{OUTB}	F_{TB}		–70			–65	dB	
Channel-to-Channel Isolation	CCI						dB	
V_{REFA} to I_{OUTB}	C_{CIBA}		–77				dB	
V_{REFB} to I_{OUTA}	C_{CIAB}		–77				dB	
Glitch Energy	EgI		10				nVs	All zeros to all ones Input Change
Current Settling Time	t_S		200			250	ns	To 1/2 LSB, R_L=100Ω, C_{EXT}=13pF
Propagation Delay	t_{PD}		100			150	ns	From 50% of digital input to 90% of final analog output current R_L=100Ω, C_{EXT}=13pF
REFERENCE INPUT[1]								
Input Resistance	R_{IN}	8		15	8	15	kΩ	
Input Resistance Matching				±1		±1	%	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			10		10	pF	
Control	C_{IN}			15		15	pF	

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS[2]								
Output Capacitance								
	$C_{OUTA/B}$			120		120	pF	DAC inputs all 1's
	$C_{OUTA/B}$			50		50	pF	DAC inputs all 0's
POWER SUPPLY[1]								
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V, or all = 5 V
				2		2	mA	All digital inputs = V_{IL}, or all = V_{IH}
TIMING SPECIFICATIONS[4]								
Chip Select to Write Set-Up Time	t_{CS}	60			80		ns	
Chip Select to Write Hold Time	t_{CH}	15			20		ns	
DAC Select to Write Set-Up Time	t_{AS}	60			80		ns	
DAC Select to Write Hold Time	t_{AH}	15			20		ns	
Data Valid to Write Set-Up Time	t_{DS}	60			80		ns	
Data Valid to Write Hold Time	t_{DH}	0			0		ns	
Write Pulse Width[5]	t_{WR}	60			80		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram *Figure 1.*
5 t_{WR} = 40ns minimum if t_{DH} > 15ns (@T = 25°C).

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... GND –0.5 to +17 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)
Digital Input Voltage to GND ..... GND –0.5 V to +7 V
I_{OUTA}, I_{OUTB} to GND ..... GND –0.5 V to +7 V
V_{REFA}, V_{REFB} to GND ..... ±25 V
V_{RFBA}, V_{RFBB} to GND ..... ±25 V
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC, PLCC 900mW
Derates above 75°C ..... 12mW/°C

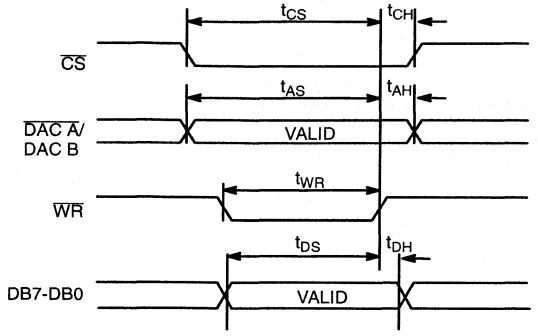
NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

DIGITAL INTERFACE

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 10nA.

The control input $\overline{DAC\ A}$/DAC B selects which DAC can accept data from the input port. Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC (*Table 1.*). When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7 (Write mode). The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches (Hold mode).



NOTE:
1. Timing measured from $(V_{IH} + V_{IL})/2$

Figure 1. Write Cycle Timing Diagram

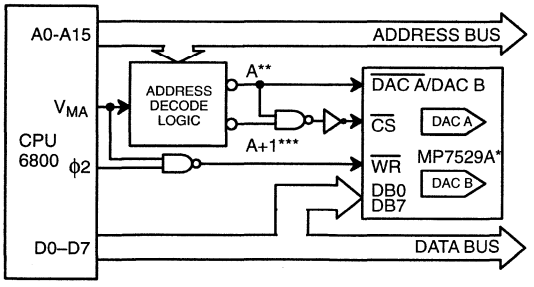
DAC A/ DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Table 1. DACs Mode Selection

4

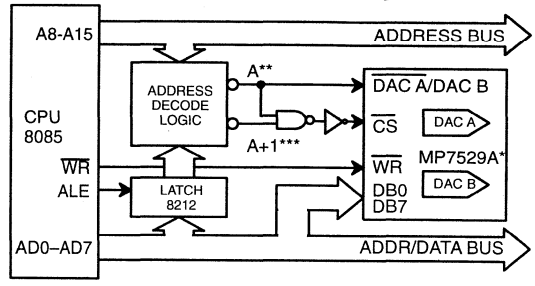
MICROPROCESSOR INTERFACE



*Analog circuitry has been omitted for clarity
**A = Decoded 7529A DAC A Address
***A+1 = Decoded 7529A DAC B Address

Figure 2. MP7529A Dual DAC to 6800 CPU Interface

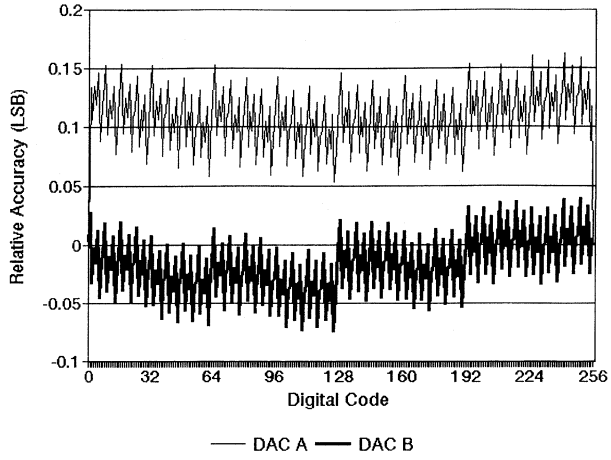
NOTE:
8085 instruction shld (store H & L direct) can update both DACS with data from H and L registers



*Analog circuitry has been omitted for clarity
**A = Decoded 7529A DAC A Address
***A+1 = Decoded 7529A DAC B Address

Figure 3. MP7529A Dual DAC to 8085 CPU Interface

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information

MP7529B

5 V CMOS
Dual Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **Very Low Total Harmonic Distortion**
- **Low Glitch Energy**
- **Fast Settling Time**
- **Four Quadrant Multiplication**
- **On-Chip Latches for Both DACs**
- **4.5 V to 5.5 V Operation**
- **Low Power Consumption**
- **TTL/5V CMOS Compatible**
- **Latch-Up Free**
- **15 V Operation: MP7529A**

BENEFITS

- **Quiet Operation in Audio Applications**
- **Easy Interface to Microprocessors**

GENERAL DESCRIPTION

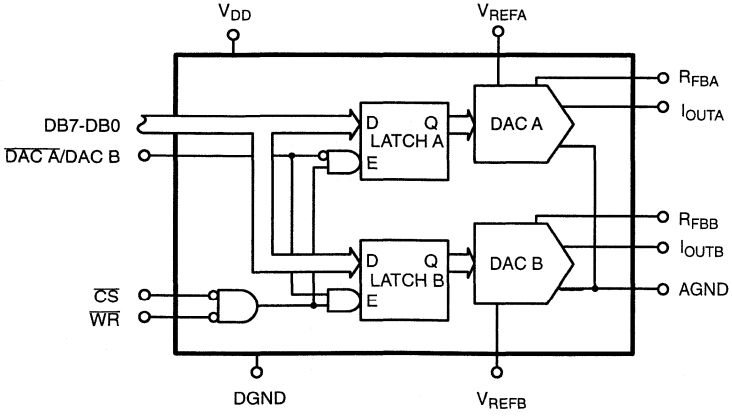
The MP7529B is a dual 8-bit Digital-to-Analog Converter featuring excellent DAC to DAC matching, tracking and specifically optimized for applications requiring low total harmonic distortion. The MP7529B is manufactured using advanced thin film resistors on a double metal CMOS process. The MP7529B incorporates a unique bit decoding technique yielding lower glitch energy, higher speed and excellent accuracy over temperature and time.

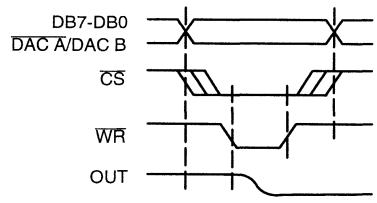
Data is transferred to either of the two D/A Converter latches via a common 8-bit TTL/5 V CMOS compatible input port. The control input $\overline{\text{DAC A}}$/DAC B determines which D/A is to be loaded.

The device operates from a 4.5 V to 5.5 V power supply, and is TTL-compatible over this range. Power dissipation is only 10 mW. Both DACs offer excellent four quadrant multiplication characteristics, and include separate reference inputs and feedback resistors. An improved latch-up resistant design eliminates the need for external protective Schottky diodes in most applications.

4

SIMPLIFIED BLOCK AND TIMING DIAGRAM



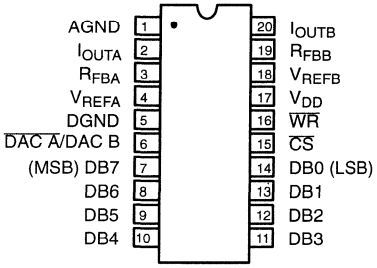


ORDERING INFORMATION

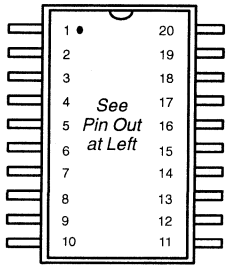
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7529BJN	±1	±1	±5
Plastic Dip	–40 to +85°C	MP7529BKN	±1/2	±1	±3
SOIC	–40 to +85°C	MP7529BJS	±1	±1	±5
SOIC	–40 to +85°C	MP7529BKS	±1/2	±1	±3
PLCC	–40 to +85°C	MP7529BJP	±1	±1	±5
PLCC	–40 to +85°C	MP7529BKP	±1/2	±1	±3

PIN CONFIGURATIONS

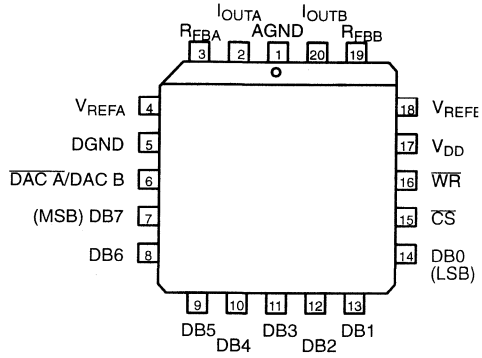
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	I_{OUTA}	Current Output of DAC A
3	R_{FBA}	Internal Feedback Resistor of DAC A
4	V_{REFA}	Reference Input Voltage of DAC A
5	DGND	Digital Ground
6	DACA/ DACB	DAC selection control
7	DB7	Data Input Bit 7 (MSB)
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4

PIN NO.	NAME	DESCRIPTION
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0	Data Input Bit 0 (LSB)
15	CS	Chip Select (Active Low)
16	WR	Write Enable (Active Low)
17	V_{DD}	Power Supply
18	V_{REFB}	Reference Input Voltage of DAC B
19	R_{FBB}	Internal Feedback Resistor of DAC B
20	I_{OUTB}	Current Output of DAC B

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.5 V to 5.5 V, Nominal V_{DD} = 5 V, V_{REF} = 10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J				±1		±1		
K				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J				±1		±1		
K				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J				±4		±5		
K				±2		±3		
Gain Temperature Coefficient[2]	TC_{GE}			±15		±15	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±100		±200	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$, ΔV_{DD} = ± 5% V_{DD} = 4.75 V, ±5%, & 5.25 V ±5%
Output Leakage Current	I_{LKG}			±50		±200	nA	
DYNAMIC PERFORMANCE[2]								
Harmonic Distortion	THD		–95				dB	V_{IN} = $6V_{RMS}$ @ 1 KHz
Digital Crosstalk	Q		30				nVs	
AC Feedthrough	F_T						dB	
V_{REFA} to I_{OUTA}	F_{TA}		–70			–65	dB	
V_{REFB} to I_{OUTB}	F_{TB}		–70			–65	dB	
Channel-to-Channel Isolation	CCI						dB	
V_{REFA} to I_{OUTB}	C_{CIBA}		–77				dB	
V_{REFB} to I_{OUTA}	C_{CIAB}		–77				dB	
Glitch Energy	Egl		10				nVs	All zeros to all ones Input Change.
Current Settling Time	t_S		200			250	ns	To 1/2 LSB, R_L=100Ω, C_{EXT}=13pF
Propagation Delay	t_{PD}		100			150	ns	From 50% of digital input to 90% of final analog output current R_L=100Ω, C_{EXT}=13pF
REFERENCE INPUT								
Input Resistance	R_{IN}	8		15	8	15	kΩ	
Input Resistance Matching				±1		±1	%	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			10		10	pF	
Control	C_{IN}			15		15	pF	

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS[2]								
Output Capacitance								
	$C_{OUTA/B}$			120		120	pF	DAC inputs all 1's
	$C_{OUTA/B}$			50		50	pF	DAC inputs all 0's
POWER SUPPLY								
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V or 5 V
				2		2	mA	All digital inputs = V_{IL} or V_{IH}
TIMING SPECIFICATIONS[4]								
Chip Select to Write Set-Up Time	t_{CS}	60			80		ns	
Chip Select to Write Hold Time	t_{CH}	15			20		ns	
DAC Select to Write Set-Up Time	t_{AS}	60			80		ns	
DAC Select to Write Hold Time	t_{AH}	15			20		ns	
Data Valid to Write Set-Up Time	t_{DS}	60			80		ns	
Data Valid to Write Hold Time	t_{DH}	0			0		ns	
Write Pulse Width[5]	t_{WR}	60			80		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.

2 Guaranteed but not production tested.

3 Digital input levels should not go below GND or exceed the positive supply voltage, otherwise damage may occur.

4 See timing diagram.

5 t_{WR} = 40ns minimum if t_{DH} > 15ns (@T = 25°C)

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +7 V

AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V

I_{OUTA}, I_{OUTB} to GND ..... GND –0.5 to V_{DD} +0.5 V

V_{REFA}, V_{REFB} to GND ..... ±25 V

V_{RFBA}, V_{RFBB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC, PLCC 900mW

Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

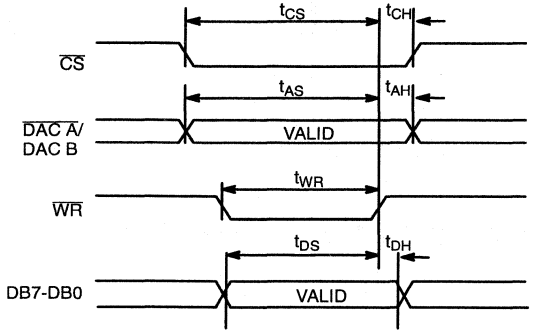
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 GND refers to AGND and DGND.

DIGITAL INTERFACE

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 10nA.

The control input $\overline{DAC\ A}$/DAC B selects which DAC can accept data from the input port. Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC (*Table 1.*). When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7 (Write mode). The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches (Hold mode).



NOTE:
1. Timing measured from $(V_{IH} + V_{IL})/2$

Figure 1. Write Cycle Timing Diagram

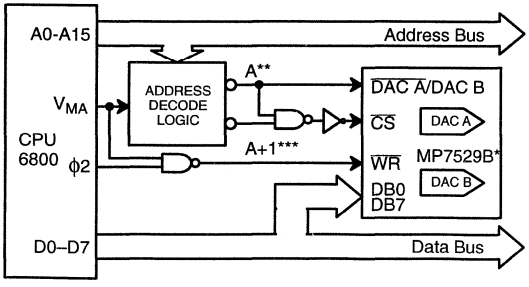
DAC A/ DAC B	CS	WR	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Table 1. DAC's Mode Selection

4

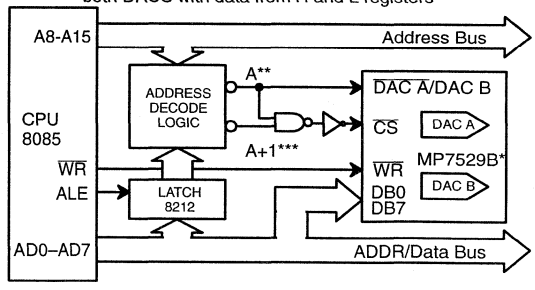
MICROPROCESSOR INTERFACE



*Analog circuitry has been omitted for clarity
**A = Decoded 7529B DAC A Address
***A + 1 = Decoded 752B9 DAC B Address

Figure 2. MP7529B Dual DAC to 6800 CPU Interface

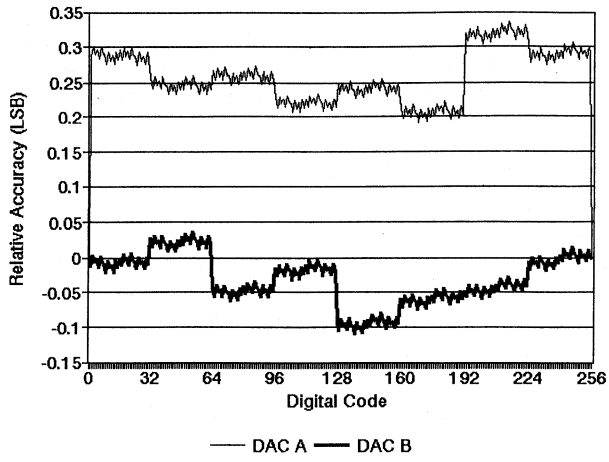
NOTE:
8085 instruction shld (store H & L direct) can update both DACS with data from H and L registers



*Analog circuitry has been omitted for clarity
**A = Decoded 7529B DAC A Address
***A + 1 = Decoded 7529B DAC B Address

Figure 3. MP7529B Dual DAC to 8085 CPU Interface

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information

MP7533

15 V CMOS
Multiplying10-Bit
Digital-to-Analog Converter

FEATURES

- **10-Bit Resolution**
- **Non-Linearity: 1/2 LSB to 2 LSB**
- **Nonlinearity Tempco: 0.2 ppm of FSR/°C, Max.**
- **Low Power Dissipation: 20 mW**
- **Current Settling Time: 500 ns**
- **Feedthrough Error: 1 mV p-p @ 10 kHz, Max.**
- **TTL/CMOS Compatible**
- **Latch-Up Free**
- **Improved Replacement for AD7533**

BENEFITS

- **Accurate Converter at Low Cost**
- **Can be used in Reverse Mode (Voltage Out)**
- **Flexible Design**

APPLICATIONS

- **Digital/Analog Multiplication**
- **Character Generation**
- **Programmable Power Supplies**
- **Gain Controlled Circuits**

4

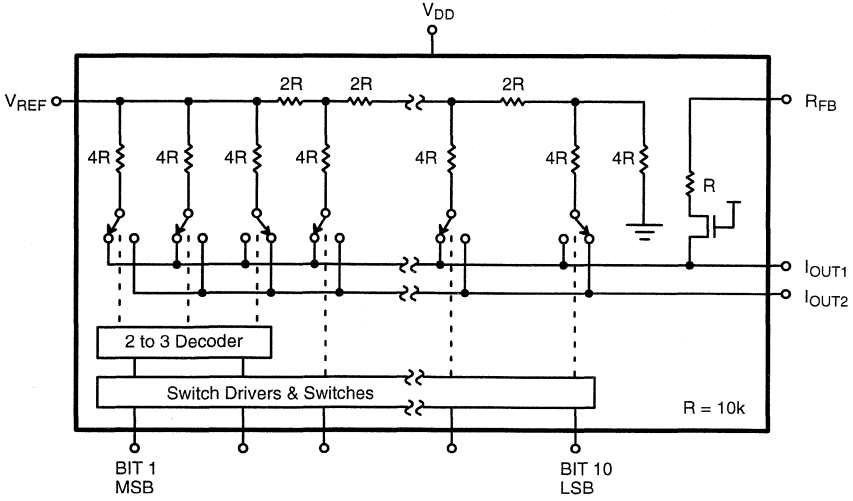
GENERAL DESCRIPTION

The MP7533 is a low cost, 10-bit multiplying Digital-to-Analog Converter. This device uses EXAR's patented advanced thin film resistor and CMOS technologies, providing up to 10-bit accuracies with TTL/CMOS compatibility.

Pin and functional equivalent to the industry standard MP7520, the MP7533 is recommended as a lower cost alternative for old MP7520 sockets or new 10-bit DAC designs.

The MP7533 applications include: digital-to-analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

SIMPLIFIED BLOCK DIAGRAM



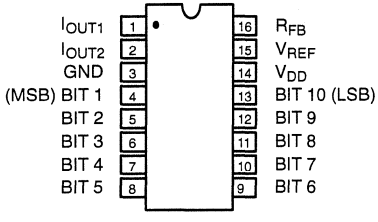
3 Segment D/A Converter with Termination to DGND
Logical "1" at Digital Input Steers Current to I_{OUT1}

ORDERING INFORMATION

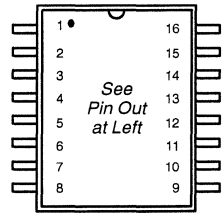
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7533JN	±2	±1	1.5
Plastic Dip	–40 to +85°C	MP7533KN	±1	±1	1.5
Plastic Dip	–40 to +85°C	MP7533LN	±1/2	±1	1.5
SOIC	–40 to +85°C	MP7533JS	±2	±1	1.5
SOIC	–40 to +85°C	MP7533KS	±1	±1	1.5
SOIC	–40 to +85°C	MP7533LS	±1/2	±1	1.5
Ceramic Dip	–40 to +85°C	MP7533AD	±2	±1	1.5
Ceramic Dip	–40 to +85°C	MP7533BD	±1	±1	1.5
Ceramic Dip	–40 to +85°C	MP7533CD	±1/2	±1	1.5
Ceramic Dip	–55 to +125°C	MP7533SD*	±2	±1	1.5
Ceramic Dip	–55 to +125°C	MP7533TD*	±1	±1	1.5
Ceramic Dip	–55 to +125°C	MP7533UD*	±1/2	±1	1.5

*Contact factory for non-compliant military processing

PIN CONFIGURATIONS *See Packaging Section for Package Dimensions*



16 Pin CDIP, PDIP (0.300")
D16, N16



16 Pin SOIC (Jedec, 0.300")
S16

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5

PIN NO.	NAME	DESCRIPTION
9	BIT 6	Data Input Bit 6
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10 (LSB)
14	V_{DD}	Positive Power Supply
15	V_{REF}	Reference Input Voltage
16	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	10			10		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
A, S, J				±2		±2		
B, T, K				±1		±1		
C, U, L				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
A, S, J				±1		±1		
B, T, K				±1		±1		
C, U, L				±1		±1		
Gain Error	GE		±0.4	±1.5		±1.5	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		±30	±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±50		±200	nA	
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT1}			52			pF	DAC Inputs all 1's
	C_{OUT1}			26			pF	DAC Inputs all 0's
	C_{OUT2}			13			pF	DAC Inputs all 1's
	C_{OUT2}			45			pF	DAC Inputs all 0's
POWER SUPPLY[4]								
Functional Voltage Range[2]	V_{DD}	4.5		15	4.5	15	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 or all = 5 V
Total Dissipation			20				mW	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested
3 Digital Input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 700mW
Derates above 75°C ..... 10mW/°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 20mA for less than 100µs.

APPLICATION NOTES

Refer to Section 8 for Applications Information

MP7541

15 V CMOS
Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four Quadrant Multiplication**
- **12-Bit Linearity**
- **Guaranteed Monotonic; All Grades; All Temperatures.**
- **TTL/15 V CMOS Compatible**
- **Stable, More Accurate Decoded Architecture**
  - **2.0 ppm/°C Typ. Gain Error Tempco**
  - **0.2 ppm/°C Max. Linearity Tempco**
  - **Lowest Sensitivity to Output Amplifier Offset**
- **Latch-Up Free**
- **Use MP7541B for New Designs**

APPLICATIONS

- **Industrial Automation**
- **Automatic Test Equipment**
- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

GENERAL DESCRIPTION

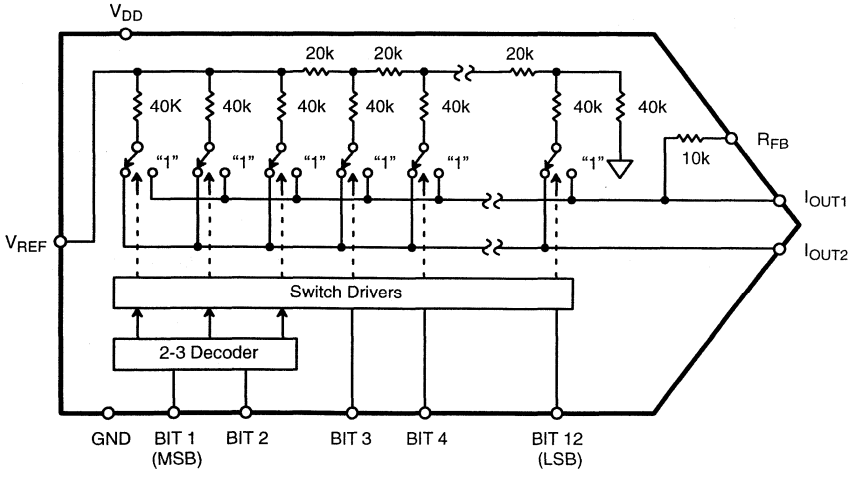
The MP7541 is a 12-Bit Digital-to-Analog Converter which is manufactured using EXAR's patented advanced thin film resistor and double metal CMOS process. The MP7541 incorporates a bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7541 outstanding features are:

Stability: Both Integral-Non-Linearity and Differential-Non-Linearity are rated at 0.2 ppm/°C maximum. Monotonicity is guaranteed over the entire temperature range. Gain Temperature Coefficient (TCGE) is 2.0 ppm/°C typical.

Lower Sensitivity to Output Amplifier Offset: Multiplying DACs provide an output current into a virtual ground of the output op amp. Additional linearity error caused by the op amp is reduced by a factor of 2 in the MP7541 versus conventional R-2R DACs.

4

SIMPLIFIED BLOCK DIAGRAM



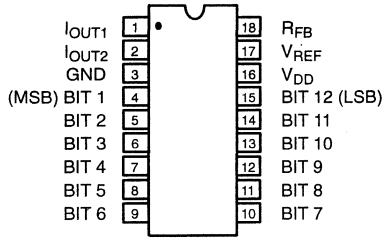
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7541JN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP7541KN	±1/2	±1	±0.4
SOIC	–40 to +85°C	MP7541JS	±1	±1	±0.4
SOIC	–40 to +85°C	MP7541KS	±1/2	±1	±0.4
Ceramic Dip	–40 to +85°C	MP7541AD	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP7541BD	±1/2	±1	±0.4
Ceramic Dip	–55 to +125°C	MP7541SD*	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP7541TD*	±1/2	±1	±0.4
Plastic Dip	–40 to +85°C	MP7541AJN	±1	±1	±8
Plastic Dip	–40 to +85°C	MP7541AKN	±1/2	±1/2	±5
SOIC	–40 to +85°C	MP7541AJS	±1	±1	±8
SOIC	–40 to +85°C	MP7541AKS	±1/2	±1/2	±5
Ceramic Dip	–40 to +85°C	MP7541AAD	±1	±1	±8
Ceramic Dip	–40 to +85°C	MP7541ABD	±1/2	±1/2	±5
Ceramic Dip	–55 to +125°C	MP7541ASD*	±1	±1	±8
Ceramic Dip	–55 to +125°C	MP7541ATD*	±1/2	±1/2	±5

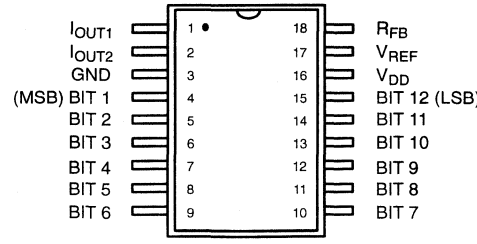
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin PDIP, CDIP (0.300")
N18, D18



18 Pin SOIC (Jedec, 0.300")
S18

MP7541B

15 V CMOS
Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **ESD Protection: 2000 V Minimum**
- **Full Four Quadrant Multiplication**
- **Low Glitch Energy**
- **12-Bit Linearity (End-Point)**
- **Guaranteed Monotonic. All Grades. All Temperatures.**
- **TTL/5 V CMOS Compatible**
- **Stable, More Accurate Segmented Architecture**
  - **2.0 ppm/°C Typ. Gain Error Tempco**
  - **0.2 ppm/°C Max. Linearity Tempco**
  - **Lowest Sensitivity to Output Amplifier Offset**
- **Latch-Up Free**

APPLICATIONS

- **Industrial Automation**
- **Automatic Test Equipment**
- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

4

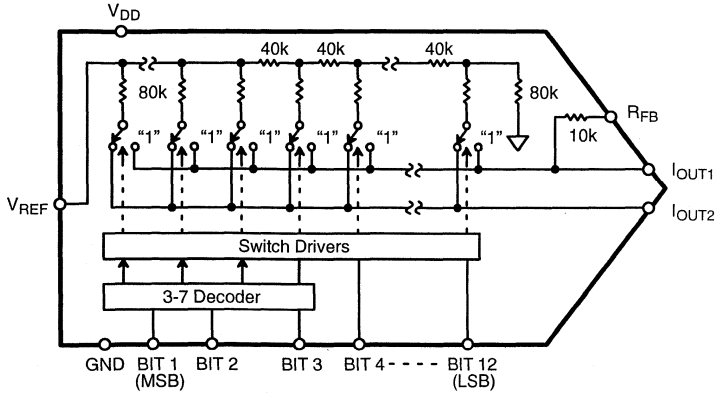
GENERAL DESCRIPTION

The MP7541B is a pin-compatible replacement which offers superior performance in latch-up and ESD protection versus the comparable 7541 and 7541A. The high ESD protection will reduce failures caused by mishandling. These devices are manufactured using patented advanced thin film resistors on a double metal CMOS process which result in ultra stable thin film and superior long life reliability and stability. The MP7541B incorporates a bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7541B's outstanding features are:

Stability: Both Integral Non-Linearity (INL) and Differential-Non-Linearity (DNL) are rated at 0.2 ppm/°C maximum. Monotonicity is guaranteed over the entire temperature range. Gain Temperature Coefficient (TCGE) is 2.0 ppm/°C typical.

Lower Sensitivity to Output Amplifier Offset: Multiplying DACs provide an output current into a virtual ground of the output op amp. Additional linearity error caused by the op amp is reduced by a factor of 3 in the MP7541B versus conventional R-2R DACs.

SIMPLIFIED BLOCK DIAGRAM



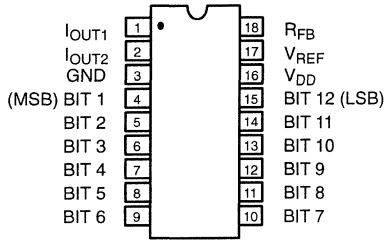
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7541BKN	±1/2	±1/2	±5
Plastic Dip	–40 to +85°C	MP7541BJN	±1	±1	±8
SOIC	–40 to +85°C	MP7541BKS	±1/2	±1/2	±5
SOIC	–40 to +85°C	MP7541BJS	±1	±1	±8
Ceramic Dip	–55 to +125°C	MP7541BTD*	±1/2	±1/2	±5
Ceramic Dip	–55 to +125°C	MP7541BSD*	±1	±1	±8

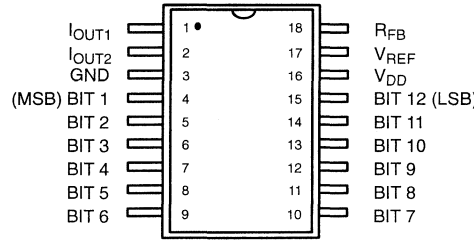
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin PDIP, CDIP (0.300")
N18, D18



18 Pin SOIC (Jedec, 0.300")
S18

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6

PIN NO.	NAME	DESCRIPTION
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10
14	BIT 11	Data Input Bit 11
15	BIT 12	Data Input Bit 12 (LSB)
16	V_{DD}	Positive Power Supply
17	V_{REF}	Reference Input Voltage
18	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

V_{DD} = + 15 V, V_{REF} = +10 V, I_{OUT1} = I_{OUT2} = GND = 0 V Unless Otherwise Noted.

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K, T				±1/2		±1/2		
J, S				±1		±1		
Differential Non-Linearity	DNL						LSB	All grades
K, T				±1/2		±1/2		monotonic over full
J, S				±1		±1		temperature range.
Gain Error	GE						LSB	Using Internal R_{FB}
K, T				±3		±5		
J, S				±6		±8		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		5	±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{LKG}		5	±10		±200	nA	Digital Inputs = 0 or 5 V
DYNAMIC PERFORMANCE[2]								RL=100Ω, C_{EXT}=13pF
Current Settling Time	t_S		0.65	1.0			µs	Full scale change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T		1.0				mV p-p	V_{REF} = 20 V p-p 10kHz, Sinewave
Glitch Energy	Egl		500				nVs	00--0 to 11--1 Input Change
Propagation Delay	t_{PD}		60				ns	From 50% of digital input to 10% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{INH}, I_{INL}			±1.0		±1.0	µA	
Input Capacitance[2]								
Data	C_{IN}			8.0		8.0	pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		100				pF	DAC all 1's
	C_{OUT1}		50				pF	DAC all 0's
	C_{OUT2}		50				pF	DAC all 1's
	C_{OUT2}		100				pF	DAC all 0's
POWER SUPPLY[3]								
Functional Voltage Range[2]	V_{DD}	4.5		16	4.5	16	V	
Supply Current	I_{DD}			1.0		1.0	mA	All Digital Inputs = 0 or 5 V

4

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 850mW
Derates above 75°C ..... 11mW/°C

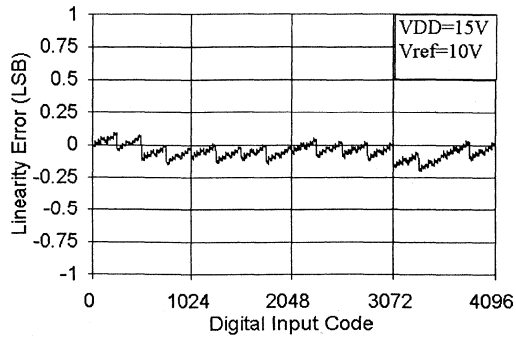
NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 20mA for less than 100µs.

APPLICATION NOTES

Refer to Section 8 for Applications Information

PERFORMANCE CHARACTERISTICS



Graph 1. Linearity Error vs. Digital Input Code

MP7542

5 V CMOS
4-Bit Input, 12-Bit
Digital-to-Analog Converter

FEATURES

- **12-Bit DAC with a 4-Bit Parallel Address for 4 & 8-Bit Microprocessor or Microcontroller Interface**
- **Nonlinearity ±1/2 LSB Tmin to Tmax**
- **Latch-Up Free**
- **Low Sensitivity to Output Amplifier V_{OS}**
- **Low Output Capacitance**
- **+5 V Supply Operation**
- **Low Power Consumption: 40mW Max.**
- **Low Cost**
- **Serial Version: MP7543**

GENERAL DESCRIPTION

The MP7542 is a precision, 12-bit CMOS 4-quadrant multiplying Digital-to-Analog Converter designed for direct interface to 4 and 8-bit microprocessors.

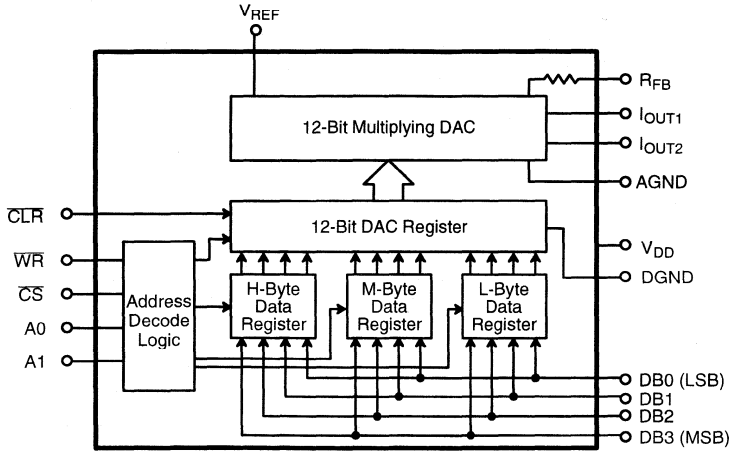
The MP7542 consists of three 4-bit registers, a 12-bit DAC register, address decoding logic, and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit nibbles and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A CLEAR input allows the 12-bit DAC register to be reset to all zeros.

The MP7542 is manufactured using advanced thin-film on monolithic double metal CMOS fabrication process. A unique decoding technique is utilized yielding excellent accuracy and stability.

The MP7542 reduces the additional linearity errors due to output amplifier offset to only 330µV per millivolt of offset versus 670 µV for the standard R-2R ladder CMOS DACs.

4

SIMPLIFIED BLOCK DIAGRAM

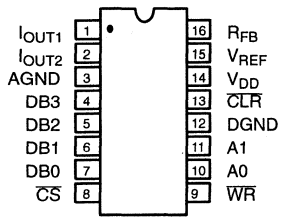


ORDERING INFORMATION

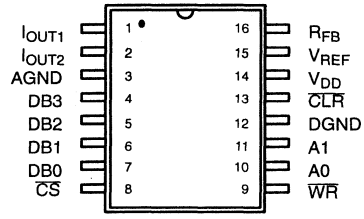
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7542JN	±1	±2	±14.5
Plastic Dip	–40 to +85°C	MP7542KN	±1/2	±1	±14.5
SOIC	–40 to +85°C	MP7542JS	±1	±2	±14.5
SOIC	–40 to +85°C	MP7542KS	±1/2	±1	±14.5
Ceramic Dip	–40 to +85°C	MP7542AD	±1	±2	±14.5
Ceramic Dip	–40 to +85°C	MP7542BD	±1/2	±1	±14.5
Ceramic Dip	–55 to +125°C	MP7542SD*	±1	±2	±14.5
Ceramic Dip	–55 to +125°C	MP7542TD*	±1/2	±1	±14.5

*Contact factory for non-compliant military processing

PIN CONFIGURATIONS *See Packaging Section for Package Dimensions*



16 Pin CDIP, PDIP (0.300")
D16, N16



16 Pin SOIC (Jedec, 0.300")
S16

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	DAC current output. Normally terminated at op amp.
2	I_{OUT2}	DAC current output. Normally terminated at ground.
3	AGND	Analog Ground
4	DB3	Data Input Bit 3 (MSB)
5	DB2	Data Input Bit 2
6	DB1	Data Input Bit 1
7	DB0	Data Input Bit 0 (LSB)

PIN NO.	NAME	DESCRIPTION
8	$\overline{CS}$	Chip Select Input
9	$\overline{WR}$	Write Input
10	A0	Address Bus Input
11	A1	Address Bus Input
12	DGND	Digital Ground
13	$\overline{CLR}$	Clear Input
14	V_{DD}	+5 V Supply Input
15	V_{REF}	Reference Input
16	R_{FB}	DAC Feedback Resistor

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1		±1		
K, B, T				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	Monotonicity
J, A, S				±2		±2		11 Bits Guaranteed
K, B, T				±1		±1		12 Bits Guaranteed
Gain Error								
J, A, S, K, B, T	GE			±12.3		±14.5	LSB	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±10		±200	nA	
DYNAMIC PERFORMANCE								R_L=100Ω, C_L=13pF
Current Settling Time[2]	t_S			2.0		2.0	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}[2]	F_T			2.5		2.5	mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0			3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
Input Capacitance[2]	C_{IN}			8		8	pF	
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT1}			260		260	pF	DAC Inputs all 1's
	C_{OUT1}			100		100	pF	DAC Inputs all 0's
	C_{OUT2}			50		50	pF	DAC Inputs all 1's
	C_{OUT2}			210		210	pF	DAC Inputs all 0's
POWER SUPPLY								
Supply Voltage[5]	V_{DD}	+4.5		+5.5	+4.5	+5.5	V	
Supply Current	I_{DD}			2.5		2.5	mA	All digital inputs = 0 V or all = 5 V

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
$\overline{WR}$ Pulse Width	t_{WR}	120			220		ns	
Address to $\overline{WR}$ Hold Time	t_{AWH}	50			65		ns	
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CWH}	50			100		ns	
$\overline{CLR}$ Pulse Width	t_{CLR}	200			300		ns	
Byte Loading, $\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS1}	60			130		ns	
Byte Loading, Address to $\overline{WR}$ Setup	t_{AWS1}	80			180		ns	
Byte Loading, $\overline{WR}$ to Data Setup	t_{DS}	50			65		ns	
Byte Loading, $\overline{WR}$ to Data Hold	t_{DH}	50			65		ns	
DAC Loading, $\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS2}	60			150		ns	
DAC Loading, Address to $\overline{WR}$ Setup	t_{AWS2}	120			240		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 700mW
Derates above 75°C ..... 10mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.
3 GND refers to AGND and DGND.

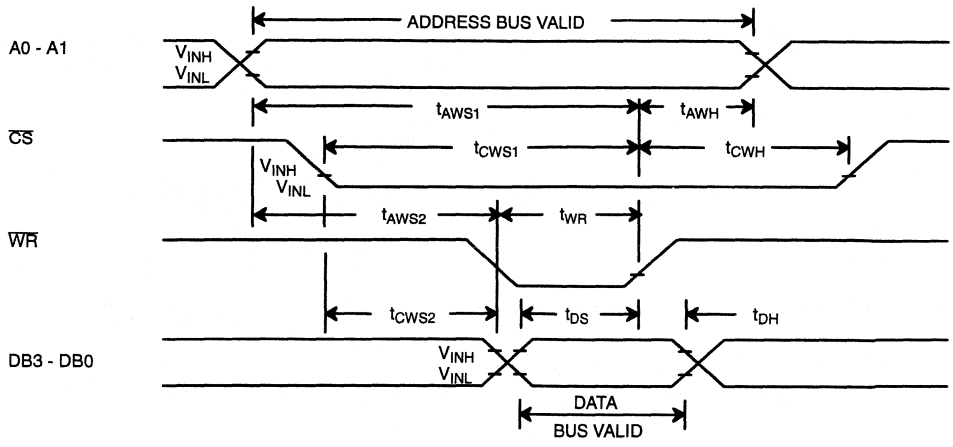


Figure 1. Timing Diagram

4

MP7542 Control Inputs					MP7542 Operation	
A1	A0	CS	WR	CLR		
X	X	X	X	0	Resets DAC 12-bit register to code 0000 0000 0000	
X	X	1	1	1	No operation; device not selected	
0	0	↗	0	1	Load LOW byte data register on edges as shown	Load applicable data register with data at D0 - D3
0	0	0	↗	1		
0	1	↗	0	1	Load MIDDLE byte data register on edges as shown	
0	1	0	↗	1		
1	0	↗	0	1	Load HIGH byte data register on edges as shown	
1	0	0	↗	1		
1	1	0	0	1	Load 12-bit DAC register with data in LOW byte, MIDDLE byte, & HIGH byte data registers	
1	1	0	0	1		

NOTES
1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. ↗ indicates LOW to HIGH transition
5. MSB XXXX XXXX XXXX LSB
   high byte, middle byte, low byte
6. Although positive-going edge of either $\overline{CS}$ or $\overline{WR}$ will load data register, timing is optimized by using $\overline{WR}$ to latch data and using $\overline{CS}$ as a device enable.

Table 1. Truth Table

APPLICATION NOTES
Refer to Section 8 for Applications Information

Interface Logic Information

The MP7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown below. $\overline{CS}$ is the decoded device address, and is derived by decoding the 14 higher order address bits. A0 and A1 are the MP7542 operation address bits, and are decoded internally in the MP7542 to point to the desired loading operation (i.e. load high byte, middle byte, low byte or DAC register). *See Table 1.*

All data loading operations are identical to the write cycle of a RAM.

Additionally, the $\overline{CLR}$ input allows the MP7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the MP7542 in a unipolar mode a CLEAR sets the DAC output to zero scale output. In the bipolar mode a CLEAR causes the DAC output to go to $-V_{REF}$.

In summary:

1. The MP7542 DAC register can be asynchronously cleared with the $\overline{CLR}$ input.
2. Each MP7542 requires only 4 bits of memory.
3. Any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) are accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

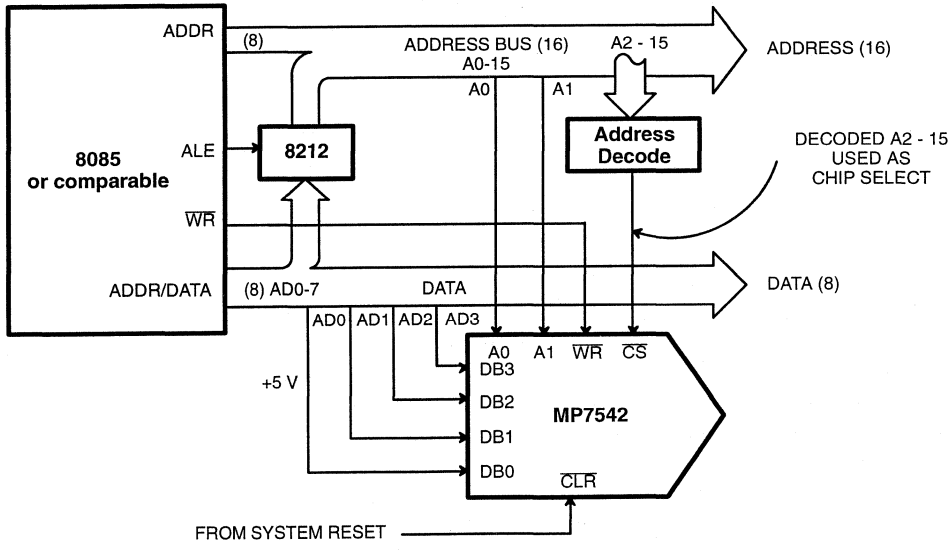


Figure 2. 8085/MP7542 Interface (Memory Mapped Output)

MP7543

5 V CMOS
Serial Input 12-Bit
Digital-to-Analog Converter

FEATURES

- **12-Bit DAC with Serial Digital Input Interface**
- **Nonlinearity ±1/2 LSB from Tmin to Tmax**
- **Lowest Sensitivity to Amplifier V_{OS}**
- **Low Output Capacitance**
- **Full 4-Quadrant Multiplication**
- **Latch-Up Free**
- **Asynchronous CLEAR Input**
- **Serial Load On Positive or Negative Strobes**
- **+5 V Supply Operation**
- **3 V Version: MP75L43**
- **4-Bit Parallel Version: MP7542**

BENEFITS

- **Compatible with Serial Addressing Systems**

4

GENERAL DESCRIPTION

The MP7543 is a precision, 12-bit CMOS 4-quadrant multiplying Digital-to-Analog Converter designed for serial interface applications.

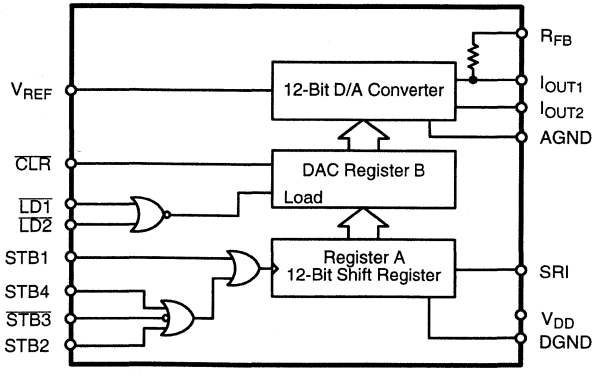
The MP7543 consists of two 12-bit registers, control logic and a 12-bit multiplying D/A converter. The input register (register A) is a 12-bit serial-in parallel-out shift register. Serial data at the SR1 pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input, with the MSB loaded first. Register B is a 12-bit parallel-in parallel-out register that follows register A. The contents of register A are loaded into register B under control of the Load inputs.

A CLEAR input is provided for the asynchronous resetting of register B to all 0's.

The MP7543 is manufactured using an advanced thin film monolithic CMOS fabrication process. A unique decoding technique is utilized yielding excellent accuracy and stability. 12-bit linearity is achieved without laser trimming.

The MP7543 reduces the additional linearity errors due to output amplifier offset to only 330 µV per millivolt of offset - half the value of a standard R-2R CMOS DAC design approach.

SIMPLIFIED BLOCK DIAGRAM



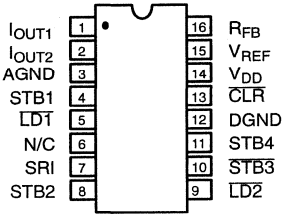
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7543JN	±1	±2	±14.5
Plastic Dip	–40 to +85°C	MP7543KN	±1/2	±1	±14.5
SOIC	–40 to +85°C	MP7543JS	±1	±2	±14.5
SOIC	–40 to +85°C	MP7543KS	±1/2	±1	±14.5
PLCC	–40 to +85°C	MP7543JP	±1	±2	±14.5
PLCC	–40 to +85°C	MP7543KP	±1/2	±1	±14.5
Ceramic Dip	–40 to +85°C	MP7543AD	±1	±2	±14.5
Ceramic Dip	–40 to +85°C	MP7543BD	±1/2	±1	±14.5
Ceramic Dip	–55 to +125°C	MP7543SD*	±1	±2	±14.5
Ceramic Dip	–55 to +125°C	MP7543TD*	±1/2	±1	±14.5

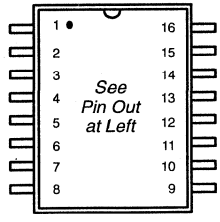
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

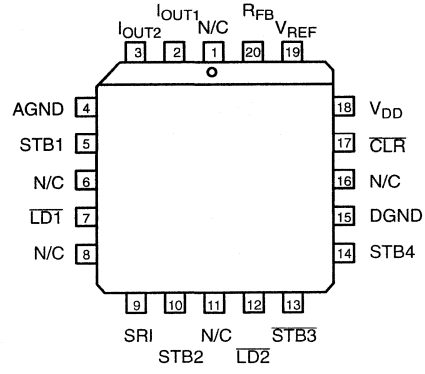
See Packaging Section for Package Dimensions



16 Pin CDIP, PDIP (0.300")
D16, N16



16 Pin SOIC (Jedec, 0.300")
S16



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PDIP, CDIP and SOIC

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	DAC current output pin. Normally terminated at op amp virtual ground.
2	I_{OUT2}	DAC current output pin. Normally terminated at AGND.
3	AGND	Analog Ground.
4	STB1	Register A Strobe 1 input, *See Table 1.*
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
6	N/C	No Connection.
7	SRI	Serial Data Input to Register A.
8	STB2	Register A Strobe 2 input, *See Table 1.*
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
10	$\overline{STB3}$	Register A Strobe 3 input, *See Table 1.*
11	STB4	Register A Strobe 4 input, *See Table 1.*
12	DGND	Digital Ground.
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000.
14	V_{DD}	+5 V Supply Input.
15	V_{REF}	Reference input. Can be positive or negative DC voltage or AC signal.
16	R_{FB}	DAC Feedback Resistor.

PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection.
2	I_{OUT1}	DAC current output pin. Normally terminated at op amp virtual ground.
3	I_{OUT2}	DAC current output pin. Normally terminated at AGND.
4	AGND	Analog Ground.
5	STB1	Register A Strobe 1 input, *See Table 1.*
6	N/C	No Connection.
7	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
8	N/C	No Connection.
9	SR1	Serial Data Input to Register A.
10	STB2	Register A Strobe 2 input, *See Table 1.*
11	N/C	No Connection.
12	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
13	$\overline{STB3}$	Register A Strobe 3 input, *See Table 1.*
14	STB4	Register A Strobe 4 input, *See Table 1.*
15	DGND	Digital Ground.
16	N/C	No Connection.
17	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000.
18	V_{DD}	+5 V Supply Input.
19	V_{REF}	Reference input. Can be positive or negative DC voltage or AC signal.
20	R_{FB}	DAC Feedback Resistor.

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1		±1		
K, B, T				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	Monotonicity:
J, A, S				±2		±2		11 Bits Guaranteed
K, B, T				±1		±1		12 Bits Guaranteed
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, K, B, S, T				±12.3		±14.5		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
J, K, A, B				±10		±10		
S, T				±10		±200		
DYNAMIC PERFORMANCE								
Current Output Settling Time[2]	t_S			2		2	µs	R_L=100Ω, C_L=13pF Full Scale Output Settles to 1/2 LSB of Final Value
AC Feedthrough at I_{OUT1}[2]	F_T			2.5		2.5	mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0			3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			260		260	pF	DAC Inputs all 1's
	C_{OUT1}			100		100	pF	DAC Inputs all 0's
	C_{OUT2}			50		50	pF	DAC Inputs all 1's
	C_{OUT2}			210		210	pF	DAC Inputs all 0's
POWER SUPPLY								
Supply Voltage	V_{DD}	4.75		5.25	4.75	5.25	V	V_{DD} = +5 V ±5% for specified performance
Supply Current	I_{DD}			2.5		2.5	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Serial Input to Strobe Set-up Time	t_{DS1}	50			100		ns	STB1 used as a strobe
Serial Input to Strobe Set-up Time	t_{DS4}	0			0		ns	STB4 used as a strobe
Serial Input to Strobe Set-up Time	t_{DS3}	0			0		ns	$\overline{STB3}$ used as a strobe
Serial Input to Strobe Set-up Time	t_{DS2}	20			40		ns	STB2 used as a strobe
Serial Input to Strobe Hold Time	t_{DH1}	30			60		ns	STB1 used as a strobe
Serial Input to Strobe Hold Time	t_{DH4}	80			160		ns	STB4 used as a strobe
Serial Input to Strobe Hold Time	t_{DH3}	80			160		ns	$\overline{STB3}$ used as a strobe
Serial Input to Strobe Hold Time	t_{DH2}	60			120		ns	STB2 used as a strobe
SRI Data Pulse Width	t_{SRI}	80			160		ns	
STB1 Pulse Width	t_{STB1}	80			160		ns	
STB4 Pulse Width	t_{STB4}	100			200		ns	
$\overline{STB3}$ Pulse Width	t_{STB3}	100			200		ns	
STB2 Pulse Width	t_{STB2}	80			160		ns	
Load Pulse Width	$t_{LD1, 2}$	150			300		ns	
Minimum time between strobing Reg. A and loading Reg. B	t_{ASB}	0			0		ns	
$\overline{CLR}$ pulse width	t_{CLR}	200			400		ns	

NOTES:

1. Full Scale Range (FSR) is 10V for unipolar mode.
2. Guaranteed but not production tested.
3. Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4. See timing diagram.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

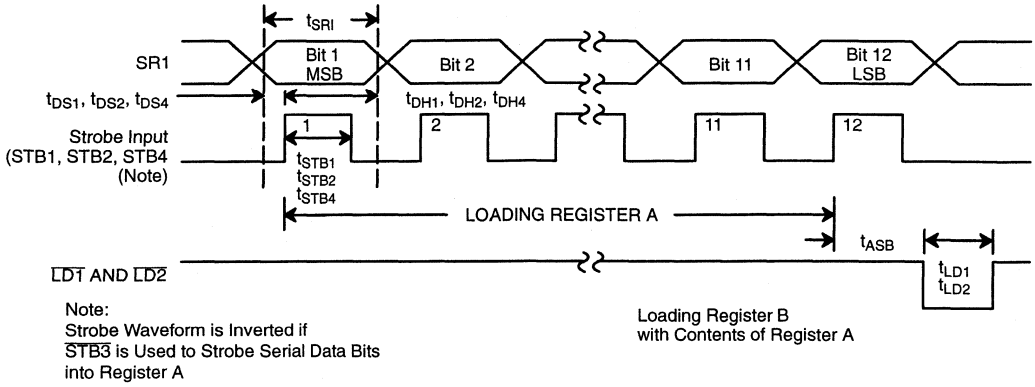
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 700mW
Derates above 75°C ..... 10mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. GND refers to AGND and DGND.

TIMING DIAGRAM



Note:
Strobe Waveform is Inverted if $\overline{STB3}$ is Used to Strobe Serial Data Bits into Register A

Loading Register B with Contents of Register A

MP7543 Logic Inputs							MP7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↑	X	X	X	Data appearing at SRI strobed into Register A	2, 3
0	1	↑	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
0	↓	0	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
↑	1	0	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B to code 0000 0000 0000 (Asynchronous)	1, 3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B with the contents of Register A	3

NOTES
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↑ is positive edge, ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table 1. Truth Table

APPLICATION NOTES

Refer to Section 8 for Applications Information

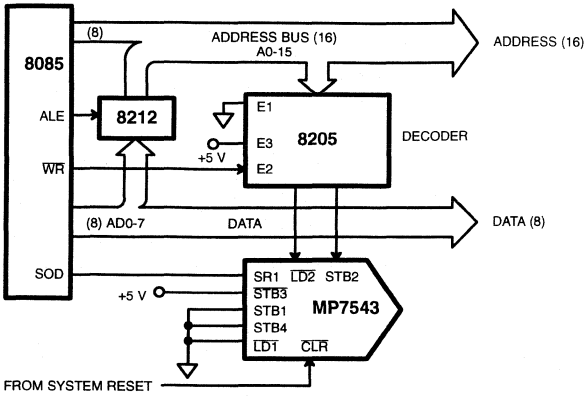


Figure 1. MP7543 8085 Interface

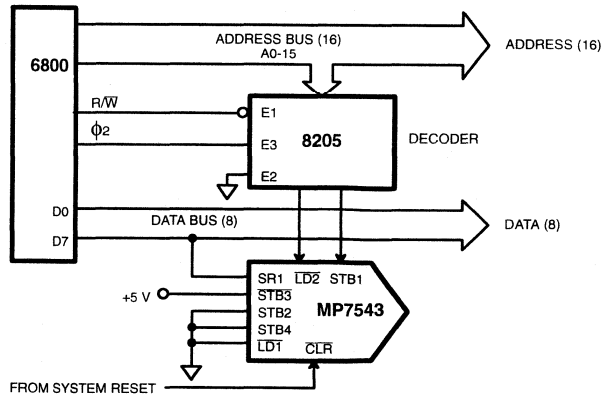


Figure 2. MP7543 MC6800 Interface

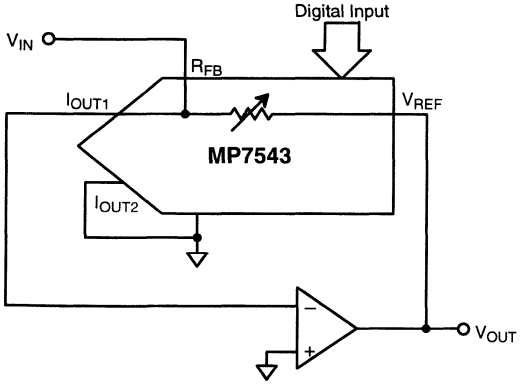
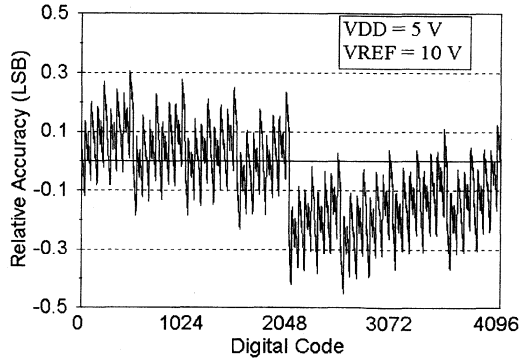


Figure 3. Digitally Programmable Gain Amplifier



Graph 1. Relative Accuracy vs. Digital Code

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MP7545

CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four Quadrant Multiplication**
- **12-Bit Resolution**
- **Gain Error Tempco (2 ppm/C max.)**
- **Latch-Up Free**
- **Single +5 V to +15 V Supply**
- **Use MP7545B for New Designs**
- **TTL/15 V VMOS Compatible**

APPLICATIONS

- **Industrial Automation**
- **Automatic Test Equipment**
- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

4

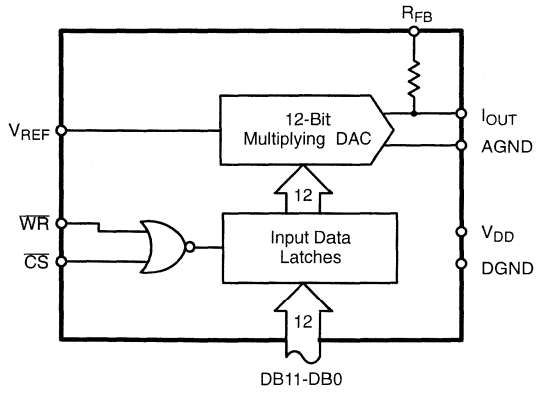
GENERAL DESCRIPTION

The MP7545 is a 12-bit CMOS multiplying Digital-to-Analog Converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The MP7545 is particularly suitable for single supply operation and applications with wide temperature variations.

The MP7545 can be used with any supply voltage from +5 V to +15 V. With CMOS logic levels at the inputs the device dissipates less than 0.5 mW for V_{DD} = +5 V.

SIMPLIFIED BLOCK DIAGRAM



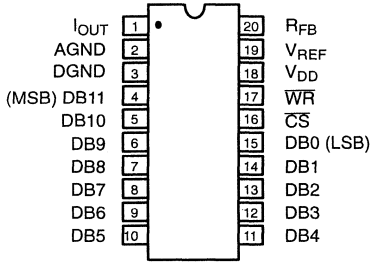
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7545JN	±2	±4	±20
Plastic Dip	–40 to +85°C	MP7545KN	±1	±1	±10
Plastic Dip	–40 to +85°C	MP7545LN	±1/2	±1	±5
SOIC	–40 to +85°C	MP7545JS	±2	±4	±20
SOIC	–40 to +85°C	MP7545KS	±1	±1	±10
SOIC	–40 to +85°C	MP7545LS	±1/2	±1	±5
PLCC	–40 to +85°C	MP7545JP	±2	±4	±20
PLCC	–40 to +85°C	MP7545KP	±1	±1	±10
PLCC	–40 to +85°C	MP7545LP	±1/2	±1	±5
Ceramic Dip	–40 to +85°C	MP7545AD	±2	±4	±20
Ceramic Dip	–40 to +85°C	MP7545BD	±1	±1	±10
Ceramic Dip	–40 to +85°C	MP7545CD	±1/2	±1	±5
Ceramic Dip	–55 to +125°C	MP7545SD*	±2	±4	±20
Ceramic Dip	–55 to +125°C	MP7545TD*	±1	±1	±10

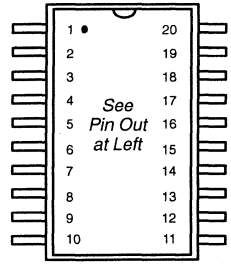
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

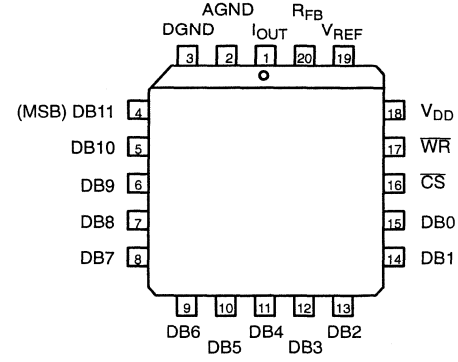
See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	$\overline{WR}$	Write (Active Low)
18	V_{DD}	Digital Supply Voltage
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
J, A, S				±4		±4		
K, B, T				±1		±1		
L, C				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±20		±20		
K, B, T				±10		±10		
L, C				±5		±5		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
J, K, L				±10		±50		
A, B, C				±10		±50		
S, T				±10		±200		
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			2		2	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20 Vp-p sinewave.
Propagation Delay	t_{PD}			300			ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			5		5	pF	
Control	C_{IN}			20		20	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}			200		200	pF	DAC Inputs all 1's
	C_{OUT}			70		70	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	280	200		380	270 typ	ns	
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}	140	100		210	150 typ	ns	
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}	250	175		400	280 typ	ns	

4

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
J, A, S				±4		±4		
K, B, T				±1		±1		
L, C				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±25		±25		
K, B, T				±15		±15		
L, C				±10		±10		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
J, K, L				±10		±50		
A, B, C				±10		±50		
S, T				±10		±200		
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			2		2	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20 Vp-p sinewave.
Glitch Energy	Egl		250				nVs	V_{REF} = AGND
Propagation Delay	t_{PD}			250			ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	13.5			13.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance[2]								
DB0-DB11	C_{IN}			5		5	pF	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	C_{IN}			20		20	pF	V_{IN} = 0

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}			200		200	pF	DAC Inputs all 1's
	C_{OUT}			70		70	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	180	120		200	150 typ	ns	
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}	90	60		120	80 typ	ns	
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}	160	100		240	170 typ	ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V
AGND to DGND ..... ±0.5 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

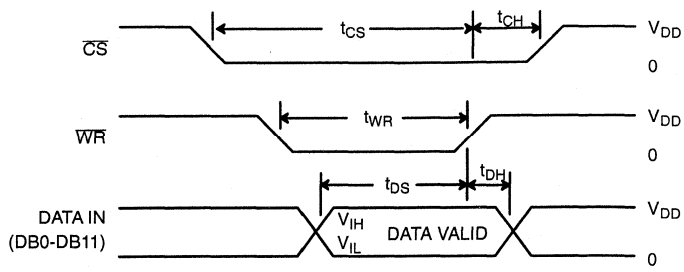


Figure 1. Write Cycle Timing Diagram

APPLICATION NOTES
Refer to Section 8 for Applications Information

Digital Section

Figure 2. shows the digital structure for one bit.

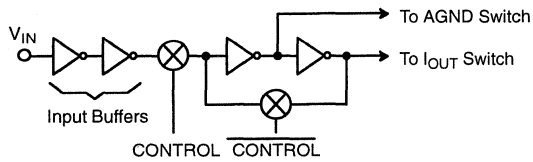


Figure 2. Digital Input Structure

The digital signals CONTROL and $\overline{CONTROL}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the MP7545 is operated with V_{DD} = 5 V, the buffers convert TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 2.0 V to 3.5 V, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The MP7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15 V the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V.

MICROPROCESSOR INTERFACING OF THE MP7545

The MP7545 can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in *Figure 3.* This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

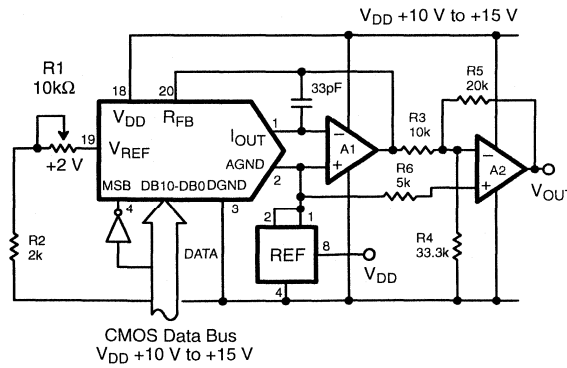


Figure 3. Single Supply "Bipolar" 2's Complement D/A Converter

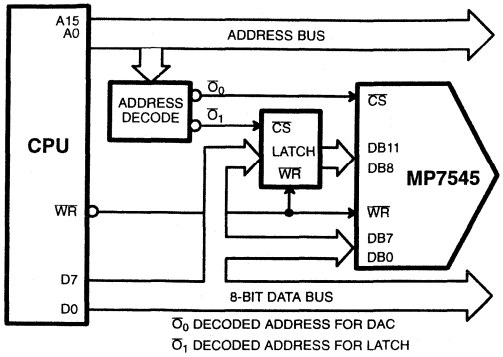


Figure 4. 8-Bit Processor to MP7545 Interface

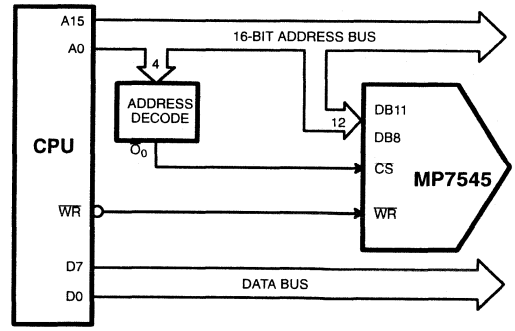
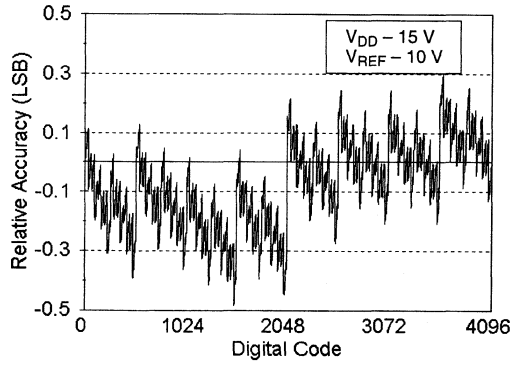


Figure 5. Connecting the MP7545 to 8-Bit Processors via the Address Bus

Figure 4. shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each MP7545 connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.



Graph 1. Relative Accuracy vs. Digital Code

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MP7545B

CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four Quadrant Multiplication**
- **12-Bit Resolution**
- **Gain Error Tempco (2 ppm/°C max.)**
- **Latch-Up Free**
- **Single +5 V to +15 V Supply**
- **TTL/15 V CMOS Compatible**
- **Rugged 2000 V ESD Protection**
- **3 V Version: MP75L45**
- **TTL/5 V VMOS Version: MP7645B**

APPLICATIONS

- **Industrial Automation**
- **Automatic Test Equipment**
- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

4

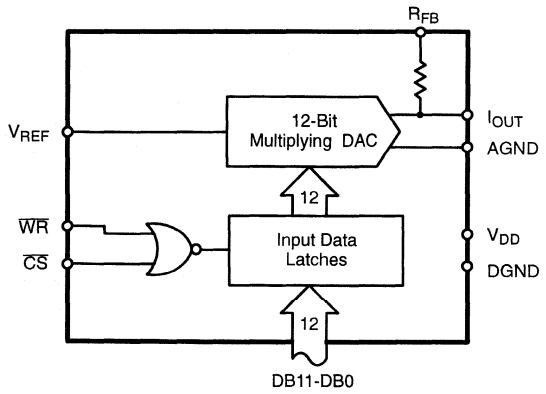
GENERAL DESCRIPTION

The MP7545B is a 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The MP7545B is particularly suitable for single supply operation and applications with wide temperature variations.

The MP7545B can be used with any supply voltage from +5 V to +15 V. With CMOS logic levels at the inputs the device dissipates less than 0.5 mW for V_{DD} = +5 V.

SIMPLIFIED BLOCK DIAGRAM

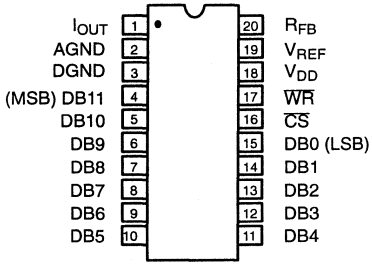


ORDERING INFORMATION

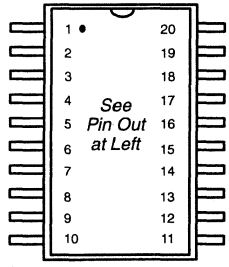
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7545BKN	±1	±1	±3
Plastic Dip	–40 to +85°C	MP7545BLN	±1/2	±1	±2
SOIC	–40 to +85°C	MP7545BKS	±1	±1	±3
SOIC	–40 to +85°C	MP7545BLS	±1/2	±1	±2
PLCC	–40 to +85°C	MP7545BKP	±1	±1	±3
PLCC	–40 to +85°C	MP7545BLP	±1/2	±1	±2

PIN CONFIGURATIONS

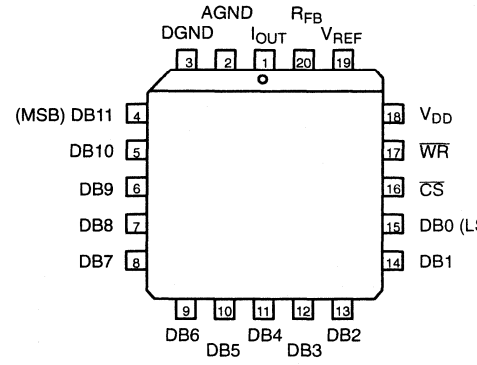
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5

PIN NO.	NAME	DESCRIPTION
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	$\overline{WR}$	Write (Active Low)
18	V_{DD}	Digital Supply Voltage
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistor

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K				±1		±1		
L				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
K				±1		±1		
L				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
K				±3		±4		
L				±2		±3		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
K, L				±10		±50		
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			1		1	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20 Vp-p sinewave.
Propagation Delay	t_{PD}		50				ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			5		5	pF	
Control	C_{IN}			20		20	pF	
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}		100				pF	DAC Inputs all 1's
	C_{OUT}		50				pF	DAC Inputs all 0's

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	100					ns	
Chip Select to Write Hold Time	t_{CH}	0					ns	
Data Valid to Write Set-Up Time	t_{DS}	100					ns	
Data Valid to Write Hold Time	t_{DH}	10					ns	
Write Pulse Width	t_{WR}	100					ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K				±1		±1		
L				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
K				±1		±1		
L				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
K				±6		±7		
L				±5		±6		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
K, L				±10		±50		
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			1		1	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20 Vp-p sinewave.
Propagation Delay	t_{PD}		50				ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	13.5			13.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance[2]								
DB0-DB11	C_{IN}			5		5	pF	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	C_{IN}			20		20	pF	V_{IN} = 0
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}		100				pF	DAC Inputs all 1's
	C_{OUT}		50				pF	DAC Inputs all 0's

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	75					ns	
Chip Select to Write Hold Time	t_{CH}	0					ns	
Data Valid to Write Set-Up Time	t_{DS}	100					ns	
Data Valid to Write Hold Time	t_{DH}	10					ns	
Write Pulse Width	t_{WR}	75					ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode and ±10V for bipolar.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

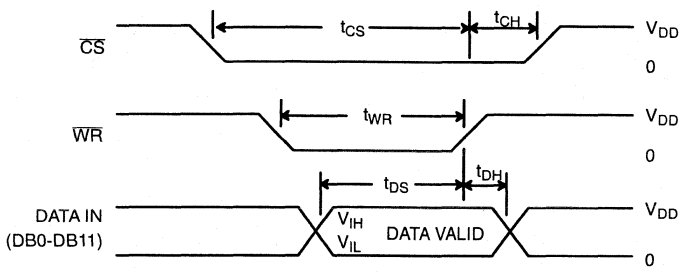
V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
AGND to DGND ..... ±0.5 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC, PLCC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

WRITE CYCLE TIMING DIAGRAM



APPLICATION NOTES

Refer to Section 8 for Applications Information

Digital Section

Figure 2. shows the digital structure for one bit.

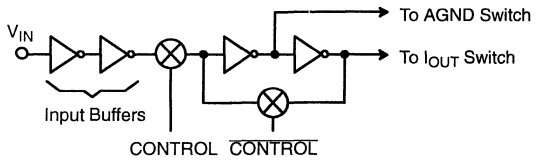


Figure 1. Digital Input Structure

The digital signals CONTROL and $\overline{CONTROL}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the MP7545B is operated with V_{DD} = 5 V, the buffers convert TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The MP7545B may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15 V the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V.

MICROPROCESSOR INTERFACING OF THE MP7545B

The MP7545B can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in *Figure 3.* This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

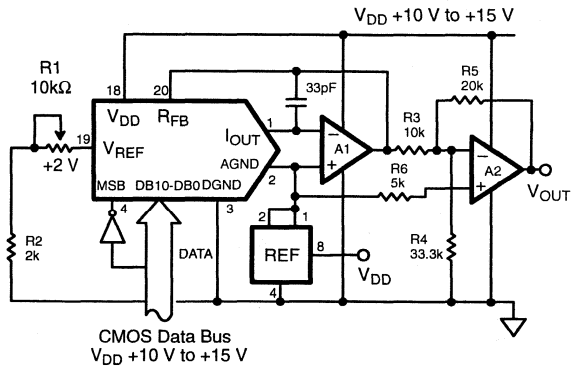


Figure 2. Single Supply "Bipolar" 2's Complement D/A Converter

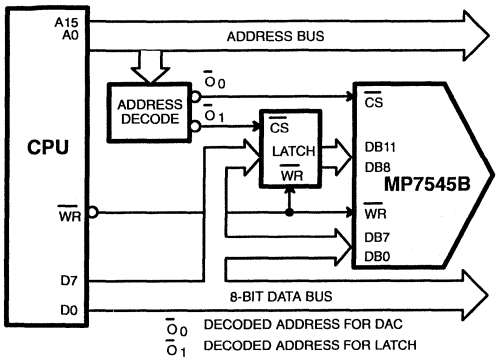


Figure 3. 8-Bit Processor to MP7545B Interface

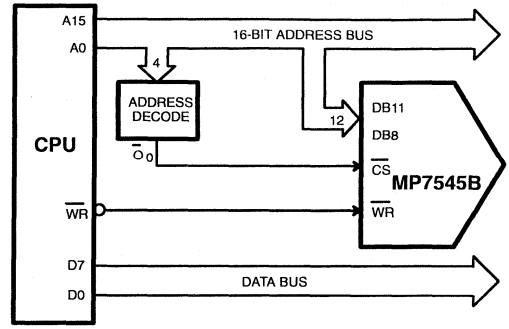
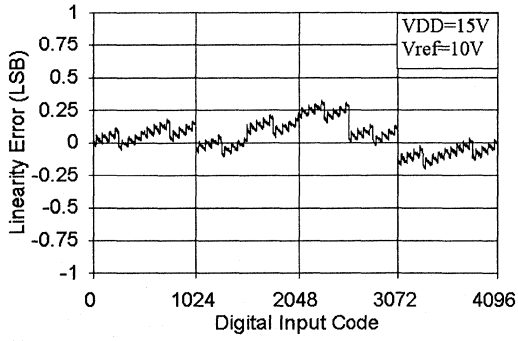


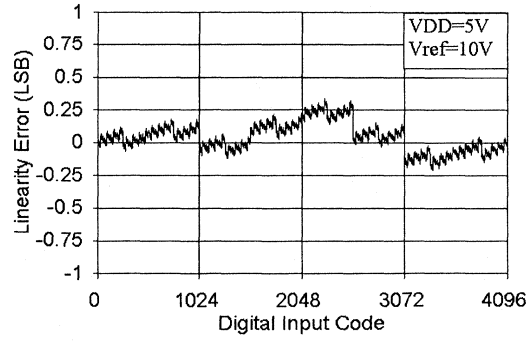
Figure 4. Connecting the MP7545B to 8-Bit Processors via the Address Bus

Figure 4. shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bush such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each MP7545B connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

PERFORMANCE CHARACTERISTICS



Graph 1. Linearity Error vs. Digital Input Code



Graph 2. Linearity Error vs. Digital Input Code

APPLICATION NOTES

Refer to Section 8 for Applications Information

MP7610

Octal 14-Bit DAC Array™ D/A Converter with Output Amplifier and Serial Data/Address µP Control Logic

FEATURES

- **Eight Independent 14-Bit DACs with Output Amplifiers**
- **Low Power 320 mW (typ.)**
- **Serial Digital Data and Address Port (3-Wire Standard)**
- **14-Bit Resolution, 12-Bit Accuracy**
- **Extremely Well Matched DACs**
- **Extremely Low Analog Ground Current (<60µA/Channel)**
- **±10 V Output Swing with ±11.4 V Supplies**
- **Zero Volt Output Preset (Data = 10 .. 00)**
- **Rugged Construction – Latch-Up Free**
- **Parallel Version: MP7611**

APPLICATIONS

- **Data Acquisition Systems**
- **ATE**
- **Process Control**
- **Self-Diagnostic Systems**
- **Logic Analyzers**
- **Digital Storage Scopes**
- **PC Based Controller/DAS**

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GENERAL DESCRIPTION

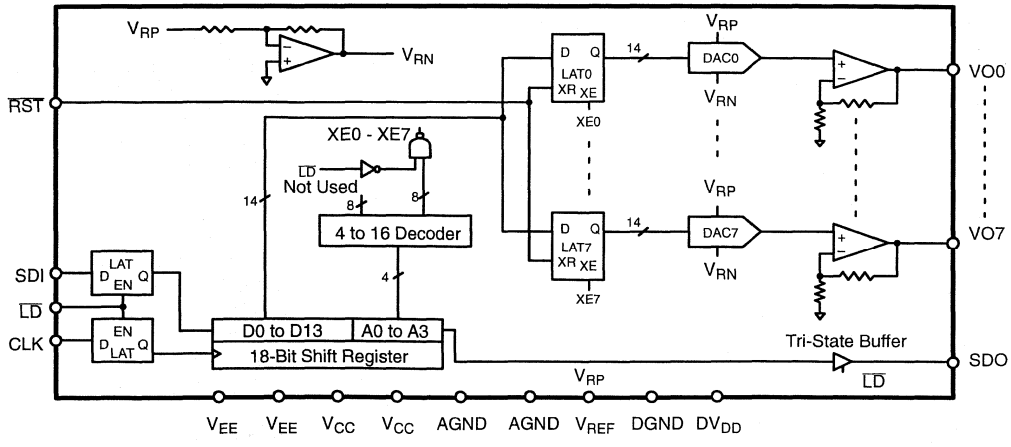
The MP7610 provides eight independent 14-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a 3-wire standard serial digital address and data port.

Typical DAC matching for C grade versions is 1.5 LSB across all codes. Accuracy of ±2 LSB for DNL and ±2 LSB for INL is also achieved for C grade. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30µs (typ.).

The MP7610 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board space.

Built using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR's patented thin-film resistor process which exhibits excellent long term stability and reliability.

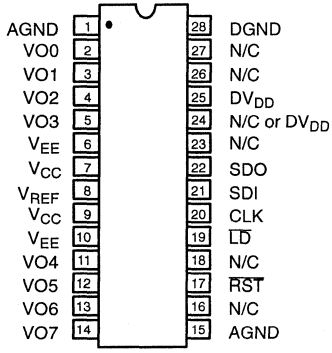
SIMPLIFIED BLOCK DIAGRAM



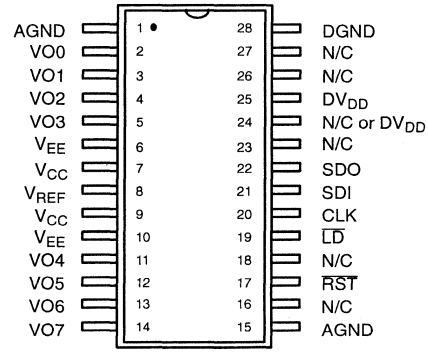
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PDIP	–40 to +85°C	MP7610BN	14	±4	±3	±24
PDIP	–40 to +85°C	MP7610AN	14	±8	±4	±32
SOIC	–40 to +85°C	MP7610BS	14	±4	±3	±24
SOIC	–40 to +85°C	MP7610AS	14	±8	±4	±32

PIN CONFIGURATIONS



28 Pin PDIP (0.400")
NW28



28 Pin SOIC (Jedec, 0.346")
SW28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	VO0	DAC 0 Output
3	VO1	DAC 1 Output
4	VO2	DAC 2 Output
5	VO3	DAC 3 Output
6	V_{EE}	Analog Negative Power Supply (–12 V)
7	V_{CC}	Analog Positive Power Supply (+12 V)
8	V_{REF}	Voltage Reference Input (+5 V)
9	V_{CC}	Analog Positive Power Supply (+12 V)
10	V_{EE}	Analog Negative Power Supply (–12 V)
11	VO4	DAC 4 Output
12	VO5	DAC 5 Output
13	VO6	DAC 6 Output
14	VO7	DAC 7 Output

PIN NO.	NAME	DESCRIPTION
15	AGND	Analog Ground
16	N/C	No Connection
17	$\overline{RST}$	Reset all DACs to 0 V Output
18	N/C	No Connection
19	$\overline{LD}$	Load Signal; Load Data to Selected DAC
20	CLK	Serial Data Clock
21	SDI	Serial Data Input
22	SDO	Shift Register Serial Output
23	N/C	No Connection
24	N/C	No Connection or DV_{DD}
25	DV_{DD}	Digital Positive Power Supply (+5 V)
26	N/C	No Connection
27	N/C	No Connection
28	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = −12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	14					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				±8		±8		
B				±4		±4		
Differential Non-Linearity	DNL						LSB	
A				±4		±4		
B				±3		±3		
Positive Full Scale Error	+FSE						LSB	
A			24	±32		±32		
B			16	±24		±24		
Negative Full Scale Error	−FSE						LSB	
A			24	±32		±32		
B			16	±24		±24		
Bipolar Zero Offset	ZOFS						LSB	
A				±16		±16		
B				±12		±12		
INL Matching	ΔINL						LSB	
A				±8		±8		
B				±6		±6		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				±16		±16		
B				±8		±8		
Bipolar Zero Matching	ΔZOFS						LSB	
A				±16		±16		
B				±12		±12		
Full Scale Error Matching	ΔFSE						LSB	
A				±16		±16		
B				±12		±12		
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µs	ZS to FS (20 V Step) 5k, 50pF load
Channel-to-Channel Crosstalk[6]	CT		0.04				LSB	DC
Digital Feedthrough[1, 6]	Q		−70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR			5			ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS

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ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for Driving the reference input
V_{REF} Voltage1, [2]	V_{REF}	3.5		6			V	
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4	V_{CC} −1.4				V	
Output Drive Current		−5		5			mA	
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	−FS to AGND
			55				mA	−FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	−12.75	−12	−5	−12.75	−5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10		10	mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20		20	mA	Bipolar zero
Digital Supply Current	I_{DD}			2		2	mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0, V_{IH} = 5.0, C_L = 20 pF
Input Clock Pulse Width	t_{CH}, t_{CL}	35					ns	
Data Setup Time	t_{DS}	15					ns	
Data Hold Time	t_{DH}	15					ns	
CLK to SDO Propagation Delay	t_{PD}			40			ns	
DAC Register Load Pulse Width	t_{LD}	35					ns	
Preset Pulse Width	t_{PR}	50					ns	
Clock Edge to Load Time	t_{CKLD1}	140					ns	Note: t_{LD} and t_{CKLD2} cannot both be min. since t_{CKLD1}=t_{CKLD2}+t_{LD}
	t_{CKLD2}	0						
$\overline{LD}$ Falling Edge to SDO Tri-state Enable	t_{HZ1}	50					ns	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL TIMING SPECIFICATIONS[1, 4] (CONT'D)								
$\overline{LD}$ Rising Edge to SDO Tri-state Disable	t_{HZ2}	50					ns	
$\overline{LD}$ Rising Edge to CLK Enable	t_{LDCK}	50					ns	
$\overline{LD}$ Set-up Time with Respect to CLK	t_{LDSU}	30					ns	

NOTES:

1 Guaranteed; not tested.
2 Specified values guarantee functionality.
3 Digital inputs should not go below digital GND or exceed DV_{DD} supply voltage.
4 *See Figures 2 and 3.* All digital input signals are specified with $t_R = t_F = 10$ ns 10% to 90% and timed from a 50% voltage level.
5 For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.
6 Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

4

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... +16.5 V
V_{EE} to AGND ..... –16.5 V
DV_{DD} to DGND ..... +6.5 V
V_{REF} to DGND ..... +7.0 V
AGND to DGND ..... ±1 V
(Functionality guaranteed for ±0.5 V only)
Digital Input & Output Voltage to DGND –0.5 to DV_{DD} +0.5V
Analog Inputs & Outputs ..... Indefinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND, DGND (provided that power dissipation of the package spec is not exceeded)

Operating Temperature Range
Extended Industrial ..... –40°C to +85°C
Maximum Junction Temperature ..... –65°C to 150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP 1150mW
Derates above 75°C ..... 15mW/°C

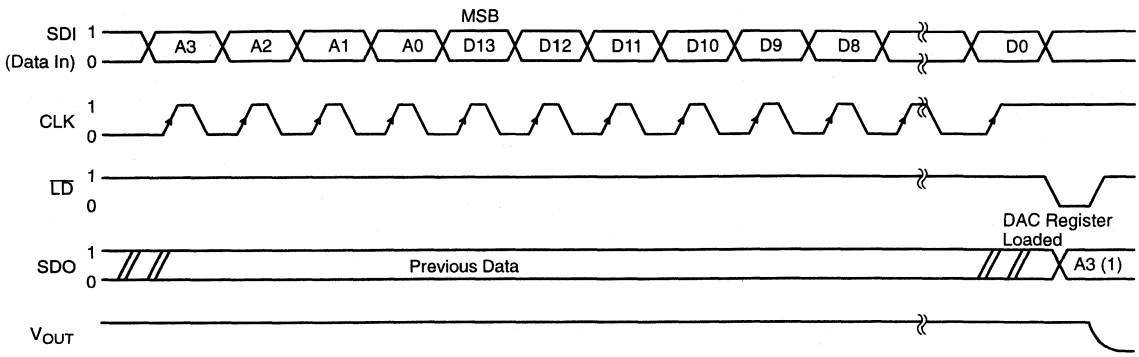
NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

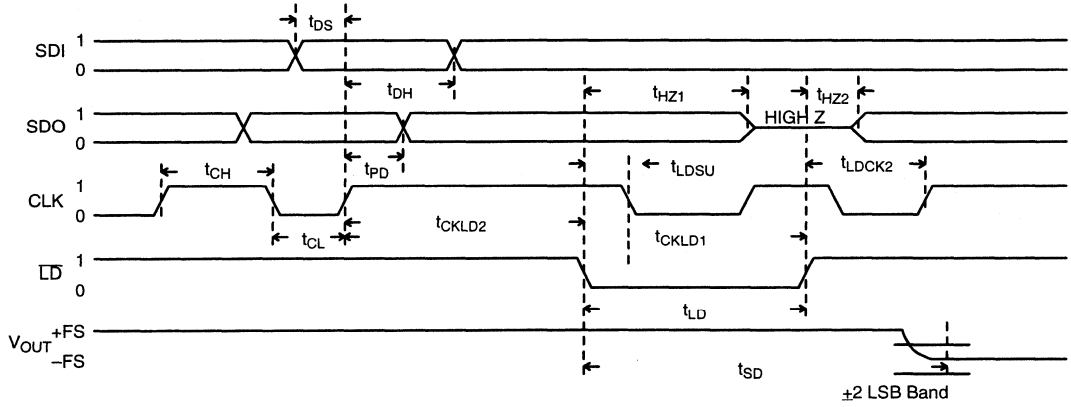
Refer to Section 8 for Applications Information

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.



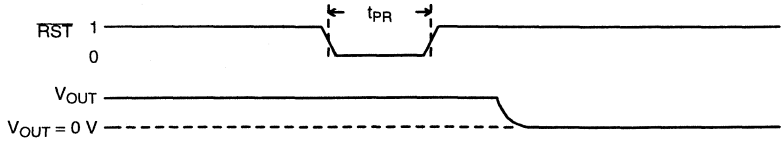
Note: (1) Because A3 is available immediately after 18th clock edge of DATA Shift-in, only 17 clock cycles are needed to complete the readback.

Figure 1. Serial Data Timing and Loading



Note: (1) CLK should be high during the falling edge of $\overline{LD}$ to insure proper function of the shift register.

Figure 2. Serial Data Input Timing ($\overline{RST}$ = "1")



Note: Reset settling time is $\leq t_{SD}$

Figure 3. Reset Operation

The MP7610 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board wire (space). If the $\overline{LD}$ signal is high, the CLK signal loads the digital input bits (SDI) into the shift register (4 bits address A3 to A0 plus 14 bits data D13 to D0 for the MP7610). The $\overline{LD}$ signal going low loads the data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data (SDI), output (SDO tri-stated) and the CLK input. This design tremendously reduces digital noise and glitch transients into the DACs due to free running CLK and SDI. Note also that the preset signal ($\overline{RST}$) resets all analog outputs to 0 volt regardless of digital inputs.

Function	A3	A2	A1	A0	$\overline{LD}$	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	0→1 Repeat	1	Data Input Valid	Data Output Valid
Stop Shifting Data In and Out	X	X	X	X	0	X	1	X	Hi-Z
Load DACs	0	0	0	0	No Operation				
DAC 0	0	0	0	1	1→0	X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0	X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0	X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0	X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0	X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0	X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0	X	1	X	Hi-Z
⋮	⋮	⋮	⋮	⋮	No Operation	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	1	1	1	0	No Operation	X	1	X	Hi-Z
⋮	1	1	1	1	No Operation	X	1	X	Hi-Z
Reset all DACs to 0 V	X	X	X	X	X	X	0	X	X

Table 1. Digital Function Truth Table
Serial In/Serial Out

Note: For timing information See Electrical Characteristics.

Hex Code	Binary Code	Output Voltage = 2 • Vr $(-1 + \frac{2 \bullet D}{16384})$ (Vr = +5 V)
0 0 0 0	00000000000000	$10 \bullet (-1 + 0) = -10$
⋮	⋮	⋮
1 F F F	01111111111111	$10 \bullet (-1 + \frac{16382}{16384}) = -1.22$ mV
2 0 0 0	10000000000000	$10 \bullet (-1 + \frac{16384}{16384}) = 0$
2 0 0 1	10000000000001	$10 \bullet (-1 + \frac{16386}{16384}) = 1.22$ mV
⋮	⋮	⋮
3 F F F	11111111111111	$10 \bullet (-1 + \frac{32766}{16384}) = 9.99878$

Table 2. MP7610
Ideal DAC Output vs. Input Code

Note: See Electrical Characteristics for real system accuracy

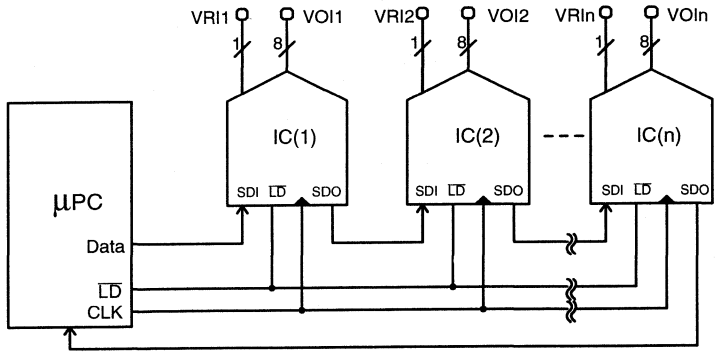


Figure 4. Simplified Diagram

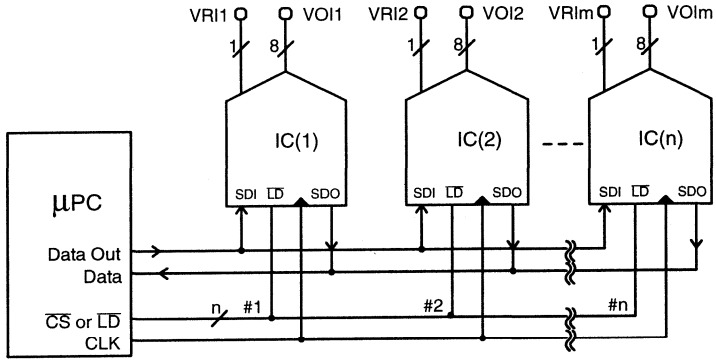


Figure 5. Simplified Diagram

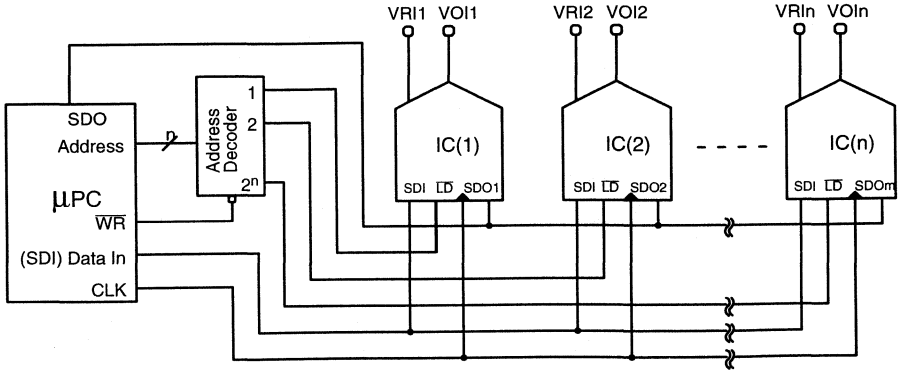
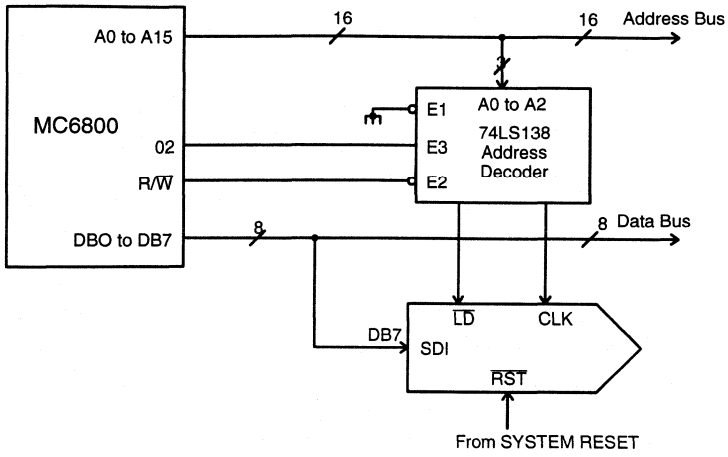
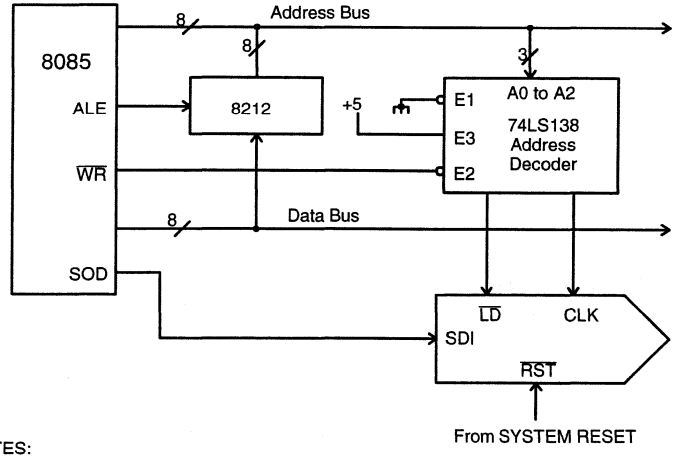


Figure 6. Simplified Diagram



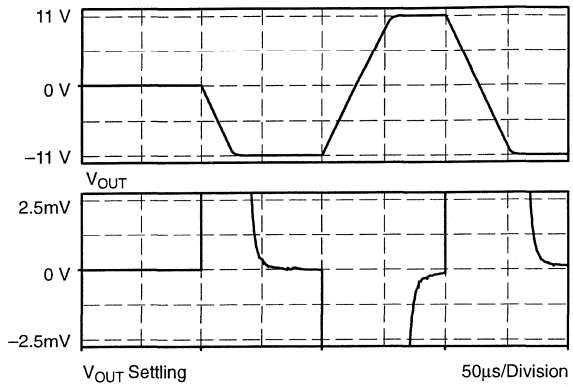
NOTES
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit.
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE to memory location 2000, R/W, and 02. A WRITE to address 4000 transfers data from input shift register to DAC register.

Figure 7. MC6800 Interface



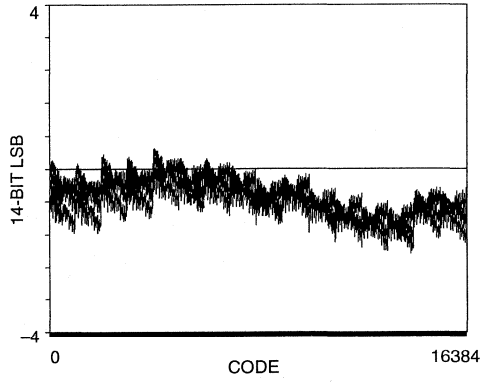
NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000.
2. Data is clocked in the DAC shift register by executing memory write instructions. The clock input is generated by decoding address 8000 and WR. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

Figure 8. 8085 Interface

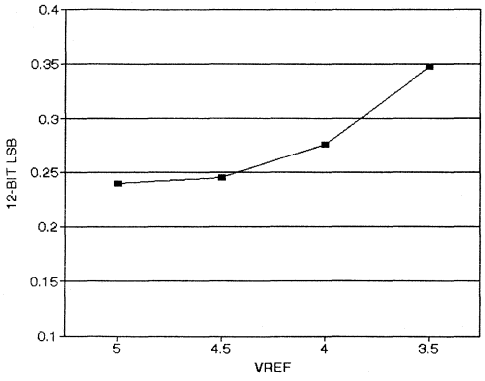


Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

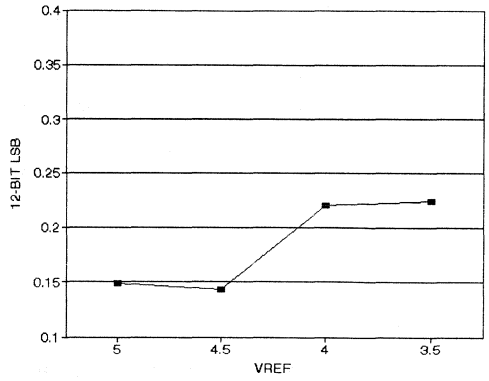
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



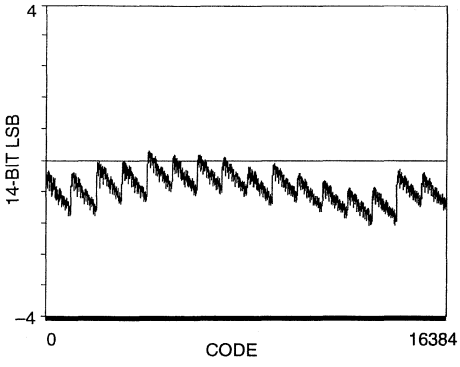
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes



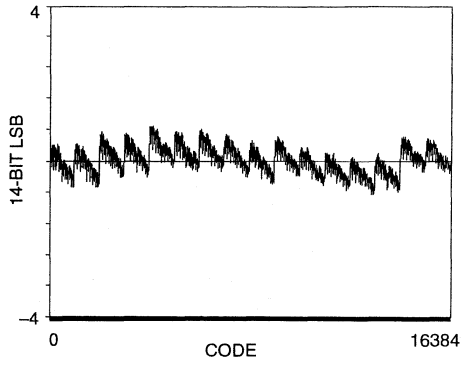
Graph 3. DAC 0 INL vs. V_{REF}



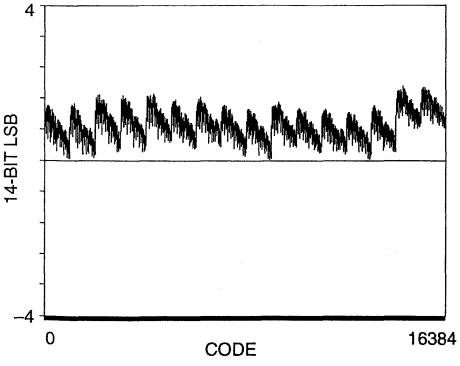
Graph 4. DAC 0 DNL vs. V_{REF}



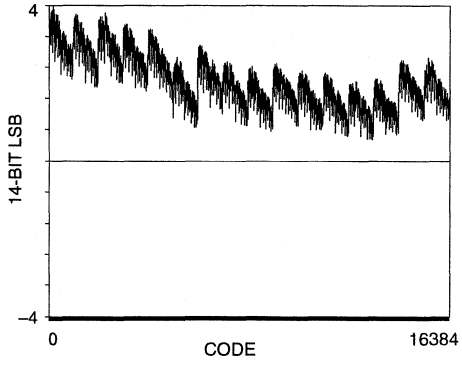
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

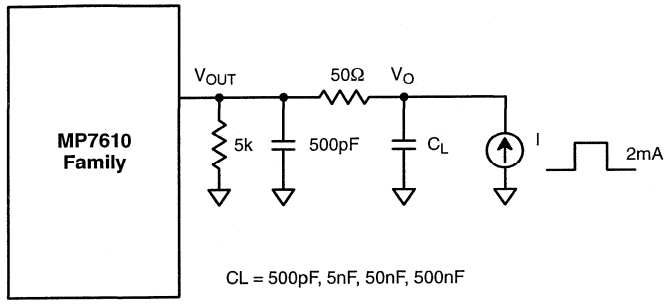
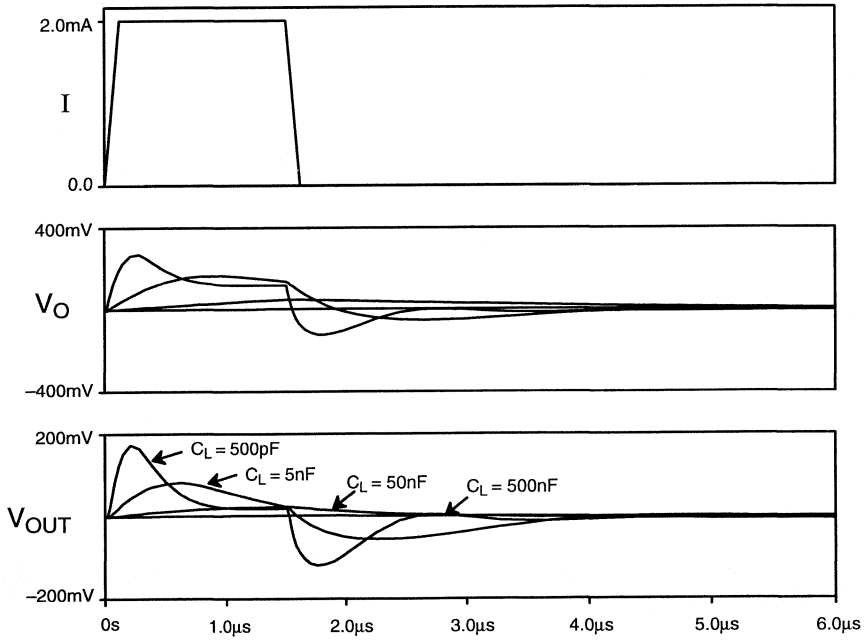


Figure 9. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF (*See Figure 9. above*)

MP7611

Octal 14-Bit DAC Array™ D/A Converter with Output Amplifier and Parallel Data/Address µP Control Logic

FEATURES

- **Eight Independent Channel 14-Bit DACs with Output Amplifiers**
- **Low Power 320 mW (typ.)**
- **Parallel Digital Data and Address Port**
- **Double Buffered Data Interface**
- **Readback of DAC Latches**
- **Zero Volt Output Preset (Data = 10 .. 00)**
- **14-Bit Resolution, 12-Bit Accuracy**
- **Extremely Well Matched DACs**
- **Extremely Low Analog Ground Current (<60µA/Channel)**
- **±10 V Output Swing with ±11.4 V Supplies**
- **Rugged Construction – Latch-Up Free**
- **Serial Version: MP7610**

APPLICATIONS

- **Data Acquisition Systems**
- **ATE**
- **Process Control**
- **Self-Diagnostic Systems**
- **Logic Analyzers**
- **Digital Storage Scopes**
- **PC Based Controller/DAS**

4

GENERAL DESCRIPTION

The MP7611 provides eight independent 14-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a parallel digital address and data port.

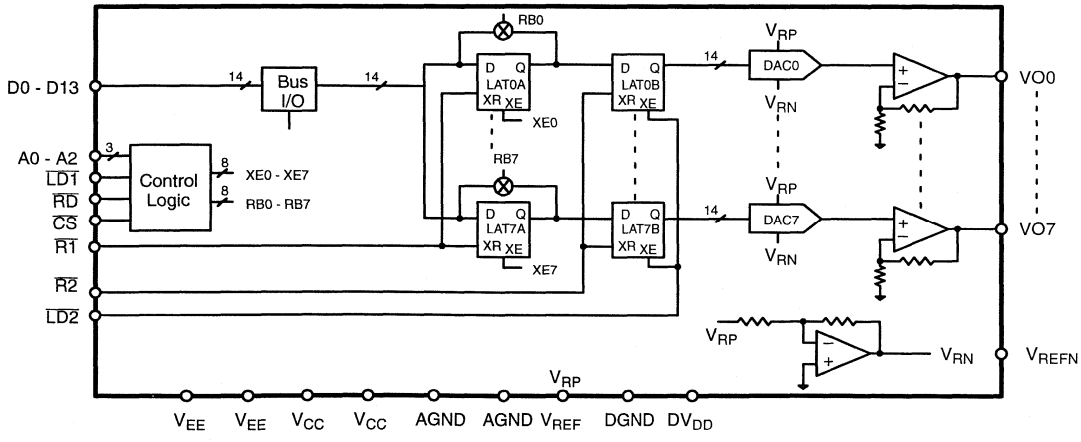
Built using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR's patented thin-film resistor process which exhibits excellent long term stability and reliability.

A standard µ-processor and TTL/CMOS compatible 14-bit input data port loads the data into the pre-selected DACS.

This device can easily be interfaced to a data bus, and digital readback of each channel is available.

Typical DAC matching for C grade versions is 1.5 LSB across all codes. Accuracy of ±2 LSB for DNL and ±2 LSB for INL is also achieved for C grades. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30µs (typ.).

SIMPLIFIED BLOCK DIAGRAM

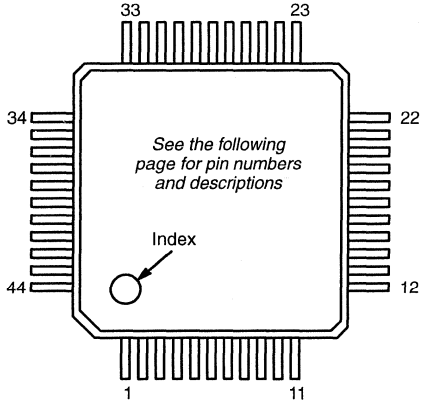


ORDERING INFORMATION

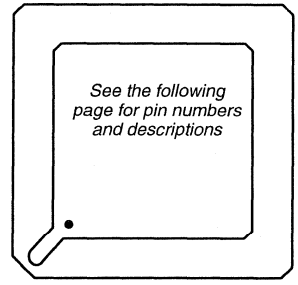
Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PQFP	–40 to +85°C	MP7611BE	14	±4	±3	±24
PQFP	–40 to +85°C	MP7611AE	14	±8	±4	±32
PGA	–40 to +85°C	MP7611BG	14	±4	±3	±24
PGA	–40 to +85°C	MP7611AG	14	±8	±4	±32
PGA	–55 to +125°C	MP7611SG	14	±8	±4	±32
PLCC	–40 to +85°C	MP7611BP	14	±4	±3	±24
PLCC	–40 to +85°C	MP7611AP	14	±8	±4	±32

PIN CONFIGURATIONS

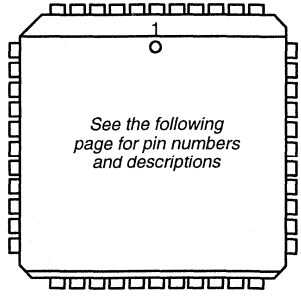
See Packaging Section for Package Dimensions



44-Pin PQFP (14 mm x 14 mm)
Q44



44-Pin PGA
G44



44-Pin PLCC
P44

PIN OUT DEFINITIONS

PLCC PIN NO.	PQFP & PGA PIN NO.	NAME	DESCRIPTION
29	1	N/C	No Connection
30	2	VO3	DAC 3 Output
31	3	VEE	Analog Negative Power Supply (–12 V)
32	4	VCC	Analog Positive Power Supply (+12 V)
33	5	N/C	No Connection or DV_{DD}
34	6	VREF	Analog Voltage Reference Input (+5 V)
35	7	VREFN	Analog Negative Voltage Reference Output (–2.5 V)
36	8	VCC	Analog Positive Power Supply (+12 V)
37	9	VEE	Analog Negative Power Supply (–12 V)
38	10	VO4	DAC 4 Output
39	11	N/C	No Connection
40	12	VO5	DAC 5 Output
41	13	VO6	DAC 6 Output
42	14	VO7	DAC 7 Output
43	15	AGND	Analog Ground (0 V)
44	16	$\overline{CS}$	Chip Select Enable
1	17	$\overline{RD}$	Read Back Enable
2	18	$\overline{R2}$	Second–Latch-Bank Reset Enable
3	19	$\overline{R1}$	First–Latch-Bank Reset Enable
4	20	$\overline{LD2}$	Second–Latch-Bank Load Enable
5	21	$\overline{LD1}$	First–Latch-Bank Load Enable
6	22	A2	Digital Address Bit 2
7	23	A1	Digital Address Bit 1
8	24	A0	Digital Address Bit 0
9	25	DB0	Digital Input Data Bit 0
10	26	DB1	Digital Input Data Bit 1
11	27	DB2	Digital Input Data Bit 2
12	28	DB3	Digital Input Data Bit 3
13	29	DB4	Digital Input Data Bit 4
14	30	DB5	Digital Input Data Bit 5
15	31	DB6	Digital Input Data Bit 6
16	32	DB7	Digital Input Data Bit 7
17	33	DB8	Digital Input Data Bit 8
18	34	DB9	Digital Input Data Bit 9
19	35	DB10	Digital Input Data Bit 10
20	36	DB11	Digital Input Data Bit 11
21	37	DB12	Digital Input Data Bit 12
22	38	DB13	Digital Input Data Bit 13 (MSB)
23	39	DVDD	Digital Positive Power Supply (+5 V)
24	40	DGND	Digital Ground (0 V)
25	41	AGND	Analog Ground (0 V)
26	42	VO0	DAC 0 Output
27	43	VO1	DAC 1 Output
28	44	VO2	DAC 2 Output

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = –12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	14					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A, S				±8		±8		
B				±4		±4		
Differential Non-Linearity	DNL						LSB	
A, S				±4		±4		
B				±3		±3		
Positive Full Scale Error	+FSE						LSB	
A, S			24	±32		±32		
B			16	±24		±24		
Negative Full Scale Error	–FSE						LSB	
A, S			24	±32		±32		
B			16	±24		±24		
Bipolar Zero Offset	ZOFS						LSB	
A, S				±16		±16		
B				±12		±12		
INL Matching	ΔINL						LSB	
A, S				±8		±8		
B				±6		±6		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A, S				±16		±16		
B				±8		±8		
Bipolar Zero Matching	ΔZOFS						LSB	
A, S				±16		±16		
B				±12		±12		
Full Scale Error Matching	ΔFSE						LSB	
A, S				±16		±16		
B				±12		±12		
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µs	ZS to FS (20 V Step) 5k, 50pF load
Channel-to-Channel Crosstalk[6]	CT		0.04				LSB	DC
Digital Feedthrough[1, 6]	Q		–70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR		5				ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for driving the reference input
V_{REF} Voltage[1, 2]	V_{REF}	3.5		6			V	
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4	V_{CC} −1.4				V	
Output Drive Current		−5		5			mA	
V_{REFN} Output Drive Current		−10		+10			µA	For test purposes only
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	−FS to AGND
			55				mA	−FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	−12.75	−12	−5	−12.75	−5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10		10	mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20		20	mA	Bipolar zero
Digital Supply Current	I_{DD}			2		2	mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0 V, V_{IH} = 5 V, C_L = 20 pF
Data Setup Time	t_{DS}	20					ns	
Data Hold Time	t_{DH}	20					ns	
Address Set-up Time	t_{AS}	100					ns	
Address Hold Time	t_{AH}	0					ns	
Chip Select to $\overline{LD1}$ Set-up Time	t_{CS1}	6					ns	
Chip Select to $\overline{LD1}$ Hold Time	t_{CH1}	0					ns	
$\overline{LD1}$ Pulse Width	t_{DL1W}	50					ns	
$\overline{LD1}$ Negative Edge to $\overline{LD2}$ Positive Edge	t_{LD1LD2}	60					ns	
$\overline{LD2}$ Pulse Width	t_{LD2W}	60					ns	
Chip Select to $\overline{RD}$ Set-Up Time	t_{CS2}	6					ns	
Chip Select to $\overline{RD}$ Hold Time	t_{CH2}	0					ns	

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL TIMING SPECIFICATIONS[1, 4] (CONT'D)								
$\overline{RD}$ Pulse Width	t_{RD}	600					ns	
High Z to Data Valid for Readback	t_{DA}	600					ns	
Data Valid for Readback to High Z	t_{DR}	200					ns	
$\overline{R1}$ Pulse Width	t_{R1W}	100					ns	
$\overline{R2}$ Pulse Width	t_{R2W}	100					ns	

NOTES:

1 Guaranteed; not tested.

2 Specified values guarantee functionality.

3 Digital inputs should not go below digital GND or exceed DV_{DD} supply voltage.

4 *See Figures 1, 2 and 3.* All digital input signals are specified with $t_R = t_F = 10$ ns 10% to 90% and timed from a 50% voltage level.

5 For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.

6 Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... +16.5 V

V_{EE} to AGND ..... –16.5 V

DV_{DD} to DGND ..... +6.5 V

VREF to DGND ..... +7.0 V

Analog Outputs & Inputs
Infinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND and DGND
(provided that power dissipation of the package spec is not exceeded)

AGND to DGND ..... ±1 V
(Functionality guaranteed for ±0.5 V only)

Digital Input & Digital Output Voltage to:
DV_{DD} ..... +.5 V
DGND ..... –.5 V

Operating Temperature Range
Extended Industrial ..... –40°C to +85°C
Military ..... –55°C to +125°C

Maximum Junction Temperature ..... 150°C

Storage Temperature Range ..... –65°C to +150°C

Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Power Dissipation Rating to 75°C
PQFP, PGA, PLCC 800mW
Derates above 75°C ..... 11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

Refer to Section 8 for Applications Information

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.

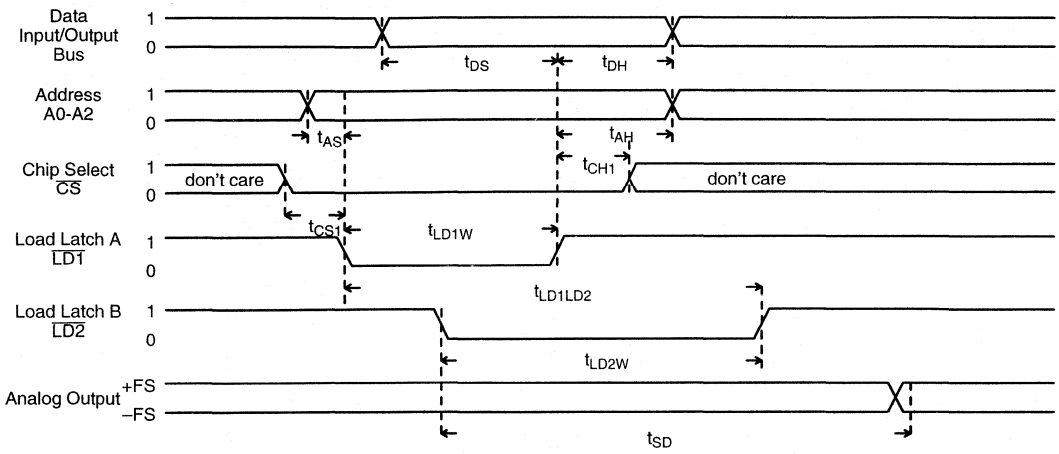


Figure 1. Loading Latch A and Updating Latch B

Notes:
(1) Chip Select ($\overline{CS}$) and Load LATCHA ($\overline{LD1}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1} = \overline{R2} = 1$.
(3) For the case where $\overline{LD2}$ is in the low state, analog output would respond to the falling edge of $\overline{LD1}$ (transparent mode).

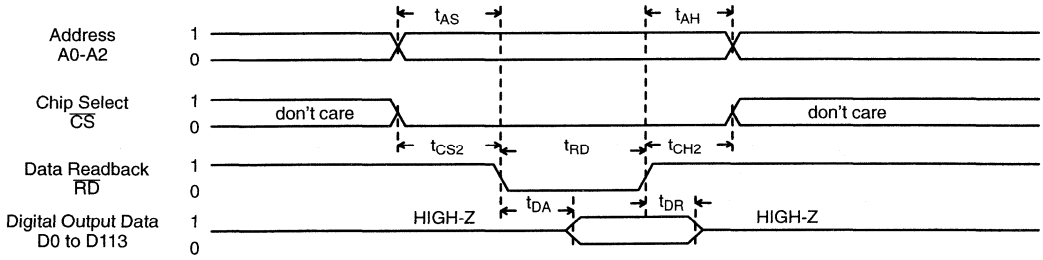


Figure 2. Read Back First Latch Bank of One DAC

Notes:
(1) Chip Select ($\overline{CS}$) and Data Readback ($\overline{RD}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1} = \overline{R2} = 1$.

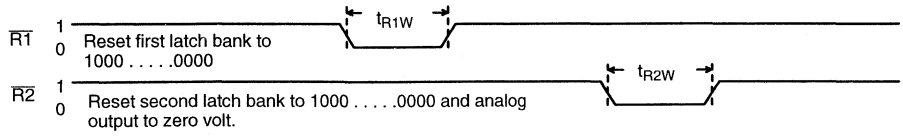


Figure 3. Reset Operations

A standard µ-processor and TTL/CMOS compatible input data port loads the data into the pre-selected DACS. If $\overline{CS} = 0$, the chip accesses digital data on the bus. Then address bits A0 to A2 select the appropriate DAC and $\overline{LD1}$ loads the data into the first-latch-bank. When all 8-channels first-latch-banks are loaded, then $\overline{LD2}$ enables the second-latch-bank and updates all 8-channels simultaneously. The selected DAC becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{LD1} = \overline{LD2} = 0$.

$\overline{R1} = 0$ resets the first-latch-bank. $\overline{R2} = 0$ resets the second-latch-bank which sets the analog output to zero volts (data = 100...00), regardless of digital inputs.

Function	A2	A1	A0	$\overline{RD}$	$\overline{LD1}$	$\overline{LD2}$	$\overline{CS}$	$\overline{R1}$	$\overline{R2}$
Load Latch 1 of DAC1	0	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC2	0	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC3	0	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC4	0	1	1	1	0→1	1	0	1	1
Load Latch 1 of DAC5	1	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC6	1	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC7	1	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC8	1	1	1	1	0→1	1	0	1	1
Load Latch 2 of DAC1→8	X	X	X	1	1	0→1	0	1	1
Read Latch 1 of DAC1	0	0	0	0	1	1	0	1	1
Read Latch 1 of DAC2	0	0	1	0	1	1	0	1	1
Read Latch 1 of DAC3	0	1	0	0	1	1	0	1	1
Read Latch 1 of DAC4	0	1	1	0	1	1	0	1	1
Read Latch 1 of DAC5	1	0	0	0	1	1	0	1	1
Read Latch 1 of DAC6	1	0	1	0	1	1	0	1	1
Read Latch 1 of DAC7	1	1	0	0	1	1	0	1	1
Read Latch 1 of DAC8	1	1	1	0	1	1	0	1	1
Reset Latch 1 of DAC1→8	X	X	X	X	X	X	X	0	1
Reset Latch 2 of DAC1→8	X	X	X	X	X	X	X	1	0

Note: 1: High, 0: Low, X: Don't Care

Table 1. Octal Parallel Data Input 14-Bit DAC Truth Table

Note: For timing information see Electrical Characteristics

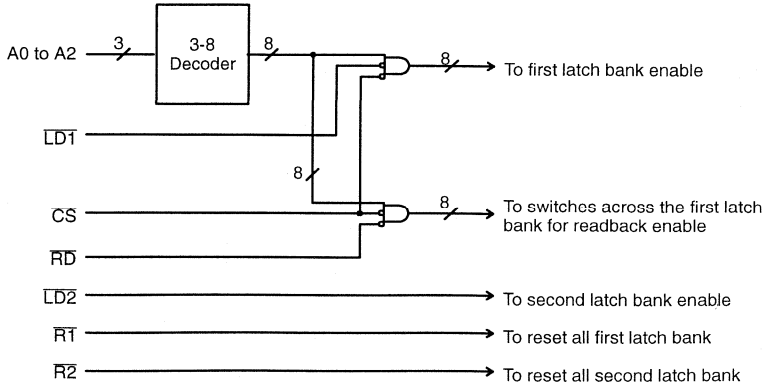


Figure 4. Simplified Parallel Logic Port

Hex Code	Binary Code	Output Voltage = 2 • Vr (–1 + $\frac{2 \bullet D}{16384}$) (Vr = +5 V)
O O O O	00000000000000	10 • (–1 + 0) = –10
⋮	⋮	⋮
1 F F F	01111111111111	10 • (–1 + $\frac{16382}{16384}$) = –1.22 mV
2 O O O	10000000000000	10 • (–1 + $\frac{16384}{16384}$) = 0
2 O O 1	10000000000001	10 • (–1 + $\frac{16386}{16384}$) = 1.22 mV
⋮	⋮	⋮
3 F F F	11111111111111	10 • (–1 + $\frac{32766}{16384}$) = 9.99878

Table 2. MP7611
Ideal DAC Output vs. Input Code

4

Note: See Electrical Characteristics for real system accuracy

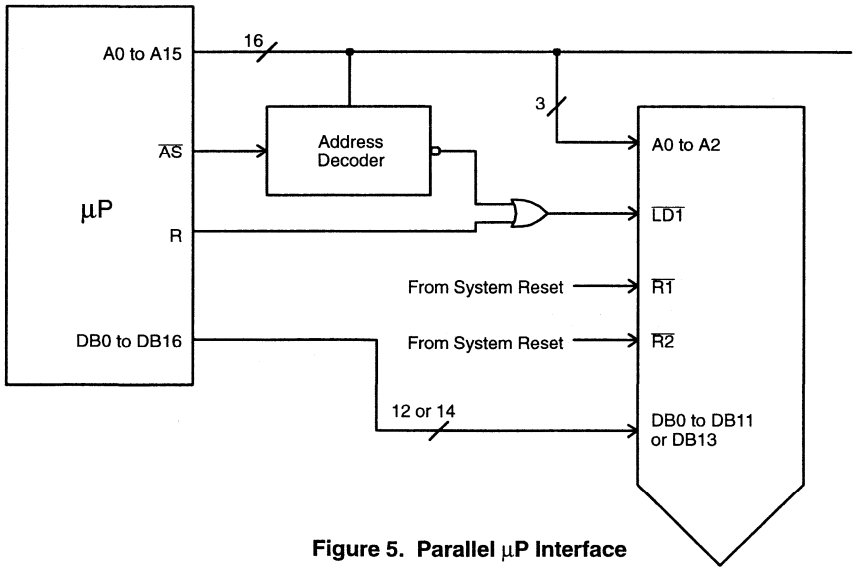
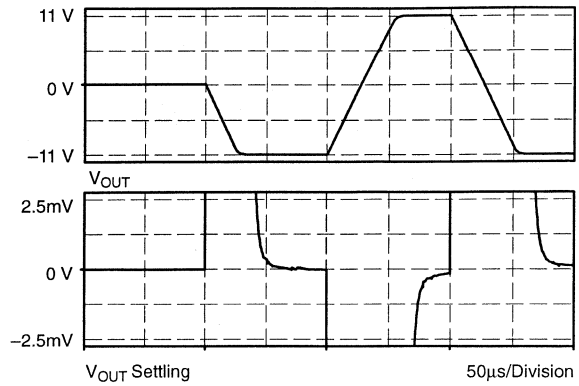
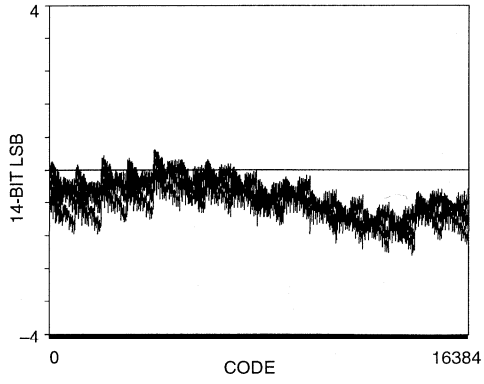


Figure 5. Parallel µP Interface

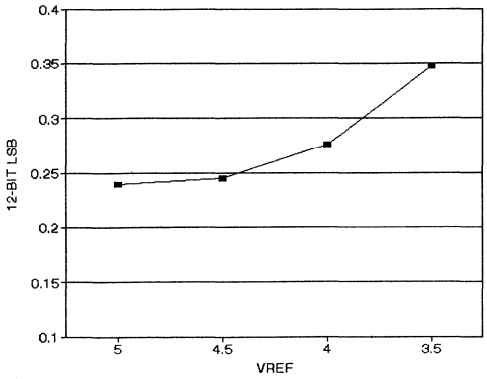


Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

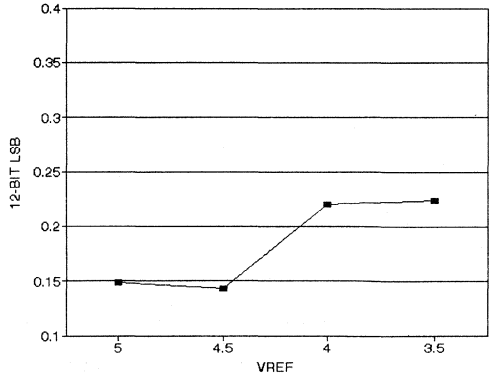
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



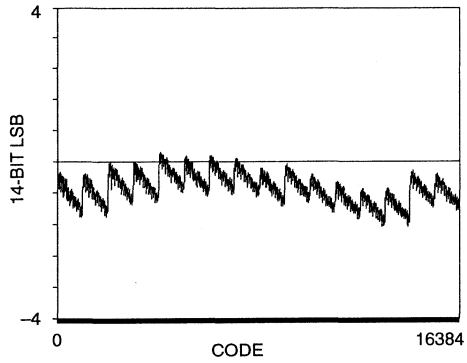
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes



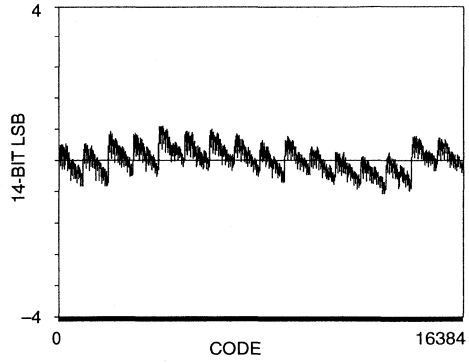
Graph 3. DAC 0 INL vs. V_{REF}



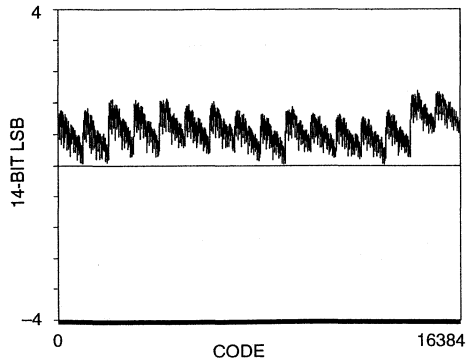
Graph 4. DAC 0 DNL vs. V_{REF}



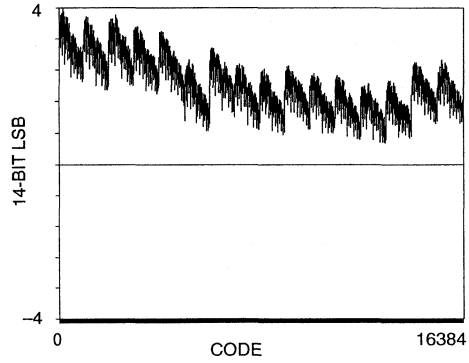
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

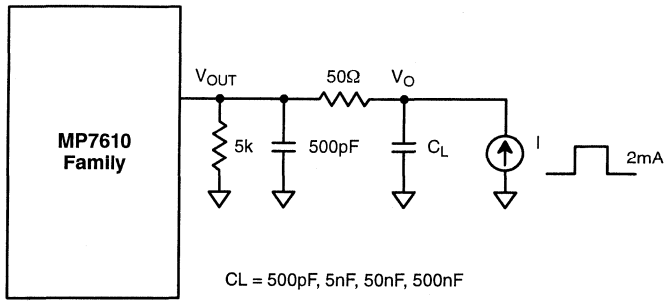
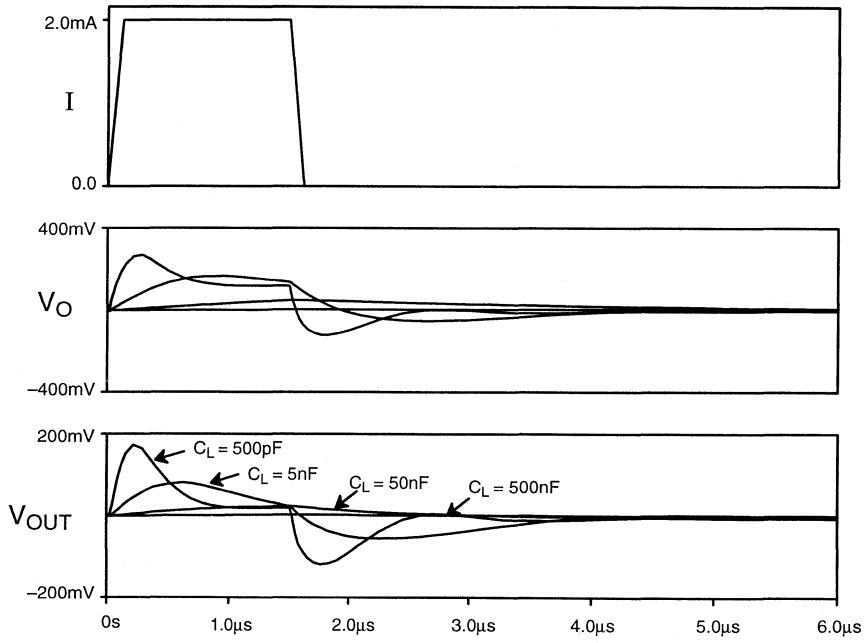


Figure 6. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF (*See Figure 9. above*)

MP7612

Octal 12-Bit DAC Array™ D/A Converter with Output Amplifier and Serial Data/Address µP Control Logic

FEATURES

- **Eight Independent 12-Bit DACs with Output Amplifiers**
- **Low Power 320 mW (typ.)**
- **Serial Digital Data and Address Port (3-Wire Standard)**
- **12-Bit Resolution, 11 Bit Accuracy**
- **Extremely Well Matched DACs**
- **Extremely Low Analog Ground Current (<60µA/Channel)**
- **±10 V Output Swing with ±11.4 V Supplies**
- **Zero Volt Output Preset (Data = 10 .. 00)**
- **Rugged Construction – Latch-Up Free**
- **Parallel Version: MP7613**

APPLICATIONS

- **Data Acquisition Systems**
- **ATE**
- **Process Control**
- **Self-Diagnostic Systems**
- **Logic Analyzers**
- **Digital Storage Scopes**
- **PC Based Controller/DAS**

4

GENERAL DESCRIPTION

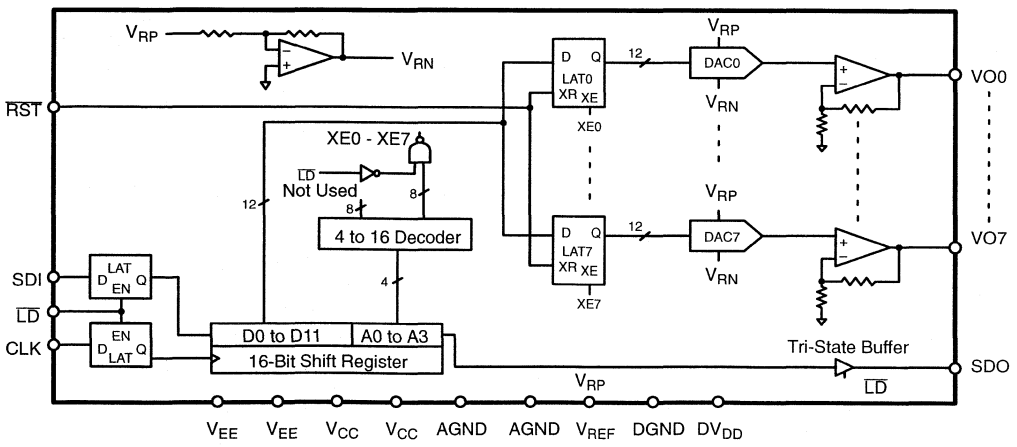
The MP7612 provides eight independent 12-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a 3-wire standard serial digital address and data port.

Typical DAC matching for B grade versions is 0.7 LSB across all codes. Accuracy of ±0.75 LSB for DNL and ±1 LSB for INL is also achieved for B grades. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30µs (typ.).

The MP7612 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board space.

Built using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR's patented thin-film resistor process which exhibits excellent long term stability and reliability.

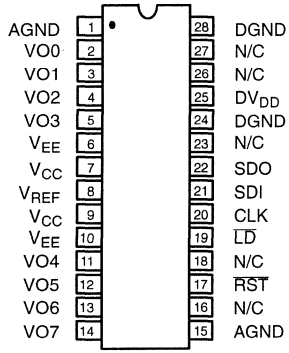
SIMPLIFIED BLOCK DIAGRAM



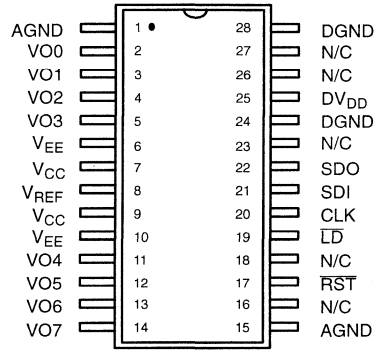
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PDIP	–40 to +85°C	MP7612BN	12	±1	±0.75	±6
PDIP	–40 to +85°C	MP7612AN	12	±2	±1	±8
SOIC	–40 to +85°C	MP7612BS	12	±1	±0.75	±6
SOIC	–40 to +85°C	MP7612AS	12	±2	±1	±8

PIN CONFIGURATIONS



28 Pin PDIP (0.400")
NW28



28 Pin SOIC (Jedec, 0.346")
SW28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	VO0	DAC 0 Output
3	VO1	DAC 1 Output
4	VO2	DAC 2 Output
5	VO3	DAC 3 Output
6	V_{EE}	Analog Negative Power Supply (–12 V)
7	V_{CC}	Analog Positive Power Supply (+12 V)
8	V_{REF}	Voltage Reference Input (+5 V)
9	V_{CC}	Analog Positive Power Supply (+12 V)
10	V_{EE}	Analog Negative Power Supply (–12 V)
11	VO4	DAC 4 Output
12	VO5	DAC 5 Output
13	VO6	DAC 6 Output
14	VO7	DAC 7 Output

PIN NO.	NAME	DESCRIPTION
15	AGND	Analog Ground
16	N/C	No Connection
17	$\overline{RST}$	Reset all DACs to 0 V Output
18	N/C	No Connection
19	$\overline{LD}$	Load Signal; Load Data to Selected DAC
20	CLK	Serial Data Clock
21	SDI	Serial Data Input
22	SDO	Shift Register Serial Output
23	N/C	No Connection
24	DGND	Digital Ground
25	DV_{DD}	Digital Positive Power Supply (+5 V)
26	N/C	No Connection
27	N/C	No Connection
28	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = −12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	12					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				±2		±2		
B				±1		±1		
Differential Non-Linearity	DNL						LSB	
A				±1		±1		
B				±0.75		±0.75		
Positive Full Scale Error	+FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Negative Full Scale Error	−FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Bipolar Zero Offset	ZOFS						LSB	
A				±4		±4		
B				±3		±3		
INL Matching	ΔINL						LSB	
A				±2		±2		
B				±1.5		±1.5		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				±4		±4		
B				±2		±2		
Bipolar Zero Matching	ΔZOFS						LSB	
A				±4		±4		
B				±3		±3		
Full Scale Error Matching	FSE						LSB	
A				±4		±4		
B				±3		±3		
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µsec	ZS to FS (20 V Step)
Channel-to-Channel Crosstalk[1, 6]	CT		0.04				LSB	DC
Digital Feedthrough[1, 6]	Q		−70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR			5			ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for driving the reference input
V_{REF} Voltage1, [2]	V_{REF}	3.5		6			V	

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4	V_{CC} −1.4				V	
Output Drive Current		−5		5			mA	
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	−FS to AGND
			55				mA	−FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	−12.75	−12	−5	−12.75	−5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10		10	mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20		20	mA	Bipolar zero
Digital Supply Current	I_{DD}			2		2	mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0, V_{IH} = 5.0, C_L = 20 pF
Input Clock Pulse Width	t_{CH}, t_{CL}	35					ns	
Data Setup Time	t_{DS}	15					ns	
Data Hold Time	t_{DH}	15					ns	
CLK to SDO Propagation Delay	t_{PD}			40			ns	
DAC Register Load Pulse Width	t_{LD}	35					ns	
Preset Pulse Width	t_{PR}	50					ns	
Clock Edge to Load Time	t_{CKLD1}	140					ns	Note: t_{LD} and t_{CKLD2} cannot both be min. since t_{CKLD1}=t_{CKLD2}+t_{LD}
	t_{CKLD2}	0						
$\overline{LD}$ Falling Edge to SDO Tri-state Enable	t_{HZ1}	50					ns	
$\overline{LD}$ Rising Edge to SDO Tri-state Disable	t_{HZ2}	50					ns	
$\overline{LD}$ Rising Edge to CLK Enable	t_{LDCK}	50					ns	
$\overline{LD}$ Set-up Time with Respect to CLK	t_{LDSU}	30					ns	

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Guaranteed; not tested.
2 Specified values guarantee functionality.
3 Digital inputs should not go below digital GND or exceed DV_{DD} supply voltage.
4 *See Figures 2 and 3.* All digital input signals are specified with $t_R = t_F = 10$ ns 10% to 90% and timed from a 50% voltage level.
5 For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.
6 Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... +16.5 V
V_{EE} to AGND ..... –16.5 V
DV_{DD} to DGND ..... +6.5 V
V_{REF} to DGND ..... +7.0 V
AGND to DGND ..... ±1 V
(Functionality guaranteed for ±0.5 V only)
Digital Input & Output Voltage to DGND –0.5 to DV_{DD} +0.5V
Analog Inputs & Outputs ..... Indefinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND, DGND (provided that power dissipation of the package spec is not exceeded)

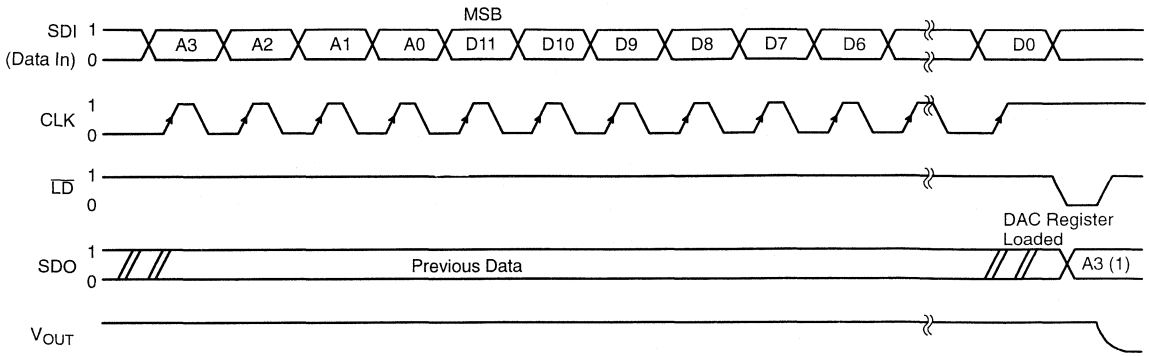
Operating Temperature Range
Extended Industrial ..... –40°C to +85°C
Maximum Junction Temperature ..... –65°C to 150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP 1150mW
Derates above 75°C ..... 15mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

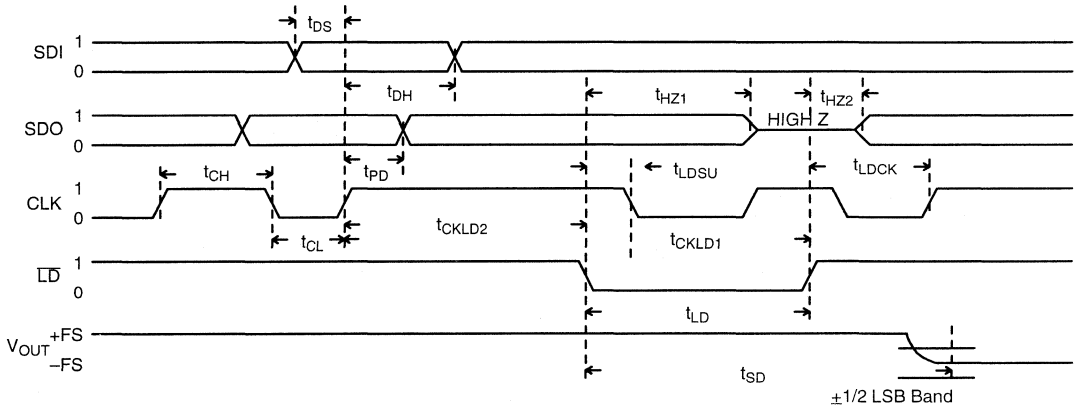
APPLICATION NOTES
Refer to Section 8 for Applications Information

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.



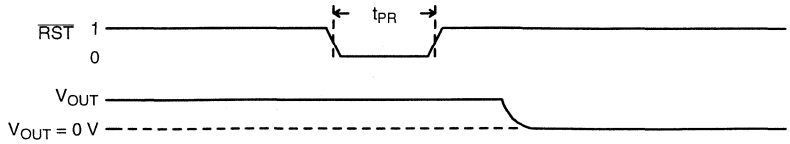
Notes: (1) Because A3 is available immediately after 16th clock edge of DATA Shift-in, only 15 clock cycles are needed to complete the readback.

Figure 1. Serial Data Timing and Loading



Notes: (1) CLK should be high during the falling edge of $\overline{LD}$ to insure proper function of the shift register.

Figure 2. Serial Data Input Timing ($\overline{RST}$ = "1")



Note: Reset settling time is ≤t_{SD} ±1/2 LSB Error Band

Figure 3. Reset Operation

The MP7612 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board wire (space). If the $\overline{LD}$ signal is high, the CLK signal loads the digital input bits (SDI) into the shift register (4 bits address A3 to A0 plus 12 bits data DB11 to DB0 for the MP7612). The $\overline{LD}$ signal going low loads the data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data (SDI), output (SDO 3-stated) and the CLK input. This design tremendously reduces digital noise and glitch transients into the DACs due to free running CLK and SDI. Note also that the preset signal ($\overline{RST}$) resets all analog outputs to 0 volt regardless of digital inputs.

Function	A3	A2	A1	A0	$\overline{LD}$	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	0→1 Repeat	1	Data Input Valid	Data Output Valid
Stop Shifting Data In and Out	X	X	X	X	0	X	1	X	Hi-Z
Load DACs	0	0	0	0	No Operation				
DAC 0	0	0	0	1	1→0	X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0	X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0	X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0	X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0	X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0	X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0	X	1	X	Hi-Z
	⋮	⋮	⋮	⋮	No Operation	X	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
	1	1	1	0	No Operation	X	1	X	Hi-Z
	1	1	1	1	No Operation	X	1	X	Hi-Z
Reset all DACs to 0 V	X	X	X	X	X	X	0	X	X

Table 1. Digital Function Truth Table
Serial In/Serial Out

Note: For timing information see Electrical Characteristics

Hex Code	Binary Code	Output Voltage = $2 \bullet Vr \left(-1 + \frac{2 \bullet D}{4096}\right)$ (Vr = +5 V)
0 0 0	000000000000	$10 \bullet (-1 + 0) = -10$
⋮	⋮	⋮
7 F F	011111111111	$10 \bullet \left(-1 + \frac{4094}{4096}\right) = -4.88$ mV
8 0 0	100000000000	$10 \bullet \left(-1 + \frac{4096}{4096}\right) = 0$
8 0 1	100000000001	$10 \bullet \left(-1 + \frac{4098}{4096}\right) = 4.88$ mV
⋮	⋮	⋮
F F F	111111111111	$10 \bullet \left(-1 + \frac{8190}{4096}\right) = 9.99512$

Table 2. MP7612
Ideal DAC Output vs. Input Code

Note: See Electrical Characteristics for real system accuracy

SERIAL INTERFACE DIAGRAMS

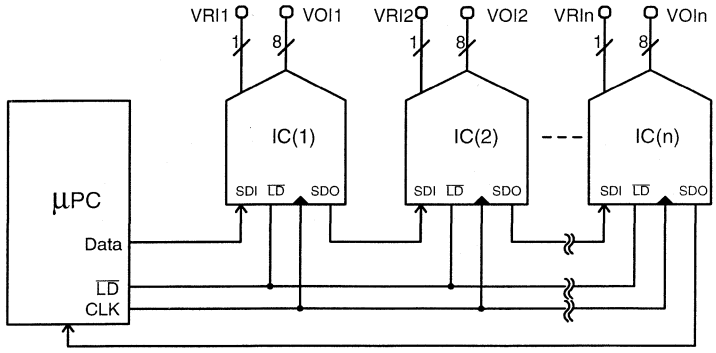


Figure 4. Simplified Diagram

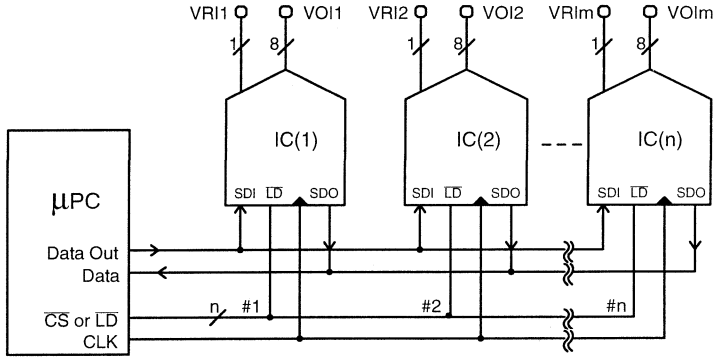


Figure 5. Simplified Diagram

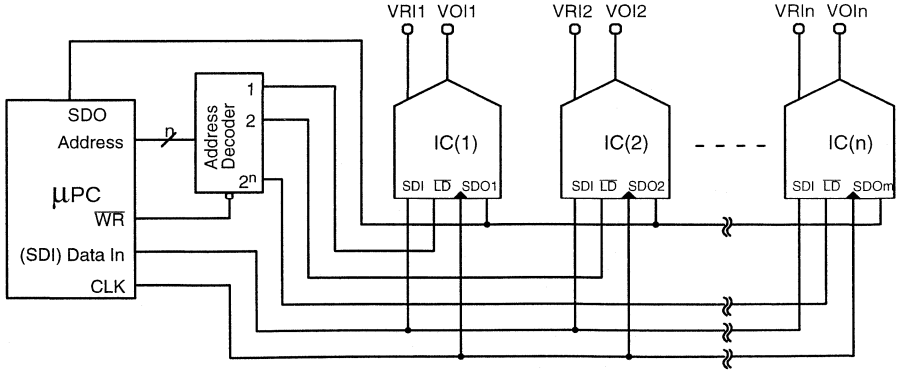
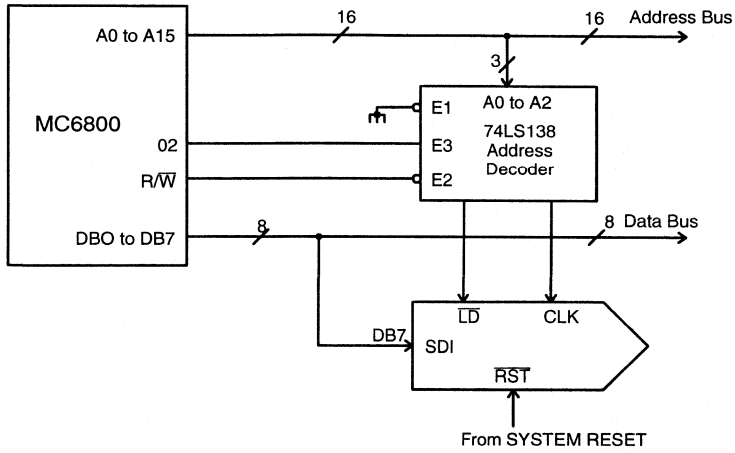


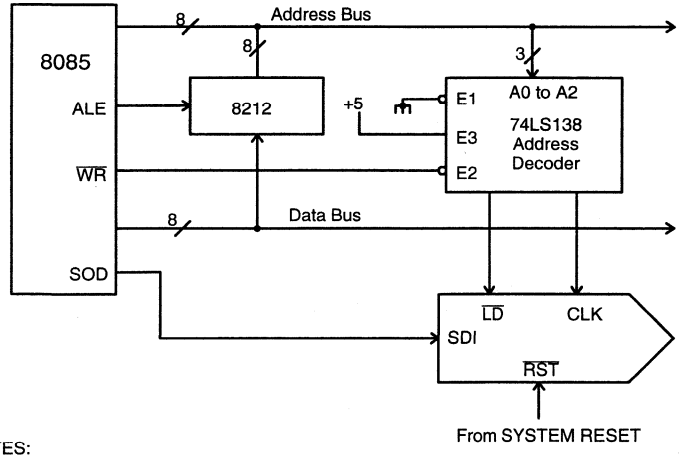
Figure 6. Simplified Diagram



NOTES
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit.
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE to memory location 2000, R/W, and 02. A WRITE to address 4000 transfers data from input shift register to DAC register.

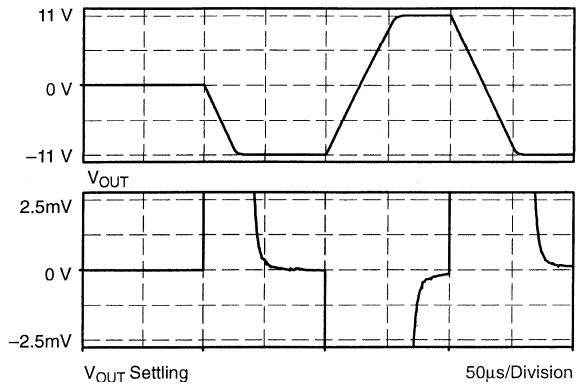
4

Figure 7. MC6800 Interface



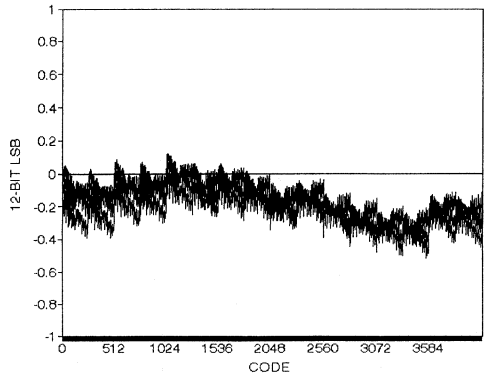
NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000.
2. Data is clocked in the DAC shift register by executing memory write instructions. The clock input is generated by decoding address 8000 and WR. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

Figure 8. 8085 Interface

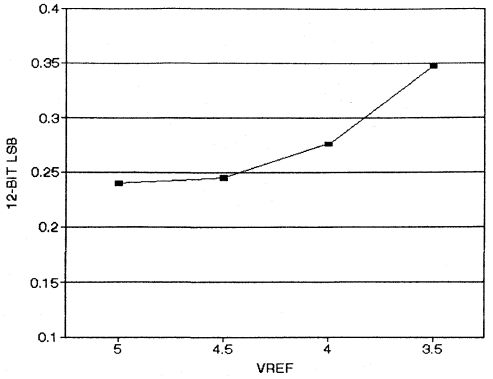


Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

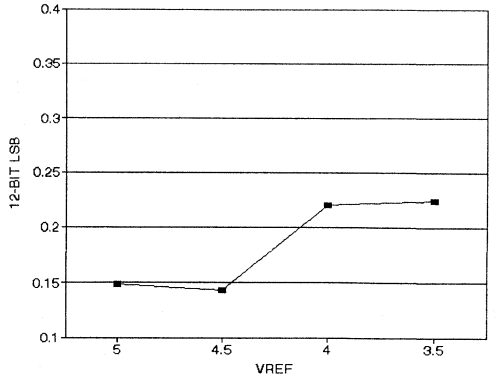
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



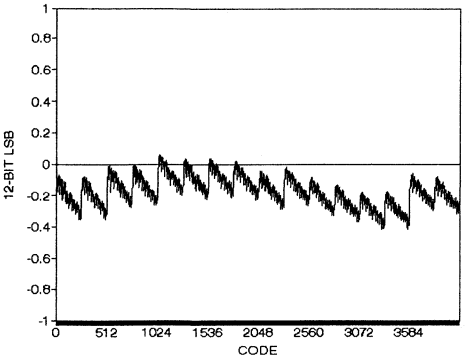
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes



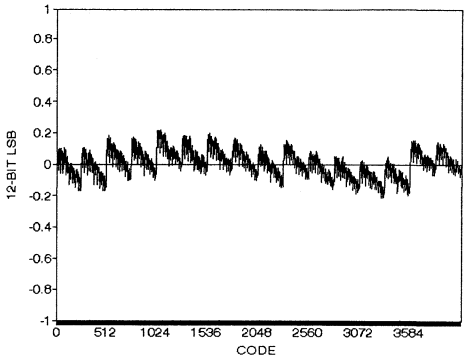
Graph 3. DAC 0 INL vs. V_{REF}



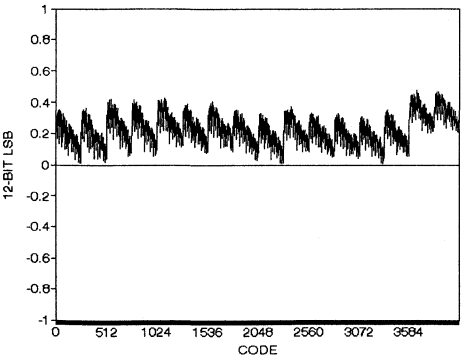
Graph 4. DAC 0 DNL vs. V_{REF}



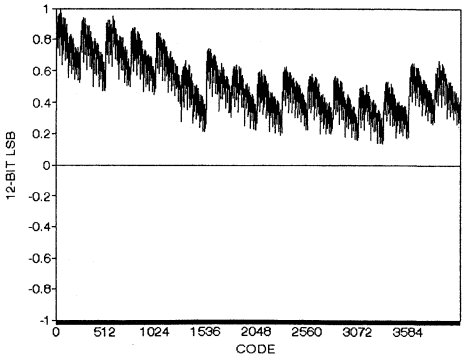
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

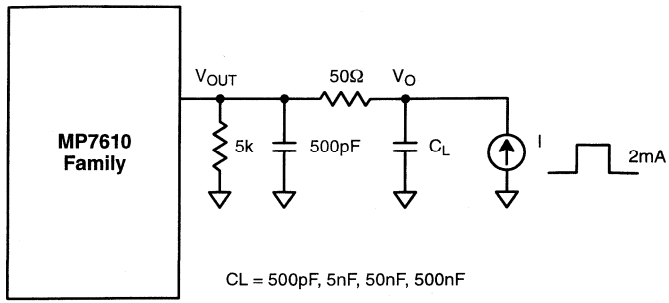
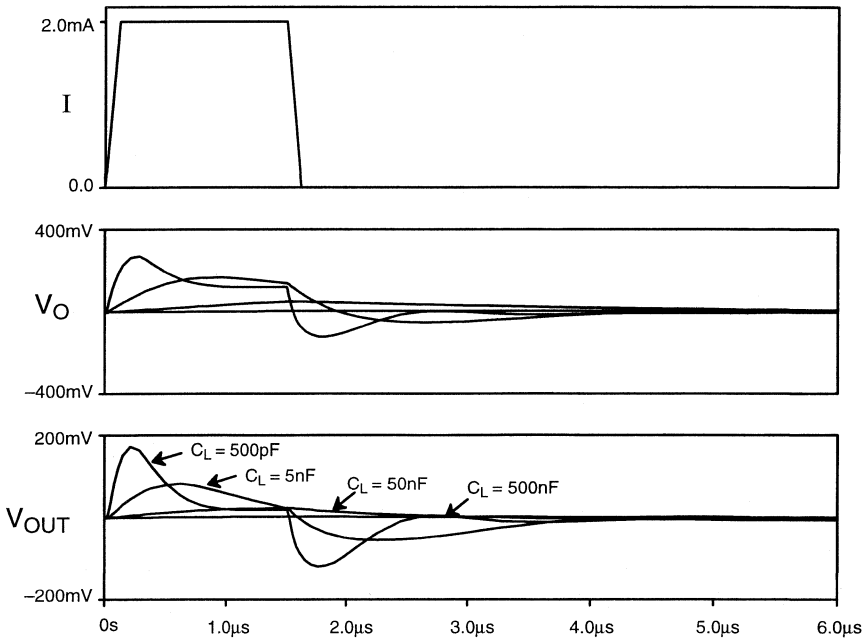


Figure 9. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF (*See Figure 9. above*)

MP7613

Octal 12-Bit DAC Array™ D/A Converter with Output Amplifier and Parallel Data/Address µP Control Logic

FEATURES

- **Eight Independent Channel 12-Bit DACs with Output Amplifiers**
- **Low Power 320 mW (typ.)**
- **Parallel Digital Data and Address Port**
- **Double Buffered Data Interface**
- **Readback of DAC Latches**
- **Zero Volt Output Preset (Data = 10 .. 00)**
- **12-Bit Resolution, 11-Bit Accuracy**
- **Extremely Well Matched DACs**
- **Extremely Low Analog Ground Current (<60µA/Channel)**
- **±10 V Output Swing with ±11.4 V Supplies**
- **Rugged Construction – Latch-Up Proof**
- **Serial Version: MP7612**

APPLICATIONS

- **Data Acquisition Systems**
- **ATE**
- **Process Control**
- **Self-Diagnostic Systems**
- **Logic Analyzers**
- **Digital Storage Scopes**
- **PC Based Controller/DAS**

4

GENERAL DESCRIPTION

The MP7613 provides eight independent 12-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a parallel digital address and data port.

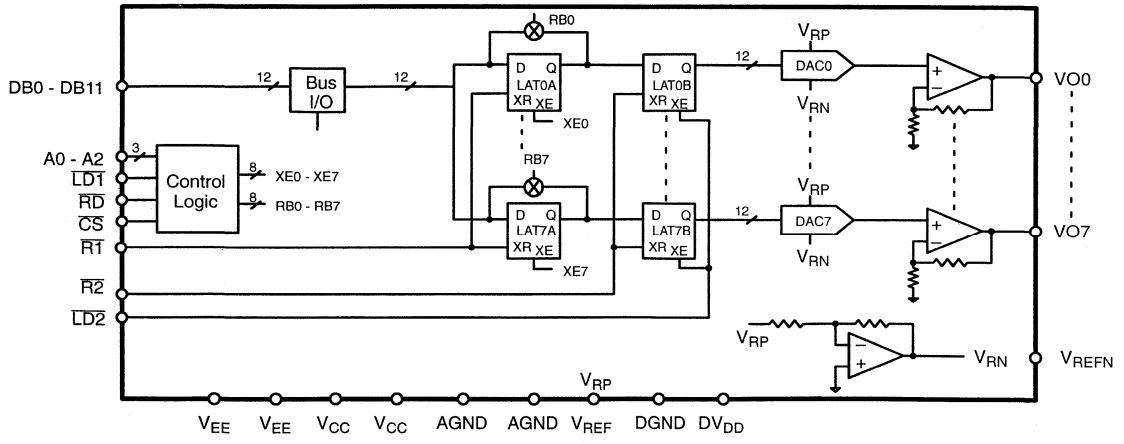
Built on using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR's patented thin-film resistor process which exhibits excellent long term stability and reliability.

A standard µ-processor and TTL/CMOS compatible 12-bit input data port loads the data into the pre-selected DACS.

This device can easily be interfaced to a data bus, and digital readback of each channel is available.

Typical DAC matching is 0.7 LSB across all codes. Accuracy of ±0.75 LSB for DNL and ±1 LSB for INL is achieved for B grade versions. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30µs (typ.).

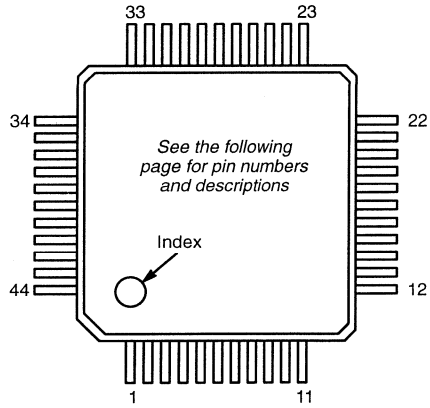
SIMPLIFIED BLOCK DIAGRAM



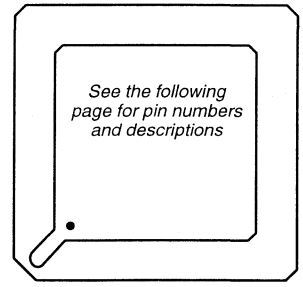
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PQFP	–40 to +85°C	MP7613BE	12	±1	±0.75	±6
PQFP	–40 to +85°C	MP7613AE	12	±2	±1	±8
PGA	–40 to +85°C	MP7613BG	12	±1	±0.75	±6
PGA	–40 to +85°C	MP7613AG	12	±2	±1	±8
PLCC	–40 to +85°C	MP7613BP	12	±1	±0.75	±6
PLCC	–40 to +85°C	MP7613AP	12	±2	±1	±8

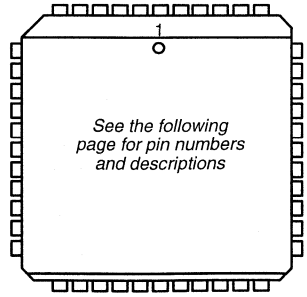
PIN CONFIGURATIONS *See Packaging Section for Package Dimensions*



44-Pin PQFP (14 mm x 14 mm)
Q44



44-Pin PGA
G44



44-Pin PLCC
P44

PIN OUT DEFINITIONS

PLCC PIN NO.	PQFP & PGA PIN NO.	NAME	DESCRIPTION
29	1	N/C	No Connection
30	2	VO3	DAC 3 Output
31	3	V_{EE}	Analog Negative Power Supply (–12 V)
32	4	V_{CC}	Analog Positive Power Supply (+12 V)
33	5	DGND	Digital Ground (0 V)
34	6	V_{REF}	Analog Positive Voltage Reference Input (+5 V)
35	7	V_{REFN}	Analog Negative Voltage Reference Output (–2.5 V)
36	8	V_{CC}	Analog Positive Power Supply (+12 V)
37	9	V_{EE}	Analog Negative Power Supply (–12 V)
38	10	VO4	DAC 4 Output
39	11	N/C	No Connection
40	12	VO5	DAC 5 Output
41	13	VO6	DAC 6 Output
42	14	VO7	DAC 7 Output
43	15	AGND	Analog Ground (0 V)
44	16	$\overline{CS}$	Chip Select Enable
1	17	$\overline{RD}$	Read Back Enable
2	18	$\overline{R2}$	Second–Latch-Bank Reset Enable
3	19	$\overline{R1}$	First–Latch-Bank Reset Enable
4	20	$\overline{LD2}$	Second–Latch-Bank Load Enable
5	21	$\overline{LD1}$	First–Latch-Bank Load Enable
6	22	A2	Digital Address Bit 2
7	23	A1	Digital Address Bit 1
8	24	A0	Digital Address Bit 0
9	25	N/C	No Connection
10	26	N/C	No Connection
11	27	DB0	Digital Input Data Bit 0 (LSB)
12	28	DB1	Digital Input Data Bit 1
13	29	DB2	Digital Input Data Bit 2
14	30	DB3	Digital Input Data Bit 3
15	31	DB4	Digital Input Data Bit 4
16	32	DB5	Digital Input Data Bit 5
17	33	DB6	Digital Input Data Bit 6
18	34	DB7	Digital Input Data Bit 7
19	35	DB8	Digital Input Data Bit 8
20	36	DB9	Digital Input Data Bit 9
21	37	DB10	Digital Input Data Bit 10
22	38	DB11	Digital Input Data Bit 11 (MSB)
23	39	DV_{DD}	Digital Positive Power Supply (+5 V)
24	40	DGND	Digital Ground (0 V)
25	41	AGND	Analog Ground (0 V)
26	42	VO0	DAC 0 Output
27	43	VO1	DAC 1 Output
28	44	VO2	DAC 2 Output

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = −12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	12					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				±2		±2		
B				±1		±1		
Differential Non-Linearity	DNL						LSB	
A				±1		±1		
B				±0.75		±0.75		
Positive Full Scale Error	+FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Negative Full Scale Error	−FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Bipolar Zero Offset	ZOFS						LSB	
A				±4		±4		
B				±3		±3		
INL Matching	ΔINL						LSB	
A				±2		±2		
B				±1.5		±1.5		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				±4		±4		
B				±2		±2		
Bipolar Zero Matching	ΔZUFS						LSB	
A				±4		±4		
B				±3		±3		
Full Scale Error Matching	ΔFSE						LSB	
A				±4		±4		
B				±3		±3		
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µs	ZS to FS (20 V Step)
Channel-to-Channel Crosstalk[1, 6]	CT		0.04				LSB	DC
Digital Feedthrough[1, 6]	Q		−70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR			5			ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for driving the reference input
V_{REF} Voltage[1, 2]	V_{REF}	3.5		6			V	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4	V_{CC} −1.4				V	
Output Drive Current		−5		5			mA	
V_{REFN} Output Drive Current		−10		+10			µA	For test purposes only
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	−FS to AGND
			55				mA	−FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	−12.75	−12	−5	−12.75	−5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10		10	mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20		20	mA	Bipolar zero
Digital Supply Current	I_{DD}			2		2	mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0 V, V_{IH} = 5 V, CL = 20 pF
Data Setup Time	t_{DS}	20					ns	
Data Hold Time	t_{DH}	20					ns	
Address Set-up Time	t_{AS}	100					ns	
Address Hold Time	t_{AH}	0					ns	
Chip Select to $\overline{LD1}$ Set-up Time	t_{CS1}	6					ns	
Chip Select to $\overline{LD1}$ Hold Time	t_{CH1}	0					ns	
$\overline{LD1}$ Pulse Width	t_{LD1W}	50					ns	
$\overline{LD1}$ Negative Edge to $\overline{LD2}$ Positive Edge	t_{LD1LD2}	60					ns	
$\overline{LD2}$ Pulse Width	t_{LD2W}	60					ns	
Chip Select to $\overline{RD}$ Set-Up Time	t_{CS2}	6					ns	
Chip Select to $\overline{RD}$ Hold Time	t_{CH2}	0					ns	
$\overline{RD}$ Pulse Width	t_{RD}	600					ns	
High Z to Data Valid for Readback	t_{DA}	600					ns	
Data Valid for Readback to High Z	t_{DR}	200					ns	
$\overline{R1}$ Pulse Width	R1W	100					ns	
$\overline{R2}$ Pulse Width	R2W	100					ns	

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1. Guaranteed; not tested.
2. Specified values guarantee functionality.
3. Digital inputs should not go below digital GND or exceed DV_{DD} supply voltage.
4. *See Figures 1, 2, and 3.* All digital input signals are specified with $t_R = t_F = 10$ ns 10% to 90% and timed from a 50% voltage level.
5. For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.
6. Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... +16.5 V

V_{EE} to AGND ..... –16.5 V

DV_{DD} to DGND ..... +6.5 V

V_{REF} to DGND ..... +7.0 V

Analog Outputs & Inputs
Infinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND and DGND
(provided that power dissipation of the package spec is not exceeded)

AGND to DGND ..... ±1 V
(Functionality guaranteed for ±0.5 V only)

Digital Input & Digital Output Voltage to:
DV_{DD} ..... +.5 V
DGND ..... –.5 V

Operating Temperature Range ..... –40°C to +85°C

Maximum Junction Temperature ..... 150°C

Storage Temperature Range ..... –65°C to +150°C

Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Power Dissipation Rating to 75°C
PQFP, PGA, PLCC 800mW
Derates above 75°C ..... 11mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

Refer to Section 8 for Applications Information

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.

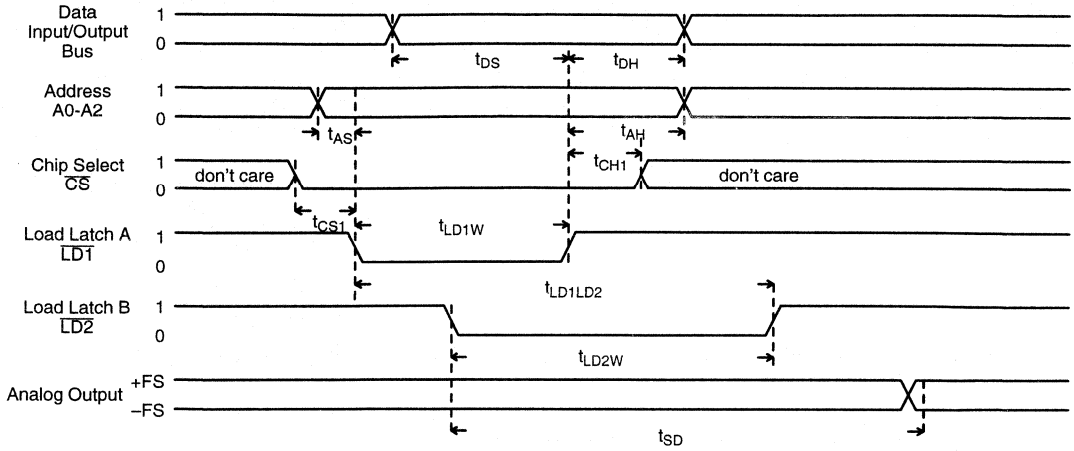


Figure 1. Loading Latch A and Updating Latch B

Notes
(1) Chip Select ($\overline{CS}$) and Load LATCHA ($\overline{LD1}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1} = \overline{R2} = 1$.
(3) For the case where $\overline{LD2}$ is in the low state, analog output would respond to the falling edge of $\overline{LD1}$ (transparent mode).

4

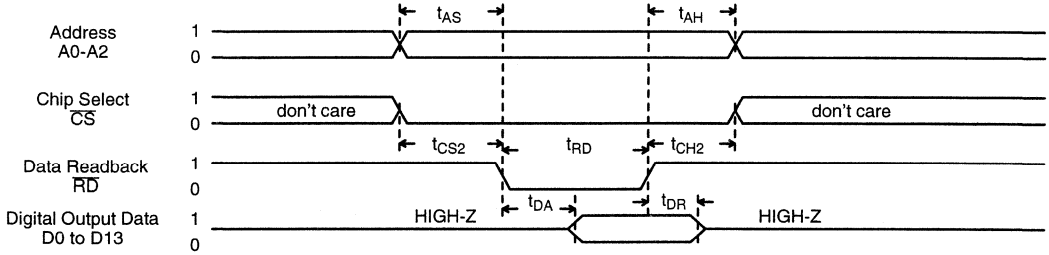


Figure 2. Read Back First Latch Bank of One DAC

Notes
(1) Chip Select ($\overline{CS}$) and Data Readback ($\overline{RD}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1} = \overline{R2} = 1$.

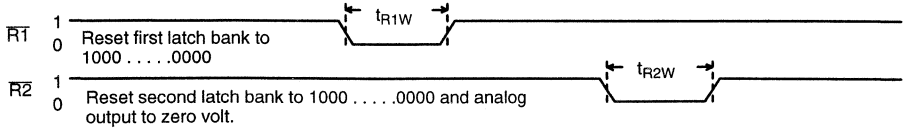


Figure 3. Reset Operations

A standard µ-processor and TTL/CMOS compatible input data port loads the data into the pre-selected DACS. If $\overline{CS} = 0$, the chip accesses digital data on the bus. Then address bits A0 to A2 select the appropriate DAC and $\overline{LD1}$ loads the data into the first-latch-bank. When all 8-channels first-latch-banks are loaded, then $\overline{LD2}$ enables the second-latch-bank and updates all 8-channels simultaneously. The selected DAC becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{LD1} = \overline{LD2} = 0$.

$\overline{R1} = 0$ resets the first-latch-bank. $\overline{R2} = 0$ resets the second-latch-bank which sets the analog output to zero volts (data = 100...00), regardless of digital inputs.

Function	A2	A1	A0	$\overline{RD}$	$\overline{LD1}$	$\overline{LD2}$	$\overline{CS}$	$\overline{R1}$	$\overline{R2}$
Load Latch 1 of DAC1	0	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC2	0	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC3	0	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC4	0	1	1	1	0→1	1	0	1	1
Load Latch 1 of DAC5	1	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC6	1	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC7	1	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC8	1	1	1	1	0→1	1	0	1	1
Load Latch 2 of DAC1→8	X	X	X	1	1	0→1	0	1	1
Read Latch 1 of DAC1	0	0	0	0	1	1	0	1	1
Read Latch 1 of DAC2	0	0	1	0	1	1	0	1	1
Read Latch 1 of DAC3	0	1	0	0	1	1	0	1	1
Read Latch 1 of DAC4	0	1	1	0	1	1	0	1	1
Read Latch 1 of DAC5	1	0	0	0	1	1	0	1	1
Read Latch 1 of DAC6	1	0	1	0	1	1	0	1	1
Read Latch 1 of DAC7	1	1	0	0	1	1	0	1	1
Read Latch 1 of DAC8	1	1	1	0	1	1	0	1	1
Reset Latch 1 of DAC1→8	X	X	X	X	X	X	X	0	1
Reset Latch 2 of DAC1→8	X	X	X	X	X	X	X	1	0

Note: 1: High, 0: Low, X: Don't Care

Table 1. Octal Parallel Data Input 14-Bit DAC Truth Table

Note: For timing information see Electrical Characteristics

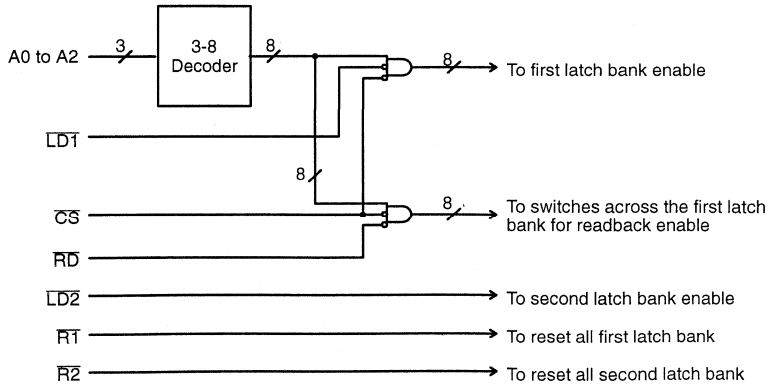


Figure 4. Simplified Parallel Logic Port

Hex Code	Binary Code	Output Voltage = 2 • Vr (–1 + $\frac{2 \bullet D}{4096}$) (Vr = +5 V)
0 0 0	000000000000	10 • (–1 + 0) = –10
⋮	⋮	⋮
7 F F	011111111111	10 • (–1 + $\frac{4094}{4096}$) = –4.88 mV
8 0 0	100000000000	10 • (–1 + $\frac{4096}{4096}$) = 0
8 0 1	100000000001	10 • (–1 + $\frac{4098}{4096}$) = 4.88 mV
⋮	⋮	⋮
F F F	111111111111	10 • (–1 + $\frac{8190}{4096}$) = 9.99512

Table 2. MP7613
Ideal DAC Output vs. Input Code

4

Note: See Electrical Characteristics on pages 28-30 for real system accuracy

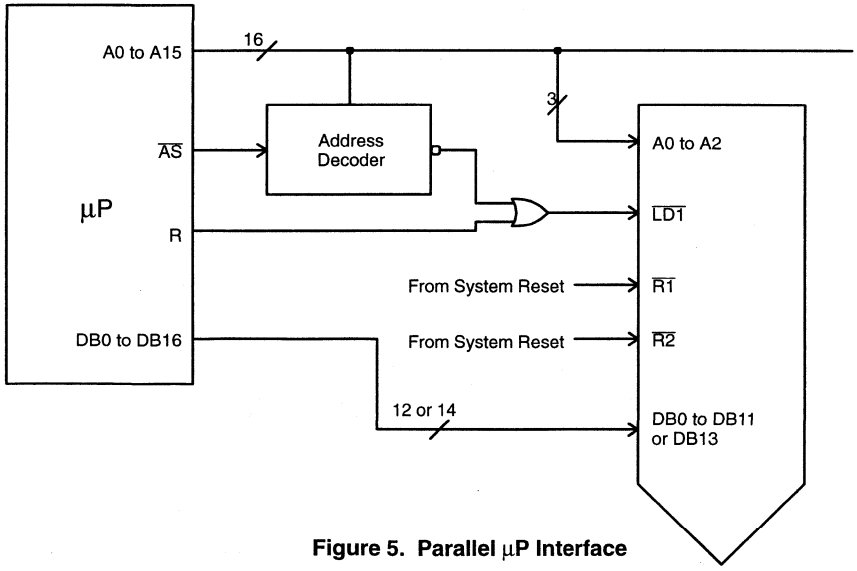
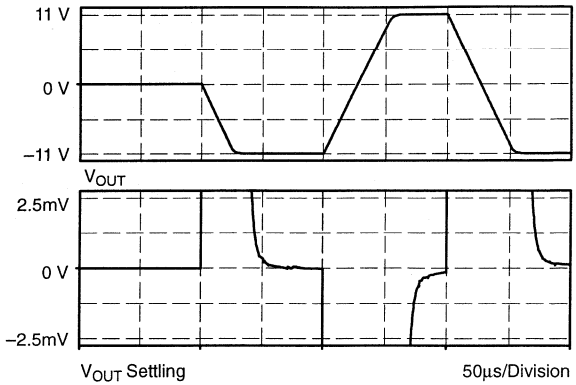
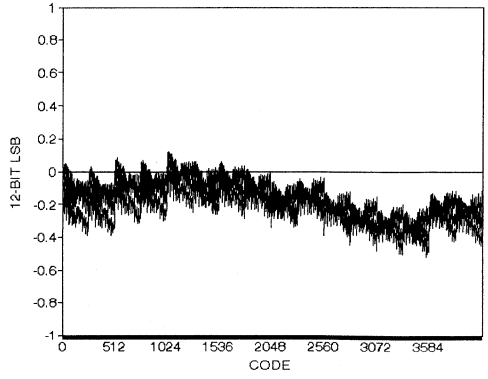


Figure 5. Parallel µP Interface

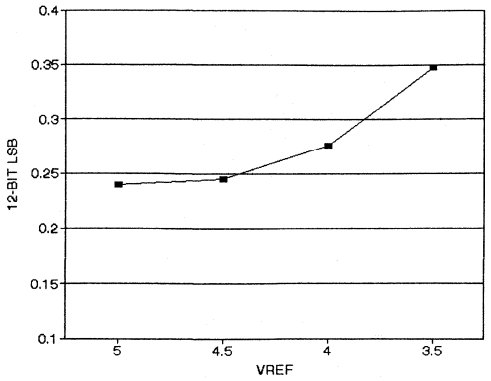


Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

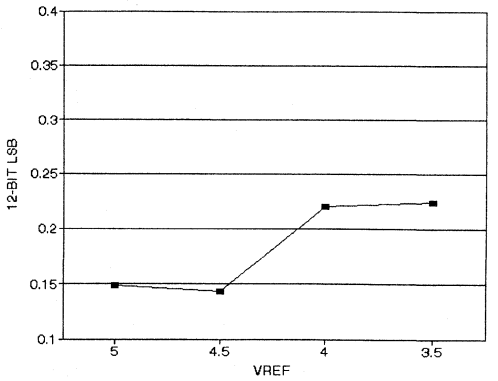
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



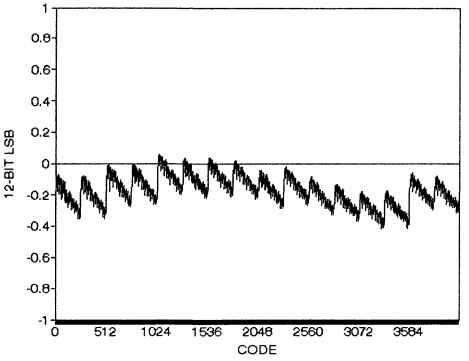
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes



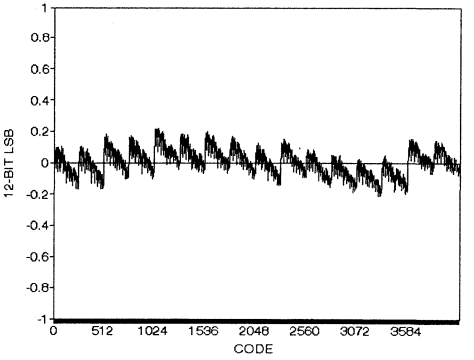
Graph 3. DAC 0 INL vs. V_{REF}



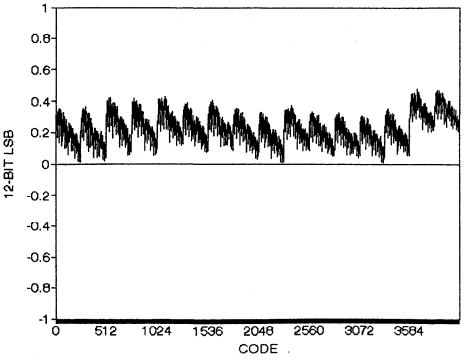
Graph 4. DAC 0 DNL vs. V_{REF}



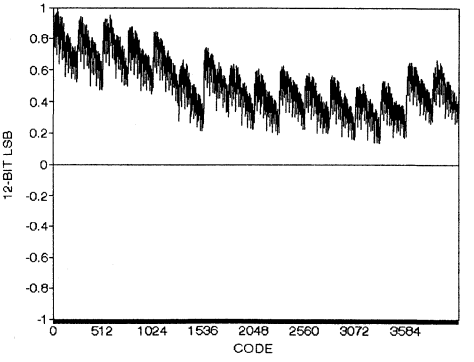
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

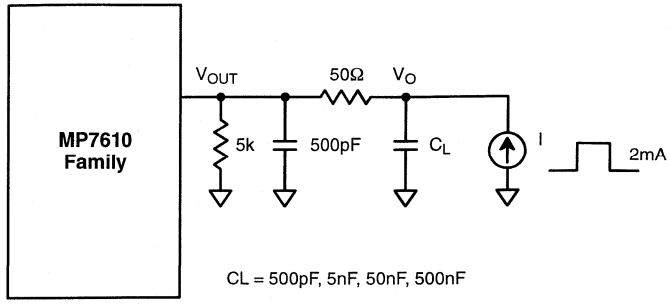
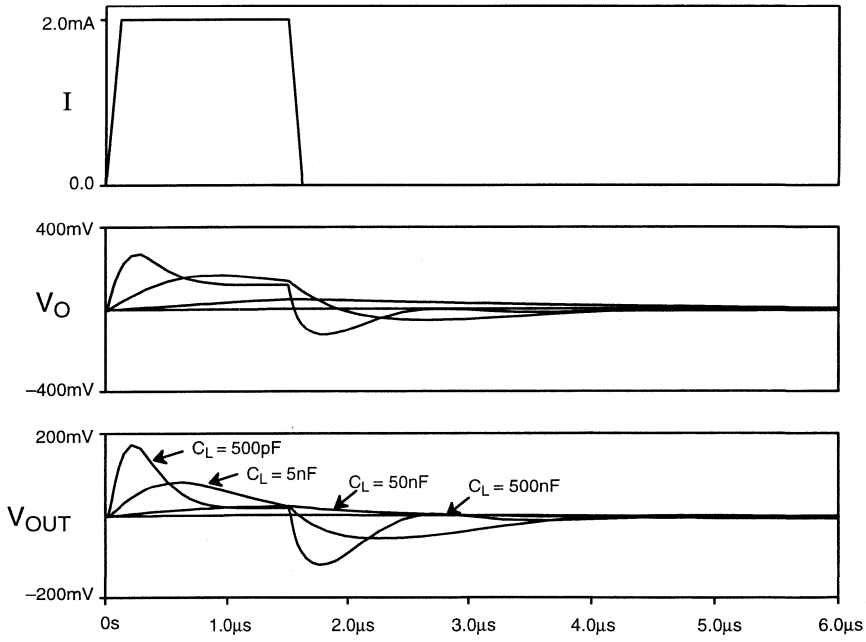


Figure 6. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF (*See Figure 9. above*)

MP7614

15 V CMOS
Multiplying 14-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four-Quadrant Multiplication**
- **Excellent Stability Over Temperature and Time**
- **Guaranteed Monotonic**
- **TTL/5 V CMOS Compatible**
- **Low Sensitivity to Output Amplifier V_{OS}**
- **Low Glitch Energy**
- **16-Bit Version: MP7616**

GENERAL DESCRIPTION

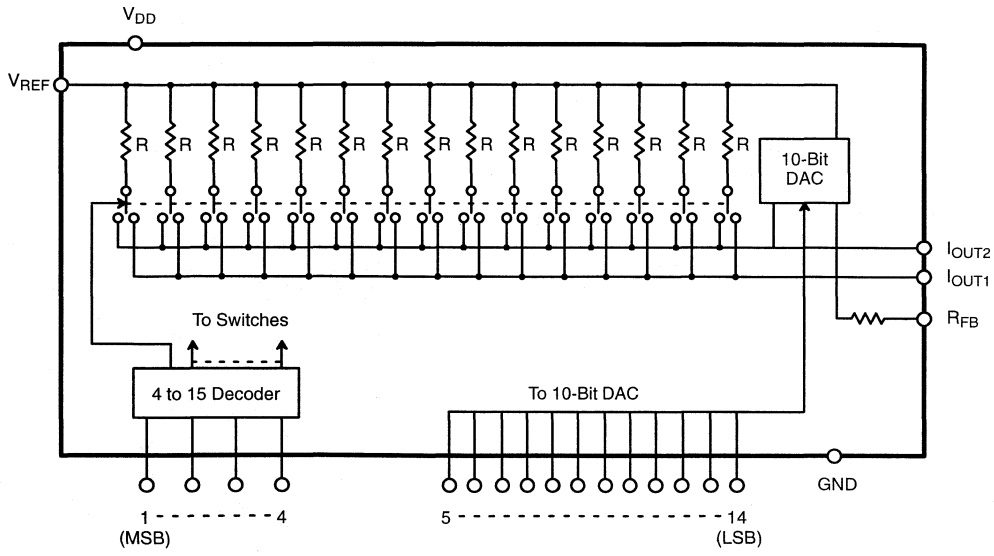
The MP7614 is a high density 14-bit CMOS multiplying Digital-to-Analog Converter. Silicon nitride passivation and untrimmed silicon chromium resistors have been combined to provide long term stability and reliability. Using the most significant bit (MSB) segmentation technique, the MP7614 features 13-bit (0.012%) differential and 12-bit (0.01%) integral linearity.

To achieve 13-bit linearity without laser trim, the MP7614 digitally decodes the four MSB's into 15 equal current sources, rather than the standard binary-weighted sources. Each resistor contributes only 1/16 full scale output thus reducing the matching accuracy requirement of the resistor and CMOS switches from 0.0015% to 0.006%.

The decoding technique achieves an eightfold improvement in differential linearity stability over temperature, an eightfold improvement in relative accuracy due to aging effects (long term stability), a fourfold improvement in glitch amplitude, and a tenfold reduction in sensitivity to output amplifier offset voltage.

4

SIMPLIFIED BLOCK DIAGRAM



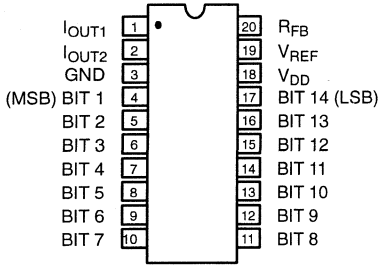
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7614JN	±4	±4	±0.8
Plastic Dip	–40 to +85°C	MP7614KN	±2	±2	±0.8
SOIC	–40 to +85°C	MP7614KS	±2	±2	±0.8
Ceramic Dip	–40 to +85°C	MP7614KD	±2	±2	±0.8
Ceramic Dip	–55 to +125°C	MP7614TD*	±2	±2	±0.8

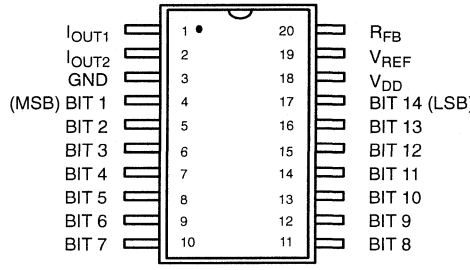
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6
10	BIT 7	Data Input Bit 7

PIN NO.	NAME	DESCRIPTION
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10
14	BIT 11	Data Input Bit 11
15	BIT 12	Data Input Bit 12
16	BIT 13	Data Input Bit 13
17	BIT 14	Data Input Bit 14 (LSB)
18	V_{DD}	Positive Power Supply
19	V_{REF}	Reference Input Voltage
20	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	14			14		Bits	
Integral Non-Linearity[5] (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, S				±4		±4		
K, T				±2		±2		
Differential Non-Linearity[5]	DNL						LSB	
J, S				±4		±4		
K, T				±2		±2		
Gain Error	GE		0.8			±0.8	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		±1.0			±2.0	ppm/°C	ΔGain/ΔTemperature
Non-Linearity Tempco[2]			±0.2			±0.5	ppm/°C	
Differential Linearity Tempco[2]			±0.2			±0.5	ppm/°C	
Power Supply Rejection Ratio	PSRR		±5	±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current[6]	I_{OUT}		±1	±10		±200	nA	
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		2				µs	To 0.01% of FSR; all digital inputs low to high and high to low
Feedthrough at I_{OUT1}	F_T		1	2			mV p-p	V_{REF} = 20 V p-p @ 10 kHz
REFERENCE INPUT								
Input Resistance	R_{IN}	1	3	10	1	10	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1.0		±1.0	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		100				pF	DAC Inputs all 1's
	C_{OUT1}		50				pF	DAC Inputs all 0's
	C_{OUT2}		50				pF	DAC Inputs all 1's
	C_{OUT2}		100				pF	DAC Inputs all 0's
POWER SUPPLY[4]								
Functional Voltage Range[2]	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}		0.4	4		4	mA	All digital inputs = 0 V or all = 5 V

4

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 Specified values guarantee functionality. Refer to other parameters for accuracy.

5 Linearity error is degraded by 65µV for every mV of voltage offset at output amplifier.

6 Output leakage current refers to I_{OUT1}. 1 LSB of current constantly flows into I_{OUT2} (30nA at 5 kΩ input impedance, V_{REF} = +10 V) due to ladder termination into I_{OUT2}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... 0 to +17 V

Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V

I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V

V_{REF} to GND ..... ±25 V

V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

CDIP, PDIP, SOIC 900mW

Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

Refer to Section 8 for Applications Information

MP7616

15 V CMOS
16-Bit Multiplying
Digital-to-Analog Converter

FEATURES

- **Monolithic CMOS Construction**
- **Full Four-Quadrant Multiplication**
- **Excellent Stability Over Temperature and Time**
- **TTL/5 V CMOS Compatible**
- **Guaranteed Monotonic**
- **Low Sensitivity to Output Amplifier Vos**
- **Low Glitch Energy**
- **Buffered Version: MP7626**
- **5 V Version: MP7616B**

GENERAL DESCRIPTION

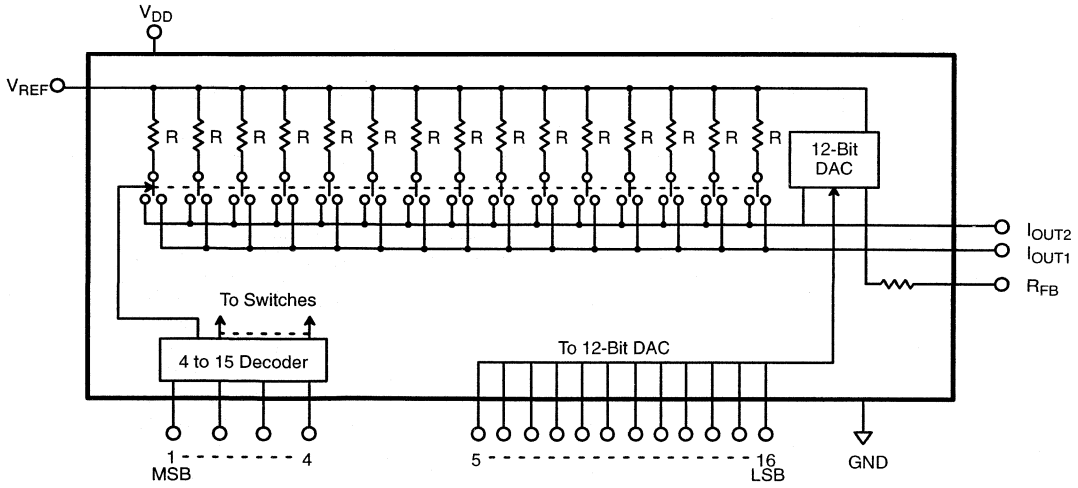
The MP7616 is a high density 16-bit CMOS multiplying Digital-to-Analog Converter. Silicon nitride passivation and untrimmed silicon chromium resistors have been combined to provide long term stability and reliability. Using the most significant bit (MSB) segmentation technique, the MP7616 features 13-bit (0.012%) differential and 12-bit (0.01%) integral linearity.

To achieve 13-bit linearity without laser trim, the MP7616 digitally decodes the four MSB's into 15 equal current sources, rather than the standard binary-weighted sources. Each resistor contributes only 1/16 full scale output thus reducing the matching accuracy requirement of the resistor and CMOS switches from 0.0015% to 0.024%.

The decoding technique achieves an eightfold improvement in differential linearity stability over temperature, an eightfold improvement in relative accuracy due to aging effects (long term stability), a fourfold improvement in glitch amplitude, and a tenfold reduction in sensitivity to output amplifier offset voltage.

4

SIMPLIFIED BLOCK DIAGRAM



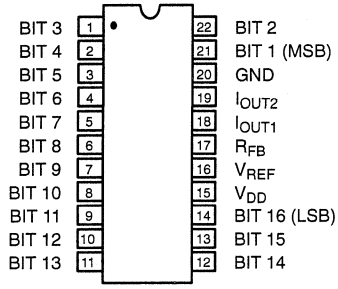
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7616JN	±14	±16	±0.8
Plastic Dip	–40 to +85°C	MP7616KN	±7	±8	±0.8
SOIC	–40 to +85°C	MP7616JS	±14	±16	±0.8
SOIC	–40 to +85°C	MP7616KS	±7	±8	±0.8
Ceramic Dip	–40 to +85°C	MP7616JD	±14	±16	±0.8
Ceramic Dip	–40 to +85°C	MP7616KD	±7	±8	±0.8
Ceramic Dip	–55 to +125°C	MP7616TD*	±7	±8	±0.8

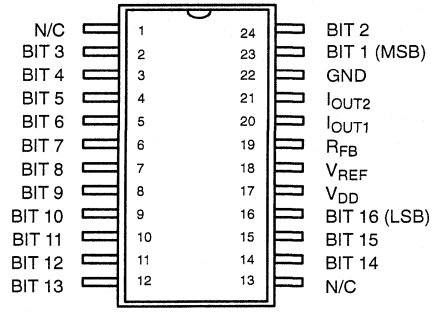
*Contact factory for non-compliant military processing

PIN CONFIGURATION

See Packaging Section for Package Dimensions



22 Pin CDIP, PDIP (0.400")
D22, N22



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

DIP	SOIC	NAME	DESCRIPTION
	1	N/C	No Connection
1	2	BIT 3	Data Input Bit 3
2	3	BIT 4	Data Input Bit 4
3	4	BIT 5	Data Input Bit 5
4	5	BIT 6	Data Input Bit 6
5	6	BIT 7	Data Input Bit 7
6	7	BIT 8	Data Input Bit 8
7	8	BIT 9	Data Input Bit 9
8	9	BIT 10	Data Input Bit 10
9	10	BIT 11	Data Input Bit 11
10	11	BIT 12	Data Input Bit 12
11	12	BIT 13	Data Input Bit 13

DIP	SOIC	NAME	DESCRIPTION
	13	N/C	No Connection
12	14	BIT 14	Data Input Bit 14
13	15	BIT 15	Data Input Bit 15
14	16	BIT 16	Data Input Bit 16 (LSB)
15	17	V_{DD}	Positive Power Supply
16	18	V_{REF}	Reference Input Voltage
17	19	R_{FB}	Internal Feedback Resistor
18	20	I_{OUT1}	Current Output 1
19	21	I_{OUT2}	Current Output 2
20	22	GND	Ground
21	23	BIT 1	Data Input Bit 1 (MSB)
22	24	BIT 2	Data Input Bit 2

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	16			16		Bits	
Integral Non-Linearity[5] (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J				±14		±14		
K, T				±7		±7		
Differential Non-Linearity[5]	DNL						LSB	
J				±16		±16		
K, T				±8		±8		
Gain Error	GE		±0.8				% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2.0	ppm/°C	ΔGain/ΔTemperature
Non-Linearity Tempco[2]						±0.5	ppm/°C	
Differential Linearity Tempco[2]						±0.5	ppm/°C	
Power Supply Rejection Ratio	PSRR		±5	±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current[6]	I_{OUT}		±1	±10		±200	nA	
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		2				µs	To 0.01% of FSR; all digital inputs low to high and high to low
Feedthrough at I_{OUT1}	F_T		1	2			mV p-p	V_{REF} = 10kHz, 20 Vp-p
REFERENCE INPUT								
Input Resistance	R_{IN}	1	3	10	1	10	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1.0		±1.0	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		100				pF	DAC Inputs all 1's
	C_{OUT1}		50				pF	DAC Inputs all 0's
	C_{OUT2}		50				pF	DAC Inputs all 1's
	C_{OUT2}		100				pF	DAC Inputs all 0's
POWER SUPPLY[4]								
Functional Voltage Range[2]	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}		0.4	4		4	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1. Full Scale Range (FSR) is 10V for unipolar mode.
2. Guaranteed but not production tested.
3. Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4. Specified values guarantee functionality. Refer to other parameters for accuracy.
5. Linearity error is degraded by 65µV for every mV of voltage offset at output amplifier.
6. Output leakage current refers to I_{OUT1}. One LSB of current constantly flows into I_{OUT2} (30nA at 5kΩ input impedance, V_{REF} = +10 V) due to ladder termination into I_{OUT2}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 1000mW
Derates above 75°C ..... 13mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

Refer to Section 8 for Applications Information

MP7623

15 V CMOS
Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Pin Compatible with MP7541**
- **12-Bit Linearity**
- **Four Quadrant Multiplication**
- **Low Feedthrough Error**
- **Latch-Up Free**
- **Ultra Stable**
  - **0.2 ppm/°C Max Linearity Tempco**
  - **2 ppm/°C Max Gain Error Tempco**
- **Guaranteed Monotonic Over Temperature**
- **Low Output Capacitance**
  - **C_{OUT1} = 52 pF at full scale, Gives Fastest Settling Times, and Larger Stable Bandwidth Capability**
- **Low (330 µV/mV) Sensitivity to Amplifier Offset**
- **Low Glitch Energy**
- **TTL/CMOS Compatible**
- **Use MP7541B for New Designs**

BENEFITS

- **Better Performance over Temperature**
- **Increased Accuracy**
- **Lower System Cost for Given Accuracy**
- **Faster Operation**

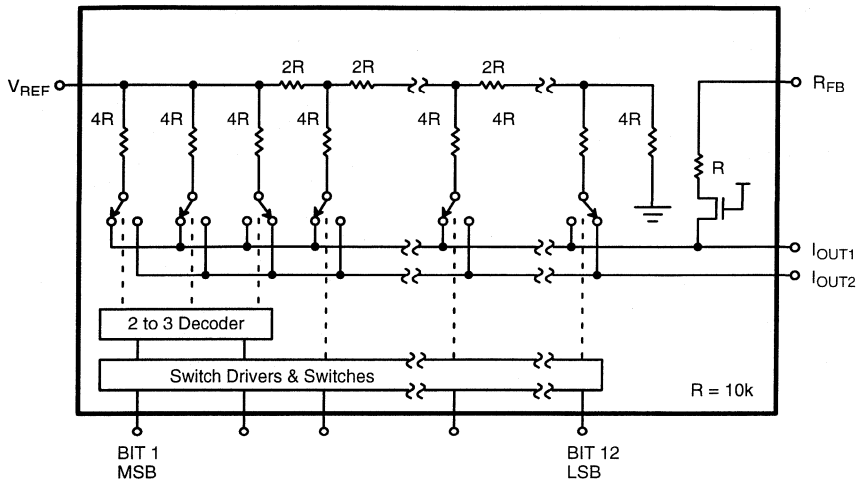
4

GENERAL DESCRIPTION

The MP7623 is a 12-bit Digital-to-Analog Converter with a substantial increase in speed and analog performance over the industry standard 7541. The MP7623 incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal or no trimming. The MP7623 is manufactured using an advanced thin film resistor and double metal CMOS process. Outstanding features include:

- Stability: Both integral and differential linearity tempco are rated at 0.2 ppm/°C maximum, and monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. Scale factor tempco is a low 2 ppm/°C maximum.
- Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at Iout1 is a low 52 pF/26 pF and 13pF / 45 pF at I_{OUT2} for the conditions full-scale/zero. This is four times less than the 7541. Lower capacitance allows the MP7623 to achieve faster CMOS DAC settling times; less than 1 µs for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available (for a given amplifier loop gain) because a smaller feedback "zero" compensating capacitor is required to offset the smaller I_{OUT} capacitance.
- Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP7623 over conventional R-2R DACs, to 330µV per millivolt of offset.

SIMPLIFIED BLOCK DIAGRAM



3 Segment D/A Converter with Termination to DGND
Logical "1" at Digital Input Steers Current to I_{OUT1}

ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7623JN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP7623KN	±1/2	±1/2	±0.4
SOIC	–40 to +85°C	MP7623JS	±1	±1	±0.4
SOIC	–40 to +85°C	MP7623KS	±1/2	±1/2	±0.4
PLCC	–40 to +85°C	MP7623JP	±1	±1	±0.4
PLCC	–40 to +85°C	MP7623KP	±1/2	±1/2	±0.4
Ceramic Dip	–40 to +85°C	MP7623AD	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP7623BD	±1/2	±1/2	±0.4
Ceramic Dip	–55 to +125°C	MP7623SD*	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP7623TD*	±1/2	±1/2	±0.4

*Contact factory for non-compliant military processing

MP7626

Microprocessor Compatible
Buffered Multiplying 16-Bit
Digital-to-Analog Converter

FEATURES

- **Four Quadrant Multiplication**
- **16-Bit Monotonicity**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Single-Buffered or Transparent Data inputs**
- **Decoded DAC Approach**
- **Latch-Up Free**
- **8-Bit Bus Version: MP7636A**

APPLICATIONS

- **Digitally Programmable References**
- **Programmable Audio Attenuator**
- **High Accuracy Process Control Systems**
- **Automatic Test Equipment**
- **Easy Interface to 8 and 16-Bit Microprocessor Buses**

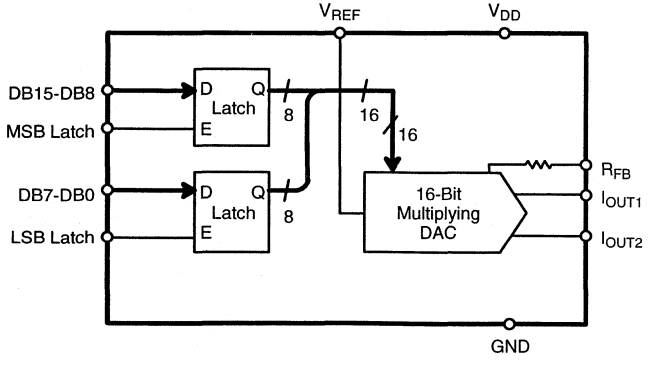
4

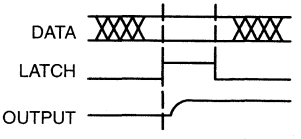
GENERAL DESCRIPTION

The MP7626 is a CMOS 16-bit Digital-to-Analog Converter (DAC) that is manufactured using advanced thin film resistors on a double metal CMOS process. It incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 16 bit differential non-linearity is achieved with minimal trimming.

Two 8-bit latches (MSB latch and LSB latch) hold the 16-bit data which are converted by the DAC. A 16-bit bus can load both latches in one cycle. An 8-bit bus loads one latch at a time. By making the latches transparent (MSB latch = LSB latch = High) the DAC will continuously convert the BIT1 - BIT16 inputs.

SIMPLIFIED BLOCK AND TIMING DIAGRAM





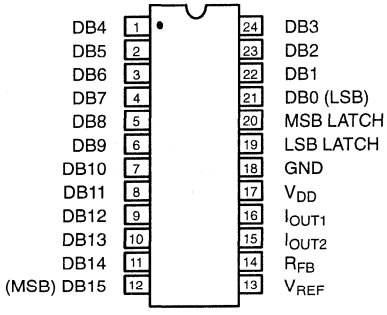
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7626JN	±4	±4	±0.1
Plastic Dip	–40 to +85°C	MP7626KN	±2	±2	±0.1
PLCC	–40 to +85°C	MP7626JP	±4	±4	±0.1
PLCC	–40 to +85°C	MP7626KP	±2	±2	±0.1
Ceramic Dip	–40 to +85°C	MP7626JD*	±4	±4	±0.1
Ceramic Dip	–40 to +85°C	MP7626KD*	±2	±2	±0.1

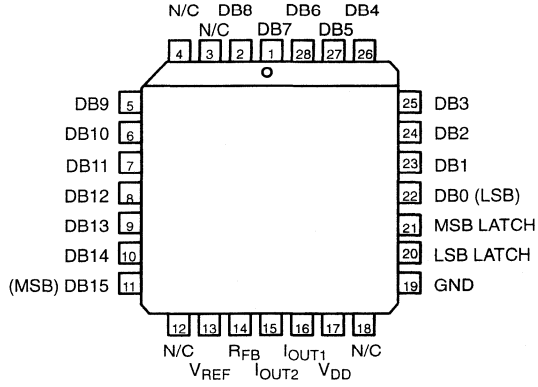
*Recommend using MP7626KN or JN

PIN CONFIGURATION

See Packaging Section for Package Dimensions



24 Pin PDIP, CDIP (0.600")
N24, D24, C24



28 Pin PLCC
P28

PIN OUT DEFINITIONS

DIP	PLCC	NAME	DESCRIPTION
1	26	DB4	Data Input Bit 4
2	27	DB5	Data Input Bit 5
3	28	DB6	Data Input Bit 6
4	1	DB7	Data Input Bit 7
5	2	DB8	Data Input Bit 8
6	5	DB9	Data Input Bit 9
7	6	DB10	Data Input Bit 10
8	7	DB11	Data Input Bit 11
9	8	DB12	Data Input Bit 12
10	9	DB13	Data Input Bit 13
11	10	DB14	Data Input Bit 14
12	11	DB15	Data Input Bit 15 (MSB)

DIP	PLCC	NAME	DESCRIPTION
13	13	V_{REF}	Reference Input Voltage
14	14	R_{FB}	Internal Feedback Resistor Pin
15	15	I_{OUT2}	Current Output 2
16	16	I_{OUT1}	Current Output 1
17	17	V_{DD}	Power Supply
18	19	GND	Ground
19	20	LSB	LSB Latch Enable
20	21	MSB	MSB Latch Enable
21	22	DB0	Data Input Bit 0 (LSB)
22	23	DB1	Data Input Bit 1
23	24	DB2	Data Input Bit 2
24	25	DB3	Data Input Bit 3

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	16			16		Bits	
Relative Accuracy	INL						LSB	Best Fit Straight Line Spec.
J				±4		±4		(Max INL – Min INL) / 2
K				±2		±2		
Differential Non-Linearity	DNL						LSB	
J				±4		±4		
K				±2		±2		
Gain Error	GE			±0.1		±0.1	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±10		±200	nA	I_{OUT1}
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S		2				µs	Full Scale Change to 0.1%
AC Feedthrough at I_{OUT1}	F_T		2				mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	2.5		7.5	2.5	7.5	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
Input Capacitance[2]								
Data	C_{IN}		5				pF	
Control	C_{IN}		5				pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			280			pF	DAC Inputs all 1's
	C_{OUT1}			120			pF	DAC Inputs all 0's
	C_{OUT2}			100			pF	DAC Inputs all 1's
	C_{OUT2}			240			pF	DAC Inputs all 0's
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	4.5		16.5	5.0	16.5	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V or all = 5 V

4

ELECTRICAL CHARACTERISTICS (CON'T)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Data Valid to Write Set-Up Time	t_{DS}	250					ns	
Write Strobe Width	t_{SW}	125					ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

Supply Voltage ..... +17 V_{DC}
Voltage at Any Digital Input ..... GND –0.5 to V_{DD} +0.5 V
DC Voltage Applied to I_{OUT1} or I_{OUT2} .. GND –0.5 to +17 V
Voltage at V_{REF}, R_{FB} Inputs ..... ±25 V

Storage Temperature Range ..... –65°C to 150°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, PLCC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

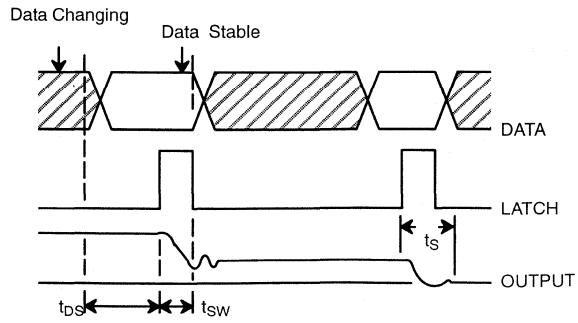
APPLICATION NOTES

Refer to Applications Section for Additional Information

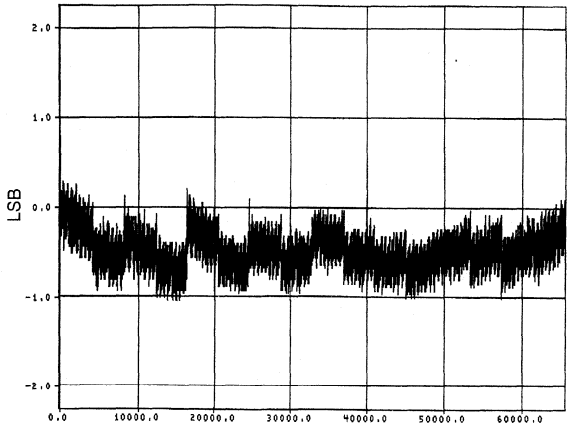
LATCH CONTROL

MSB LATCH	LSB LATCH	FUNCTION
0	0	Data Latched (Held)
1	0	Transfer (DB15-DB8) to DAC
0	1	Transfer (DB7-DB0) to DAC
1	1	Transparent Mode

TIMING DIAGRAM



PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code

4

APPLICATION NOTES

Refer to Section 8 for Applications Information

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MP7628

5 V CMOS
Quad Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **Readback Capability for all DACs**
- **On-Chip Latches for All DACs**
- **Linearity Grades to ±1/8 LSB**
- **Single Supply Voltage (5 Volt)**
- **DACs Matched to 1%**
- **Four Quadrant Multiplication**
- **Microprocessor TTL/CMOS Compatible**
- **Latch-Up Free**
- **Dual Version: MP7529B**

APPLICATIONS

- **Microprocessor Controlled Gain and Attenuation Circuits**
- **Microprocessor Controlled/Programmable Power Supplies**
- **Hardware Redundant Applications Requiring Data Readback**

GENERAL DESCRIPTION

The MP7628 is a quad 8-bit Digital-to-Analog Converter designed using a decoded DAC architecture featuring excellent DAC-to-DAC matching and guaranteed monotonicity.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

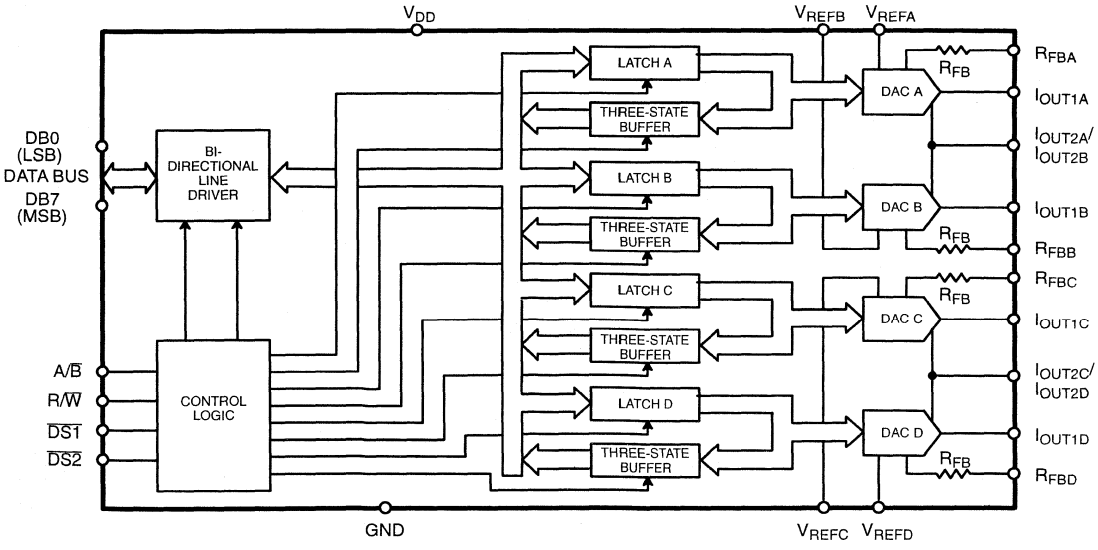
The readback function allows the user to poll or read the data latches, eliminating the need for storing information in RAM. In the event the microprocessor power supply is interrupted, it can poll the DACs to establish the last known system state.

Data is transferred into any of the four DAC data latches via common 8-bit TTL/CMOS compatible input port. Control inputs $\overline{DS1}$, $\overline{DS2}$ and A/$\overline{B}$ determine which DAC is to be loaded. The MP7628's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors.

The device operates at +5 V power supply and dissipates less than 5mW.

All DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

SIMPLIFIED BLOCK DIAGRAM



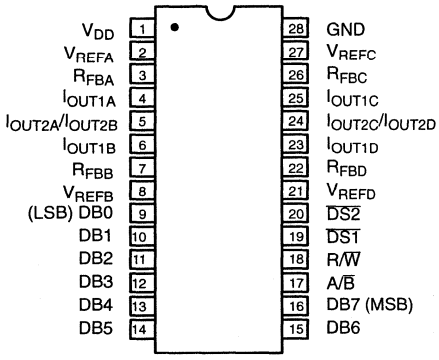
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7628JN	±1/2	±1/2	±1.8
Plastic Dip	–40 to +85°C	MP7628KN	±1/4	±1/4	±0.9
SOIC	–40 to +85°C	MP7628JS	±1/2	±1/2	±1.8
SOIC	–40 to +85°C	MP7628KS	±1/4	±1/4	±0.9
PLCC	–40 to +85°C	MP7628JP	±1/2	±1/2	±1.8
PLCC	–40 to +85°C	MP7628KP	±1/4	±1/4	±0.9
Ceramic Dip	–40 to +85°C	MP7628AD	±1/2	±1/2	±1.8
Ceramic Dip	–40 to +85°C	MP7628BD	±1/4	±1/4	±0.9
Ceramic Dip	–55 to +125°C	MP7628SD*	±1/2	±1/2	±1.8
Ceramic Dip	–55 to +125°C	MP7628TD*	±1/4	±1/4	±0.9

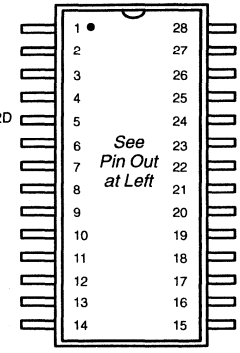
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

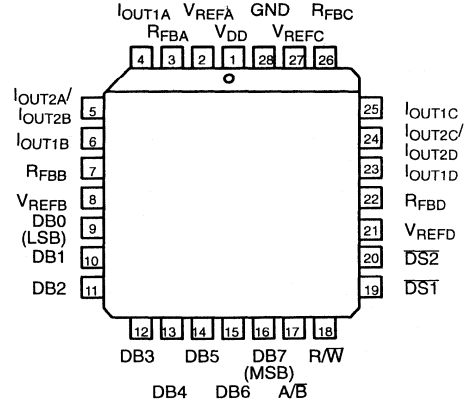
See Packaging Section for Package Dimensions



28 Pin CDIP, PDIP (0.600")
D28, N28



28 Pin SOIC (Jedec, 0.300")
S28



28 Pin PLCC
P28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{DD}	Power Supply
2	V_{REFA}	Reference Voltage for DAC A
3	R_{FBA}	Feedback Resistor for DAC A
4	I_{OUT1A}	Current Output 1 DAC A
5	I_{OUT2A}/ I_{OUT2B}	Current Output 2 DAC A/DAC B
6	I_{OUT1B}	Current Output 1 DAC B
7	R_{FBB}	Feedback Resistor for DAC B
8	V_{REFB}	Reference Voltage for DAC B
9	DB0	Data Input Bit 0 (LSB)
10	DB1	Data Input Bit 1
11	DB2	Data Input Bit 2
12	DB3	Data Input Bit 3
13	DB4	Data Input Bit 4
14	DB5	Data Input Bit 5
15	DB6	Data Input Bit 6
16	DB7	Data Input Bit 7 (MSB)
17	$A/\overline{B}$	DAC Selection
18	$R/\overline{W}$	Read/Write
19	$\overline{DS1}$	Control 1
20	$\overline{DS2}$	Control 2
21	V_{REFD}	Reference Voltage for DAC D
22	R_{FBD}	Feedback Resistor for DAC D
23	I_{OUT1D}	Current Output 1 DAC D
24	I_{OUT2C}/ I_{OUT2D}	Current Output 2 DAC C/DAC D
25	I_{OUT1C}	Current Output 1 DAC C
26	R_{FBC}	Feedback Resistor for DAC C
27	V_{REFC}	Reference Voltage for DAC C
28	GND	Ground

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
Gain Error	GE						% FSR	Using Internal R_{FB}
J, A, S				±1.5		±1.8		Digital Inputs = V_{INH}
K, B, T				±0.8		±0.9		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±200		±400	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5% Digital Inputs = V_{INH}
Output Leakage Current (all)	I_{OUT1}			±50		±200	nA	Digital Inputs = V_{INL}
REFERENCE INPUT								
Voltage Range[2]				±20		±20	V	
Input Resistance	R_{IN}	12		28	12	28	kΩ	
DIGITAL INPUTS[3]								
Logic Thresholds								
V_{INH}		2.4			2.4		V	
V_{INL}				0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]	C_{IN}		3				pF	
DATA BUS OUTPUTS								
Output Capacitance[2]	C_{OUT}		7				pF	
Input Leakage Current	I_{LKG}			±1		±10	µA	
ANALOG OUTPUTS								
Propagation Delay[2]		500			750		ns	From digital input to 90% of final analog output current
Output Capacitance[2]								
	C_{OUT}		120				pF	DAC Inputs all 1's
	C_{OUT}		80				pF	DAC Inputs all 0's
Glitch Energy[2]		160			440		nVs	Typical for code transition from all 0's to all 1's

ELECTRICAL CHARACTERISTICS (CON'T)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[5]								
Functional Voltage Range[2]	V_{DD}	4.5		5.5	4.5	5.5	V	
Supply Current	I_{DD}			50		50	µA	All digital inputs = 0 V or all = 5 V
SWITCHING CHARACTERISTICS[2, 4]								
Data Write Time	t_W	320			400		ns	
Write Strobe Req.	t_{DSW}	200			250		ns	
Data Hold Time	t_{DHLD}	40			50		ns	
Data Read Time	t_R	480			600		ns	
3-state Hold Time	t_{TSHD}	240			300		ns	
Read Strobe Req.	t_{DSR}	320			400		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagrams.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

4

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

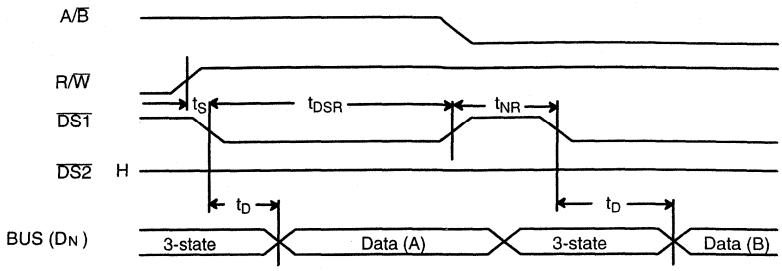
V_{DD} to GND ..... +7 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND (2) ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

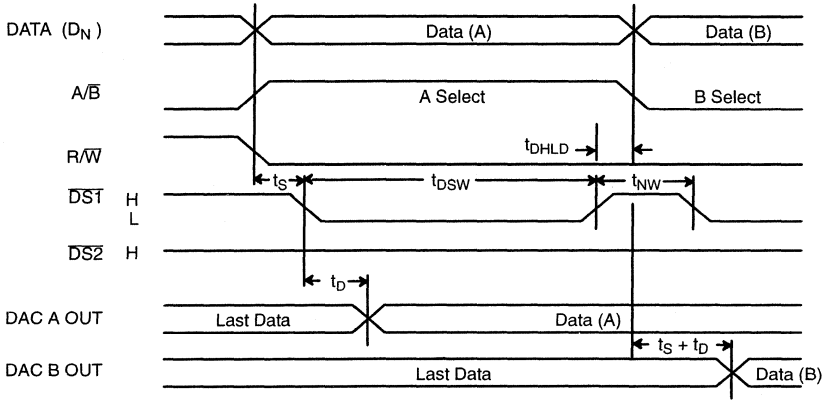
TIMING DIAGRAM READ CYCLE



Set up time for BUS, A/B, R/W	= 40 ns	t_S
Minimum DS = low pulse	= 320 ns	t_{DSR} (min)
Minimum time between DS = low pulses	= 120 ns	t_{NR}
Data delay time	= 200 ns	t_D

$t_R = t_{DSR} + t_{NR}$

TIMING DIAGRAM WRITE CYCLE



Set up time for BUS, A/B, R/W	= 40 ns	t_S
Minimum DS = low pulse	= 200 ns	t_{DSW} (min)
Minimum time between DS = low pulses	= 120 ns	t_{NW}
Data delay time	= 110 ns	t_D

$t_W = t_{DSW} + t_{NW}$

MODE SELECTION TABLE

DS1	DS2	A/B	R/W	MODE	DAC
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A & C
L	L	L	L	WRITE	B & D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = LOW STATE
H = HIGH STATE
X = DON'T CARE

INTERFACE LOGIC INFORMATION

DAC Selection: All DAC latches share a common 8-bit input port. The control inputs $\overline{DS1}$, $\overline{DS2}$, A/$\overline{B}$ select which DAC can accept data from the input port.

Mode Selection: Inputs $\overline{DS}$ and R/$\overline{W}$ control the operating mode of the selected DAC. *See Mode Selection Table on the previous page.*

Write Mode: When $\overline{DS}$ and R/$\overline{W}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7.

Hold Mode: The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{DS}$ and R/$\overline{W}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When $\overline{DS}$ is low and R/$\overline{W}$ is high, the selected DAC is in the read mode and the data held in the appropriate latch is outputed to the data bus.

APPLICATION NOTES

Refer to Section 8 for Applications Information

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MP7633

15 V CMOS
10-Bit Multiplying
Digital-to-Analog Converter

FEATURES

- Full Four-Quadrant Multiplying DAC
- Guaranteed Monotonic over Temperature
- Non-Linearity: ±1/2 LSB Achieved without Trimming
- Ultra Stable: 0.2 ppm/°C Max Linearity Tempco
- 2 ppm/°C Max Gain Error Tempco
- Low Output Capacitance
- Low Sensitivity to Amplifier Offset 330 μV/mV
- Low Glitch Energy
- Low Feedthrough Error
- TTL/5 V CMOS Compatible
- Latch-Up Free
- Improved Replacement for AD7533, AD7520
- Low Cost

APPLICATIONS

- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control

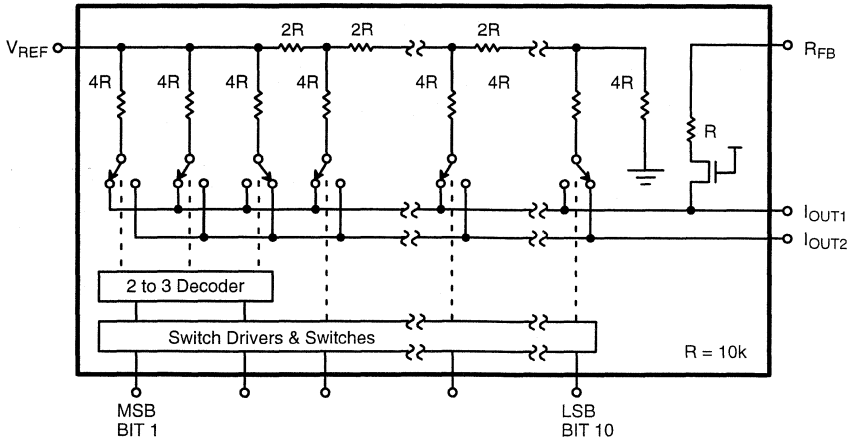
4

GENERAL DESCRIPTION

The MP7633 is pin and functionally equivalent to industry's standard AD7533, AD7520 and AD7530. The MP7633 is recommended when lower output capacitance is required. The MP7633 incorporates a unique decoding technique yielding excellent accuracy and stability (0.2 ppm/°C linearity drift and 2 ppm/°C scale factor drift) over temperature and time.

The 2-3 bit decoding architecture of the MP7633 results in low output capacitances of 52/26pF at I_{OUT1} and 13/45pF at I_{OUT2}, low sensitivity to output amplifier offset of 330 μV per millivolt offset, eliminating the need for trim pots in many applications.

SIMPLIFIED BLOCK DIAGRAM



3 Segment D/A Converter with Termination to GND.
Logical "1" at Digital Input Steers Current to I_{OUT1}

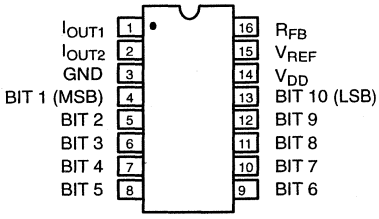
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7633JN	±2	±2	±0.4
Plastic Dip	–40 to +85°C	MP7633KN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP7633LN	±1/2	±1/2	±0.4
SOIC	–40 to +85°C	MP7633JS	±2	±2	±0.4
SOIC	–40 to +85°C	MP7633KS	±1	±1	±0.4
SOIC	–40 to +85°C	MP7633LS	±1/2	±1/2	±0.4
PLCC	–40 to +85°C	MP7633JP	±2	±2	±0.4
PLCC	–40 to +85°C	MP7633KP	±1	±1	±0.4
PLCC	–40 to +85°C	MP7633LP	±1/2	±1/2	±0.4
Ceramic Dip	–40 to +85°C	MP7633AD	±2	±2	±0.4
Ceramic Dip	–40 to +85°C	MP7633BD	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP7633CD	±1/2	±1/2	±0.4
Ceramic Dip	–55 to +125°C	MP7633SD*	±2	±2	±0.4
Ceramic Dip	–55 to +125°C	MP7633TD*	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP7633UD*	±1/2	±1/2	±0.4

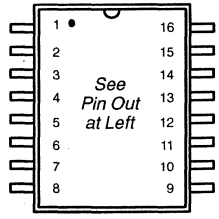
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

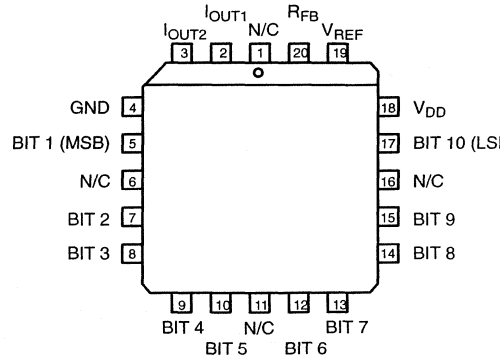
See Packaging Section for Package Dimensions



16 Pin CDIP, PDIP (0.300")
D16, N16



16 Pin SOIC (Jedec, 0.300")
S16



20 Pin PLCC
P20

PIN OUT DEFINITIONS

16 Pin CDIP, PDIP, SOIC

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10 (LSB)
14	V_{DD}	Positive Power Supply
15	V_{REF}	Reference Input Voltage
16	R_{FB}	Internal Feedback Resistor

20 Pin PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	I_{OUT1}	Current Output 1
3	I_{OUT2}	Current Output 2
4	GND	Ground
5	BIT 1	Data Input Bit 1 (MSB)
6	N/C	No Connection
7	BIT 2	Data Input Bit 2
8	BIT 3	Data Input Bit 3
9	BIT 4	Data Input Bit 4
10	BIT 5	Data Input Bit 5
11	N/C	No Connection
12	BIT 6	Data Input Bit 6
13	BIT 7	Data Input Bit 7
14	BIT 8	Data Input Bit 8
15	BIT 9	Data Input Bit 9
16	N/C	No Connection
17	BIT 10	Data Input Bit 10 (LSB)
18	V_{DD}	Positive Power Supply
19	V_{REF}	Reference Input Voltage
20	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	10			10		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C, U				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C, U				±1/2		±1/2		
Gain Error	GE		±0.3	±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		±5	±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$, ΔV_{DD} = ±5%
Output Leakage	I_{OUT}		<1	±10		±200	nA	I_{OUT1} V_{IN} = 0 V I_{OUT2} V_{IN} = V_{DD}
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		500	1000			ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T			1			mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
Voltage Input Range[2]			±10	±25			V	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			+0.8		+0.8	V	
Input Leakage Current	I_{LKG}			±1.0		±1.0	µA	V_{IN} = 0 V and V_{DD}
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT1}			52			pF	DAC Inputs all 1's
	C_{OUT1}			26			pF	DAC Inputs all 0's
	C_{OUT2}			13			pF	DAC Inputs all 1's
	C_{OUT2}			45			pF	DAC Inputs all 0's
Scale Factor[2]			100				µA/V_{REF}	
POWER SUPPLY[4]								
Functional Voltage Range[2]	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or all = 5 V, 15 V

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital Input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

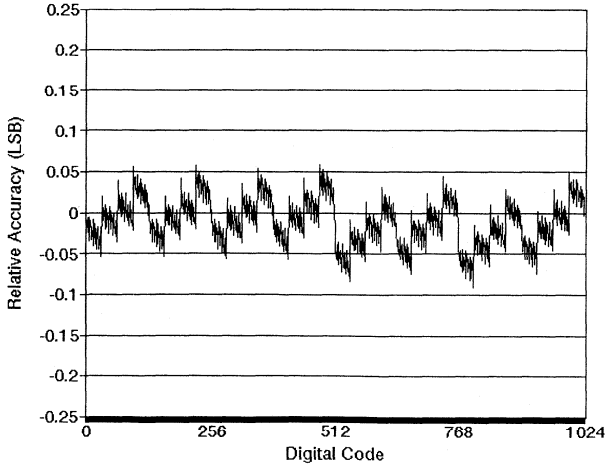
V_{DD} to GND ..... –0.5, +17 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND (2) ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 800mW
Derates above 75°C ..... 11mW/°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

4

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information

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MP7636A

15 V CMOS Microprocessor Compatible Double-Buffered, Multiplying 16-Bit Digital-to-Analog Converter

FEATURES

- **Four Quadrant Multiplication**
- **16-Bit Monotonicity**
- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **Low Feedthrough Error**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Double Buffered**
- **Decoded DAC Approach**
- **Latch-Up Free**

BENEFITS

- **High Accuracy Performance at Low Cost**
- **Easy Interface with 8-Bit Microprocessors**
- **Simple Upgrade of MP1230A Family to High Accuracy (Pin Compatible)**
- **Reduced Board Space**
- **16-Bit Bus Version: MP7626**

GENERAL DESCRIPTION

The MP7636A is manufactured using advanced thin film resistors on a double metal CMOS process. The MP7636A incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 16-bit differential non-linearity is achieved with minimal laser trim.

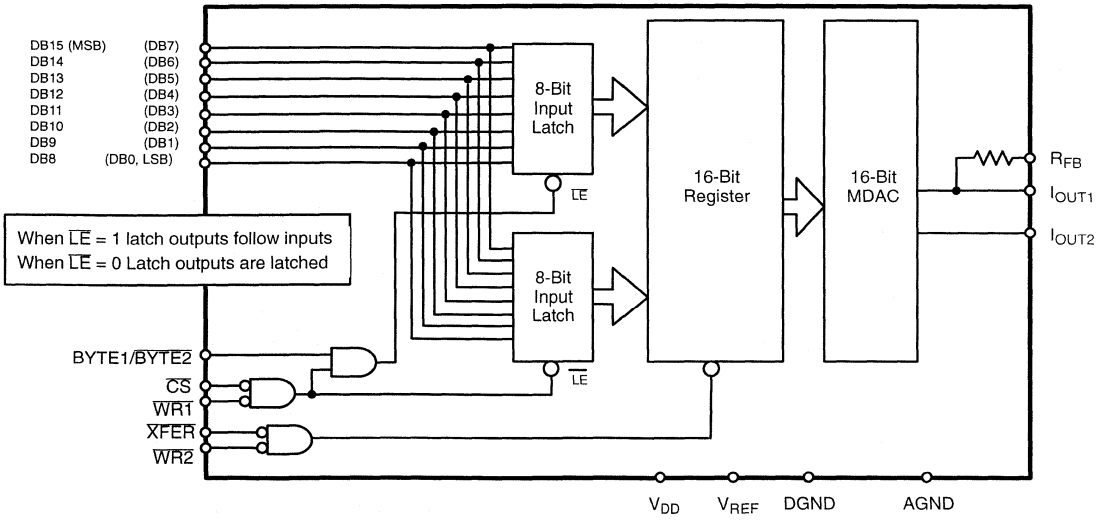
The MP7636A is packaged in a 20-pin 300 mil wide DIP and is a direct 16-bit replacement for the 12-bit DAC1230 series. Full pin-for-pin compatibility allows existing systems to be upgraded to 16 bits without hardware modification.

The MP7636A provides 16-bit data loading through 8 input data lines for direct interface to 8-bit data buses. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP7636A uses a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$ = 1.

4

SIMPLIFIED BLOCK DIAGRAM



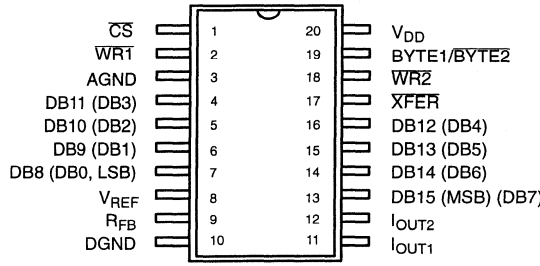
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	–40 to +85°C	MP7636AJS	±4	±4	0.1
SOIC	–40 to +85°C	MP7636AKS	±2	±2	0.1

*Contact factory for non-compliant military processing

PIN CONFIGURATION

See Packaging Section for Package Dimensions



20 Pin SOIC (Jedec, 0. 300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{CS}$	Chip Select (Active Low)
2	$\overline{WR1}$	Write1 (Active Low)
3	AGND	Analog Ground
4	DB11 (DB3)	Data Input Bit 11 (MSB) Data Input Bit 3
5	DB10 (DB2)	Data Input Bit 10 Data Input Bit 2
6	DB9 (DB1)	Data Input Bit 9 Data Input Bit 1
7	DB8 (DB0)	Data Input Bit 8 Data Input Bit 0 (LSB)
8	V_{REF}	Reference Input Voltage
9	R_{FB}	Internal Feedback Resistor
10	DGND	Digital Ground
11	I_{OUT1}	Current Output 1

PIN NO.	NAME	DESCRIPTION
12	I_{OUT2}	Current Output 2
13	DB15 (MSB) (DB7)	Data Input Bit 15 (Most Significant Bit) Data Input Bit 7
14	DB14 (DB6)	Data Input Bit 14 Data Input Bit 6
15	DB13 (DB5)	Data Input Bit 13 Data Input Bit 5
16	DB12 (DB4)	Data Input Bit 12 Data Input Bit 4
17	$\overline{XFER}$	Transfer Control Signal (Active Low)
18	$\overline{WR2}$	Write 2 (Active Low)
19	BYTE1/ $\overline{BYTE2}$	Byte Sequence Control
20	V_{DD}	Power Supply

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	16			16		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, S				±4		±4		
K, L, T				±2		±2		
Differential Non-Linearity	DNL						LSB	All grades guaranteed monotonic over full operating temperature range.
J, S				±4		±4		
K, T				±2		±2		
L				±1		±2		
Gain Error	GE			±0.1		±0.1	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±10		±200	nA	I_{OUT1} only
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		2				µs	To 1/2 LSB R_L=100Ω, C_{EXT}=13pF
AC Feedthrough at I_{OUT1}	F_T		2				mV p-p	V_{REF} = 20 V p-p Sine wave @ 10kHz
REFERENCE INPUT								
Input Resistance	R_{IN}	2.5		7.5	2.5	7.5	kΩ	
LOGIC INPUTS[3]								
Input High Voltage	V_{INH}	3.0	2.4		3.0		V	
Input Low Voltage	V_{INL}			0.8		0.8	V	
Input Current	I_{LKG}			±1		±1	µA	
Input Capacitance								
Data	C_{IN}		5				pF	
Control	C_{IN}		5				pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			280			pF	DAC all 1's
	C_{OUT1}			120			pF	DAC all 0's
	C_{OUT2}			100			pF	DAC all 1's
	C_{OUT2}			240			pF	DAC all 0's

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[5]								
Functional Voltage Range[2]	V_{DD}	4.5		16.5	5.0	16.5	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs 0 V or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
$\overline{CS}$ to $\overline{WR}$ Set-Up Time	t_{CS}	150					ns	
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CH}	10					ns	
Data Valid to $\overline{WR}$ Set-Up Time	t_{DS}	70					ns	
Data Valid to $\overline{WR}$ Hold Time	t_{DH}	70					ns	
$\overline{WR}$, $\overline{XFER}$ Pulse Width	t_W	150					ns	

NOTES:

(1) Full Scale Range (FSR) is 10V for unipolar mode.
(2) Guaranteed but not production tested.
(3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
(4) See timing diagram.
(5) Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

Voltage at Any Digital Input ..... GND –0.5 to V_{DD} +0.5 V
Voltage at V_{REF} Input ..... ±25 V
DC Voltage Applied to I_{OUT1} or I_{OUT2} GND –0.5 V to +17 V
Supply Voltage (V_{DD}) ..... +17 V_{DC}

AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)
Storage Temperature Range ..... –65°C to 150°C
Package Power Dissipation Rating to 75°C
SOIC 900mW
Derates above 75°C ..... 12mW/°C

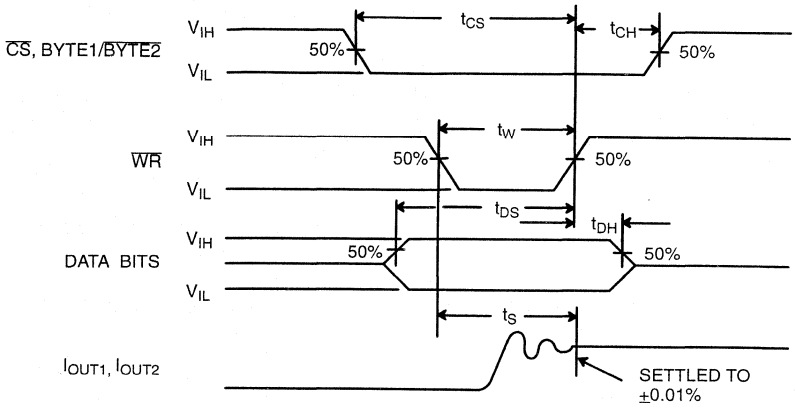
NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

APPLICATION NOTES

Refer to Section 8 for Applications Information

TIMING DIAGRAM



DEFINITION OF CONTROL SIGNALS:

$\overline{CS}$: Chip Select (Active low).
It will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1 (Active low)
The $\overline{WR1}$ is used to load the digital data bits (DB) into the input latch.

BYTE1/$\overline{BYTE2}$: Byte sequence control.
The BYTE1/$\overline{BYTE2}$ control pin is used to select MSB and LSB both input latches.

$\overline{WR2}$: Write 2 (Active low).
It will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer control signal (Active low).
This signal, in combination with $\overline{WR2}$, causes the 16-bit data which is available in the input latches to transfer to the DAC register.

DB0 to DB15: Digital Inputs.
DB0 is the least significant digital input (LSB) and DB15 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1 Bus.
I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in the DAC register.

I_{OUT2}: DAC Current Output 2 Bus.
I_{OUT2} is a complement of I_{OUT1}. The ladder termination has been tied to I_{OUT2} internally.

R_{FB}: Feedback Resistor.
This internal feedback resistor should always be used (not an external resistor) since it matches the resistors in the DAC and tracks these resistor over temperature.

V_{REF}: Reference Voltage Input.
This input connects an external precision voltage source to the internal DAC. The V_{REF} can be selected over the range of +25V to –25V or the analog signal for a 4-quadrant multiplying mode application.

V_{DD}: Power Supply Voltage.
This is the power supply pin for the part. The V_{DD} can be from +5 V DC to +15 V DC, however optimum voltage is +15 V DC.

AGND: Analog Ground.
Back gate of the DAC N-channel current steering switches.

DGND: Digital Ground .

The timing diagrams for updating the DAC register are shown in *Figures 1* and *2.*

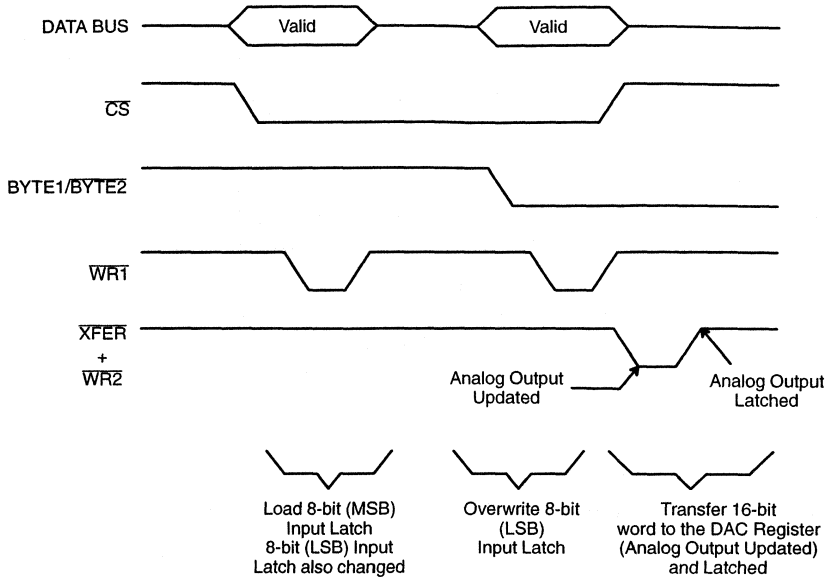


Figure 1. Typical Interface with an 8-bit Data Bus

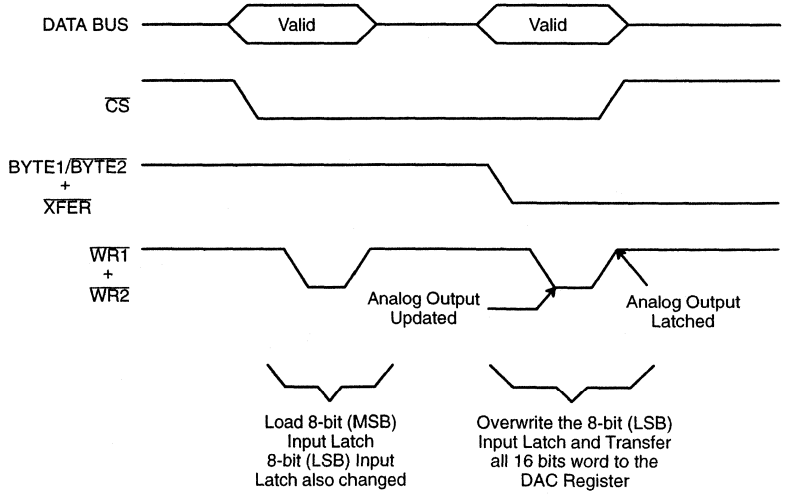
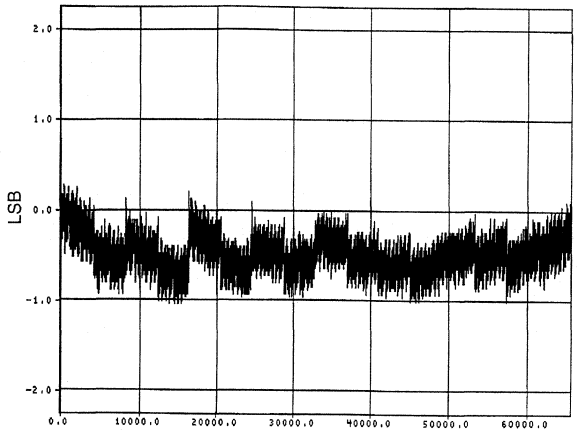


Figure 2. Automatic Transfer



Graph 1. Relative Accuracy vs. Digital Code

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MP7641

8-Channel Voltage Output
10 MHz Input Bandwidth 8-Bit
Multiplying DACs with
Serial Digital Port

FEATURES

- **8 Independent 2-Quadrant Multiplying 8-Bit DACs**
- **Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability**
- **High Speed:**
  - **12.5 MHz Digital Clock Rate**
  - **V_{REF} to V_{OUT} Settling Time: 150ns to 8–bit (typ)**
  - **Voltage Reference Input Bandwidth: 10 MHz**
- **Low Power: 150mW**
- **Low AC Voltage Reference Feedthrough**
- **Excellent Channel-to-Channel Isolation**
- **DNL = ±0.8 LSB, INL = ±1 LSB (typ)**
- **DACs Matched to ±0.5% (typ)**
- **Chip Select Available: MP7651**
- **Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz**
- **V_{REF}/2 Output Preset Level**
- **Latch-Up Free**
- **ESD Protection: 2000 V Minimum**

APPLICATIONS

- **Direct High-Frequency Automatic Gain Control**
- **Video AGC & CCD Level AGC**
- **Convergence Adjustment for High-Resolution Monitors (Workstations)**

4

GENERAL DESCRIPTION

The MP7641 is ideal for direct gain control of video, composite video, CCD and other high frequency analog signals. The device includes 8-channels of high speed, high bandwidth, two quadrant multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving a ±1mA (typ) to a load. DNL of better than ±0.8 LSB is achieved with a channel-to-channel matching of better than 0.5% (typ). Stability, matching, and precision of the DACs are achieved by using EXAR's thin film technology. Also, excellent channel-to-channel isolation is achieved with EXAR's BiCMOS process which cannot be achieved using a typical CMOS technology.

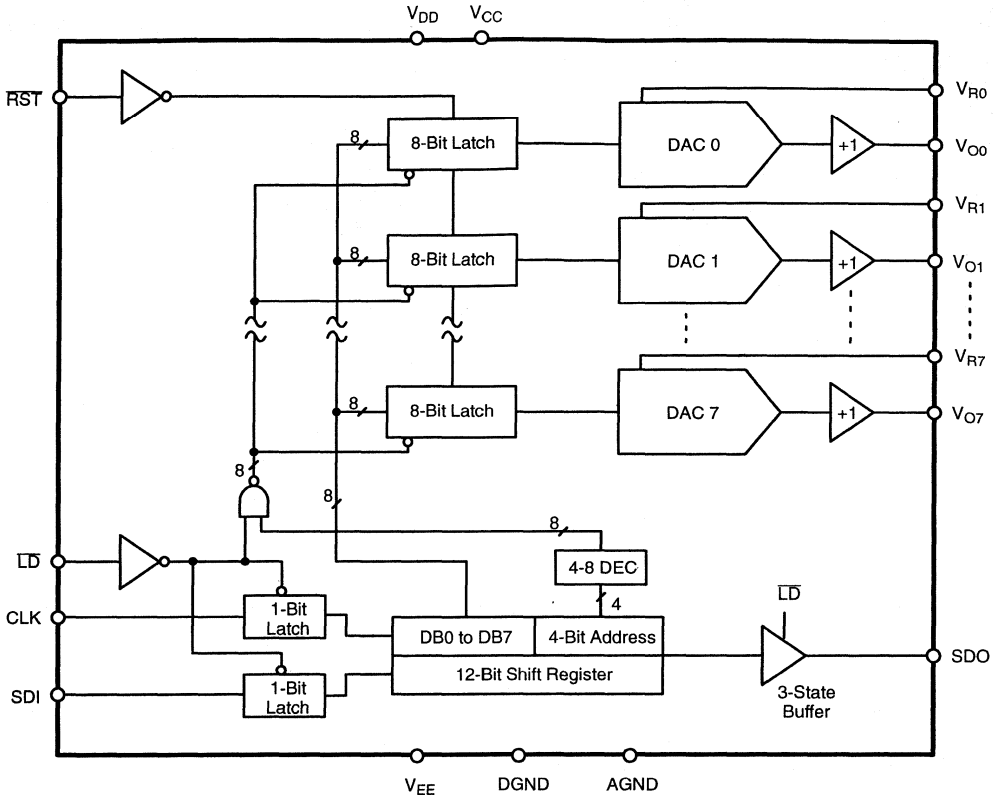
An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 10 MHz (typ), fast output settling time, and V_{REF} feedthrough isolation of –65dB or better. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal is achieved.

The combination of a constant input Z and the ability to vary AGND within ±300 mV allows flexibility for optimum system design.

The MP7641 has a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire (space).

The MP7641 is fabricated on a junction isolated, high speed BiCMOS (BiCMOS IV™) process with thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

SIMPLIFIED BLOCK DIAGRAM©

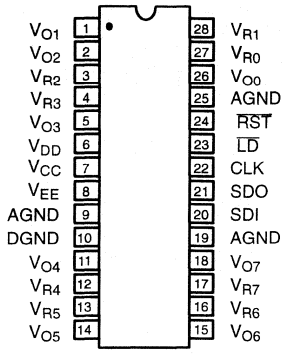


ORDERING INFORMATION

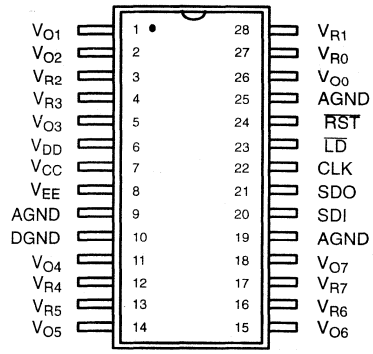
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	–40 to +85°C	MP7641AS	±1	±0.8	±1.5
Plastic Dip	–40 to +85°C	MP7641AN	±1	±0.8	±1.5

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (EIAJ, 0.335")
R28

4

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{O1}	DAC 1 Output
2	V_{O2}	DAC 2 Output
3	V_{R2}	DAC 2 Reference Input
4	V_{R3}	DAC 3 Reference Input
5	V_{O3}	DAC 3 Output
6	V_{DD}	Digital Positive Supply
7	V_{CC}	Analog Positive Supply
8	V_{EE}	Analog Negative Supply
9	AGND	Analog Ground
10	DGND	Digital Ground
11	V_{O4}	DAC 4 Output
12	V_{R4}	DAC 4 Reference Input
13	V_{R5}	DAC 5 Reference Input
14	V_{O5}	DAC 5 Output
15	V_{O6}	DAC 6 Output

PIN NO.	NAME	DESCRIPTION
16	V_{R6}	DAC 6 Reference Input
17	V_{R7}	DAC 7 Reference Input
18	V_{O7}	DAC 7 Output
19	AGND	Analog Ground
20	SDI	Serial Data/Address Input
21	SDO	Serial Data Output
22	CLK	Shift Register Clock
23	$\overline{LD}$	Load Signal; Load Data to Selected DACs
24	$\overline{RST}$	Reset Signal; Reset all DACs to $V_{REF}/2$
25	AGND	Analog Ground
26	V_{O0}	DAC 0 Output
27	V_{R0}	DAC 0 Reference Input
28	V_{R1}	DAC 1 Reference Input

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = +5 V, V_{EE} = −5 V, V_{REF} = 3 V and −3 V, T = 25°C, Output Load = Open, AGND=DGND=0 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DC CHARACTERISTICS								
Resolution (All Grades)	N	8			8		Bits	
Differential Non-Linearity	DNL			±0.8		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Monotonicity			Guaranteed		Guaranteed			
Gain Error	GE			±1.5		±1.5	% FSR	FSR = Full Scale Range[1]
Zero Scale Offset	Z_{OFS}		±20	±75		±75	mV	
Output Drive Capability	I_O		±1				mA	
REFERENCE INPUTS								
Impedance of V_{REF}	REF	6	12	18	6	18	kΩ	
Voltage Range	V_R	V_{EE} +1.5		V_{CC} −1.8		V	V_{REF}	Max Swing is AGND ±3 V
DYNAMIC CHARACTERISTICS[2]								R_L = 5 k, C_L = 20 pF
Input to Output Bandwidth			10				MHz	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Input to Output Settling Time[5]			150				ns	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		10				MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r	5	8				MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		275	300		325	ns	V_R=0 to V_R = 3V Step[6] to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		275	300		325	ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		−65				dB	Codes=0 @ 1 MHz
Group Delay	GD		20				ns	
Harmonic Distortion	T_{HD}		0.5				%	V_{REF}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		−75				dB	@ 1 MHz, single channel
Digital Feedthrough	Q			1			nVS	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR			0.02			%/%	ΔV=±5%
POWER CONSUMPTION								
Positive Supply Current	I_{CC}		15	25		30	mA	V_{REF} = 0 V
Negative Supply Current	I_{EE}		15	25		30	mA	V_{REF} = 0 V
Power Dissipation	P_{DISS}		150	250		300	mW	V_{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS								
Logic High[3]	V_{IH}	2.4			2.4		V	
Logic Low[3]	V_{IL}			0.8		0.8	V	
Input Current	I_L			±10		±10	µA	
Input Capacitance[2]	C_L			8		8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS[2, 4]								
Input Clock Pulse Width	t_{CH}, t_{CL}	40			50		ns	
Data Setup Time	t_{DS}	10			10		ns	
Data Hold Time	t_{DH}	15			15		ns	
CLK to SDO Propagation Delay	t_{PD}			40		50	ns	
DAC Register Load Pulse Width	t_{LD}	100			100		ns	
Reset Pulse Width	t_{RST}	50			60		ns	
Clock Edge to Load Rising Edge	t_{CKLD1}	100			100		ns	
Clock Edge to Load Falling Edge	t_{CKLD2}	0			0		ns	
Load Falling Edge to SDO 3-state Enable	t_{HZ1}	50			60		ns	
Load Rising Edge to SDO 3-state Disable	t_{HZ2}	35			50		ns	
Load Falling Edge to CLK Disable	t_{LDCK1}	25			40		ns	
Load Rising Edge to CLK Enable	t_{LDCK2}	35			50		ns	
LD Set-up Time with Respect to CLK	t_{LDSU}	15			20		ns	

NOTES

1 Full Scale Range (FSR) is 3V.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 *See Figures 2 and 3.*

5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL POSITIVE SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = 10 V, V_{EE} = 0 V, V_{REF} = 3 V and −3 V, T = 25°C, Output Load = Open, AGND = (V_{CC} + V_{EE})/2 = 5 V, DGND = 0 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DC CHARACTERISTICS								
Resolution (All Grades)	N	8			8		Bits	
Differential Non-Linearity	DNL			±0.8		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Monotonicity			Guaranteed		Guaranteed			
Gain Error	GE			±1.5		±1.5	% FSR	FSR = Full Scale Range[1]
Zero Scale Offset	Z_{OFS}		±20	±75		±75	mV	
Output Drive Capability	I_O		±1				mA	
REFERENCE INPUTS								
Impedance of V_{REF}	REF	6	12	18	6	18	kΩ	
Voltage Range	V_R	V_{EE} +1.5		V_{CC} −1.8		V	V_{REF}	Max Swing is AGND ±3 V
DYNAMIC CHARACTERISTICS[2]								R_L = 5 k, C_L = 20 pF
Input to Output Bandwidth			10				MHz	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Input to Output Settling Time[5]			150				ns	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		10				MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r	5	8				MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		275	300		325	ns	V_R=0 to V_R = 3V Step[6] to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		275	300		325	ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		–65				dB	Codes=0 @ 1 MHz
Group Delay	GD		20				ns	
Harmonic Distortion	T_{HD}		0.5				%	V_{REF}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		–75				dB	@ 1 MHz, single channel
Digital Feedthrough	Q			1			nVS	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR			0.02			%/%	ΔV=±5%
POWER CONSUMPTION								
Positive Supply Current	I_{CC}		15	25		30	mA	V_{REF} = 0 V
Negative Supply Current	I_{EE}		15	25		30	mA	V_{REF} = 0 V
Power Dissipation	P_{DISS}		150	250		300	mW	V_{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS								
Logic High[3]	V_{IH}	2.4			2.4		V	
Logic Low[3]	V_{IL}			0.8		0.8	V	
Input Current	I_L			±10		±10	µA	
Input Capacitance[2]	C_L			8		8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS[2, 4]								
Input Clock Pulse Width	t_{CH}, t_{CL}	40			50		ns	
Data Setup Time	t_{DS}	10			10		ns	
Data Hold Time	t_{DH}	15			15		ns	
CLK to SDO Propagation Delay	t_{PD}			40		50	ns	
DAC Register Load Pulse Width	t_{LD}	100			100		ns	
Reset Pulse Width	t_{RST}	50			60		ns	
Clock Edge to Load Rising Edge	t_{CKLD1}	100			100		ns	
Clock Edge to Load Falling Edge	t_{CKLD2}	0			0		ns	
Load Falling Edge to SDO 3-state Enable	t_{HZ1}	50			60		ns	
Load Rising Edge to SDO 3-state Disable	t_{HZ2}	35			50		ns	
Load Falling Edge to CLK Disable	t_{LDCK1}	25			40		ns	
Load Rising Edge to CLK Enable	t_{LDCK2}	35			50		ns	
LD Set-up Time with Respect to CLK	t_{LDSU}	15			20		ns	

NOTES

1 Full Scale Range (FSR) is 3V.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 *See Figures 2 and 3.*
5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

4

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1,2]

V_{CC} to AGND ..... +6.5 V
V_{EE} to AGND ..... –6.5 V
V_{CC} to DGND ..... +13.0 V
V_{EE} to DGND ..... –6.5 V
V_{Ri} to AGND ..... V_{CC} to V_{EE}
V_{Oi} to AGND ..... V_{CC} to V_{EE}
Digital Input & Output Voltage to DGND –0.5 to V_{DD} +0.5 V

Operating Temperature Range
Extended Industrial ..... –40°C to +85°C
Maximum Junction Temperature ..... –65°C to 150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 6mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATIONS INFORMATION

Refer to Section 8 for Applications Information

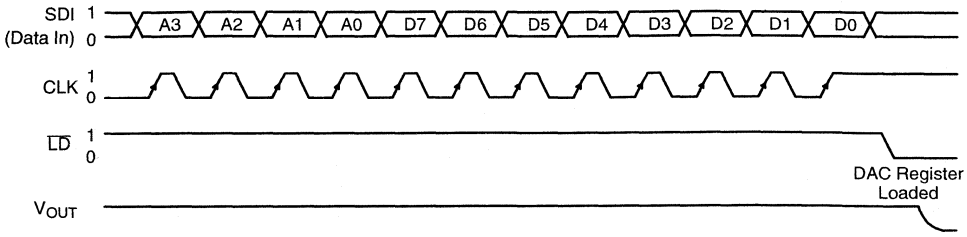


Figure 1. Serial Data Timing and Loading

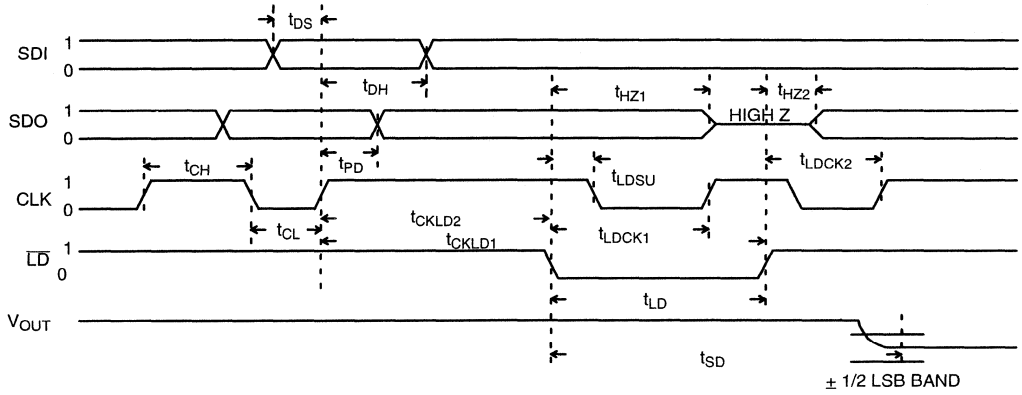


Figure 2. Detail Serial Data Input Timing ($\overline{RST}$ = "1")

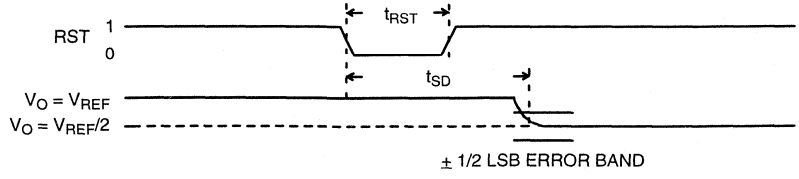


Figure 3. RESET Operation

THEORY OF OPERATION

The MP7641 is equipped with a serial data 3-wire standard μ-processor logic interface to reduce pin count, package size, and board wire (space). This interface consists of $\overline{LD}$ which controls the transfer of data to the selected DAC channel, SDI (serial data/address input), CLK (shift register clock) and SDO (serial data output). When the $\overline{LD}$ signal is high, CLK signal loads the digital input bits (SDI) into the 12-bit shift register (4 bits address A3 to A0, then 8 bits data D7 to D0). The $\overline{LD}$ signal going low loads this data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data input (SDI), output (SDO 3-stated) and the CLK input. This design tremendously reduces digital noise, and glitch transients into the DACs due to free running CLK and SDI. Also, 3-stating the SDO output with $\overline{LD}$ signal would allow read back of pre-stored digital data of the selected package using one SDO wire for all DAC ICs on the board. Note also that the reset signal ($\overline{RST}$) resets all analog outputs to 1/2 of V_{REF}, regardless of any digital inputs. Note that the input V_{Ri} is referenced to AGND.

Function	A3	A2	A1	A0	$\overline{LD}$	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	0→1 Repeat	1	Data Input Valid	Data Output Valid
Stop Shifting Data In and Out	X	X	X	X	0	X	1	X	Hi-Z
Load DACs									
	0	0	0	0	No Operation				
DAC 0	0	0	0	1	1→0	X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0	X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0	X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0	X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0	X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0	X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0	X	1	X	Hi-Z
⋮	⋮	⋮	⋮	⋮	No Operation	X	⋮	⋮	⋮
					⋮	X			
					⋮	X			
	1	1	1	0	No Operation	X	1	X	Hi-Z
	1	1	1	1	No Operation	X	1	X	Hi-Z
Reset all DACs to $V_{REF/2}$	X	X	X	X	X	X	0	X	X

Table 1. Digital Function Truth Table
Serial In/Serial Out

DB7 MSB	DB6	DB5	DB4	DB3	DB2	DB1	DB0 LSB	DAC Output Voltage $V_{Oi} = AGND + (V_{Ri} - AGND)(\frac{D}{256})$
0	0	0	0	0	0	0	0	AGND
0	0	0	0	0	0	0	1	$(V_{Ri} - AGND)(\frac{1}{256}) + AGND$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{Ri} - AGND)(\frac{254}{256}) + AGND$
1	1	1	1	1	1	1	1	$(V_{Ri} - AGND)(\frac{255}{256}) + AGND$

Table 2. DAC Transfer Function
Analog Output vs. Digital Code

OPERATION WITH DUAL POSITIVE POWER SUPPLIES

For the dual positive supplies operation, V_{CC} = +10 V, V_{DD} = 5 V, V_{EE} = 0 V and analog output zero level is to be referenced to (V_{CC} + V_{EE}) /2 by setting the AGND pin to 5 V.

MICROPROCESSOR INTERFACE

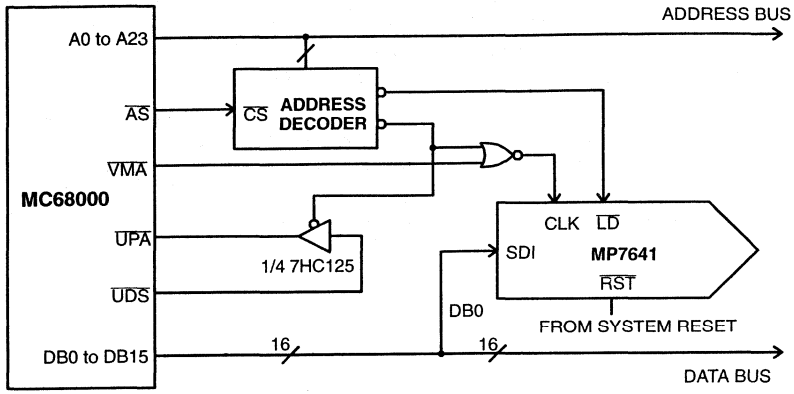
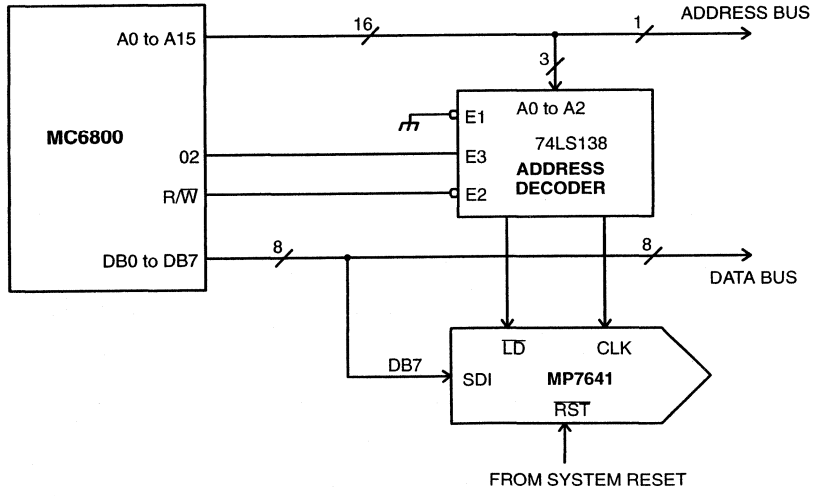


Figure 4. MC68000 Interface (Simplified Diagram)



NOTES:
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE location 2000, R/$\overline{W}$, and 02. A WRITE to address 4000 transfers data from the input shift register to the DAC register.

Figure 5. MC6800 Interface (Simplified Diagram)

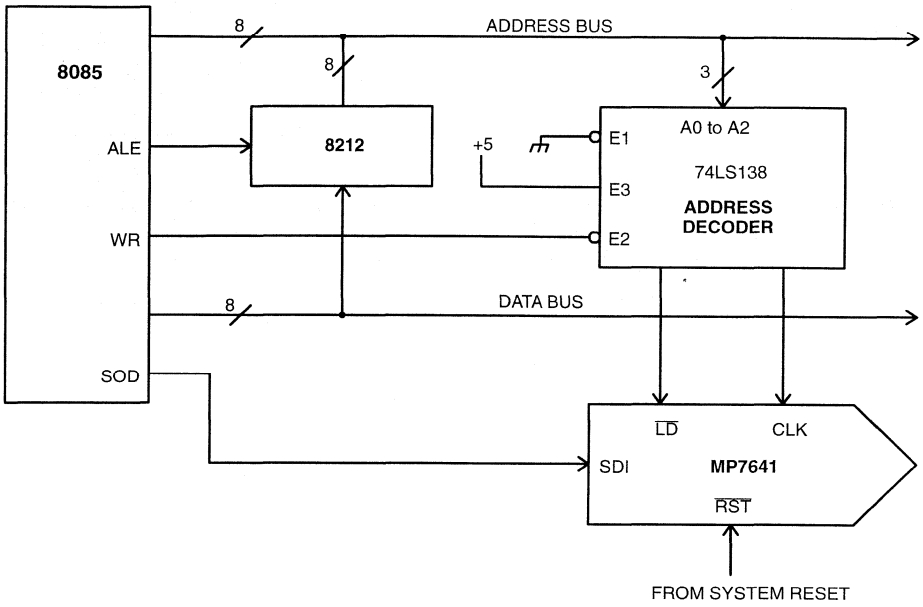


Figure 6. 8085 Interface (Simplified Diagram)

NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000
2. Data is clocked into the DAC shift register by executing memory write instructions. the clock input is generated by decoding address 8000 and $\overline{WR}$. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

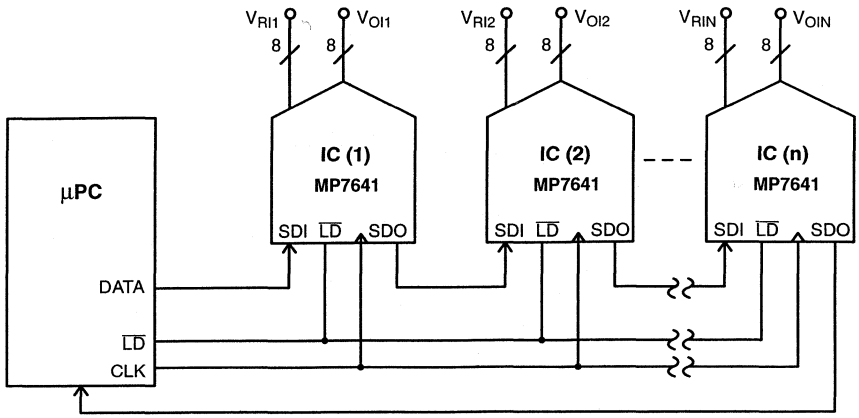


Figure 7. Simplified Diagram
Configuration A

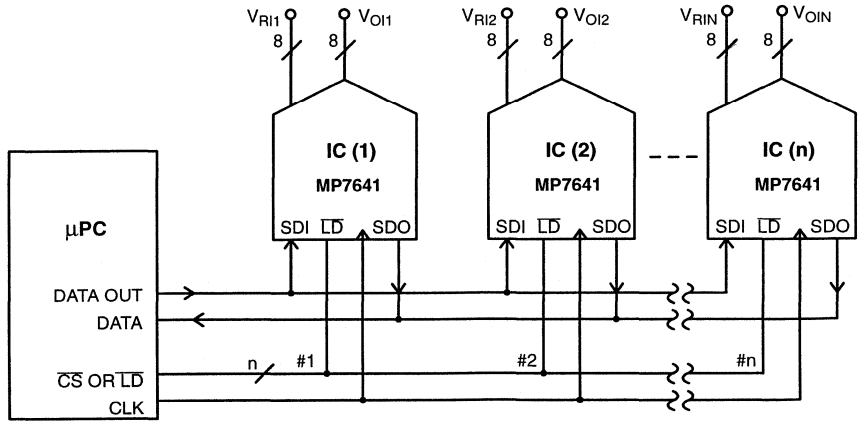


Figure 8. Simplified Diagram
Configuration B

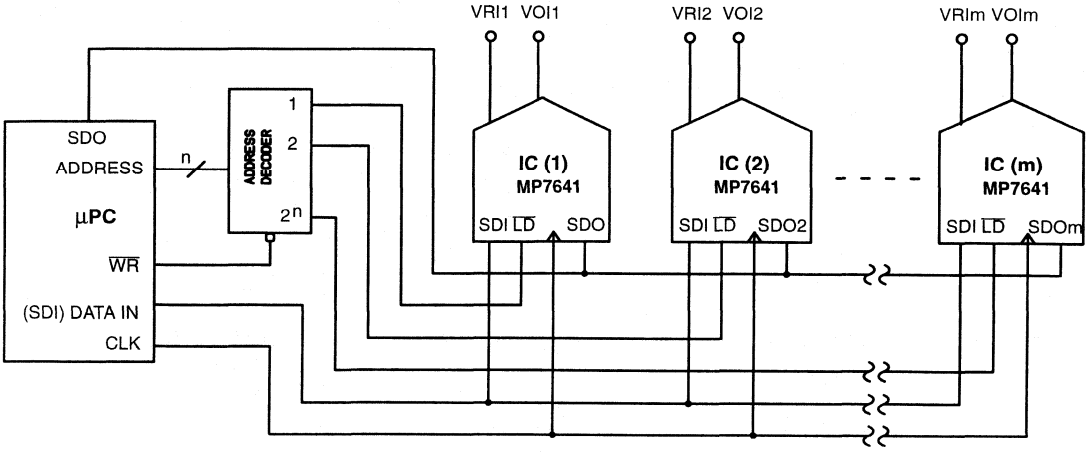


Figure 9. Simplified Diagram
Configuration C

4

MP7641 EVALUATION BOARD

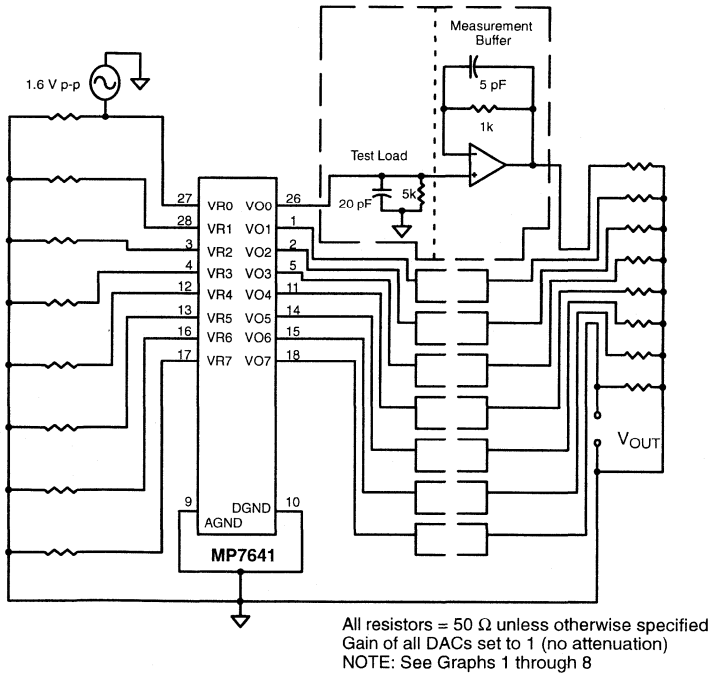
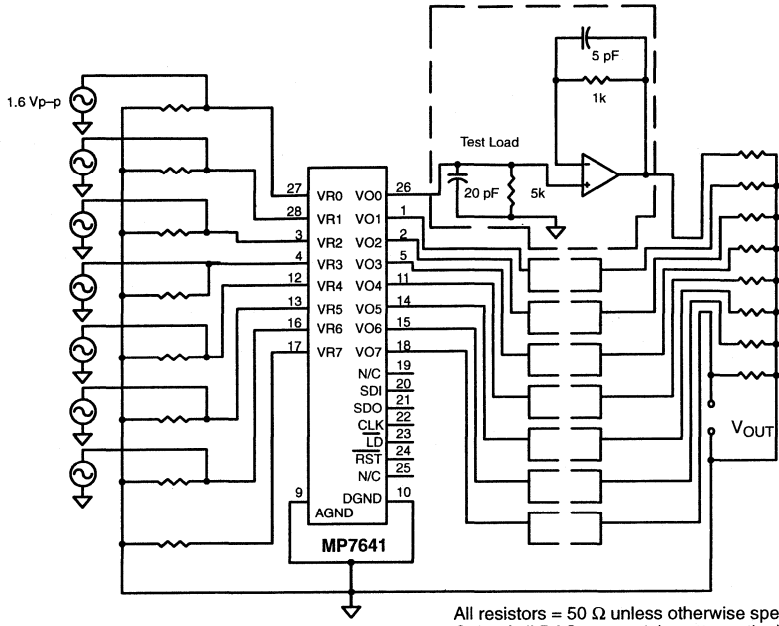
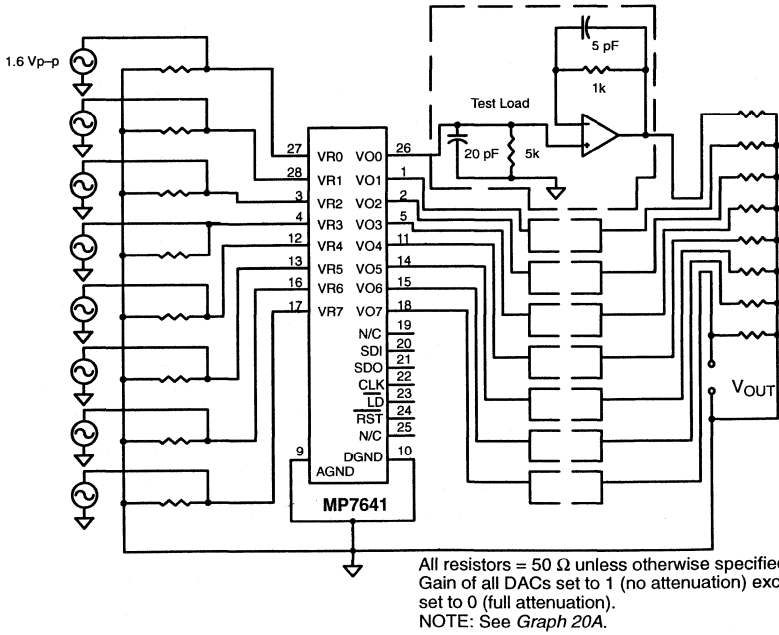


Figure 10. Single Channel Crosstalk



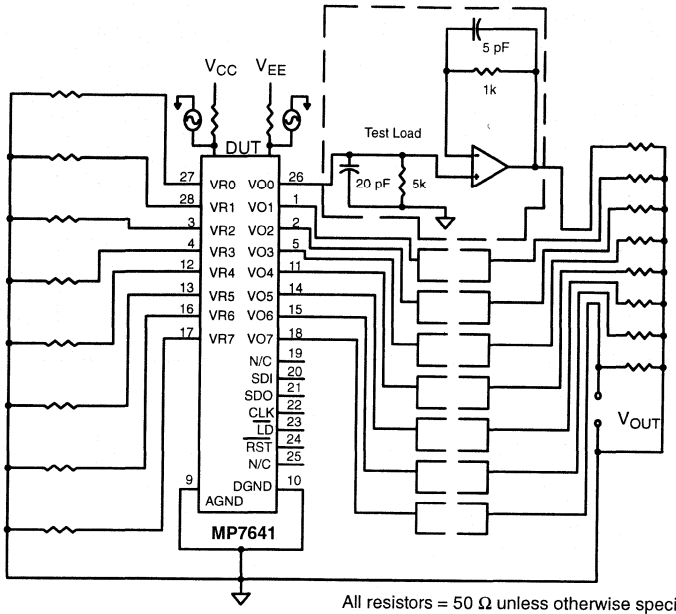
All resistors = 50 Ω unless otherwise specified.
Gain of all DACs set to 1 (no attenuation).
NOTE: See *Graph 20B.*

Figure 11. All Hostile Crosstalk



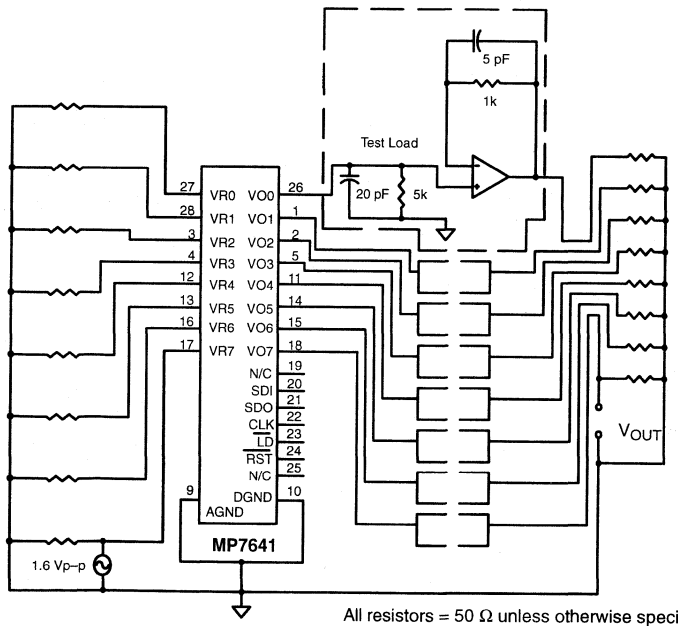
All resistors = 50 Ω unless otherwise specified.
Gain of all DACs set to 1 (no attenuation) except monitored DAC set to 0 (full attenuation).
NOTE: See *Graph 20A.*

Figure 12. All Hostile Crosstalk & Feedthrough



All resistors = 50 Ω unless otherwise specified.
Gain of all DACs set to 1 (no attenuation).
NOTE: See *Figure 12.*

Figure 13. PSRR

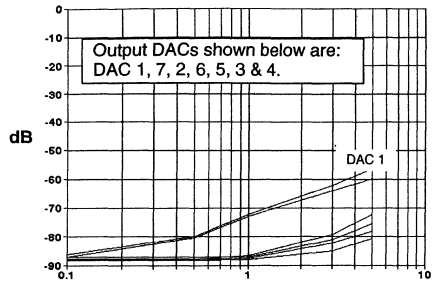


All resistors = 50 Ω unless otherwise specified.
NOTE: See *Graph 16.*

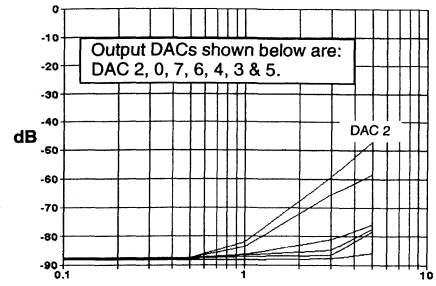
Figure 14. Frequency Response / THD Response

PERFORMANCE CHARACTERISTICS

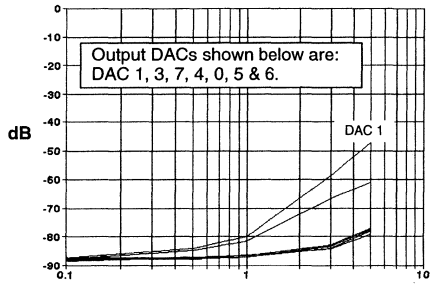
Channel-to-Channel Crosstalk (Gain vs. Frequency; All DACs set to full scale; V_{REF}=1.6 Vp-p)



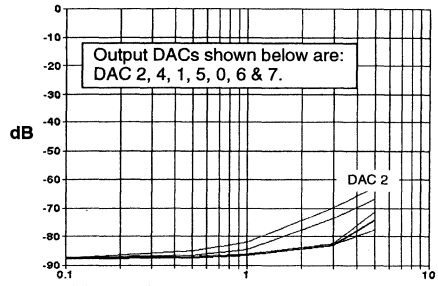
Graph 1.



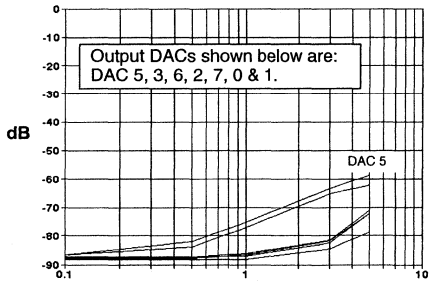
Graph 2.



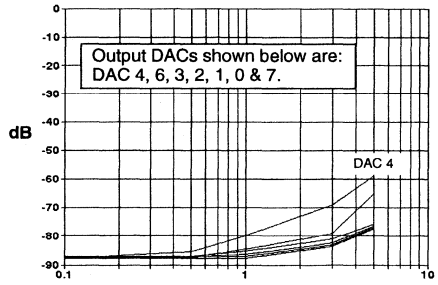
Graph 3.



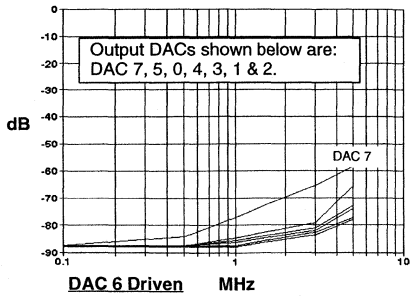
Graph 4.



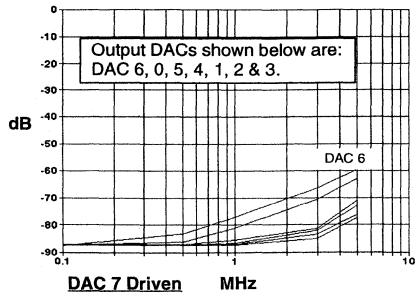
Graph 5.



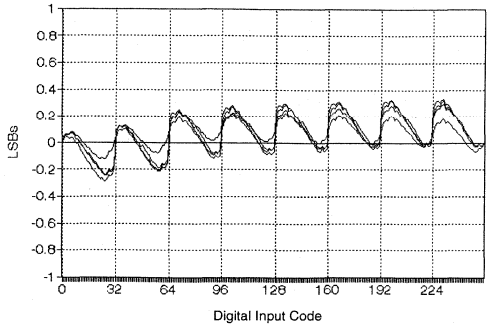
Graph 6.



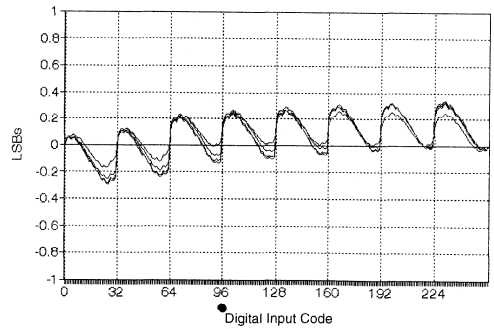
Graph 7.



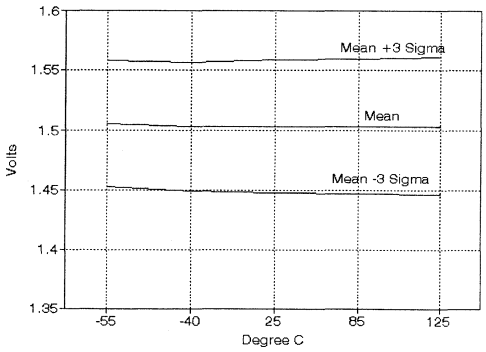
Graph 8.



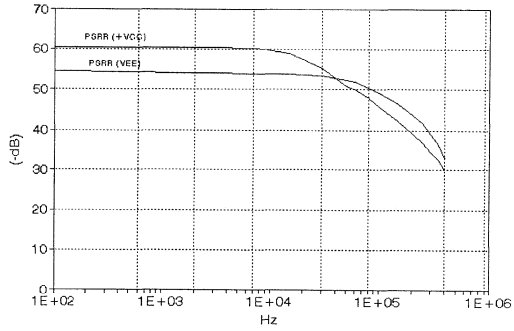
Graph 9. Linearity Error vs. Digital Input Code DACs 0 to 3



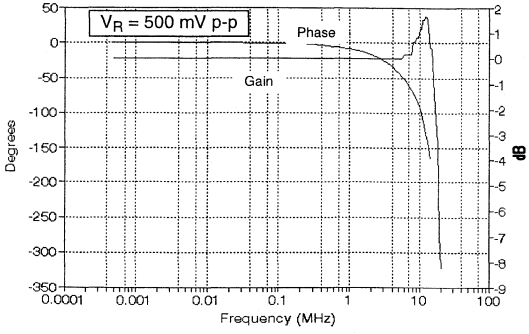
Graph 10. Linearity Error vs. Digital Input Code DACs 4 to 7



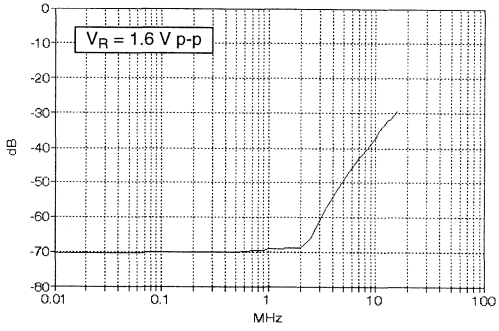
Graph 11. Reset Voltage vs. Temperature



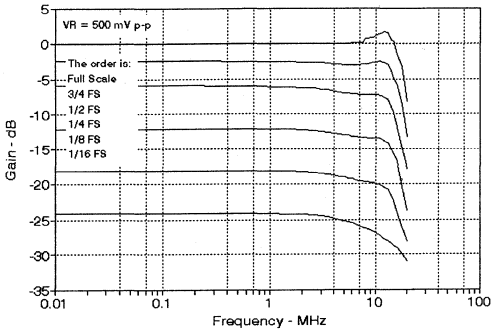
Graph 12. PSRR vs. Frequency



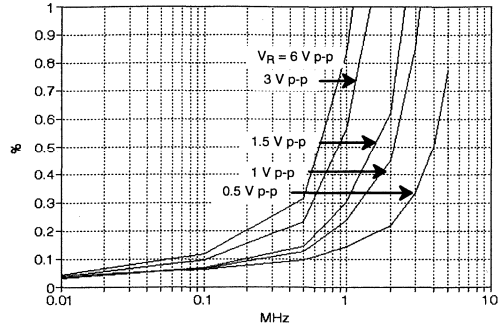
Graph 13. Gain & Phase vs. Frequency



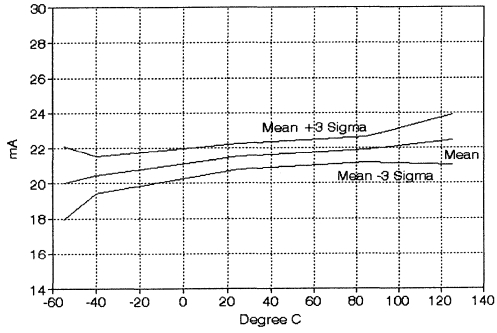
Graph 14. Feedthrough vs. Frequency



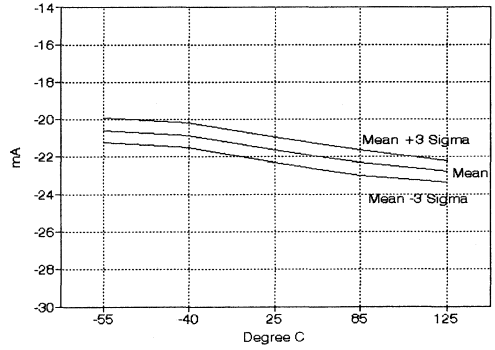
Graph 15. Gain (V_O/V_R) vs. Frequency Open Loop/Unloaded Output*



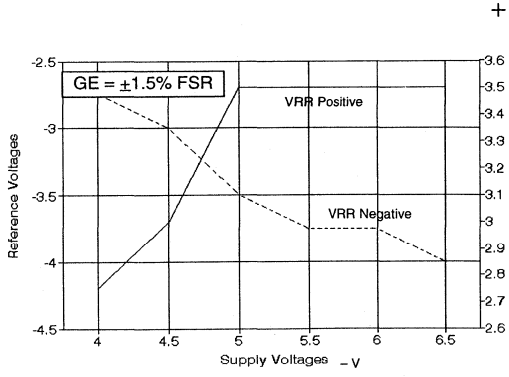
Graph 16. THD vs. Frequency



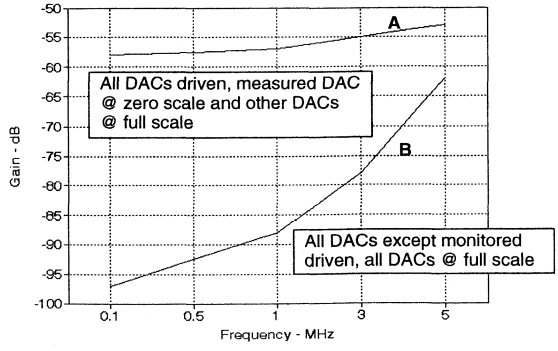
Graph 17. I_{CC} vs. Temperature



Graph 18. I_{EE} vs. Temperature

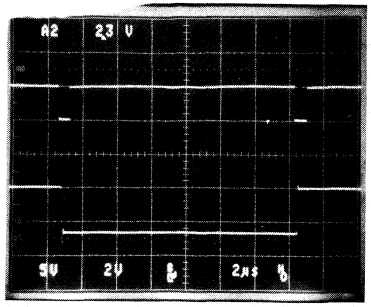


Graph 19. Reference Input Voltage Range vs. Supply Voltages

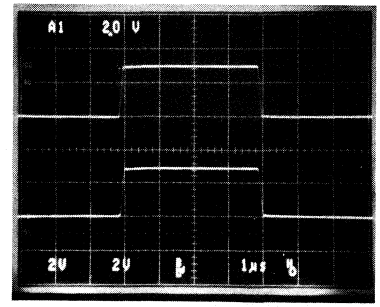


Graph 20. All Channel Crosstalk vs. Frequency

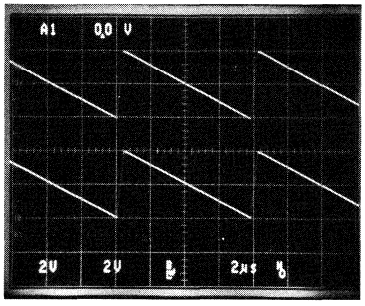
* A 2K or 5K resistor across output and V_{EE} will remove peaking (see Graph 26).



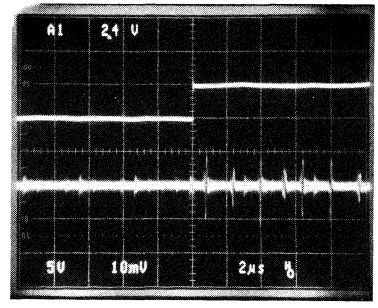
Graph 21. Digital Settling



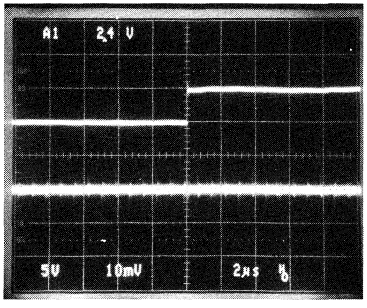
Graph 22. Pulse Response ($t_R = t_F$ = 100 ns for V_R)



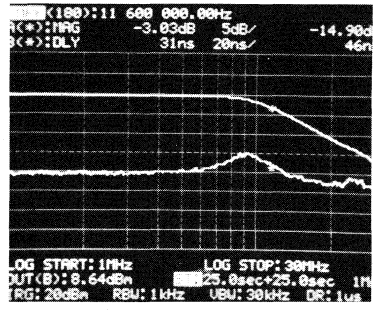
Graph 23. 128 kHz Sawtooth Waveform Response



Graph 24. Clock and SDI Feedthrough



Graph 25. Clock/SDI Feedthrough



Graph 26. Typical Gain and Group Delay vs. Frequency (with 5K resistor across output to V_{EE})

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MP7643

4-Channel, Programmable Gain Voltage Output, 15 MHz Input Bandwidth 8-Bit DACs with Multiplying Parallel Digital Data Port

EXAR

FEATURES

- **Programmable Gain**
- **4 Independent 2-Quadrant Multiplying 8-Bit DACs with Output Amplifiers**
- **Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability**
- **High Speed:**
  - **12.5 MHz Digital Clock Rate**
  - **V_{REF} to V_{OUT} Settling Time: 150ns to 8-bit (typ)**
  - **Voltage Reference Input Bandwidth: 15 MHz**
- **Very Low Noise Gain Control**
- **Low Power: 80mW**
- **Low AC Voltage Reference Feedthrough**
- **Excellent Channel-to-Channel Isolation**
- **DNL = ±0.5 LSB, INL = ±1 LSB (typ)**
- **DACs Matched to ±0.5% (typ)**
- **Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz**
- **Latch-Up Free**
- **ESD Protection: 2000 V Minimum**

APPLICATIONS

- **Direct High-Frequency Automatic Gain Control**
- **Video AGC & CCD Level AGC**
- **Convergence Adjustment for High-Resolution Monitors (Workstations)**
- **Multiplier Replacement**

4

GENERAL DESCRIPTION

The MP7643 is ideal for digital gain control of high frequency analog signals such as video, composite video and CCD. The device includes 4-channels of high speed, wide bandwidth, two quadrant multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving a ±1mA (typ) load. DNL of better than ±0.5 LSB is achieved with a channel-to-channel matching of typically 0.5%. Stability, matching, and precision of the DACs are achieved by using MPS' thin film technology. Excellent channel-to-channel isolation is also achieved with MPS' BiCMOS process which cannot be achieved using a typical CMOS technology.

An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 15 MHz (typ), fast output settling time of 150 ns, and excellent V_{REF} feedthrough isolation. The negative feedback terminal of the output op amp is available for user gain control. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal is achieved.

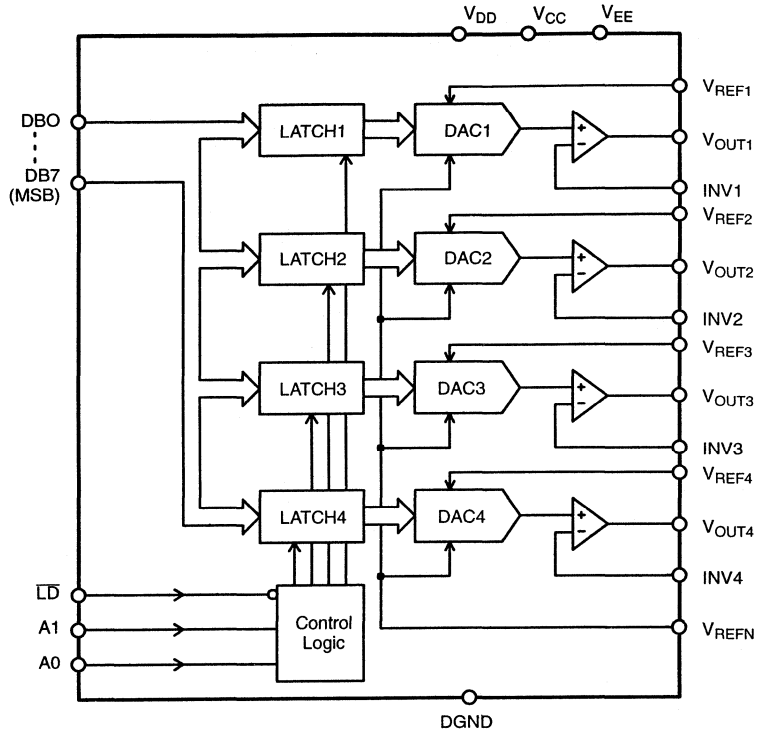
The combination of a constant input Z and the ability to vary V_{REFN} within V_{CC} −1.8 V to V_{EE} +1.5 V allows flexibility for optimum system design.

The MP7643 is fabricated on a junction isolated, high speed BiCMOS (BiCMOS IV™) process with thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

ORDERING INFORMATION

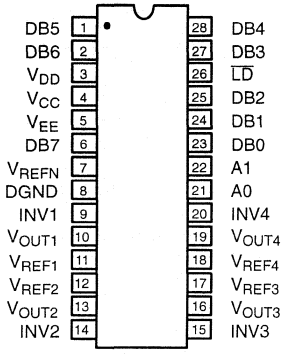
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	−40 to +85°C	MP7643AS	±1	±0.5	±1.5
Plastic Dip	−40 to +85°C	MP7643AN	±1	±0.5	±1.5

SIMPLIFIED BLOCK DIAGRAM

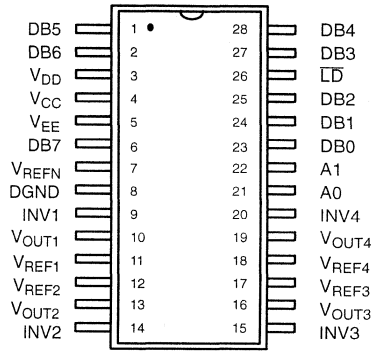


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (Jedec, 0.300")
S28

4

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB5	Data Input Bit 5
2	DB6	Data Input Bit 6
3	V_{DD}	Digital Positive Supply
4	V_{CC}	Analog Positive Supply
5	V_{EE}	Analog Negative Supply
6	DB7	Data Input Bit 7
7	V_{REFN}	Negative Reference Input
8	DGND	Digital Ground
9	INV1	Inverting Input 1
10	V_{OUT1}	DAC 1 Output
11	V_{REF1}	DAC 1 Positive Reference Input
12	V_{REF2}	DAC 2 Positive Reference Input
13	V_{OUT2}	DAC 2 Output
14	INV2	Inverting Input 2

PIN NO.	NAME	DESCRIPTION
15	INV3	Inverting Input 3
16	V_{OUT3}	DAC 3 Output
17	V_{REF3}	DAC 3 Positive Reference Input
18	V_{REF4}	DAC 4 Positive Reference Input
19	V_{OUT4}	DAC 4 Output
20	INV4	Inverting Input 4
21	A0	DAC Address Bit 0
22	A1	DAC Address Bit 1
23	DB0	Data Input Bit 0
24	DB1	Data Input Bit 1
25	DB2	Data Input Bit 2
26	$\overline{LD}$	Load Data to Selected DAC
27	DB3	Data Input Bit 3
28	DB4	Data Input Bit 4

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = +5 V, V_{EE} = –5 V, V_{REF} = 3 V and –3 V, T = 25°C, Output Load = No Resistive Load, V_{REFN} = DGND = 0 V, Gain = 1

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DC CHARACTERISTICS						
Resolution (All Grades)	N	8			Bits	
Differential Non-Linearity	DNL		±0.5	±0.8	LSB	
Integral Non-Linearity	INL		±1	±1	LSB	
Monotonicity			Guaranteed			
Gain Error	GE			±1.5	% FSR	FSR = Full Scale Range[1]
Zero Scale Offset	Z_{OFS}			±50	mV	
Output Drive Capability	I_O		±1		mA	
REFERENCE/INV INPUTS						
Impedance of V_{REF}	REF	6		18	kΩ	
Voltage Range	V_{RP}	V_{EE} +1.5		V_{CC} –1.8	V	V_{REF} Max Swing is V_{REFN} ±3 V
INV DC Voltage Range	V_{RN}	V_{EE} +1		0	V	
DYNAMIC CHARACTERISTICS[2]						R_L = 5 k, C_L = 20 pF
Input to Output Bandwidth			15		MHz	V_R = 1.6 V p–p, R_L = 5k to V_{EE}
Input to Output Settling Time[5]			150		ns	V_R = 1.6 V p–p, R_L = 5k to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15		MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15		MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		300		ns	V_R=0 to V_R = 3V Step[6] to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		300		ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		TBD		dB	Codes=0 @ 1 MHz
Group Delay	GD		TBD		ns	
Harmonic Distortion	T_{HD}		TBD		%	V_{REF}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		TBD		dB	@ 1 MHz, single channel
Digital Feedthrough	Q		TBD		nVS	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR		±0.05		%/%	ΔV=±5%
POWER CONSUMPTION						
Positive Supply Current	I_{CC}			12	mA	V_{REF} = 0 V
Negative Supply Current	I_{EE}			12	mA	V_{REF} = 0 V
Power Dissipation	P_{DISS}		80		mW	V_{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS						
Logic High[3]	V_{IH}	2.4			V	
Logic Low[3]	V_{IL}			0.8	V	
Input Current	I_L			±10	µA	
Input Capacitance[2]	C_L		8		pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS (2, 4)						
Address to $\overline{LD}$ Setup	t_{AS}	70			ns	
Address to $\overline{LD}$ Hold	t_{AH}	0			ns	
Data to $\overline{LD}$ Setup	t_{DS}	70			ns	
Data to $\overline{LD}$ Hold	t_{DH}	0			ns	
$\overline{LD}$ Pulse Width	t_{LD}	70			ns	
$\overline{PRESET}$ Pulse Width	t_{PR}	50			ns	

NOTES
1. Full Scale Range (FSR) is 3V.
2. Guaranteed but not production tested.
3. Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4. *See Figure 1.*
5. For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

4

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to V_{REFN} ..... +6.5 V
V_{EE} to V_{REFN} ..... –6.5 V
V_{CC} to DGND ..... +13.0 V
V_{EE} to DGND ..... –6.5 V
V_{REF} 1-4 to DGND, V_{REFN} ..... V_{CC} to V_{EE}
V_{OUT} 1-4 to DGND, V_{REFN} ..... V_{CC} to V_{EE}
Digital Input & Output Voltage to DGND –0.5 to V_{DD} +0.5 V

Operating Temperature Range
Extended Industrial ..... –40°C to +85°C
Maximum Junction Temperature ..... –65°C to 150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC, PLCC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

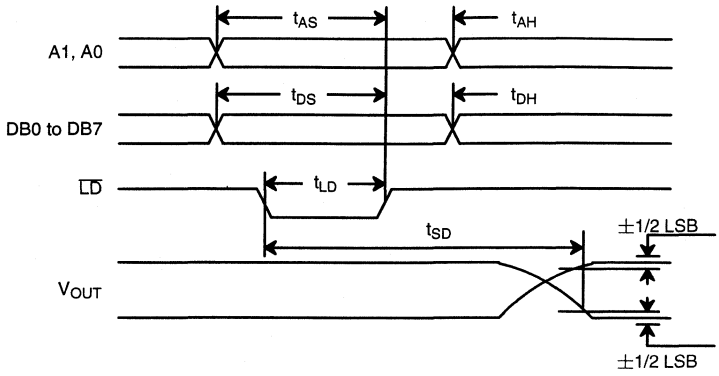


Figure 1. Timing Diagram

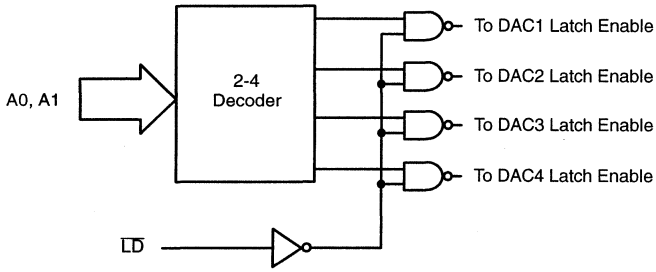


Figure 2. Input Control Logic (Simplified) Block Diagram

LD	A1	A0	Operation
L	L	L	DAC1 Transparent
↑	L	L	DAC1 Latched
L	L	H	DAC2 Transparent
↑	L	H	DAC2 Latched
L	H	L	DAC3 Transparent
↑	H	L	DAC3 Latched
L	H	H	DAC4 Transparent
↑	H	H	DAC4 Latched
H	X	X	No Operation

Table 1. Truth Table

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DAC Output Voltage $V_{Oi} = V_{REFN} + (V_{Ri} - AGND)\left(\frac{D}{256}\right)$
0	0	0	0	0	0	0	0	V_{REFN}
0	0	0	0	0	0	0	1	$(V_{Ri} - V_{REFN})\left(\frac{1}{256}\right) + V_{REFN}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{Ri} - V_{REFN})\left(\frac{254}{256}\right) + V_{REFN}$
1	1	1	1	1	1	1	1	$(V_{Ri} - V_{REFN})\left(\frac{255}{256}\right) + V_{REFN}$

Note: These outputs must be ratioed up for gain in the output amplifier.

Table 2. DAC Transfer Function
Analog Output vs. Digital Code (With V_{REF} Shorted to INV)

THEORY OF OPERATION

The MP7643 is a 4-channel multiplying D/A converter that incorporates a novel open loop architecture invented by MPS. The design produces the wider bandwidth, faster settling time, more constant group delay, and a lower noise operation compared to the conventional R-2R based architectures. This device is particularly useful in applications where analog multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Analog multipliers produce higher noise and offset. This design allows for digital control of gain with constant and very low noise from the low gain through high gain ranges of operation.

Linearity Characteristics

Each DAC achieves DNL $\leq \pm 0.5$ LSB (typ), INL $\leq \pm 1$ LSB (typ), and gain error $\leq \pm 1.5\%$. Since all 4 channel D/A converters are fabricated on the same IC, the linearity matching and gain matching of $\pm 0.5\%$ (typ) is achieved.

AC and Transient Settling Characteristics

The novel subranging architecture delivers a 15 MHz (typ.) –3 dB bandwidth. With all codes = 1 and a 1.6 V step impulse at V_{REF}(1-4), the analog output settles to 8 bits of accuracy in typically 150 ns (with R_L = 5k to V_{EE}). Also with V_{REF} = 3 V or –3 V and a FS to ZS or ZS to FS code change, the respective analog output settles to 8 bits typically in 300 ns. Note that the AC performance specifications also match between all 4 channels. The above AC and transient performance is achieved with each channel consuming only 20 mW (typ.) with either $\pm$5 V or 0 V to 10 V supplies.

Digital Interface

The MP7643 allows direct interface to most microprocessor buses without additional I/O circuitry. *Figure 1.* and *Figure 2.* describe the operation, specification and interface characteristics of the logic port.

The address bits A0 and A1 determine which D/A channel is selected. When $\overline{LD}$ input is low the respective latch of the D/A is enabled (digital input data becomes transparent to the latch and the selected DAC channel), and digital data is loaded into the selected DAC.

Power Supplies and Voltage Reference DC Voltage Ranges

For the single supply operation, V_{CC} = +10 V, V_{DD} = +5 V, and V_{EE} = GND = 0 V. The V_{OUT} 1-4 and V_{REF} 1-4 range would be V_{CC} –1.8 V (10 – 1.8 = 8.2 V) to V_{EE} +1.5 V (0 + 1.5 = 1.5 V). V_{REFN} is the equivalent of AGND for this DAC. In this mode V_{REFN} can be set at (V_{CC} + V_{EE})/2 = (10 + 0)/2 = 5 V. V_{REFN} DC range can, however, be set from V_{EE} +1.5 = 1.5 V to V_{CC} – 1.5 = 8.2 V. Refer to *Table 2.* for the relationship equations.

For the dual supply operation, V_{CC} = +5, V_{DD} = +5, and V_{EE} = –5 V. The V_{OUT} 1-4 and V_{REF} 1-4 range would be V_{CC} –1.8 V (5 V –1.8 = 3.2 V) to V_{EE} +1.5 V (–5 + 1.5 = –3.5 V). In this mode V_{REFN} can be set to (V_{CC} + V_{EE})/2 = (5 – 5)/2 = 0 V. However, V_{REFN} DC range can be set from V_{EE} +1.5 V = 3.5 V to V_{CC} –1.8 = +3.2 V. Refer to *Table 2.* for the relationship equations.

About the INV Input and its DC Voltage Range

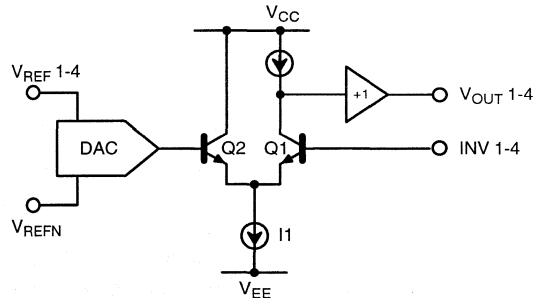
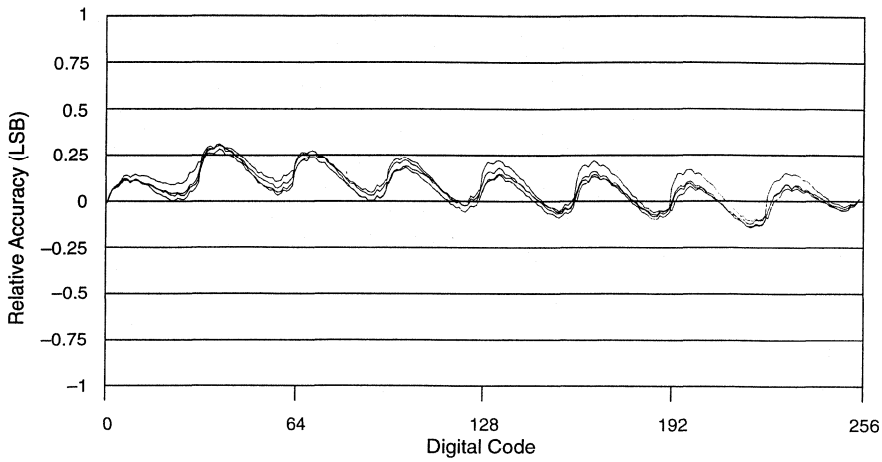


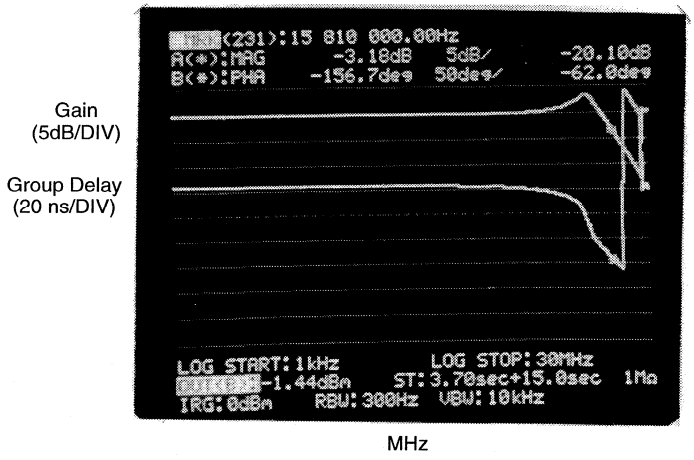
Figure 3. Simplified Block Diagram

As noted in the specification table, the max DC value of the INV input pin is V_O. *Figure 3.* shows a simplified block diagram of the internal circuitry around INV. If V_{INV} exceeds V_O, Q1 will saturate and the amp and consequently the DAC becomes nonfunctional.

The min DC range of INV is limited to V_{be} (Q1) and V_{CE} (sat) of I_1. Therefore, INV (min-DC) = V_{EE} +1 V.



Graph 1. Relative Accuracy vs. Digital Code
DACs 1 to 4



Graph 2. Typical Gain and Group Delay vs. Frequency
(with 5K Resistor Across Output to V_{EE})

MP7645

15 V CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Differential Linearity ±1/2 LSB Tmin to Tmax**
- **Microprocessor Compatible**
- **Low Glitch Energy**
- **Gain Error Tempco (2 ppm/°C max)**
- **Low Output Capacitance (50 pF)**
- **Low Sensitivity to Amplifier Offset (330μV/mV)**
- **Four Quadrant Multiplication**
- **Latch-Up Free**
- **TTL/5 V CMOS Compatible**
- **Low Power Consumption (20 mW)**
- **Guaranteed Monotonic**
- **Use MP7645B for New Designs**

GENERAL DESCRIPTION

The MP7645 is a precision 12-bit CMOS 4-quadrant multiplying DAC with an on-board data latch. The latch is loaded by a single 12-bit wide word. The MP7645 interfaces directly to most 12 or 16-bit bus systems. Data is loaded into the input latch under the control of $\overline{CS}$ and $\overline{WR}$ inputs. These control inputs are level triggered; tying these inputs low makes the input latch transparent allowing direct unbuffered operation of the DAC.

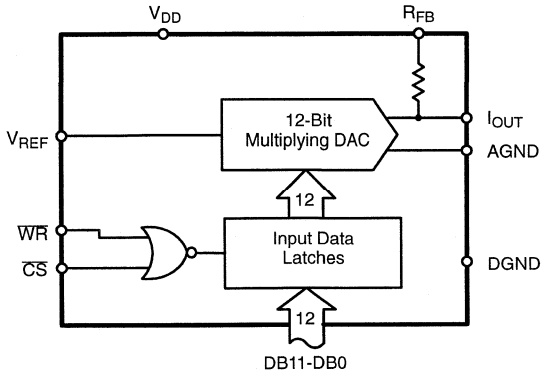
– Stability – The MP7645 incorporates a unique decoding technique yielding excellent accuracy and stability over temperature. Monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. The MP7645 offers a superior alternative for the MP7545. The gain error specification of 2 ppm/°C over a 100°C temperature range equals 0.8 LSB of error.

– Digital Feedthrough – Almost directly related to output capacitance, the MP7645 has 5 to 8 times less digital feedthrough than similar buffered DACs, and additional digital buffering is not necessary.

– Low Output Capacitance - Due to smaller FET cell geometries, the output capacitance at 25/50 pF is 5 times less than standard R-2R CMOS DACs. Lower capacitance allows the MP7645 to achieve the fastest CMOS DAC settling times possible; less than 1 μsec for full scale response to 0.01% when utilizing a high speed output amplifier. The MP7645 is more stable over a larger bandwidth than similar DACs.

– Low Sensitivity to Output Amplifier Offset – CMOS DACs must operate into virtual ground. The additional linearity error incurred by amplifier offset is reduced by a factor of at least 2 in the MP7645 over conventional DACs, to 330μV per millivolt offset. Trim pots can be eliminated by using a low offset amplifier such as an OP-07 or OP-27.

SIMPLIFIED BLOCK DIAGRAM



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MP7645B

CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Greater than 2000 V ESD Protection**
- **Differential Linearity ±1/2 LSB Tmin to Tmax**
- **Microprocessor Compatible**
- **Low Glitch Energy**
- **Gain Error Tempco (2 ppm/°C max)**
- **Low Sensitivity to Amplifier Offset**
- **Four Quadrant Multiplication**
- **Latch-Up Free**
- **TTL/5 V CMOS Compatible**
- **Guaranteed Monotonic**

4

GENERAL DESCRIPTION

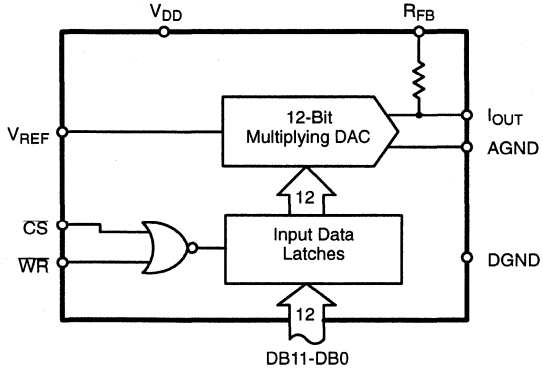
The MP7645B is an improved precision, monolithic 12-bit CMOS 4-quadrant multiplying DAC with an on-board data latch. The latch is loaded by a single 12-bit wide word. Data is loaded into the input latch under the control of $\overline{CS}$ and $\overline{WR}$ inputs. These control inputs are level triggered; tying these inputs low makes the input latch transparent allowing direct unbuffered operation of the DAC.

– Stability – The MP7645B incorporates a unique decoding technique yielding excellent accuracy and stability over temperature. Monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. The gain error specification of 2 ppm/°C over a 100°C temperature range equals 0.8 LSB of error.

– Digital Feedthrough – The MP7645B has 5 to 8 times less digital feedthrough than similar buffered DACs.

– Low Sensitivity to Output Amplifier Offset – The additional linearity error incurred by amplifier offset is reduced by a factor of at least 3 in the MP7645B over conventional DACs. High latch-up resistance and high ESD protection make this a rugged, reliable attenuator!

SIMPLIFIED BLOCK DIAGRAM

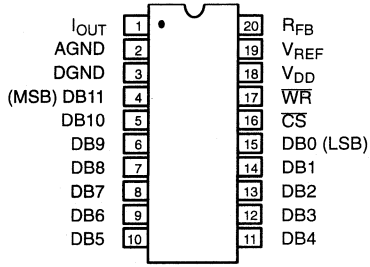


ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7645BKN	±1	±1	±0.2
Plastic Dip	–40 to +85°C	MP7645BLN	±1/2	±1/2	±0.2
Ceramic Dip	–40 to +85°C	MP7645BBD	±1	±1	±0.2
Ceramic Dip	–40 to +85°C	MP7645BCD	±1/2	±1/2	±0.2

PIN CONFIGURATION

See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Current Output Port
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5

PIN NO.	NAME	DESCRIPTION
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select Input (Active Low)
17	$\overline{WR}$	Write Input (Active Low)
18	V_{DD}	Positive Voltage Power Supply
19	V_{REF}	Reference Voltage Input
20	R_{FB}	Feedback Resistor Input

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K, B				±1		±1		
L, C				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
K, B				±1		±1		
L, C				±1/2		±1/2		
Gain Error	GE						% FSR	Using Internal R_{FB}
K, B				±0.2		±0.2		
L, C				±0.2		±0.2		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Monotonicity			Guaranteed		Guaranteed			
K, L								12-Bit Monotonic Tmin to Tmax
Power Supply Rejection Ratio	PSRR			±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
K, L, B, C				±10		±200		
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		1			2 typ	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5			5	mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
Propagation Delay	t_{PD}		50				ns	From digital input change to 90% of final value
REFERENCE INPUT								
Input Resistance	R_{IN}	7	11	25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3			3.0		V	
Logical "0" Voltage	V_{IL}			+0.8		+0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			5		5	pF	DB0-DB11
Control	C_{IN}			20		20	pF	$\overline{WR}$, $\overline{CS}$
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}		50				pF	DAC Inputs all 0's
	C_{OUT}		100				pF	DAC Inputs all 1's

4

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V or all = 5 V
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	180					ns	
Chip Select to Write Hold Time	t_{CH}	0					ns	
Write Pulse Width	t_{WR}	100					ns	
Data Valid to Write Set-Up Time	t_{DS}	100					ns	
Data Valid to Write Hold Time	t_{DH}	10					ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V
AGND to DGND ..... ±0.5 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

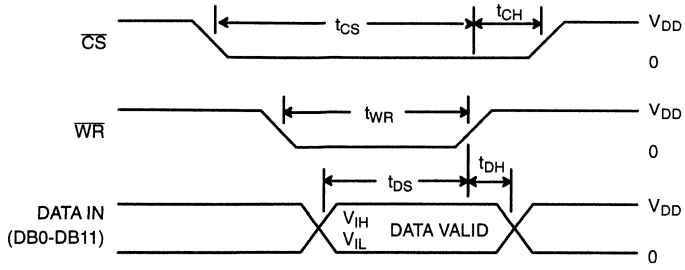
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP 950mW
Derates above 75°C ..... 13mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.
3 GND refers to AGND and DGND.

WRITE CYCLE TIMING DIAGRAM



APPLICATION NOTES

Refer to Section 8 for Applications Information

4

MICROPROCESSOR INTERFACING OF THE MP7645B

The MP7645B can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown (*NO TAG*). This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

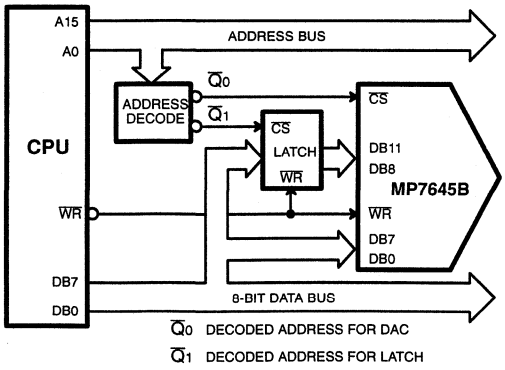


Figure 1. 8-Bit Processor to MP7645B Interface

NO TAG shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080 and Z80. This technique uses the 12 lower address lines of the processor addresses bus to supply data to the DAC, thus each MP7645B connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

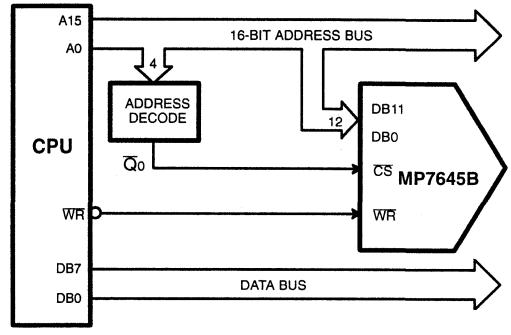


Figure 2. Connecting the MP7645B to 8-Bit Processors via the Address Bus

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MP7651

8-Channel, Voltage Output
10 MHz Input Bandwidth 8-Bit Multiplying
DACs with Serial Digital Data Port
and Chip Select Decoder

FEATURES

- 8 Independent 2-Quadrant Multiplying 8-Bit DACs
- Serial Digital Input Data and Address Port (3-Wire Standard) plus Internal Chip Address Decoder©
- Dual Supplies (±5 V typ.)
- High Speed:
  - 12.5 MHz Digital Clock Rate
  - V_{REF} to V_{OUT} Settling Time: 150ns to 8-bit (typ)
  - Voltage Reference Input Bandwidth: 10 MHz (typ)
- Low Power: 150mW (typ)
- Low AC Voltage Reference Feedthrough
- Excellent Channel-to-Channel Isolation
- DNL = ±0.8 LSB, INL = ±1 LSB (typ)
- DACs Matched to ±0.5% (typ)
- Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz
- V_{REF}/2 Output Preset Level
- Latch-Up Proof
- Greater than 2000 V ESD Protection

APPLICATIONS

- ATE
- Process Control (Low Noise)
- Convergence Adjustment for High Resolution Monitors (Work Stations)
- Digital Gain/Attenuation/Offset Control
- Trimmer Replacement

4

GENERAL DESCRIPTION

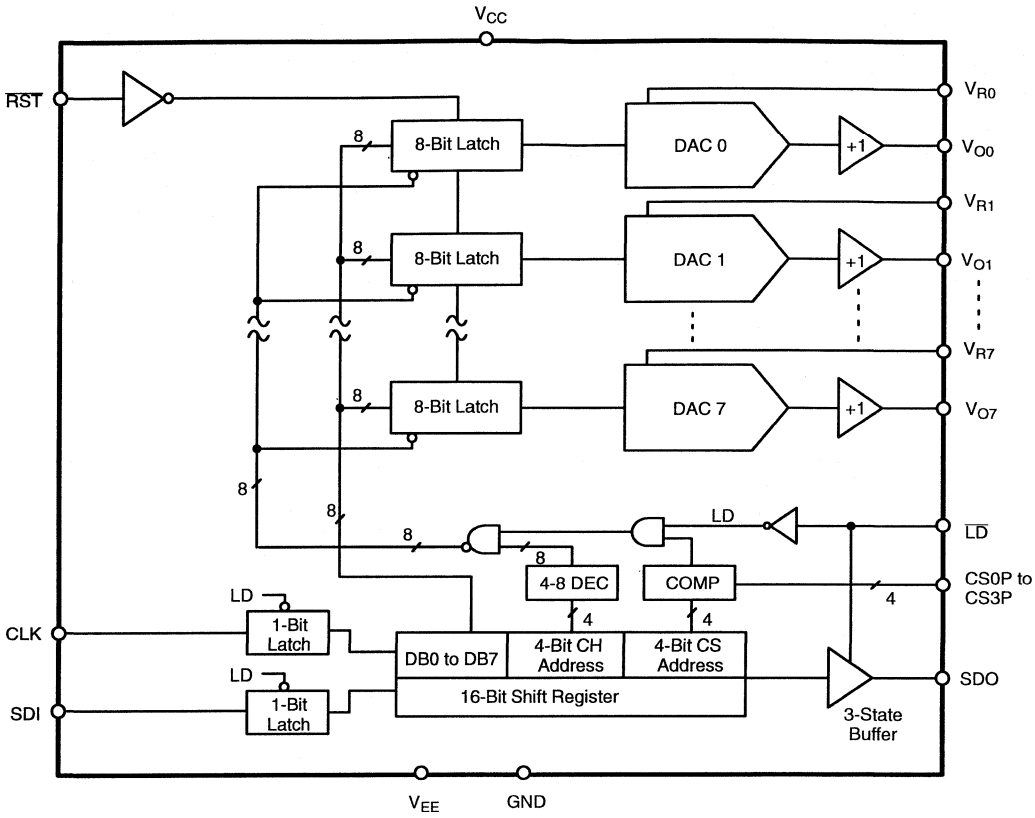
The MP7651 is ideal for direct gain control of video, composite video, CCD and other high frequency analog signals. The device includes 8-channels of high speed, high bandwidth, two quadrant, multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving ±1mA (typ) to a load. DNL of better than ±0.8 LSB is achieved with a channel-to-channel matching of better than 0.5%. Stability, matching, and precision of the DACs is achieved by using EXAR's thin film technology. Also, excellent channel-to-channel isolation is achieved with EXAR's BiCMOS process which cannot be achieved using a typical CMOS technology.

An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 10 MHz (typ), fast output settling time, and V_{REF} feedthrough isolation of –65dB or better. In addition, low distortion in the order of 0.25% with a 1 V p–p, 1 MHz signal.

A specified and constant input impedance of each V_{REF+} input gives flexibility for optimal system design. The serial data 3-wire standard µ-processor logic interface reduces pin count, package size (28 pin), and board wire (space). Additionally, the internal chip select decoder allows for easy daisy chaining without the addition of separate control logic.

MP7651 is fabricated on a junction isolated, high speed, dual metal, linear compatible BiCMOS (BiCMOS IV™) thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

SIMPLIFIED BLOCK DIAGRAM©

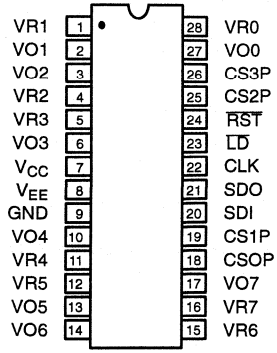


ORDERING INFORMATION

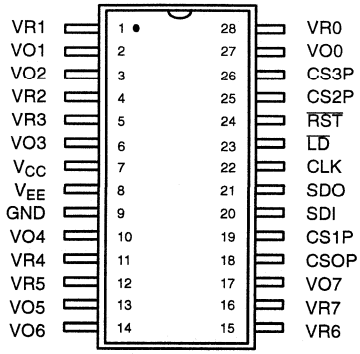
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	–40 to +85°C	MP7651AS	±1	±0.8	±1.5
Plastic Dip	–40 to +85°C	MP7651AN	±1	±0.8	±1.5

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (EIAJ, 0.335")
R28

4

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	VR1	DAC 1 Reference Input
2	VO1	DAC 1 Output
3	VO2	DAC 2 Output
4	VR2	DAC 2 Reference Input
5	VR3	DAC 3 Reference Input
6	VO3	DAC 3 Output
7	V_{CC}	Positive Supply
8	V_{EE}	Negative Supply
9	GND	Ground
10	VO4	DAC 4 Output
11	VR4	DAC 4 Reference Input
12	VR5	DAC 5 Reference Input
13	VO5	DAC 5 Output
14	VO6	DAC 6 Output
15	VR6	DAC 6 Reference Input

PIN NO.	NAME	DESCRIPTION
16	VR7	DAC 7 Reference Input
17	VO7	DAC 7 Output
18	CSOP	Chip Select Bit 0 (LSB)
19	CS1P	Chip Select Bit 1
20	SDI	Serial Data/Address Input
21	SDO	Serial Data Output
22	CLK	Shift Register Clock
23	$\overline{LD}$	Load Signal; Load Data to Selected DACs
24	$\overline{RST}$	Reset Signal; Reset all DACs to $V_{REF}/2$
25	CS2P	Chip Select Bit 2
26	CS3P	Chip Select Bit 3 (MSB)
27	VO0	DAC 0 Output
28	VR0	DAC 0 Reference Input

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Noted: V_{CC} = +5 V, V_{EE} = –5 V and –3 V, V_{REF} = 3 V and –3 V, T = 25°C, Output Load = Open

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DC CHARACTERISTICS								
Resolution (All Grades)	N	8			8		Bits	
Differential Non-Linearity	DNL			±0.8		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Monotonicity			Guaranteed		Guaranteed			
Gain Error	GE			±1.5		±1.5	% FSR	FSR = Full Scale Range (1)
Zero Scale Offset	Z_{OFS}		±20	±75		±75	mV	
Output Drive Capability	I_O		±1				mA	
REFERENCE INPUTS								
Impedance of V_{REF}	REF	6	12	18	6	18	kΩ	
Voltage Range	V_R	V_{EE} +1.5		V_{CC}–1.8		V	V_{REF}	Max Swing is AGND ±3 V
DYNAMIC CHARACTERISTICS[2]								R_L = 5 k, C_L = 20 pF
Input to Output Bandwidth			10				MHz	V_R = 1.6 V p–p, R_L = 5k to V_{EE}
Input to Output Settling Time[5]			150				ns	V_R = 1.6 V p–p, R_L = 5k to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		10				MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r	5	8				MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		275	300		325	ns	V_R=0 to V_R = 3V Step (6) to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		275	300		325	ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		–65				dB	Codes=0 @ 1 MHz
Group Delay	GD		20				ns	
Harmonic Distortion	T_{HD}		0.5				%	V_{REF}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		–75				dB	@ 1 MHz, single channel
Digital Feedthrough	Q			1			nVs	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR			0.02			%/%	Δ V = ±5%
POWER CONSUMPTION								
Positive Supply Current	I_{CC}		15	25		30	mA	V_{REF} = 0 V
Negative Supply Current	I_{EE}		15	25		30	mA	V_{REF} = 0 V
Power Dissipation	P_{DISS}		150	250		300	mW	V_{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS								
Logic High[3]	V_{IH}	2.4			2.4		V	
Logic Low[3]	V_{IL}			0.8		0.8	V	
Input Current	I_L			±10		±10	µA	
Input Capacitance[2]	C_L			8		8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS[2, 4]								
Input Clock Pulse Width	t_{CH}, t_{CL}	40			50		ns	
Data Setup Time	t_{DS}	10			10		ns	
Data Hold Time	t_{DH}	15			15		ns	
CLK to SDO Propagation Delay	t_{PD}			40		50	ns	
DAC Register Load Pulse Width	t_{LD}	100			100		ns	
Reset Pulse Width	t_{RST}	50			60		ns	
Clock Edge to Load Rising Edge	t_{CKLD1}	100			100		ns	
Clock Edge to Load Falling Edge	t_{CKLD2}	0			0		ns	
Load Falling Edge to SDO 3-state Enable	t_{HZ1}	50			60		ns	
Load Rising Edge to SDO 3-state Disable	t_{HZ2}	35			50		ns	
Load Falling Edge to CLK Disable	t_{LDCK1}	25			40		ns	
Load Rising Edge to CLK Enable	t_{LDCK2}	35			50		ns	
LD Set-up Time with Respect to CLK	t_{LDSU}	15			20		ns	
CS0-CS3 Set-Up Time with Respect to $\overline{LD}$	t_{CSLD}	25			35		ns	

NOTES:
1. Full Scale Range (FSR) is 3V.
2. Guaranteed but not production tested.
3. Digital Input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4. *See Figures 2 and 3.*
5. For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to GND ..... +6.5 V
V_{EE} to GND ..... –6.5 V
V_{Ri} to GND ..... V_{CC} to V_{EE}
V_{Oi} to GND ..... V_{CC} to V_{EE}
Digital Input & Output Voltage to GND ..... GND –0.5 to V_{CC} +0.5 V
Operating Temperature Range
Extended Industrial ..... –40°C to +85°C

Maximum Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 6mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATIONS INFORMATION

Refer to Section 8 for Applications Information

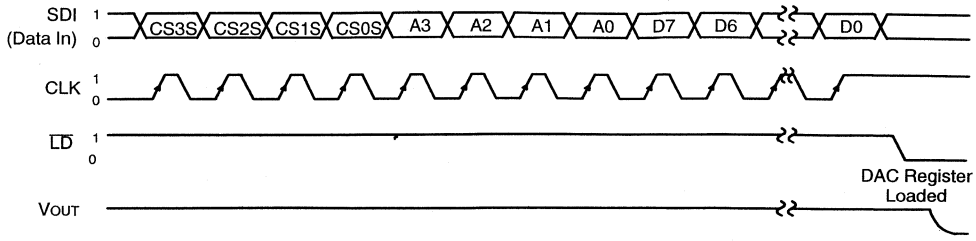


Figure 1. Serial Data Timing and Loading

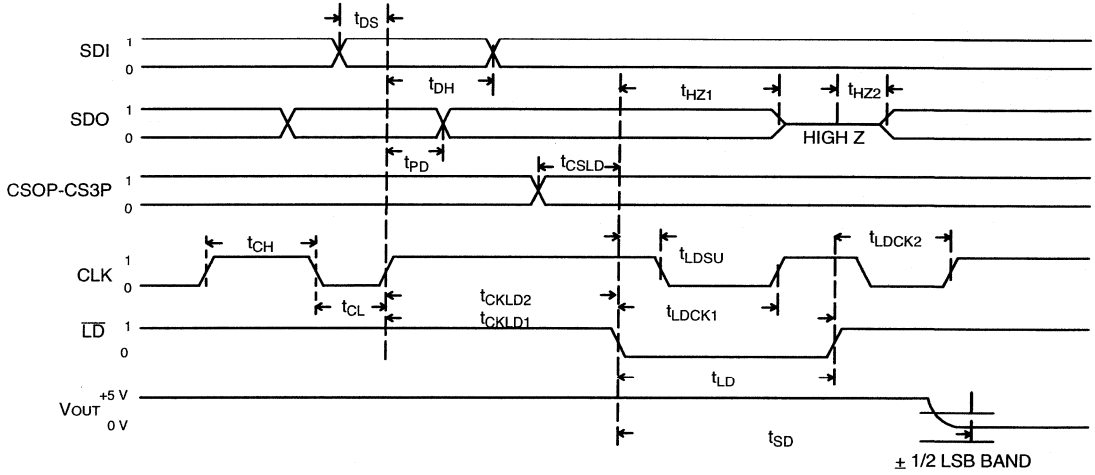


Figure 2. Detail Serial Data Input Timing ($\overline{RST}$ = "1")

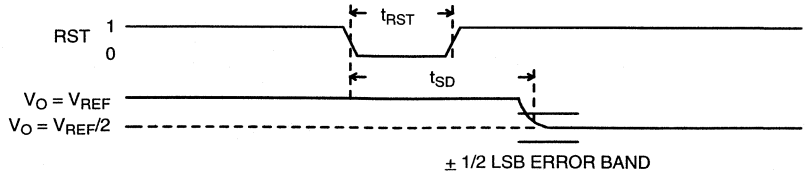


Figure 3. RESET Operation

THEORY OF OPERATION

MP7651 is equipped with a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size (28 pin), and board wire (space). This interface consists of $\overline{LD}$ which controls the transfer of data to the selected DAC channel, SDI (serial data/address input), CLK (shift register clock) and SDO (serial data output). When the $\overline{LD}$ signal is high, CLK signal loads the digital input bits (SDI) into the 16-bit shift register (8 bits data D7 to D0, plus 4 bits address A3 to A0, and 4 bits of Chip Select data CS0S to CS3S). If the CS0S to CS3S in the shift register match the parallel chip-select address (CS0P to CS3P) for the selected chip, then the $\overline{LD}$ signal going low loads the data into the selected DAC of that chip. The $\overline{LD}$ signal going low also disables the serial data input (SDI), output (SDO 3-stated) and the CLK input. This design tremendously reduces digital noise, and glitch transients into the DACs due to free running CLK and SDI. Also, 3-stating the SDO output with $\overline{LD}$ signal would allow read back of pre-stored digital data of the selected package using one SDO wire for all DAC ICs on the board. Note also that the reset signal ($\overline{RST}$) resets all analog outputs to 1/2 of V_{REF}, regardless of any digital inputs. Also note that the input V_{Ri} is referenced to GND.

Function	A3	A2	A1	A0	$\overline{LD}$	CS0S	CS1S	CS2S	CS3S	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	X	X	X	X	0→1 Repeat	1	Data Input	Data Output
Stop Shifting Data In and Out	X	X	X	X	0	X	X	X	X	X	1	X	Hi-Z
Load DACs													
	0	0	0	0	No Operation								
DAC 0	0	0	0	1	1→0					X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0					X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0					X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0					X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	Matched with 4 parallel chip select data CS0P to CS3P				X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0					X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0					X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0					X	1	X	Hi-Z
	⋮	⋮	⋮	⋮	No Operation					X	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮					X	⋮	⋮	⋮
	1	1	1	0	No Operation					X	1	X	Hi-Z
	1	1	1	1	No Operation					X	1	X	Hi-Z
Reset all DACs to VREF/2	X	X	X	X	X	X	X	X	X	X	0	X	X

Table 1. Digital Function Truth Table
Serial In/Serial Out

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DAC Output Voltage $V_{Oi} = AGND + (V_{Ri} - AGND)(\frac{D}{256})$
0	0	0	0	0	0	0	0	AGND
0	0	0	0	0	0	0	1	$(V_{Ri} - AGND)(\frac{1}{256}) + AGND$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{Ri} - AGND)(\frac{254}{256}) + AGND$
1	1	1	1	1	1	1	1	$(V_{Ri} - AGND)(\frac{255}{256}) + AGND$

Table 2. DAC Transfer Function
Analog Output vs. Digital Code

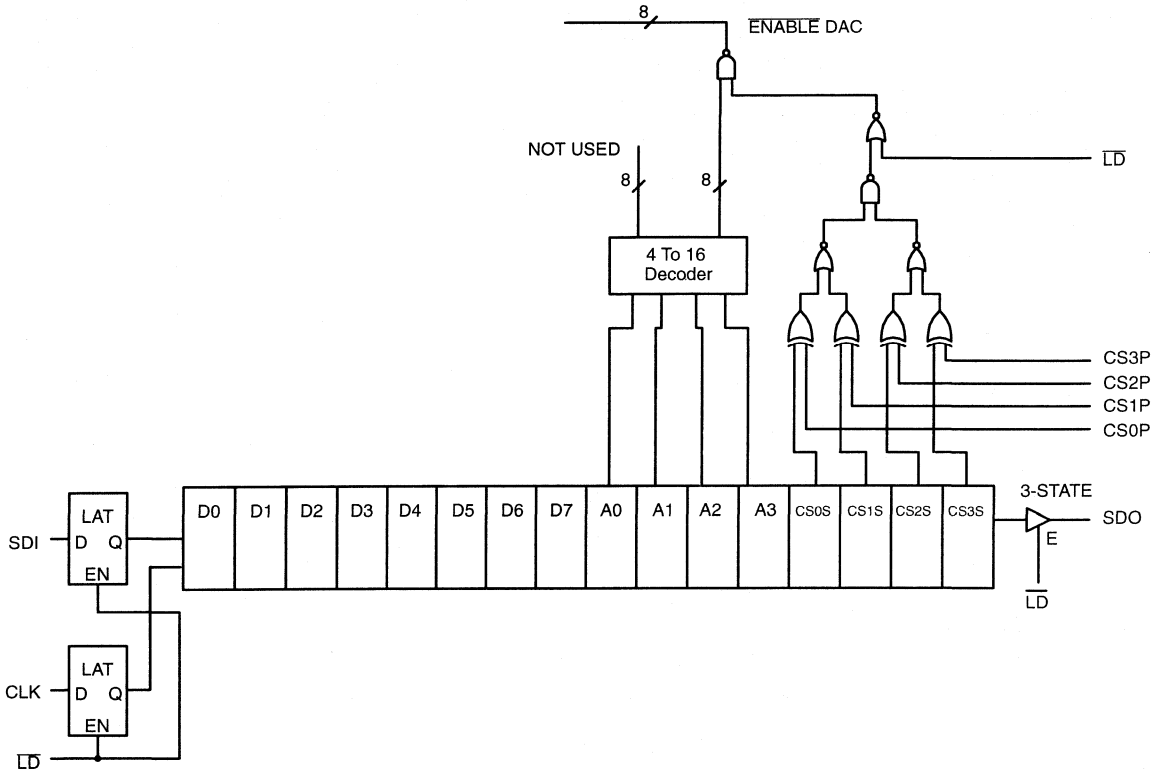


Figure 4. Internal Chip Address Decoder Plus Logic Interface

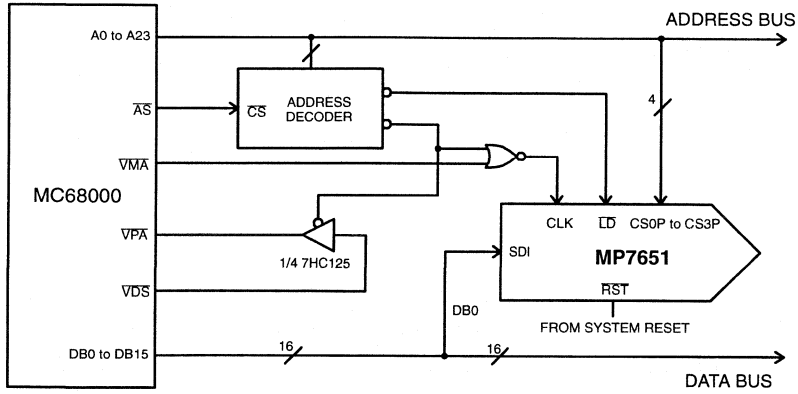
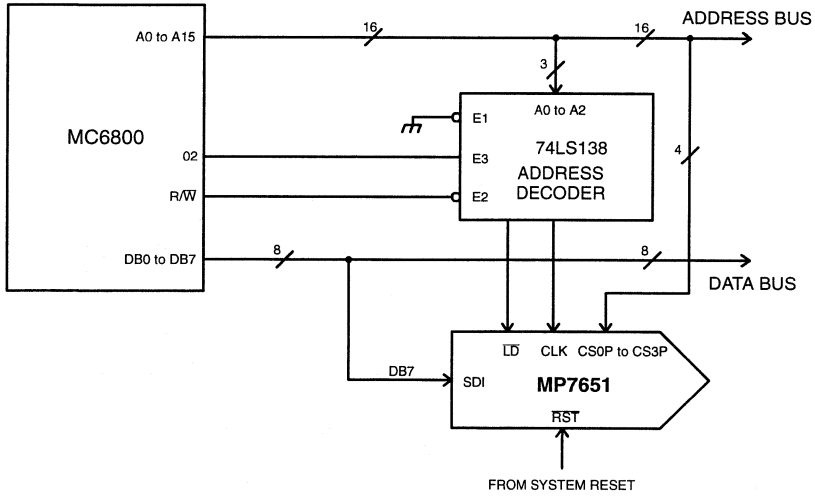


Figure 5. MC68000 Interface (Simplified Diagram)



NOTES:
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE location 2000, R/$\overline{W}$, and 02. A WRITE to address 4000 transfers data from the input shift register to the DAC register.

Figure 6. MC6800 Interface (Simplified Diagram)

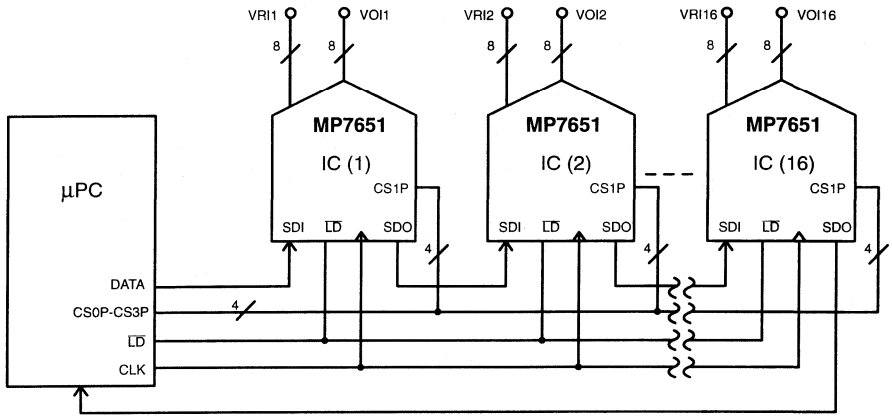


Figure 7. Simplified Diagram
Configuration A

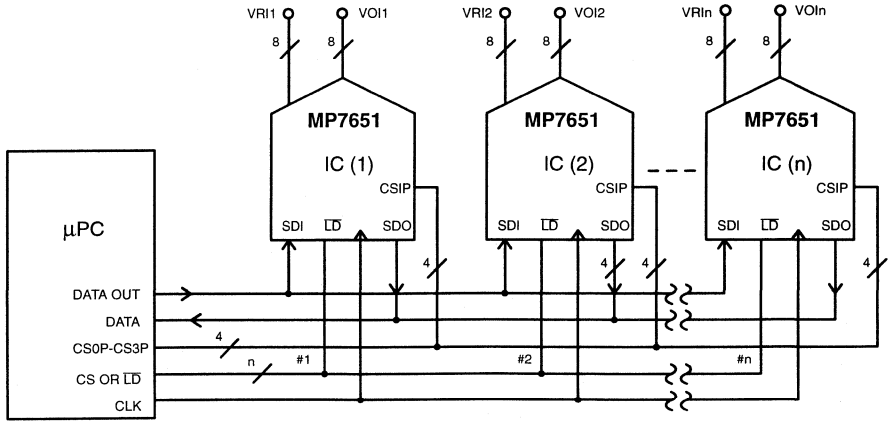


Figure 8. Simplified Diagram
Configuration B

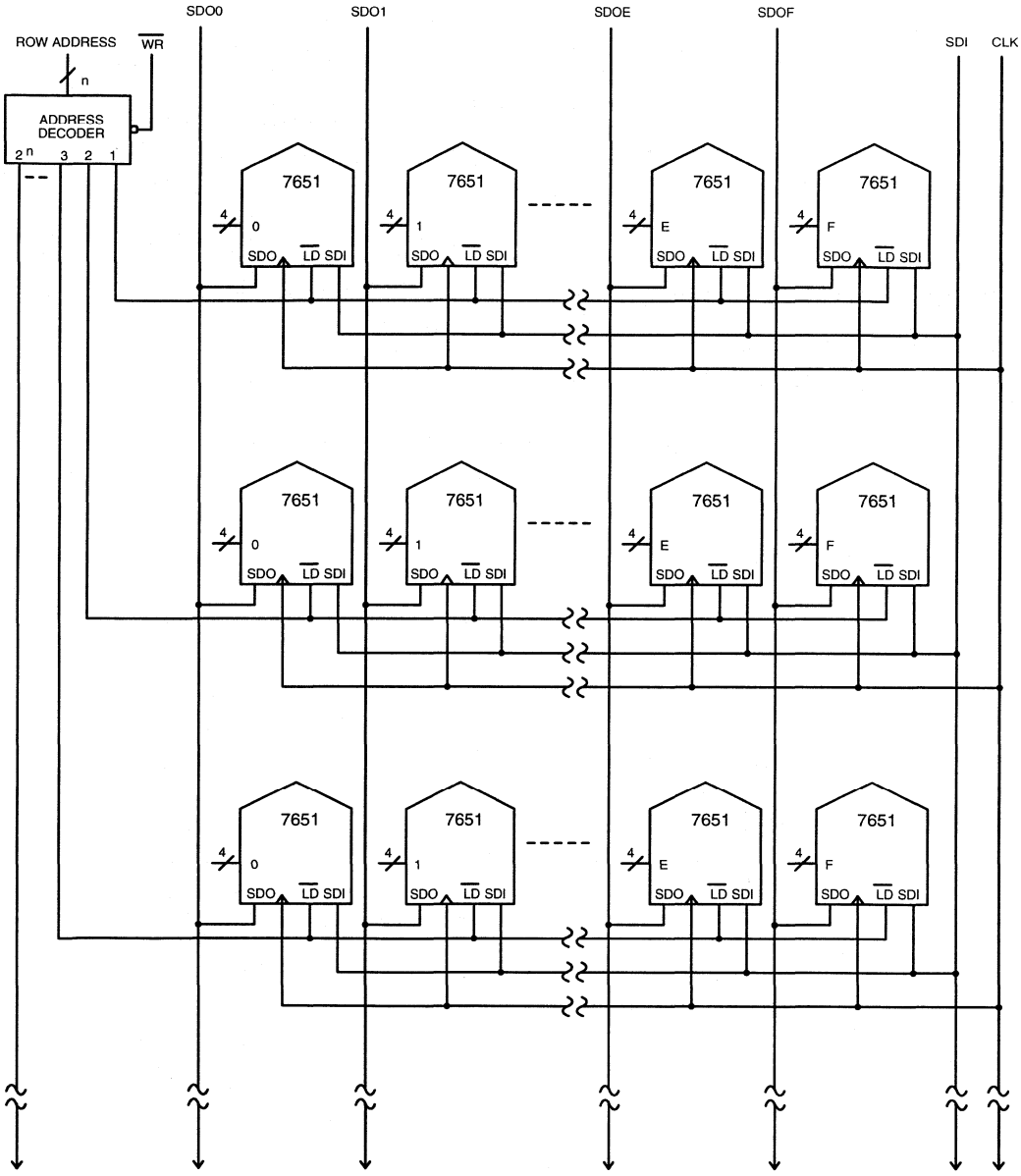
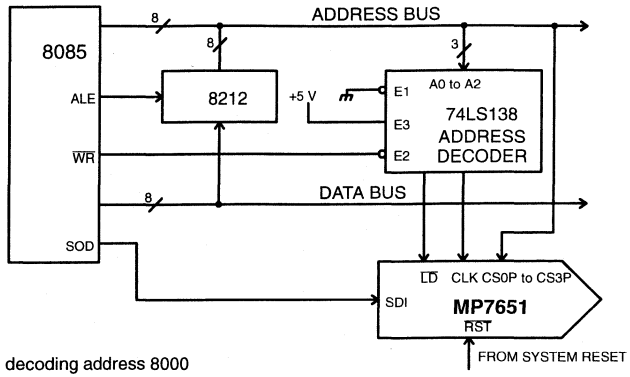


Figure 9. Simplified Diagram
Configuration C



NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000
2. Data is clocked into the DAC shift register by executing memory write instructions. The clock input is generated by decoding address 8000 and $\overline{WR}$. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

Figure 10. 8085 Interface (Simplified Diagram)

MP7651 EVALUATION BOARD

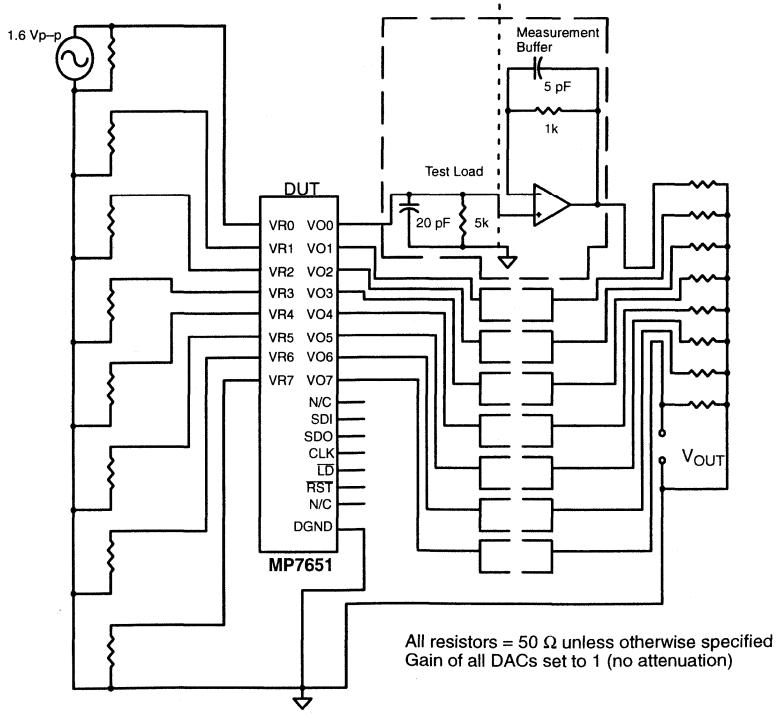
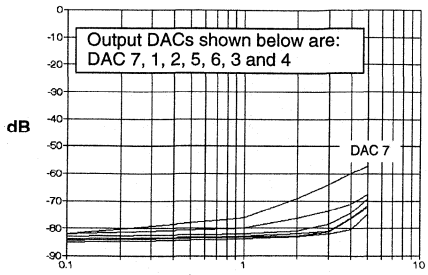


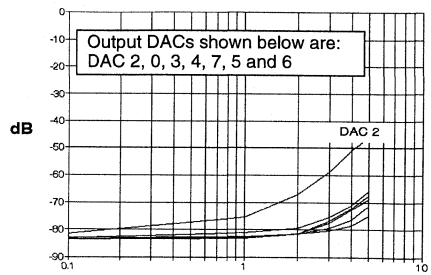
Figure 15. Crosstalk Measurement Set-Up

PERFORMANCE CHARACTERISTICS

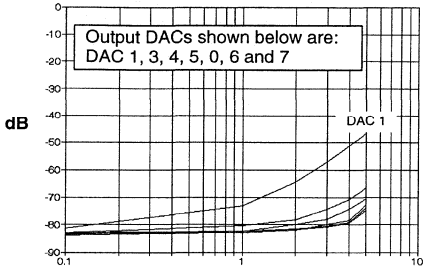
Channel-to-Channel Crosstalk (Gain vs. Frequency; All DACs set to full scale; V_{REF}=1.6 Vp-p)



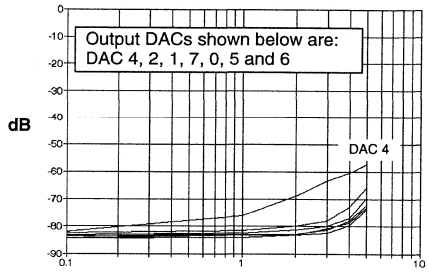
Graph 1.



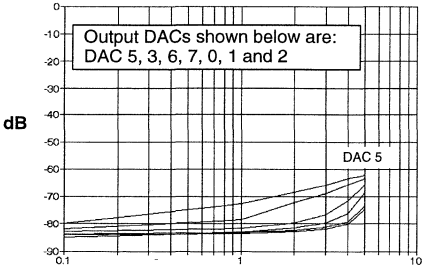
Graph 2.



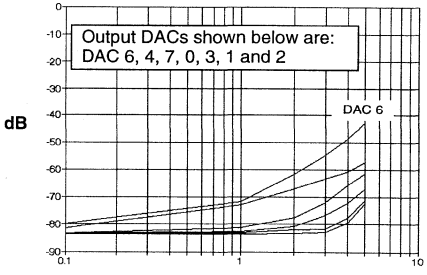
Graph 3.



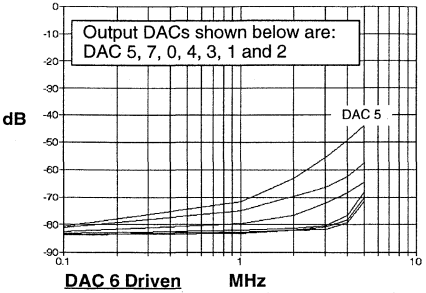
Graph 4.



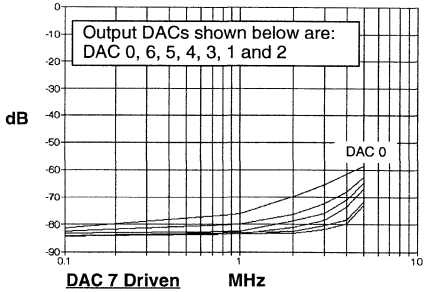
Graph 5.



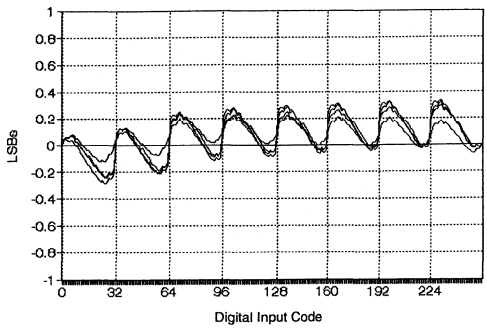
Graph 6.



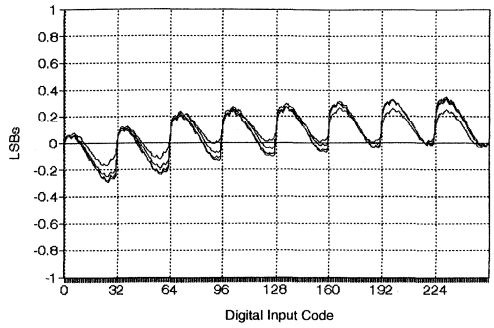
Graph 7.



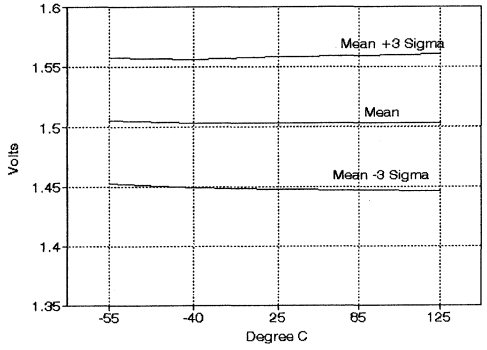
Graph 8.



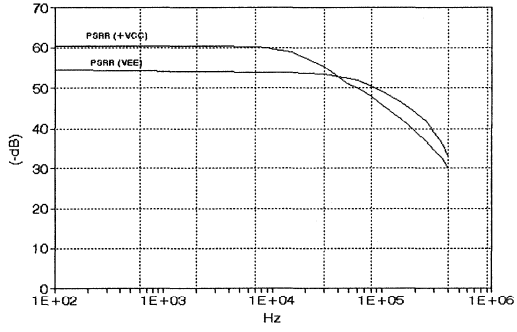
Graph 9. Linearity Error vs. Digital Input Code DACs 0 to 3



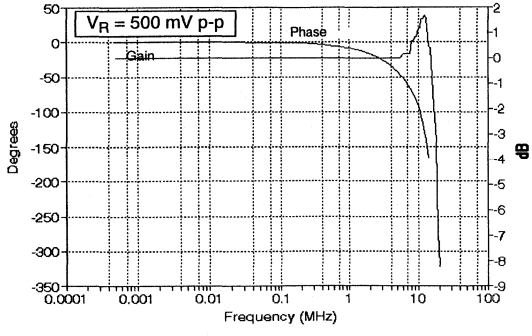
Graph 10. Linearity Error vs. Digital Input Code DACs 4 to 7



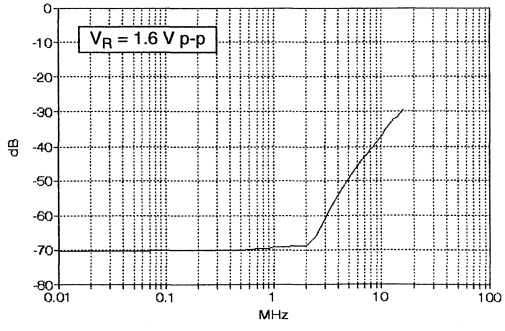
Graph 11. Preset Voltage vs. Temperature



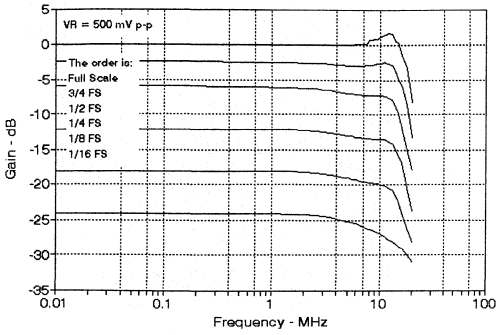
Graph 12. PSRR vs. Frequency



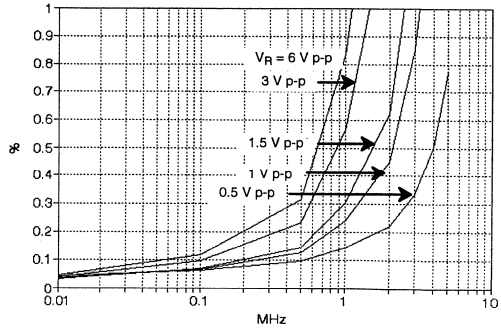
Graph 13. Gain & Phase vs. Frequency



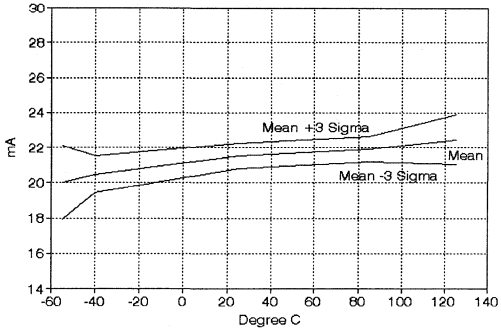
Graph 14. Feedthrough vs. Frequency



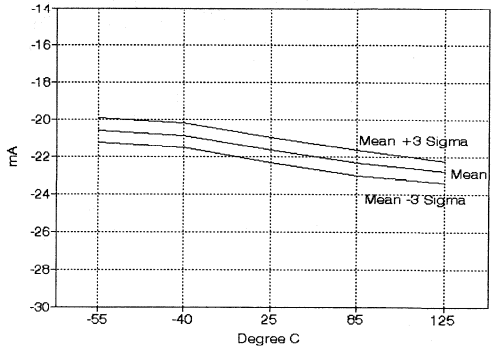
Graph 15. Gain (V_O/V_R) vs. Frequency Open Loop/Unloaded Output*



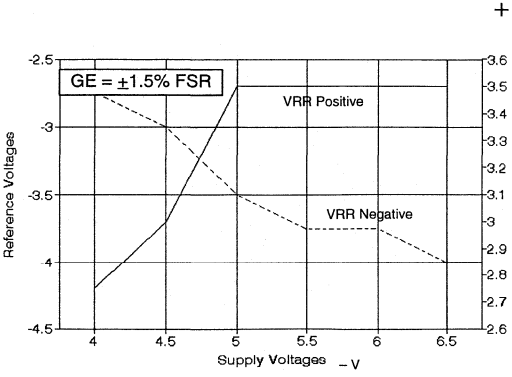
Graph 16. THD vs. Frequency



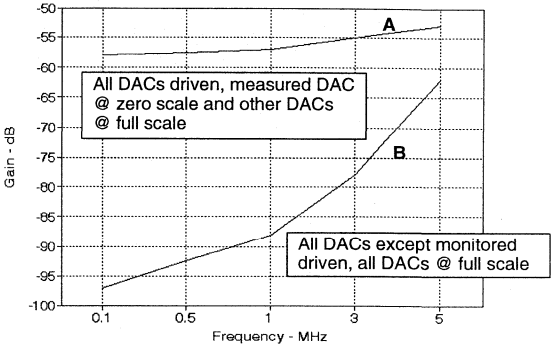
Graph 17. I_{CC} vs. Temperature



Graph 18. I_{EE} vs. Temperature

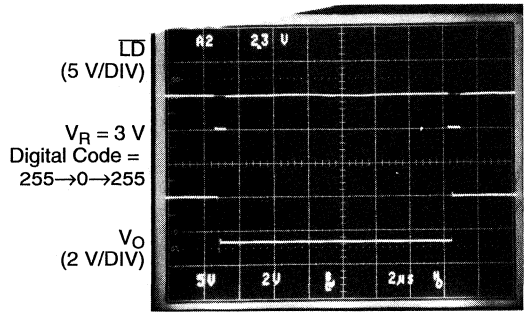


Graph 19. Reference Input Voltage Range vs. Supply Voltages

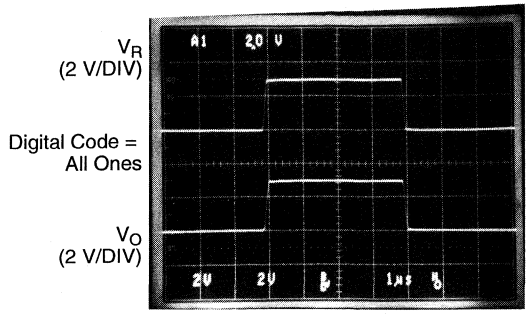


Graph 20. All Channel Crosstalk vs. Frequency

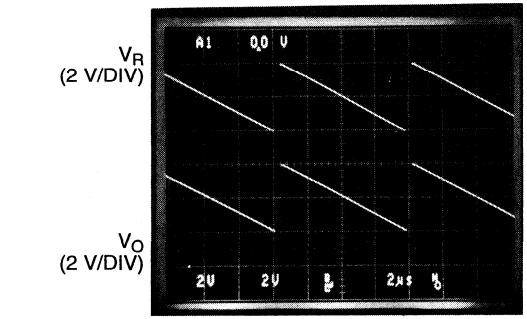
* A 2K or 5K resistor across output and V_{EE} will remove peaking (See graph 26).



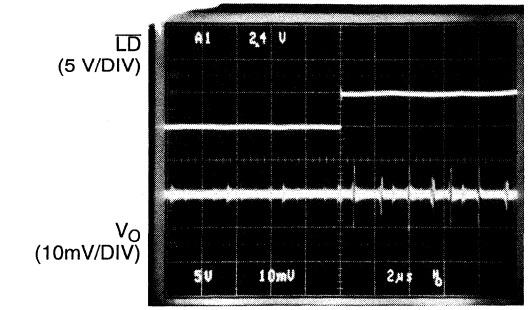
Graph 21. Digital Settling



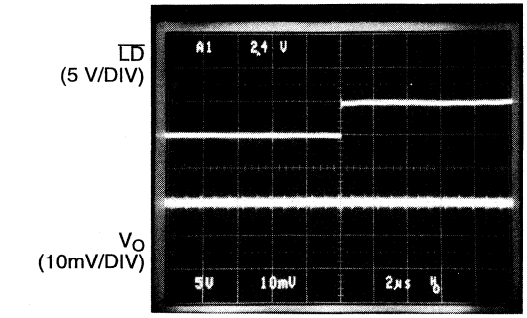
Graph 22. Pulse Response ($t_R = t_F$ = 100 ns for V_R)



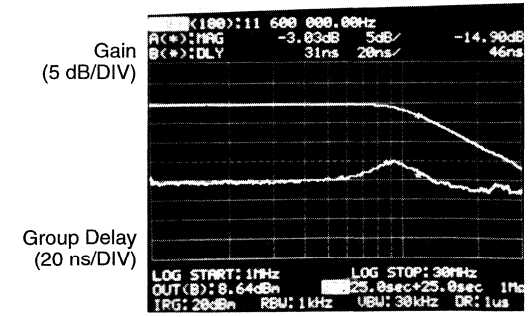
Graph 23. 128 kHz Sawtooth Waveform Response



Graph 24. Clock and SDI Feedthrough



Graph 25. Clock/SDI Feedthrough



Graph 26. Typical Gain and Group Delay vs. Frequency (with 5K resistor across output to V_{EE})

MP7652

4-Channel Voltage Output
15 MHz, Input Bandwidth, 8-Bit Multiplying
DACs with 3-Wire Serial Digital Port
and Independent References

EXAR

FEATURES

- Independent References
- 4 Independent 2-Quadrant Multiplying 8-Bit DACs
- Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability
- High Speed:
  - 12.5 MHz Digital Clock Rate
  - V_{REF} to V_{OUT} Settling Time: 150ns to 8–bit (typ)
  - Voltage Reference Input Bandwidth: 15 MHz
- Low Power: 80mW
- Low AC Voltage Reference Feedthrough
- Excellent Channel-to-Channel Isolation
- DNL = ±0.5 LSB, INL = ±1 LSB (typ)
- DACs Matched to ±0.5% (typ)
- Very Low Noise
- Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz
- V_{REF}/2 Output Preset Level
- Latch-Up Free
- ESD Protection: 2000 V Minimum

APPLICATIONS

- Direct High-Frequency Automatic Gain Control
- Video AGC & CCD Level AGC
- Convergence Adjustment for High-Resolution Monitors (Workstations)

4

GENERAL DESCRIPTION

The MP7652 is ideal for digital gain control of high frequency analog signals such as video, composite video, CCD and others. The device includes 4-channels of high speed, wide bandwidth, two quadrant multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving a ±1mA (typ) load. DNL of better than ±0.5 LSB is achieved with a channel-to-channel matching of typically 0.5%. Stability, matching, and precision of the DACs are achieved by using MPS' thin film technology. Also, excellent channel-to-channel isolation is achieved with EXAR's BiCMOS process which cannot be achieved using a typical CMOS technology.

An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 15 MHz (typ), fast output settling time of 150 ns, and excellent V_{REF} feedthrough isolation. The bottom of each DAC reference string is brought out separately for totally isolated operation. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal is achieved.

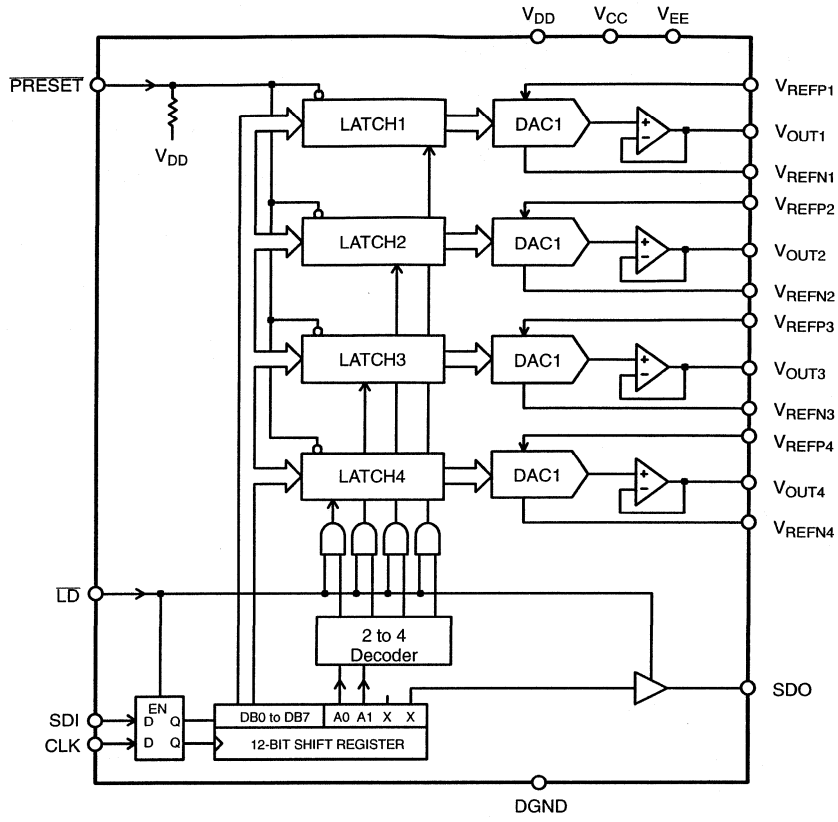
The combination of a constant input Z and the ability to vary V_{REFN} within V_{CC} –1.8 and V_{EE} +1.5 V allows flexibility for optimum system design.

The MP7652 is fabricated on a junction isolated, high speed BiCMOS (BiCMOS IV™) process with thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

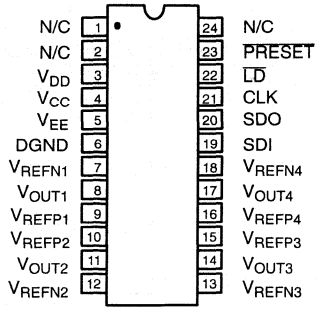
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	–40 to +85°C	MP7652AS	±1	±0.5	±1.5
Plastic Dip	–40 to +85°C	MP7652AN	±1	±0.5	±1.5

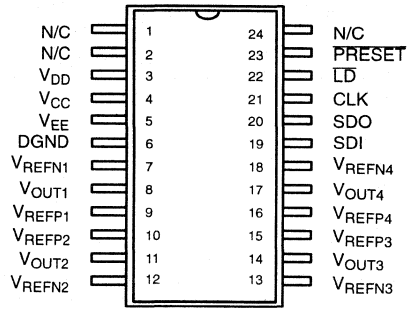
SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

4

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	N/C	No Connection
3	V_{DD}	Digital Positive Supply
4	V_{CC}	Analog Positive Supply
5	V_{EE}	Analog Negative Supply
6	DGND	Digital Ground
7	V_{REFN1}	DAC 1 Negative Reference Input
8	V_{OUT1}	DAC 1 Output
9	V_{REFP1}	DAC 1 Positive Reference Input
10	V_{REFP2}	DAC 2 Positive Reference Input
11	V_{OUT2}	DAC 2 Output
12	V_{REFN2}	DAC 2 Negative Reference Input
13	V_{REFN3}	DAC 3 Negative Reference Input

PIN NO.	NAME	DESCRIPTION
14	V_{OUT3}	DAC 3 Output
15	V_{REFP3}	DAC 3 Positive Reference Input
16	V_{REFP4}	DAC 4 Positive Reference Input
17	V_{OUT4}	DAC 4 Output
18	V_{REFN4}	DAC 4 Negative Reference Input
19	SDI	Serial Data and Address Input
20	SDO	Serial Data Output
21	CLK	Shift Register Clock Input
22	$\overline{LD}$	Load Data to Selected DAC
23	$\overline{PRESET}$	Preset all DACs to 1/2 ($V_{REF} - V_{REFN}$). $\overline{PRESET}$ is internally connected to V_{DD} through 300 kΩ.
24	N/C	No Connection

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = +5 V, V_{EE} = –5 V, V_{REFP} = 3 V and –3 V, T = 25°C, Output Load = Open, DGND=V_{REFN} = 0 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DC CHARACTERISTICS						
Resolution (All Grades)	N	8			Bits	
Differential Non-Linearity	DNL			±0.8	LSB	
Integral Non-Linearity	INL			±1	LSB	
Monotonicity			Guaranteed			
Gain Error	GE			±1.5	% FSR	FSR = Full Scale Range[1]
Zero Scale Offset	Z_{OFS}			±50	mV	
Output Drive Capability	I_O		±1		mA	
REFERENCE/INV INPUTS						
Impedance of V_{REF}	REF	6		18	kΩ	
Voltage Range	V_R	V_{EE} +1.5		V_{CC} –1.8	V	V_{REFP} Max Swing is V_{REFN} ±3 V
V_{REFN} DC Voltage Range	INV Pos.		V_O		V	
	INV Neg.		V_{EE} ±1		V	
DYNAMIC CHARACTERISTICS[2]						R_L = 5 kΩ, C_L = 20 pF
Input to Output Bandwidth			15		MHz	V_{REFP}=1.6 Vp–p, R_L=5kΩ, to V_{EE}
Input to Output Settling Time[6]			150		ns	V_{REFP}=1.6Vp–p, R_L=5kΩ, to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15		MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15		MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		275		ns	V_{REFP}=0 to V_{REFP} = 3V Step[6] to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		275		ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		TBD		dB	Codes=0 @ 1 MHz
Group Delay	GD		TBD		ns	
Harmonic Distortion	T_{HD}		TBD		%	V_{REFP}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		TBD		dB	@ 1 MHz, single channel
Digital Feedthrough	Q		TBD		nVs	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR		±0.5		%/%	ΔV=±5%
POWER CONSUMPTION						
Positive Supply Current	I_{CC}		12		mA	V_{REFP} = 0 V
Negative Supply Current	I_{EE}		12		mA	V_{REFP} = 0 V
Power Dissipation	P_{DISS}		80		mW	V_{REFP} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS						
Logic High[3]	V_{IH}	2.4			V	
Logic Low[3]	V_{IL}			0.8	V	
Input Current	I_L			±10	µA	
Input Capacitance[2]	C_L			8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS[2, 4]						
Input Clock Pulse Width	t_{CH}, t_{CL}	60			ns	
Data Setup Time	t_{DS}	70			ns	
Data Hold Time	t_{DH}	0			ns	
CLK to SDO Propagation Delay	t_{PD}			150	ns	
DAC Register Load Pulse Width	t_{LD}	100			ns	
PRESET Pulse Width	t_{PR}	50			ns	
Clock Edge to Load Rising Edge	t_{CKLD1}	100			ns	
Clock Edge to Load Falling Edge	t_{CKLD2}	0			ns	
Load Falling Edge to SDO Tri-state Enable	t_{HZ1}	80			ns	
Load Rising Edge to SDO Tri-state Disable	t_{HZ2}	40			ns	
Load Falling Edge to CLK Disable	t_{LDCK1}	30			ns	
Load Rising Edge to CLK Enable	t_{LDCK2}	60			ns	
LD Set-up Time with Respect to CLK	t_{LDSU}	20			ns	

NOTES

1 Full Scale Range (FSR) is 3V.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 *See Figures 1 and 2.*

5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to V_{REFN} ..... +6.5 V
V_{EE} to V_{REFN} ..... –6.5 V
V_{CC} to DGND ..... +13.0 V
V_{EE} to DGND ..... –6.5 V
V_{REFP} 1-4 to DGND, V_{REFN} ..... V_{CC} to V_{EE}
Digital Input & Output Voltage to DGND –0.5 to V_{DD} +0.5 V
Operating Temperature Range
Extended Industrial ..... –40°C to +85°C

Maximum Junction Temperature ..... –65°C to 150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 6mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

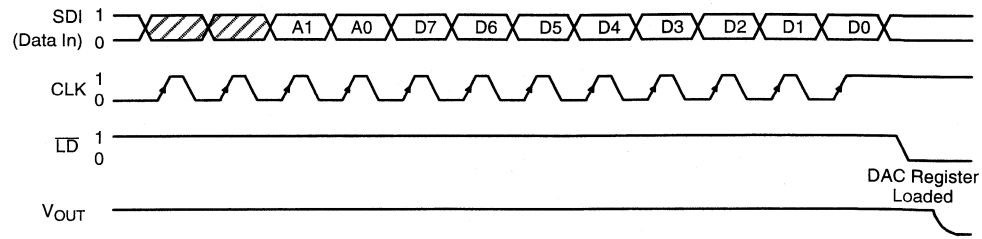


Figure 1. Serial Data Timing and Loading

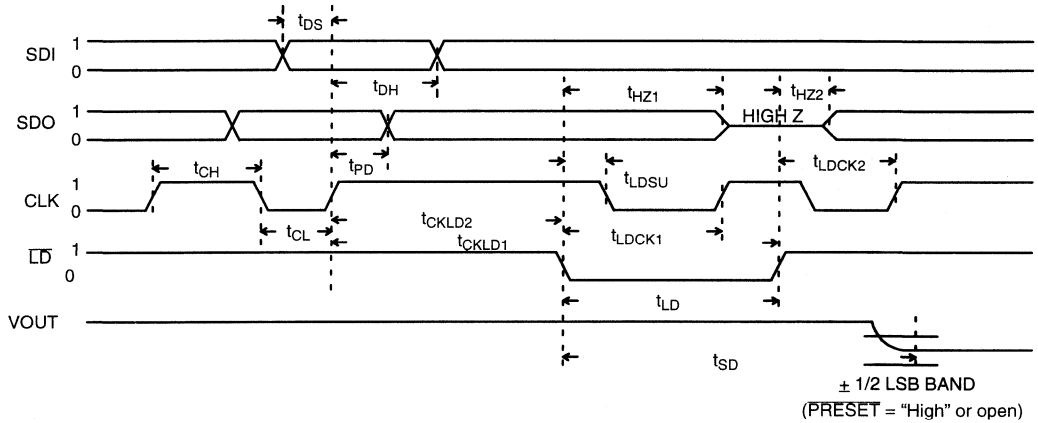


Figure 2. Detail Serial Data Input Timing

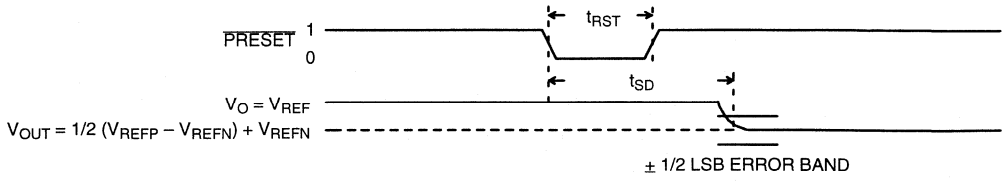


Figure 3. PRESET Operation

THEORY OF OPERATION

The MP7652 is a 4-channel multiplying D/A converter that incorporates a novel open loop architecture invented by MPS. The design produces the widest bandwidth, fastest settling time, most constant group delay, and a very low noise operation compared to the conventional R-2R based architectures (given an equal technology platform). This device is particularly useful in applications where analog multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Analog multipliers produce much higher noise and. This design allows for digital control of gain with constant and very low noise for all gain settings.

Linearity Characteristics

Each DAC achieves DNL $\leq \pm 0.5$ LSB (typ), INL $\leq \pm 1$ LSB (typ), and gain error $\leq \pm 1.5\%$. Since all 4 channel D/A converters are fabricated on the same IC, the linearity matching and gain matching of $\pm 0.5\%$ (typ) is achieved.

AC and Low Noise Performance

The novel subranging architecture delivers a 15 MHz (type) –3 dB bandwidth. A constant group delay of 70 ns (typ) is achieved to frequencies up to 8 MHz. Analog output settling time for a code change of FS to ZS and ZS to FS with $V_{REFP} = 3$ V, is typically 150 ns (with $R_L = 5$ k to V_{EE}). Also, with all codes set to FS (all 1s) and a V_{REFP} 3 V step, the analog output will settle to 8 bits in less than 110 ns (typ). Note that the AC performance specifications also match to between all 4 channels. The above AC and transient performance is achieved with each channel consuming only 20 mW (typ) with 10 V p-p supplies.

Serial Port

MP7652 is equipped with a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire (space). This interface consists of $\overline{LD}$ which controls the transfer of data to the selected DAC channel, SDI (serial data/address input), CLK (shift register clock) and SDO (serial data output). When the $\overline{LD}$ signal is high, CLK signal loads the digital input bits (SDI) into the 12-bit shift register. The $\overline{LD}$ signal going low loads this data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data input (SDI), output (SDO tri-stated) and the CLK input. This design tremendously reduces digital noise, and glitch transients into the DACs due to free running CLK and SDI. Also, tri-stating the SDO output with $\overline{LD}$ signal would allow read back of pre-stored digital data of the selected package using one SDO wire for all DAC ICs on the board. When the $\overline{PRESET}$ signal is low, the output of all DACs are 1/2 of ($V_{REFP} + V_{REFN}$), regardless of any digital inputs. Note that V_{REFP} is referenced to V_{REFN}.

Power Supplies and Voltage Reference DC Voltage Ranges

For the single supply operation, $V_{CC} = +10$ V, $V_{DD} = +5$ V, and $V_{EE} = DGND = 0$ V. The V_O 1-4 and V_{REFP} 1-4 range would be $V_{CC} - 1.8$ V ($10 - 1.8 = 8.2$ V) to $V_{EE} + 1.5$ V ($0 + 1.5 = 1.5$ V). V_{REFN} is the equivalent of AGND for this DAC. In this mode V_{REFN} can be set at $(V_{CC} + V_{EE})/2 = (10 + 0)/2 = 5$ V. V_{REFN} 1-4 DC range can also be set from $V_{EE} + 1.5 = 1.5$ V to $V_{CC} - 1.5 = 8.2$ V. Refer to *Table 2.* for the relationship equations.

For the dual supply operation, $V_{CC} = +5$, $V_{DD} = +5$, and $V_{EE} = -5$ V. The V_{OUT} 1-4 and V_{REFP} 1-4 range would be $V_{CC} - 1.8$ V ($-1.8 = 3.2$ V) to $V_{EE} + 1.5$ V ($-5 + 1.5 = -3.5$ V). In this mode V_{REFN} can be set to $(V_{CC} + V_{EE})/2 = (5 - 5)/2 = 0$ V. Similarly, V_{REFN} 1-4 DC range can be set from $V_{EE} + 1.5$ V = 3.5 V to $V_{CC} - 1.8 = +3.2$ V. Refer to *Table 2.* for the relationship equations.

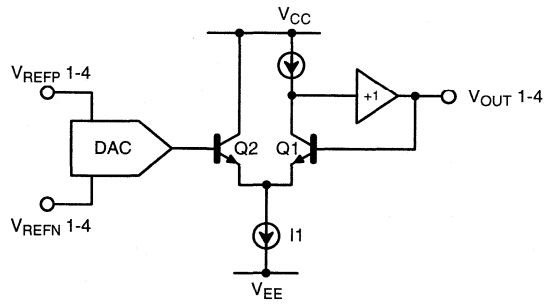


Figure 4. Simplified Block Diagram

Inputs				Internal Address		Output	
$\overline{\text{PRESET}}$	SDI	CLK	$\overline{\text{LD}}$	A1	A0	SDO	Operation
0	X	X	X	X	X	X	Preset all DACs to 1/2 ($V_{REFP} + V_{REFN}$)
1	Data In	0→1	1	X	X	Last bit of shift reg.	Shift data in and out
1	X	X	0	0	0	Hi-Z	DAC 1 Transparent
1	X	X	0→1	0	0	Last bit of shift reg.	DAC 1 Latched
1	X	X	0	0	1	Hi-Z	DAC 2 Transparent
1	X	X	0→1	0	1	Last bit of shift reg.	DAC 2 Latched
1	X	X	0	1	0	Hi-Z	DAC 3 Transparent
1	X	X	0→1	1	0	Last bit of shift reg.	DAC 3 Latched
1	X	X	0	1	1	Hi-Z	DAC 4 Transparent
1	X	X	0→1	1	1	Last bit of shift reg.	DAC 4 Latched

Table 1. Digital Function Truth Table
Serial In/Serial Out

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DAC Output Voltage $V_{OUTi} = V_{REFNi} + (V_{REFPi} - V_{REFNi})\left(\frac{D}{256}\right)$
0	0	0	0	0	0	0	0	V_{REFN}
0	0	0	0	0	0	0	1	$(V_{REFP} - V_{REFN})\left(\frac{1}{256}\right) + V_{REFN}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{REFP} - V_{REFN})\left(\frac{254}{256}\right) + V_{REFN}$
1	1	1	1	1	1	1	1	$(V_{REFP} - V_{REFN})\left(\frac{255}{256}\right) + V_{REFN}$

Table 2. DAC Transfer Function
Analog Output vs. Digital Code

OPERATION WITH DUAL POSITIVE POWER SUPPLIES

For the dual positive supplies operation, V_{CC} = +10 V, V_{DD} = 5 V, V_{EE} = 0 V and analog output zero level is to be referenced to (V_{CC} + V_{EE}) /2 by setting the AGND pin to 5 V.

MICROPROCESSOR INTERFACE

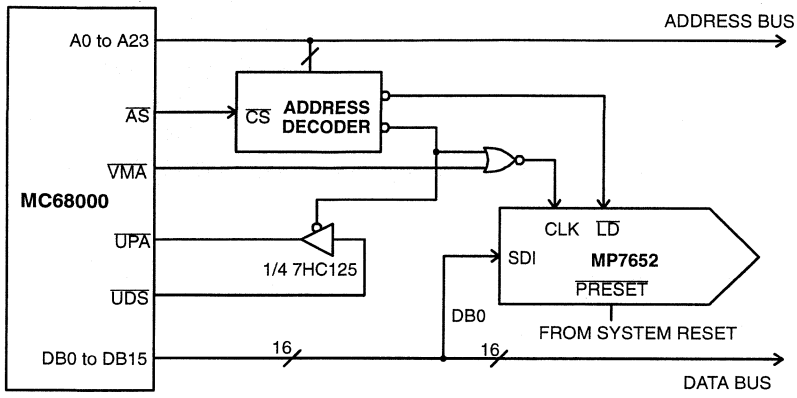
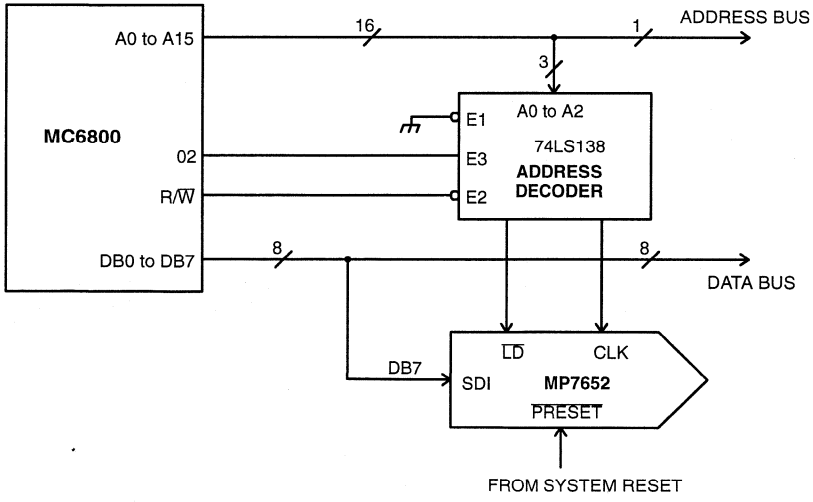


Figure 5. MC68000 Interface (Simplified Diagram)



NOTES:
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE location 2000, R/$\overline{W}$, and 02. A WRITE to address 4000 transfers data from the input shift register to the DAC register.

Figure 6. MC6800 Interface (Simplified Diagram)

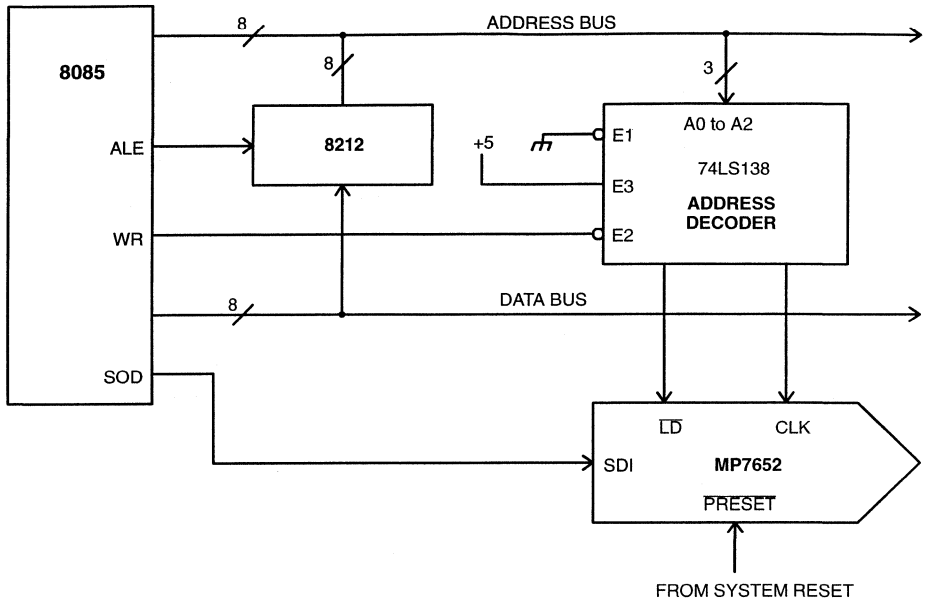


Figure 7. 8085 Interface (Simplified Diagram)

NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000
2. Data is clocked into the DAC shift register by executing memory write instructions. the clock input is generated by decoding address 8000 and $\overline{WR}$. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

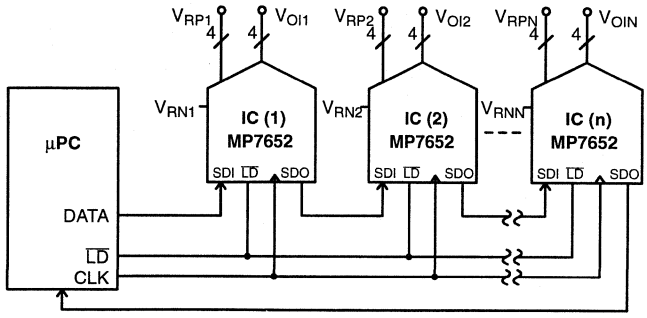


Figure 8. Simplified Diagram
Configuration A

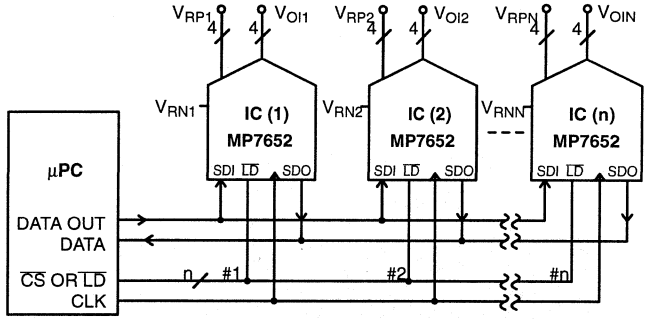


Figure 9. Simplified Diagram
Configuration B

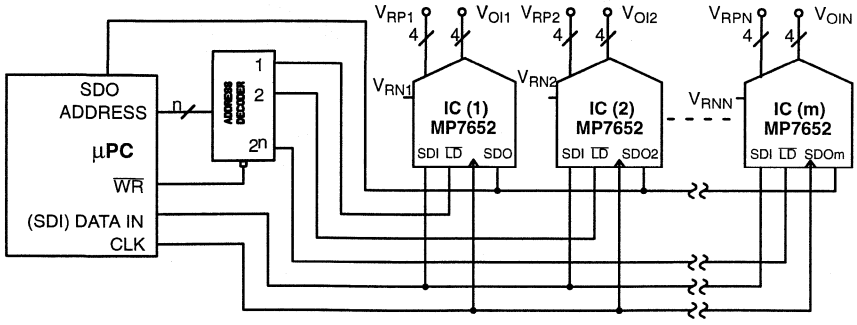
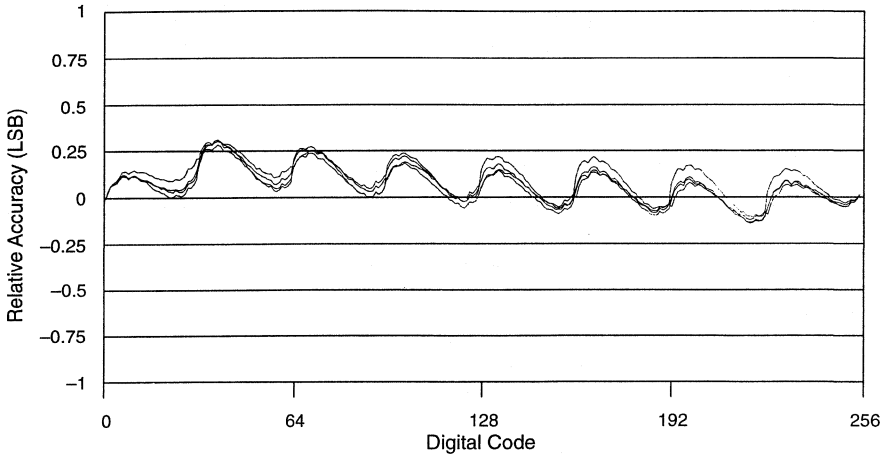
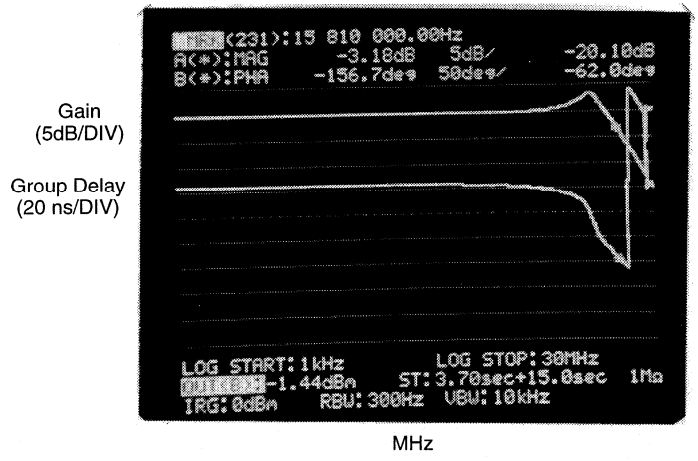


Figure 10. Simplified Diagram
Configuration C



Graph 3. Relative Accuracy vs. Digital Code
DACs 1 to 4



Graph 4. Typical Gain and Group Delay vs. Frequency
(with 5K Resistor Across Output to V_{EE})

MP7670

8-Channel, Voltage Output,
5 MHz, 4 Quadrant Multiplying
8-Bit D/A Converter with
Serial Digital Data Port

EXAR

FEATURES

- 8 Independent 4-Quadrant Multiplying 8-Bit DACs
- High Speed:
  - Settling Time: 2.5 μs to ±1 LSB (typ)
  - Slew Rate: 5 V/μs (typ)
  - Voltage Reference Input Bandwidth: 5 MHz (V_{IN} = 100 mV p-p)
- Low Power: 80 mW (typ)
- DACs Matched to ±0.5% (typ)
- Power on Preset to Zero Volts for All Outputs
- Midscale Preset, all DAC Outputs are Zero Volts
- Latch-Up Free
- Greater than 2000 V ESD Protection

APPLICATIONS

- Analog Multiplier Replacement
- High-Frequency Gain Control using DACs
- Convergence Adjustment for Displays and Monitors

4

GENERAL DESCRIPTION

The MP7670 is an 8-channel, 4 quadrant multiplying, 8-bit accurate digital-to-analog converter with a 5 MHz input bandwidth. It includes an output drive amplifier per channel capable of driving a ±7 mA to a load. DNL of ±0.25 LSB is achieved with a channel-to-channel matching of better than 0.5% (typ). Stability, matching, and precision of the DACs are achieved by using MPS' thin film technology.

The MP7670 is ideal for direct gain control of high frequency analog signals. The bipolar output amplifier has low noise which produces a very sharp signal output particularly in display and monitor applications.

A proprietary subranging architecture provides wide signal bandwidth from V_{IN} to output up to 5 MHz (typ), fast output settling time, and V_{IN} feedthrough isolation of –60dB (typ).

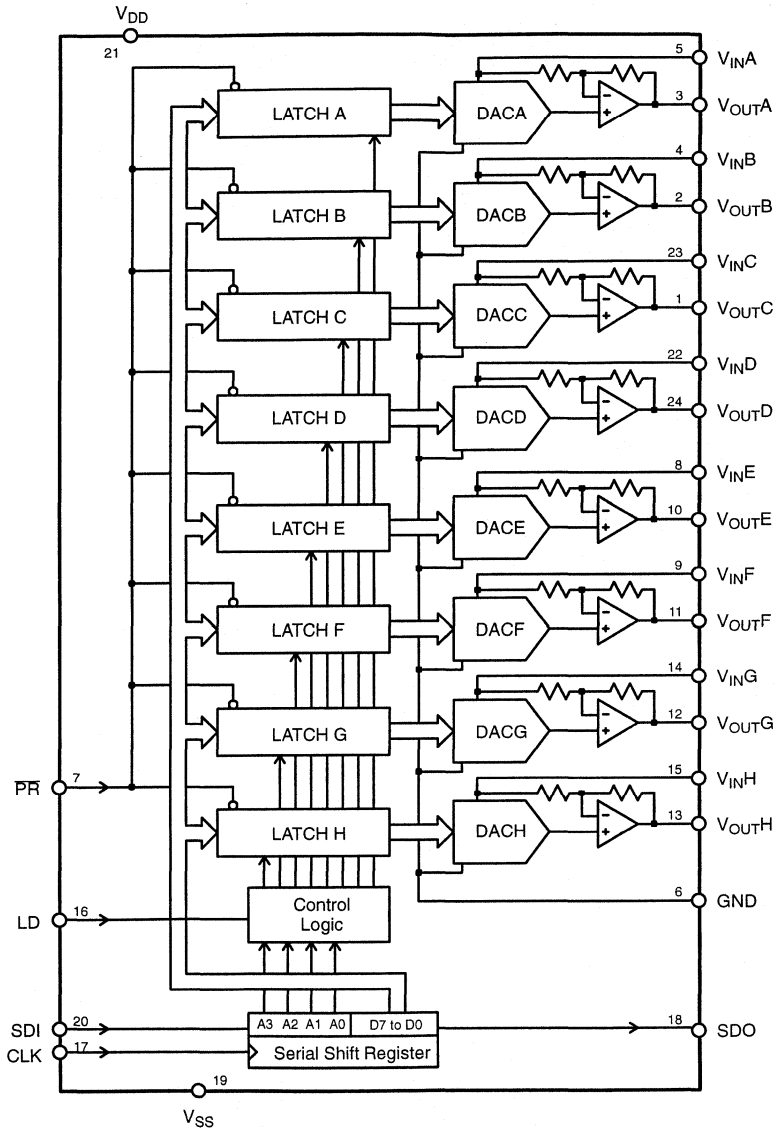
The MP7670 has a serial data 3-wire standard μ-processor logic interface to reduce pin count, package size, and board wire (space).

The MP7670 is fabricated on a junction isolated, high speed BiCMOS1™ process with thin film resistors.

ORDERING INFORMATION

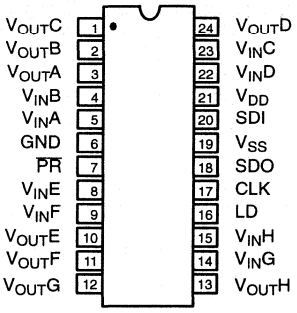
Package Type	Temperature Range	Part No.
Plastic Dip	–40 to +85°C	MP7670AN
SOIC	–40 to +85°C	MP7670AS

SIMPLIFIED BLOCK DIAGRAM

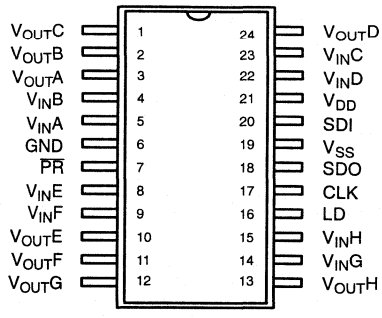


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

4

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output

PIN NO.	NAME	DESCRIPTION
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input
17	CLK	Serial Clock Input
18	SDO	Serial Data Output
19	V_{SS}	Negative Power Supply
20	SDI	Seral Data Input
21	V_{DD}	Positive Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{SS} = –5 V, GND = 0 V, $V_{IN}X$ = 3 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DC CHARACTERISTICS						
Resolution (All Grades)	N	8			Bits	
Differential Non-Linearity	DNL		±1/4	±1	LSB	
Integral Non-Linearity	INL			±1	LSB	
Monotonicity			Guaranteed			
Gain Error	GE		±1/2		LSB	
DAC OUTPUT						
Output Offset	V_{BZE}		3	25	mV	$\overline{PR}$ = 0, Sets Code = 80_H
Voltage Range	OVR	–3		3	V	
Output Current	I_{OUT}		±10		mA	ΔV_{OUT} <1 LSB
Capacitive Load	CL			200	pF	No oscillations
REFERENCE INPUTS						
Input Resistance of one DAC	R_{IN}	5			KΩ	R_{IN} (typ) = 15KΩ//Rx Rx = 20KΩ/(1-Code/256)
Input Capacitance[2]	C_{IN}		15	25	pF	
Voltage Range[1]	IVR	–3		3	V	
DYNAMIC CHARACTERISTICS[2]						
Input to Output Bandwidth Small Signal	BWS	2	5		MHz	Code = FS, $V_{IN}X$ = 100 mVp-p
Input to Output Bandwidth Large Signal	BWL		3		MHz	Code = FS, $V_{IN}X$ = 1 Vp-p
Slew Rate	SR		5		V/µs	Measured 10% to 90%, $\Delta V_{OUT}X$ = ±6 V
V_{IN} Feedthrough	F_{DT}		–60		dB	Code = HS, up to f = 100 kHz
Total Harmonic Distortion	T_{HD}		0.02		%	$V_{IN}X$ = 4 V p-p, Code = FS f = 1 kHz, f_{LP} = 80 kHz
Spot Noise Voltage	e_N		0.17		µV/√Hz	f = 1 kHz
Output Settling Time	t_S		2.5	5.0	µs	±1 LSB, Code = 0 to FS
Channel-to-Channel Crosstalk	C_T	60			dB	Measured between adjacent channels, f = 100 kHz
Digital Feedthrough	Q		6		nVs	$V_{IN}X$ = 0 V, Code = 0 to FS
DIGITAL INPUTS						
Logic High[3]	V_{IH}	2.4			V	
Logic Low[3]	V_{IL}			0.8	V	
Input Current	I_L			±1	µA	
Input Capacitance[2]	C_L			8	pF	
DIGITAL OUTPUTS						
Logic High	V_{OH}	3.5			V	I_{OH} = –0.4 mA
Logic Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
POWER SUPPLIES						
Power Supply Range	V_{DD}	4.5		5.5	V	
	V_{SS}	–5.5		–4.5	V	
Power Supply Rejection Ratio						
Positive	PSRR+		0.0002	0.01	%/%	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%
Negative	PSRR–		0.0002	0.01	%/%	$\overline{PR}$ = 0 V, ΔV_{SS} = ±5%
Power Dissipation	P_{DISS}		80	130	mW	$\overline{PR}$ = 0 V
Power Supply Current	I_{DD}		8	13	mA	$\overline{PR}$ = 0 V
Negative Supply Current	I_{SS}		8	13	mA	$\overline{PR}$ = 0 V
DIGITAL TIMING SPECIFICATIONS[2, 4]						
Input Clock Pulse Width	t_{CH}, t_{CL}	80			ns	
Data Setup Time	t_{DS}	40			ns	
Data Hold Time	t_{DH}	20			ns	
CLK to SDO Propagation Delay	t_{PD}			120	ns	
Load Pulse Width	t_{LD}	70			ns	
Preset Pulse Width	t_{PR}	50			ns	
Clock Edge to Load	t_{CKLD}	30			ns	
Load Edge to Next Clk Edge	t_{LDCK}	60			ns	

NOTES

1 Maximum input voltage is 2 V less than V_{DD}.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 See timing diagram.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +6.5 V
V_{SS} to GND ..... –6.5 V
V_{INA-H} to GND ..... V_{DD} to V_{SS}
V_{OUTA-H} to GND ..... V_{DD} to V_{SS}
Digital Input & Output Voltage to GND . –0.5 to V_{DD} +0.5 V
Operating Temperature Range
Extended Industrial ..... –40°C to +85°C

Maximum Junction Temperature ..... –65°C to +150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

THEORY OF OPERATION

The MP7670 contains 8 independent 4-quadrant multiplying D/A converters with output amplifiers. The design has incorporated a novel approach that provides fast, accurate, low noise, low distortion, small size, and low power in the same device. This device is particularly useful in applications where multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Also note that typical multipliers tend to increase noise particularly for low gain settings and have high offsets. The MP7670 design delivers a very low, constant noise, and low offset with digital control through the entire gain ranges of the D/A converter.

Linearity Characteristics

Each D/A converter in the MP7670 achieves DNL $\leq \pm 0.25$ LSB (typ), and gain error $\leq \pm 0.2\%$ (typ). Since all 8 channels of MP7670 are fabricated in the same IC, the linearity, gain matching, and input-output characteristics of all 8 channels match extremely well.

The Logic Interface and Serial Port

The MP7670 is equipped with a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire (small size). This interface consists of LD which controls the transfer of data to the selected DAC channels that are fed through the SDI (serial digital data and address bits) with the CLK (digital input shift register clock). Please refer to the following timing diagrams and truth tables for logic details.

A SDO (serial digital data output driver) is connected to the other side of the input shift register and would save SDI bus space by allowing the daisy chaining of several MP7670s (connecting SDI of device 2 to SDO of device 1).

When the LD signal is low, CLK signal loads the digital input bits (SDI) into the 12-bit shift register. The LD signal going high loads this data into the selected DACs. Also, when the $\overline{PR}$ signal is low, the output of all DACs would be reset to 0 volts.

Power Supplies and Input Voltage Ranges

The MP7670 is capable of functioning with $\pm 5V$ and $\pm 3V$ supplies. The output and input DC ranges are limited to within ± 2 V from each positive and negative supplies. For example, with supplies at $\pm 5V$, the recommended output range is $\pm 3V$.

The MP7670 design eliminates any code dependent current change into its GND, hence easing the board level design by eliminating the stringent need for other types of DACs for low GND impedance wiring considerations at board level.

Each output of the MP7670 DAC has an output amplifier driver delivering less than 0.05Ω of output impedance through a push-pull linear output stage. Each output and input characteristics parameter match extremely well, given that all channels are fabricated in the same IC.

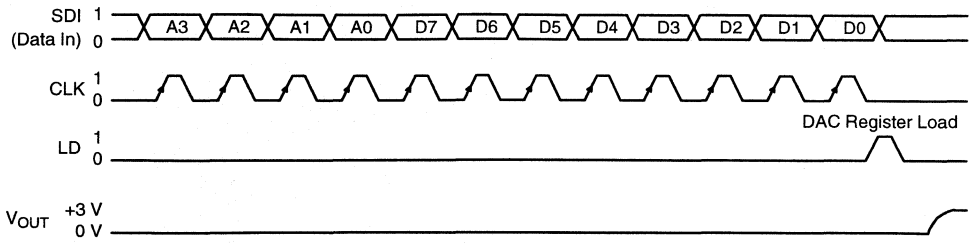


Figure 1. Serial Data Timing and Loading

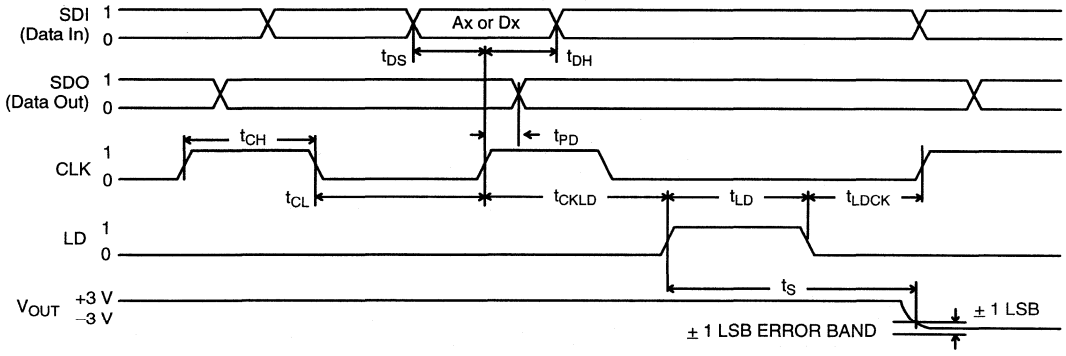


Figure 2. Detail Serial Data Input Timing ($\overline{PR}$ = "1")

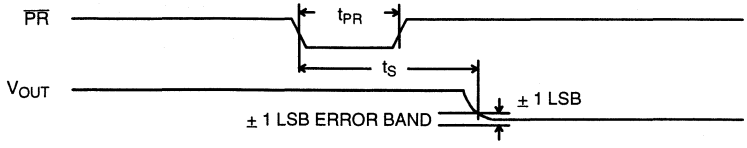


Figure 3. PRESET Timing

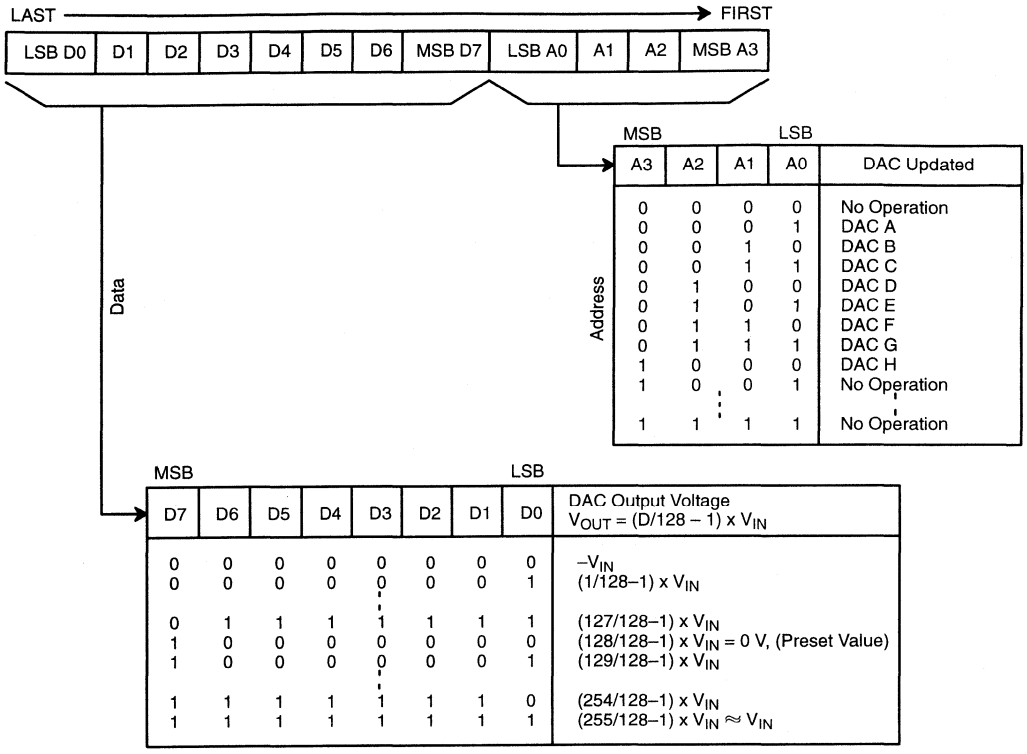


Table 1. Serial Input Format

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X	↑	L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

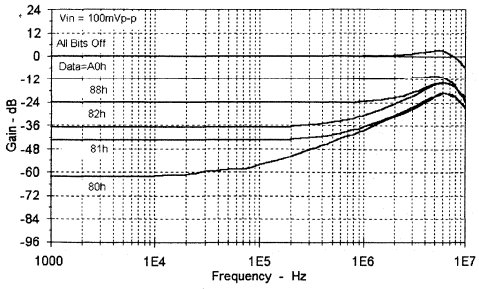
*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

Table 2. Control Logic Truth Table

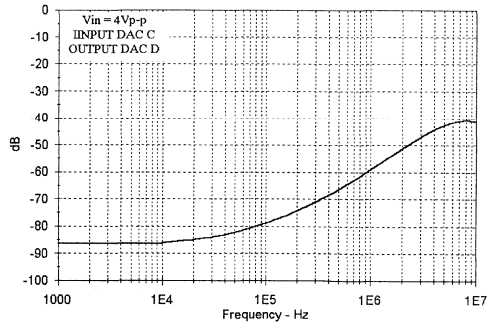
Decimal Input (D)	V_{OUT} (D)	Comments (V_{IN} = 3 V)
0	–3.00 V	Inverted FS
1	–2.98	
127	–0.02	
128	0.00	Zero Output
129	0.02	
254	2.95	
255	2.98	Full Scale (FS)

Table 3. DAC Transfer Function

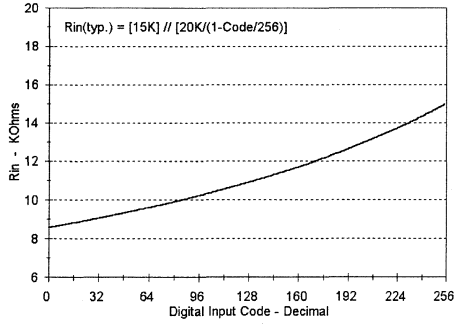
PERFORMANCE CHARACTERISTICS



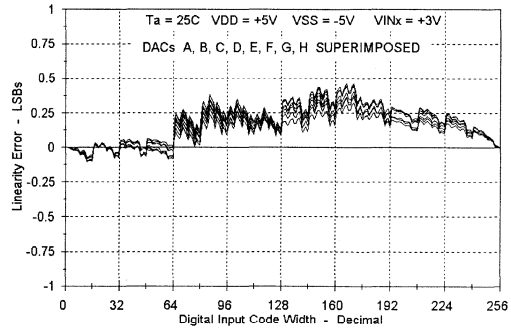
Graph 1. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency



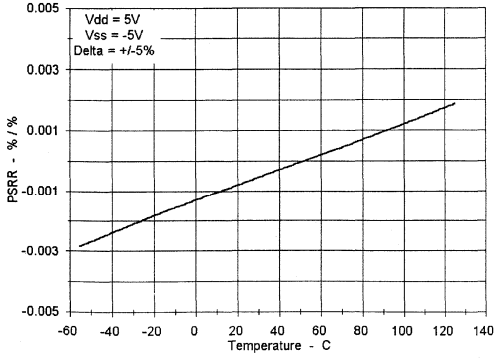
Graph 2. DAC Crosstalk vs. Frequency



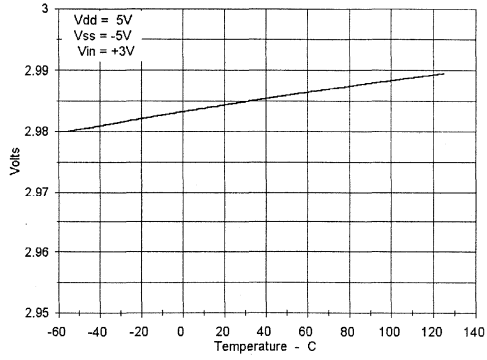
Graph 3. DAC Input Resistance vs. Digital Input Code



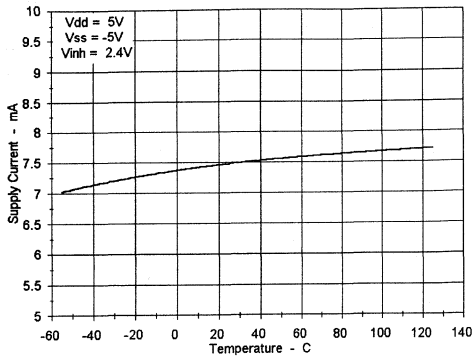
Graph 4. Linearity Error vs. Digital Input Code



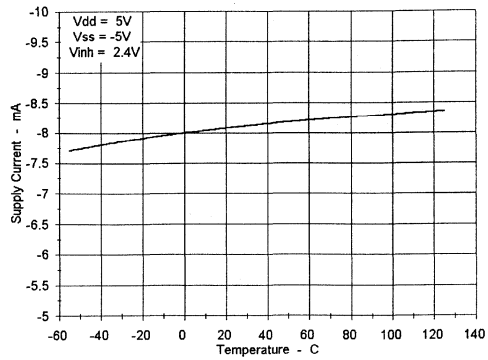
Graph 5. PSRR (DC) vs. Temperature



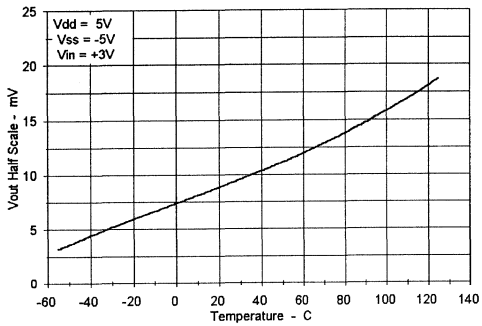
Graph 6. V_{OUT} Full Scale vs. Temperature



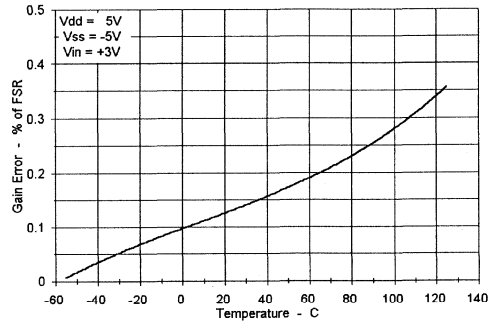
Graph 7. Supply Current (I_{DD}) vs. Temperature



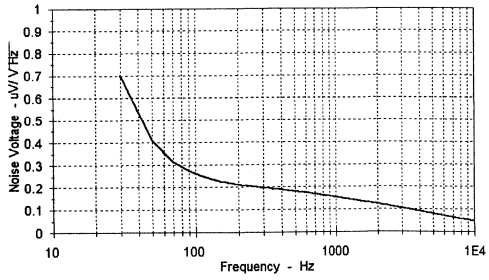
Graph 8. Supply Current (I_{SS}) vs. Temperature



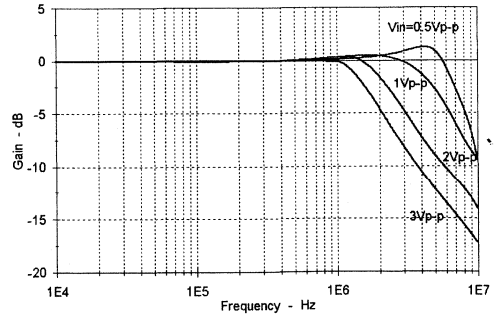
Graph 9. V_{OUT} Offset Error vs. Temperature



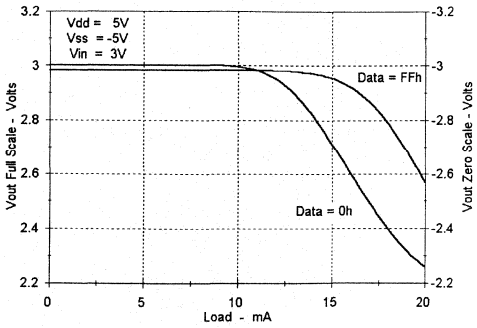
Graph 10. Gain Error vs. Temperature



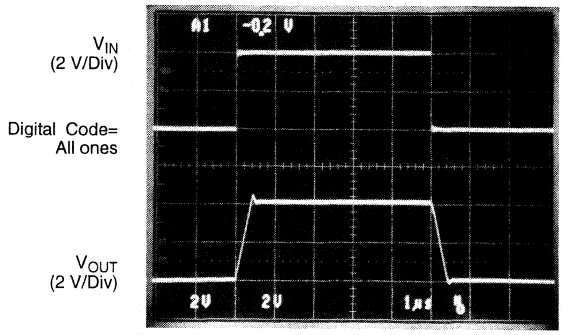
Graph 11. Voltage Noise Density vs. Frequency



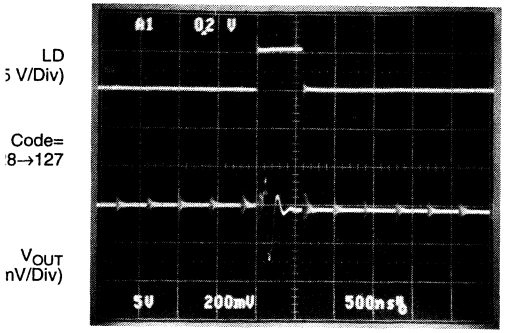
Graph 12. Varying Reference Input DAC Gain vs. Frequency



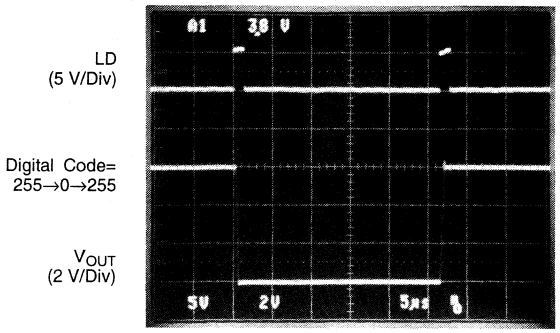
Graph 13. V_{OUT} Output Drive Capability



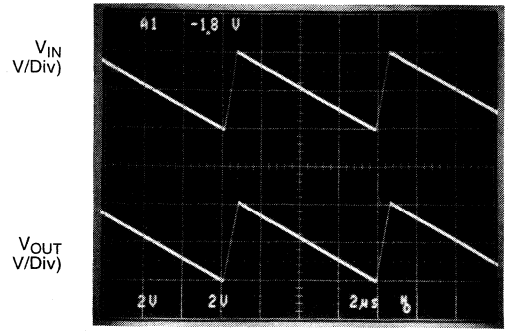
Graph 14. Pulse Response



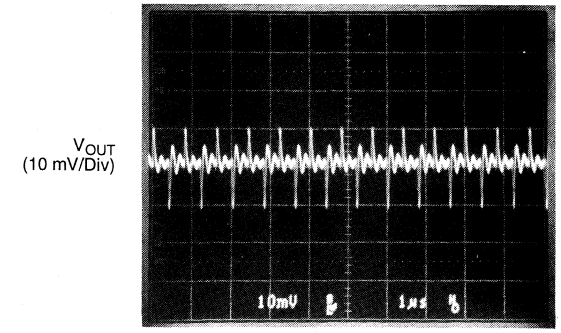
Graph 15. 1 LSB Digital Step Change



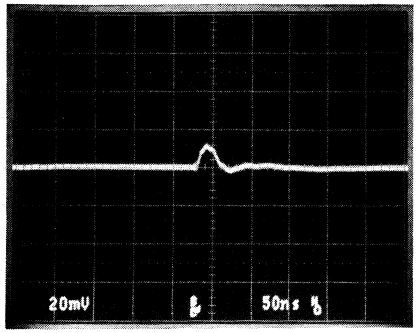
Graph 16. Settling Time



Graph 17. 128kHz Sawtooth Waveform Response



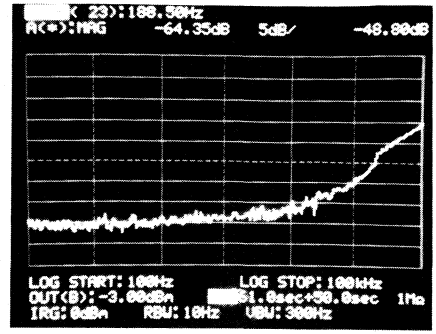
Graph 18. Clock Feedthrough



V_{OUT} (20 mV/Div)

50 ns/Div

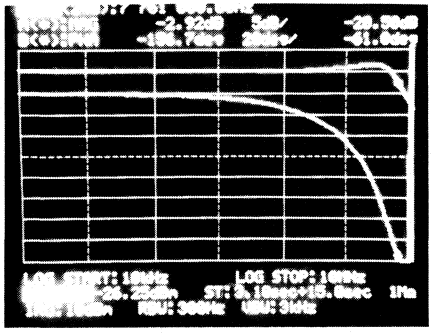
Graph 19. Digital Crosstalk



V_{OUT} (5 dB/Div)

kHz

Graph 20. PSRR vs. Frequency

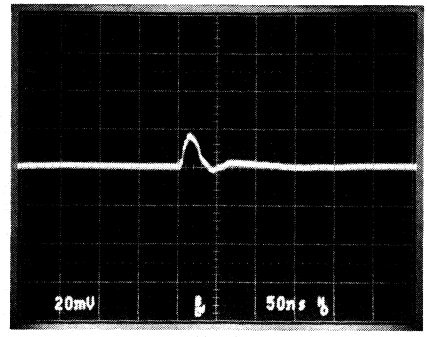


Gain (5 dB/Div)

Phase 20°/Div

MHz

Graph 21. Gain & Phase vs. Frequency



V_{OUT} (20 mV/Div)

50 ns/Div

Graph 22. Digital Feedthrough

MP7680

5 V CMOS 12-Bit
Quad Double-Buffered Multiplying
Digital-to-Analog Converter

FEATURES

- MPS Pioneered Segmented DAC Approach
- Four Double-Buffered 12-bit DACs on a Single Chip
- Independent Reference Inputs
- Lowest Gain Error in a Multiple DAC Chip
- Guaranteed Monotonic - All Grades, All Temperatures
- TTL/5 V CMOS Compatible Inputs
- Industry Standard Digital Interface
- Four Quadrant Multiplication
- Latch-Up Free

BENEFITS

- Reduced Board Space; Lower System Cost.
- Independent Control of DACs
- Excellent DAC-to-DAC Matching and Tracking

APPLICATIONS

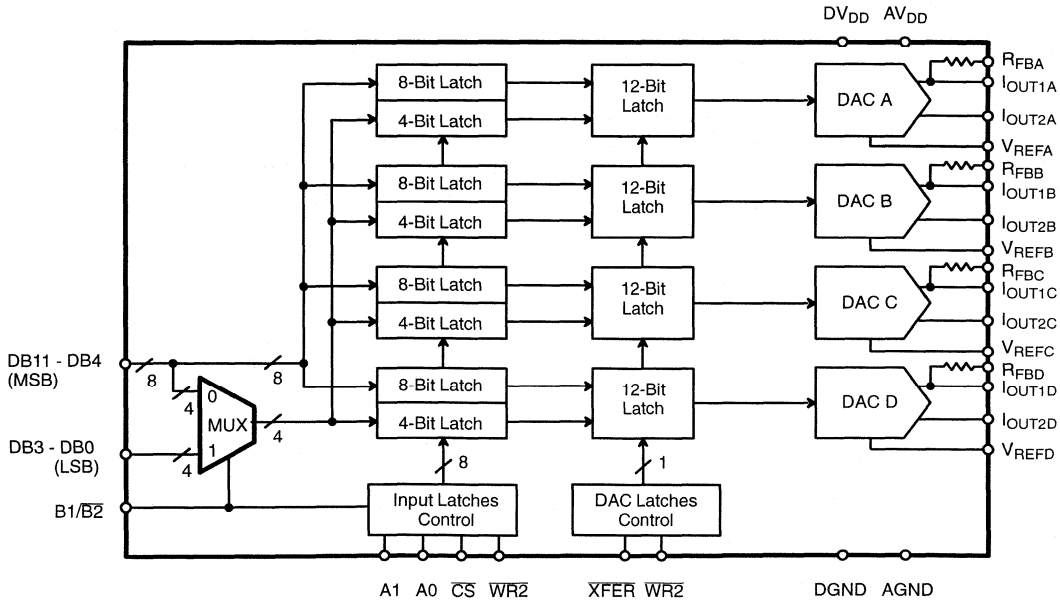
- Function Generators
- Automatic Test Equipment
- Precision Process Controls
- Recording Studio Control Boards

GENERAL DESCRIPTION

The MP7680 and the integrate four 12-bit four-quadrant-multiplying DACs with independent reference inputs and excellent matching characteristics. The MP7680 grades offer 1/2, 1 and 2 LSB of relative accuracy. The superior offers a low 2 LSB of gain error.

Each DAC has double-buffering (an 8 and 4-bit latch and a 12-bit latch) between the data bus (DB11 - DB0) and the DAC. The internal 4-bit mux allows the use of 8 or 16-bit buses. The flexible latch control logic allows to update one or more DACs simultaneously.

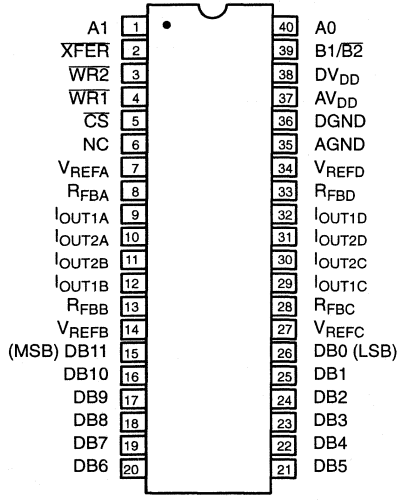
SIMPLIFIED BLOCK DIAGRAM



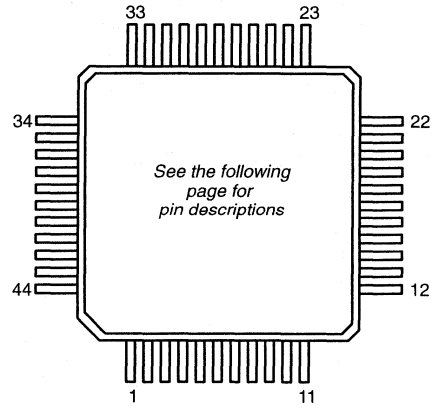
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7680JN	±2	±4	±16
Plastic Dip	–40 to +85°C	MP7680KN	±1	±2	±16
Ceramic Dip	–40 to +85°C	MP7680JD	±2	±4	±16
Ceramic Dip	–40 to +85°C	MP7680KD	±1	±2	±16
PQFP	–40 to +85°C	MP7680JE	±2	±4	±16
PQFP	–40 to +85°C	MP7680KE	±1	±2	±16
Ceramic Dip	–55 to +125°C	MP7680SD	±2	±4	±16

PIN CONFIGURATIONS



40 Pin PDIP, CDIP (0.600")
N40, D40



44 Pin PQFP
Q44

PIN OUT DEFINITIONS

40 Pin PDIP, CDIP

PIN NO.	NAME	DESCRIPTION
1	A1	DAC Address Bit 1
2	$\overline{XFER}$	Transfer: Updates all DAC's
3	$\overline{WR2}$	Write 2: Gates the $\overline{XFER}$ Function
4	$\overline{WR1}$	Write 1: Gates the DAC Selection
5	$\overline{CS}$	Chip Select
6	NC	No Connection
7	V_{REFA}	Reference Input for DAC A
8	R_{FBA}	Feedback Resistor for DAC A
9	I_{OUT1A}	Current Output A
10	I_{OUT2A}	Complement of Output A
11	I_{OUT2B}	Complement of Output B
12	I_{OUT1B}	Current Output B
13	R_{FBB}	Feedback Resistor for DAC B
14	V_{REFB}	Reference Input for DAC B
15 – 26	DB11 to DB0	Input Data Bits 11 (MSB) to 0 (LSB)
27	V_{REFC}	Reference input for DAC C
28	R_{FBC}	Feedback Resistor for DAC C
29	I_{OUT1C}	Current Output C
30	I_{OUT2C}	Complement of Output C
31	I_{OUT2D}	Complement of Output D
32	I_{OUT1D}	Current Output D
33	R_{FBD}	Feedback Resistor for DAC D
34	V_{REFD}	Reference input for DAC D
35	AGND	Analog Ground
36	DGND	Digital Ground
37	AV_{DD}	Analog Power Supply
38	DV_{DD}	Digital Power Supply
39	B1/$\overline{B2}$	Select Input Format (8/4 or 12 bits in)
40	A0	DAC Address Bit 0

44 Pin PQFP

PIN NO.	NAME	DESCRIPTION
1	NC	No Connection
2	V_{REFA}	Reference Input for DAC A
3	R_{FBA}	Feedback Resistor for DAC A
4	I_{OUT1A}	Current Output A
5	I_{OUT2A}	Complement of Output A
6	NC	No Connection
7	I_{OUT2B}	Complement of Output B
8	I_{OUT1B}	Current Output B
9	R_{FBB}	Feedback Resistor for DAC B
10	V_{REFB}	Reference Input for DAC B
11-16	DB11 to DB6	Input Data Bits 11 (MSB) to 6
17	NC	No Connection
18-23	DB5-DB0	Input Data Bits 5 to 0 (LSB)
24	V_{REFC}	Reference input for DAC C
25	R_{FBC}	Feedback Resistor for DAC C
26	I_{OUT1C}	Current Output C
27	I_{OUT2C}	Complement of Output C
28	NC	No Connection
29	I_{OUT2D}	Complement of Output D
30	I_{OUT1D}	Current Output D
31	R_{FBD}	Feedback Resistor for DAC D
32	V_{REFD}	Reference input for DAC D
33	AGND	Analog Ground
34	DGND	Digital Ground
35	AV_{DD}	Analog Power Supply
36	DV_{DD}	Digital Power Supply
37	B1/$\overline{B2}$	Select Input Format (8/4 or 12 bits in)
38	A0	DAC Address Bit 0
39	NC	No Connection
40	A1	DAC Address Bit 1
41	$\overline{XFER}$	Transfer: Updates all DAC's
42	$\overline{WR2}$	Write 2: Gates the $\overline{XFER}$ Function
43	$\overline{WR1}$	Write 1: Gates the DAC Selection
44	$\overline{CS}$	Chip Select

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5 V, V_{REF} = +10 V, I_{OUT1} = I_{OUT2} = DGND = AGND = 0 V Unless Otherwise Noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
K				±1		±1		
J, S				±2		±2		
Differential Non-Linearity	DNL						LSB	
K				±1		±2.0		
J, S				±4		±4.0		
Gain Error	GE						LSB	Using Internal R_{FB}
K				±16		±16		
J, S				±16		±16		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±70	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±50		±200	nA	I_{OUT1} V_{IN} = 0 V I_{OUT2} V_{IN} = V_{DD}
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_{EXT}=13pF
Current Settling Time	t_S		1.0				µs	Full scale change to 1/2 LSB
REFERENCE INPUT								
Input Resistance	R_{IN}	3	5	7	3	7	kΩ	
Voltage Input Range[2]	V_{IN}		±10	±25			V	
DIGITAL INPUTS								
Input High Voltage	V_{IH}	2.4			2.4		V	
Input Low Voltage	V_{IL}			0.8		0.8	V	
Input Current	I_{LKG}			±1		±4	µA	V_{IN} = 0 V and V_{DD}
Input Capacitance[2]								
Data	C_{IN}		7.0				pF	
Control	C_{IN}		7.0				pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		100				pF	DAC all 1's
	C_{OUT1}		50				pF	DAC all 0's
	C_{OUT2}		50				pF	DAC all 1's
	C_{OUT2}		100				pF	DAC all 0's

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[4]								
Functional Voltage Range	V_{DD}	4.5		5.5	4.5	5.5	V	
Supply Current	I_{DD}			2		2	mA	Digital inputs = V_{IL} or V_{IH}
				1		1	mA	Digital inputs = 0 or 5 V
TIMING CHARACTERISTICS[2, 3]								
Write Pulse Width	t_{WR}	75			85		ns	
Chip Select Set-Up Time	t_{CS}	100			120		ns	
Address Set-Up Time	t_{AS}	100			120		ns	
Chip Select and Address Hold Time	t_H	0			0		ns	
Latch Select Set-Up Time	t_{BS}	120			150		ns	
Latch Select Hold Time	t_{BH}	10			15		ns	
Data Valid Set-Up Time	t_{DS}	100			120		ns	
Data Valid Hold Time	t_{DH}	0			0		ns	
Transfer Pulse Width	t_{XFER}	65			75		ns	
Write Cycle (per DAC)	t_{WC}	175			200		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.

2 Guaranteed but not production tested.

3 See timing diagram (*Figure 1.*).

4 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package. DC voltage differences will cause undesirable internal currents.

Specifications are subject to change without notice

4

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

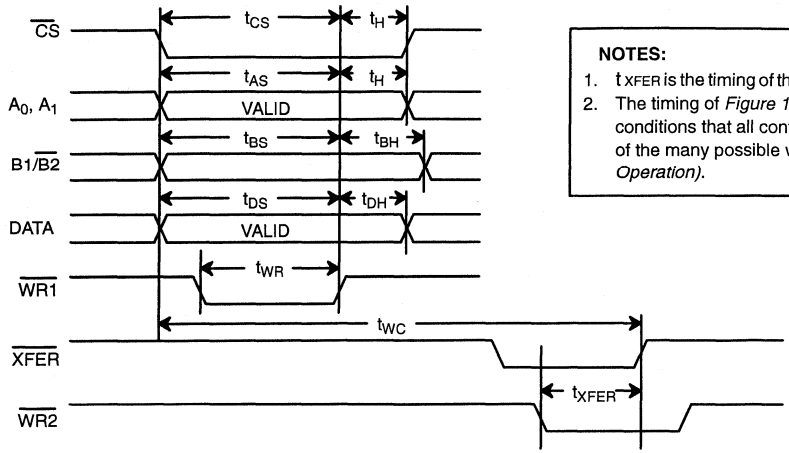
V_{DD} to AGND ..... –0.5 to +7 V
V_{DD} to DGND ..... –0.5 to +7 V
Digital Input Voltage to DGND ... GND –0.5 to V_{DD} +0.5 V
Any I_{OUT1}, I_{OUT2} to AGND ..... GND –0.5 to V_{DD} +0.5 V
Any V_{REF} to AGND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Any V_{RFB} to AGND ..... ±25 V
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, PQFP 800mW
Derates above 75°C ..... 11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.



NOTES:

1. t_{XFER} is the timing of the condition $\overline{XFER} = \overline{WR2}$ = Low.
2. The timing of *Figure 1.* reproduces graphically the conditions that all control signals must meet in any of the many possible writing cycles (*see Theory of Operation).*

Figure 1. Write Cycle Timing (Each DAC)

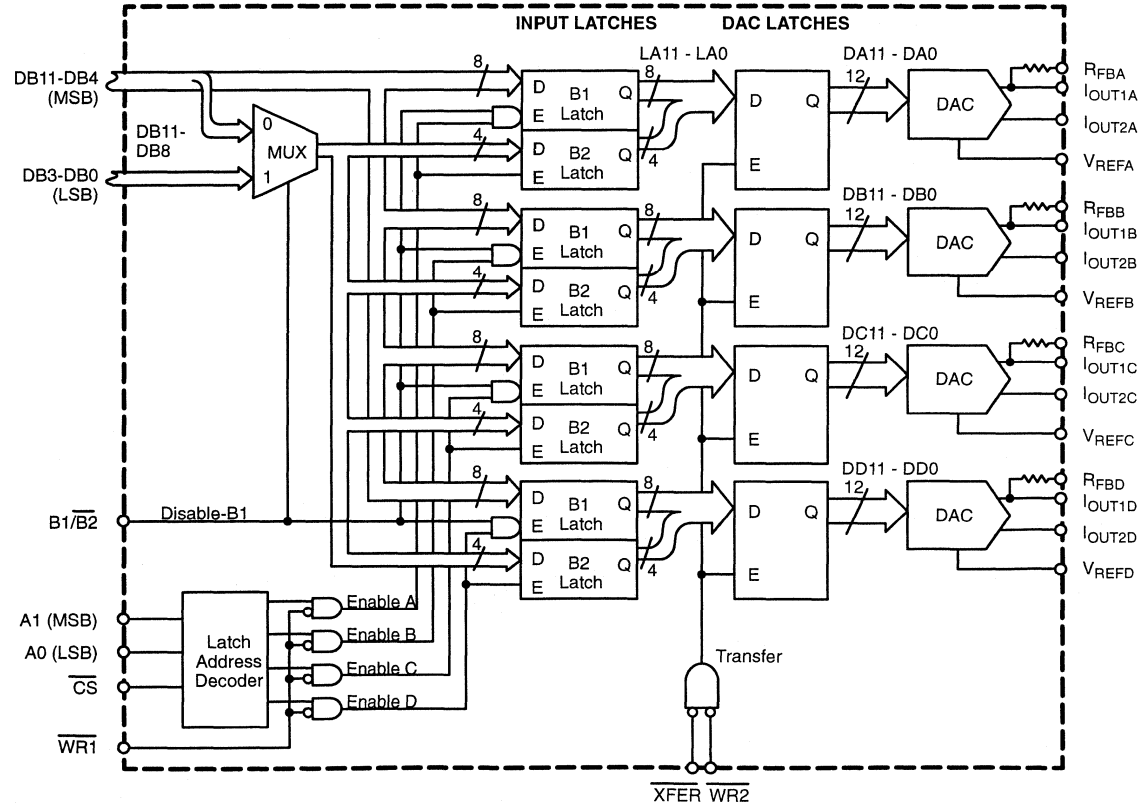


Figure 2. Latches Control Logic

THEORY OF OPERATION

Digital Interface

Figure 2. shows the internal control logic. The logic that controls the writing of the input latches and the one that controls the DAC latches are completely separated. It is easy to understand how the MP7680/80A works by understanding each basic operation.

Writing to Input Latches

By keeping B1/$\overline{B2}$ = high, a 12-bit bus has direct access to the 12 bits of the input latches. The condition $\overline{CS}$ = $\overline{WR1}$ = 0 loads the values contained in the data bus DB11-DB0 into the input latch addresses by A_1, A_0 (*Figure* 3a, *Table 1.*).

A_1	A_0	SELECTED DAC
0	0	A
0	1	B
1	0	C
1	1	D

Table 1. DAC Selection

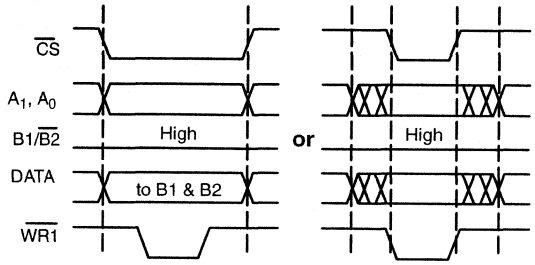


Figure 3a. 12 Bit Write Cycle

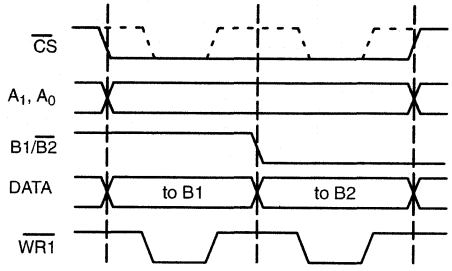


Figure 3b. 8-Bit Double Write Cycle

Figure 3. Write Cycles to Input Latches

An 8-bit bus must use two cycles. The second cycle is like the first one with the difference that B1/$\overline{B2}$ = low (*Figure 3b*). During the second cycle the condition B1/$\overline{B2}$ = low muxes DB11-DB8 to the B2 latches (*Figure 2.*).

Two important notes:

1) Timing diagrams show the inputs $\overline{CS}$, A_1, A_0, DB11-DB0 to be stable during the entire writing cycle. In reality all the above signals can change (*Figure 3a*) as long as they meet the timing conditions specified in the Electrical Characteristic Table.

2) Only 16-bit bus cycles are shown in the next few examples of interface timing. It is possible to generate an 8-bit interface timing by replacing a single 12-bit write cycle (*Figure 3a*) with a double 8-bit write cycles (*Figure 3b*). 8-bit applications should ground inputs DB3-DB0.

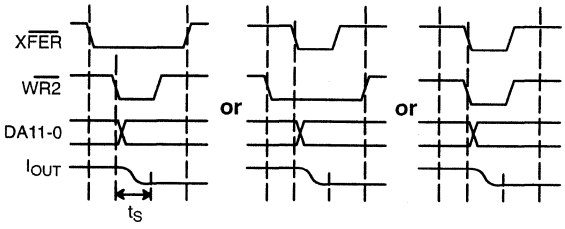


Figure 4. Transfer Cycles from Input Latches to DAC Latches

Transferring Data to the DAC Latches

Once one or all of the input latches have been loaded, the condition $\overline{XFER}$ = $\overline{WR2}$= low transfers the content of ALL the input latches in the DAC latches. The output of the DAC latches (DA11-DA0) changes and the DAC current (I_{OUT}) will reach a new stable value within the settling time t_S (*Figure 4.*).

Examples of DACs updating sequences:

1) Simultaneous updates of any number of DACs. The system uses from one (two) to four (eight) cycles to write from a 12 (8) bit bus into B1/$\overline{B2}$ latches. One transfer cycle updates the output of all DACs (*Figure 5.*)
2) Individual DAC update. The condition $\overline{WR2}$ = $\overline{XFER}$ = low makes the DAC latches transparent. A writing to the B1/$\overline{B2}$ latches updates the DAC outputs (*Figure 6.*).
3) Automatic transfer to DAC latches. An 8-bit bus can update any DAC with two cycles by connecting $\overline{WR1}$ = $\overline{WR2}$ and B1/$\overline{B2}$= $\overline{XFER}$. This is the correct individual DAC update for 8-bit busses (*Figure 7.*).
4) Transfer by a second device. A processor may load the input latches while the final $\overline{XFER}$ pulse is left to another device.

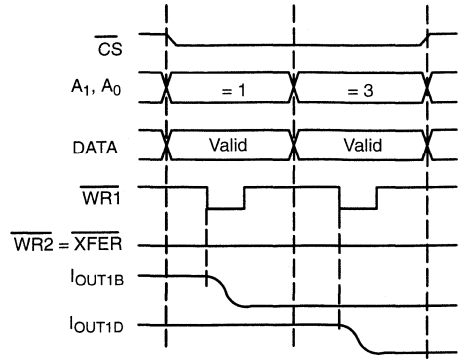


Figure 6. Individual DAC Update

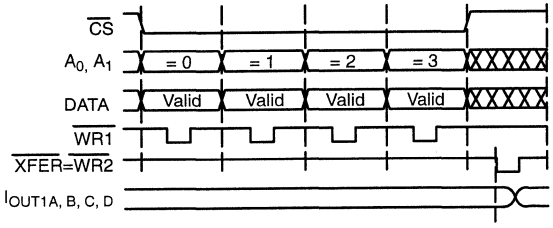


Figure 5. Simultaneous Updates of DACs

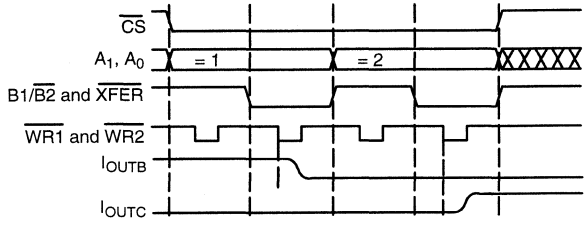


Figure 7. Automatic Transfer to DAC Latches

APPLICATION NOTES

Refer to Section 8 for Applications Information

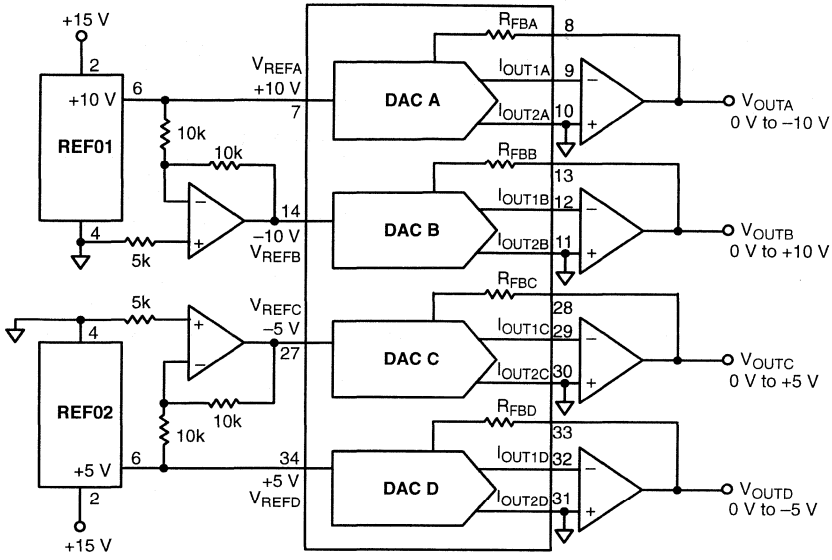


Figure 8. Digitally Programmable Quad Voltage Output ±10 V, ±5 V

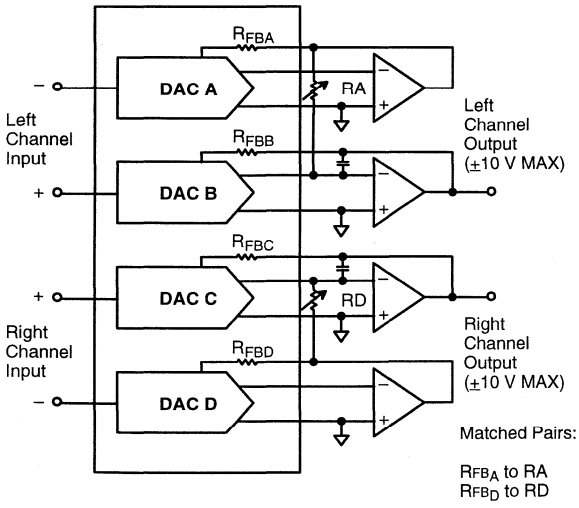


Figure 9. "Clickless" Audio Attenuator/Amplifier

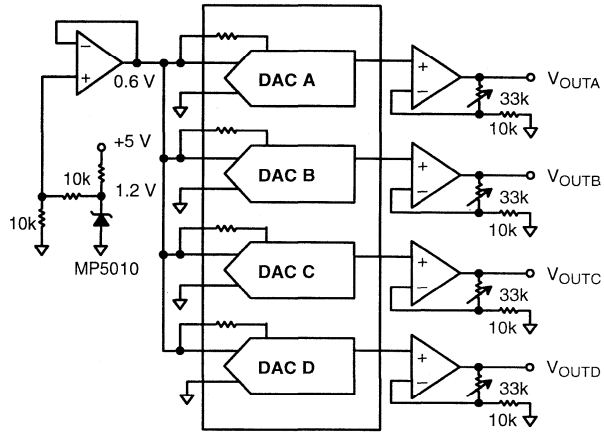


Figure 10. Quad DAC for Single +5 V Supply

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MP8840

8-Channel, Voltage Output, 2 MHz, 4 Quadrant Multiplying, 8-Bit DAC with Serial Digital Data Port

EXAR

FEATURES

- **8 Independent 4-Quadrant Multiplying 8-Bit DACs**
- **High Speed:**
  - **Settling Time: 3.5 μs to ±1 LSB**
  - **Slew Rate: 4 V/μs**
  - **Voltage Reference Input Bandwidth: 2.5 MHz (V_{IN} = 100 mV p-p)**
- **Low Power: 80 mW (typ)**
- **DACs Matched to ±0.5% (typ)**
- **Midscale Preset, All DAC Outputs are Zero Volts**
- **Latch-Up Free**
- **Greater than 2000 V ESD Protection**
- **5 MHz Version: MP7670**

APPLICATIONS

- **Analog Multiplier Replacement**
- **High-Frequency Gain Control using DACs**
- **Convergence Adjustment for Displays and Monitors**
- **Potentiometer Adjustment Replacement**

4

GENERAL DESCRIPTION

The MP8840 is an 8-channel, 4 quadrant multiplying, 8-bit accurate digital-to-analog converter with a 2.5 MHz input bandwidth. It includes an output drive amplifier per channel capable of driving a ±5 mA minimum to a load. DNL of ±1/4 LSB (typ) is achieved with a channel-to-channel matching of better than 0.5% (typ). Stability, matching, and precision of the DACs are achieved by using EXAR's thin film technology.

The MP8840 is ideal for direct gain control of high frequency analog signals. The bipolar output amplifier has low noise which produces a very sharp signal output particularly in display and monitor applications.

A proprietary subranging architecture provides wide signal bandwidth from V_{IN} to output up to 2.5 MHz (typ), fast output settling time, and V_{IN} feedthrough isolation of –60dB (typ).

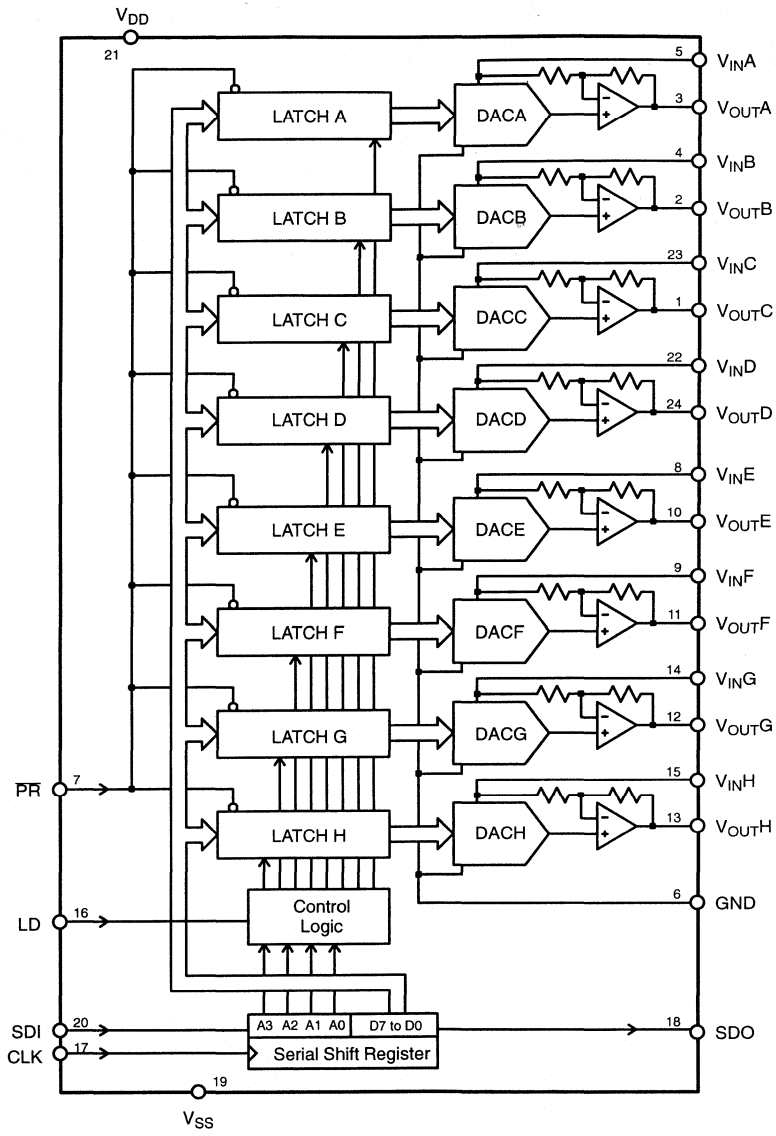
The MP8840 has a serial data 3-wire standard μ-processor logic interface to reduce pin count, package size, and board wire (space).

The MP8840 is fabricated on a junction isolated, high speed BiCMOS1™ process with thin film resistors.

ORDERING INFORMATION

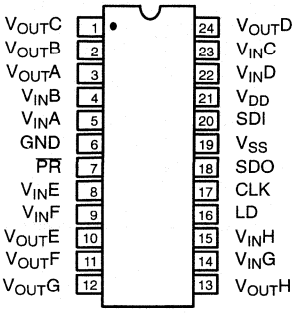
Package Type	Temperature Range	Part No.
Plastic Dip	–40 to +85°C	MP8840AN
SOIC	–40 to +85°C	MP8840AS

SIMPLIFIED BLOCK DIAGRAM

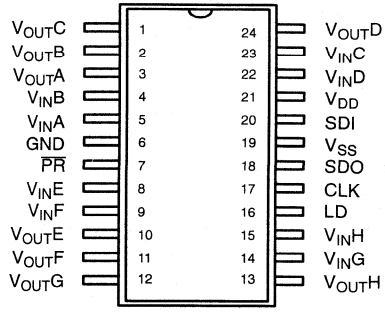


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

4

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output

PIN NO.	NAME	DESCRIPTION
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input
17	CLK	Serial Clock Input
18	SDO	Serial Data Output
19	V_{SS}	Negative Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{SS} = –5 V, GND = 0 V, $V_{IN}X$ =3 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DC CHARACTERISTICS								
Resolution (All Grades)	N	8			8		Bits	
Differential Non-Linearity	DNL		±1/4	±1		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Monotonicity			Guaranteed					
DAC OUTPUT								
Output Offset	V_{BZE}		3	25			mV	$\overline{PR}$ = 0, Sets Code = 80_H
Voltage Range	OVR	–3		3	–3	3	V	
Output Current	I_{OUT}	±5	±10		±5		mA	ΔV_{OUT} <1 LSB
Capacitive Load	CL			200		200	pF	No oscillations
REFERENCE INPUTS								
Input Resistance of one DAC	R_{IN}	5			5		KΩ	R_{IN} (typ) = 15KΩ//Rx Rx = 20KΩ/(1-Code/256)
Input Capacitance[2]	C_{IN}		19	30			pF	
Voltage Range[1]	IVR	–3		3	–3	3	V	
DYNAMIC CHARACTERISTICS[2]								
Input to Output Bandwidth	BW	1	2.5				MHz	Code = FS, $V_{IN}X$ = 100 mV p-p
Slew Rate	SR	1.3	4.0				V/µs	Measured 10% to 90%, $\Delta V_{OUT}X$ = ±6 V
V_{IN} Feedthrough	F_{DT}		–60				dB	Code = HS, up to f = 100 kHz
Total Harmonic Distortion	T_{HD}		0.02				%	$V_{IN}X$ = 4 V p-p, Code = FS f = 1 kHz, f_{LP} = 80 kHz
Spot Noise Voltage	e_N		0.17				µV/√Hz	f = 1 kHz
Output Settling Time	t_S		3.5	6.0			µs	+1 LSB, Code = 0 to FS
Channel-to-Channel Crosstalk	C_T	60					dB	Measured between adjacent channels, f = 100 kHz
Digital Feedthrough	Q		6				nVs	$V_{IN}X$ = 0 V, Code = 0 to FS
DIGITAL INPUTS								
Logic High[3]	V_{IH}	2.4			2.4		V	
Logic Low[3]	V_{IL}			0.8		0.8	V	
Input Current	I_L			±1		±1	µA	
Input Capacitance[2]	C_L			8		8	pF	
DIGITAL OUTPUTS								
Logic High	V_{OH}	3.5			3.5			I_{OH} = –0.4 mA
Logic Low	V_{OL}			0.4		0.4		I_{OL} = 1.6 mA
POWER SUPPLIES								
Power Supply Range	V_{DD}	4.5		5.5	4.5	5.5	V	
	V_{SS}	–5.5		–4.5	–5.5	–4.5	V	
Power Supply Rejection Ratio								
Positive	PSRR+		0.0002	0.01			%/%	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%
Negative	PSRR–		0.0002	0.01			%/%	$\overline{PR}$ = 0 V, ΔV_{SS} = ±5%

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
POWER SUPPLIES (CONT'D)								
Power Dissipation	P_{DISS}		80	150			mW	$\overline{PR}$ = 0 V
Power Supply Current	I_{DD}		8	15			mA	$\overline{PR}$ = 0 V
Negative Supply Current	I_{SS}		8	15			mA	PR = 0 V
DIGITAL TIMING SPECIFICATIONS[2, 4]								
Input Clock Pulse Width	t_{CH}, t_{CL}	80					ns	
Data Setup Time	t_{DS}	40					ns	
Data Hold Time	t_{DH}	20					ns	
CLK to SDO Propagation Delay	t_{PD}			120			ns	
Load Pulse Width	t_{LD}	70					ns	
Preset Pulse Width	t_{PR}	50					ns	
Clock Edge to Load	t_{CKLD}	30					ns	
Load Edge to Next Clk Edge	t_{LDCK}	60					ns	

NOTES

1 Maximum input voltage is 2 V less than V_{DD}.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 See timing diagram.

4

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +6.5 V
V_{SS} to GND ..... –6.5 V
V_{INA-H} to GND ..... V_{DD} to V_{SS}
V_{OUTA-H} to GND ..... V_{DD} to V_{SS}
Digital Input & Output Voltage to GND . –0.5 to V_{DD} +0.5 V
Operating Temperature Range
Extended Industrial ..... –40°C to +85°C

Maximum Junction Temperature ..... –65°C to +150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

THEORY OF OPERATION

The MP8840 contains 8 independent 4-quadrant multiplying D/A converters with output amplifiers. The design has incorporated a novel approach that provides fast, accurate, low noise, low distortion, small size, and low power in the same device. This device is particularly useful in applications where multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Also note that typical multipliers tend to increase noise particularly for low gain settings and have high offsets. The MP8840 design delivers a very low, constant noise, and low offset with digital control through the entire gain range of the D/A converter.

Linearity Characteristics

Each D/A converter in the MP8840 achieves DNL $\leq \pm 0.25$ LSB (typ), and gain error $\leq \pm 0.5\%$ (typ). Since all 8 channels of MP8840 are fabricated in the same IC, the linearity, gain, and input-output characteristics of all 8 channels match extremely well.

The Logic Interface and Serial Port

The MP8840 is equipped with a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire. This interface consists of LD which controls the transfer of data to the selected DAC channels that are fed through the SDI (serial digital data and address bits) with the CLK (digital input shift register clock). Please refer to the following timing diagrams and truth tables for logic details.

A SDO (serial digital data output driver) is connected to the other side of the input shift register and would save SDI bus space by allowing the daisy chaining of several MP8840s (connecting SDI of device 2 to SDO of device 1).

When the LD signal is low, CLK signal loads the digital input bits (SDI) into the 12-bit shift register. The LD signal going high loads this data into the selected DACs. Also, when the $\overline{PR}$ signal is low, the output of all DACs would be reset to 0 volts.

Power Supplies and Input Voltage Ranges

The output and input DC ranges are limited to within ± 2 V from each positive and negative supplies. For example, with supplies at ± 5V, the recommended output range is ± 3V.

The MP8840 design eliminates any code dependent current change into its GND, hence easing the board level design by eliminating the stringent need for other types of DACs for low GND impedance wiring considerations at board level.

Each output of the MP8840 DAC has an output amplifier driver delivering less than 0.05Ω of output impedance through a push-pull linear output stage. Each output and input characteristics parameter match extremely well, given that all channels are fabricated in the same IC.

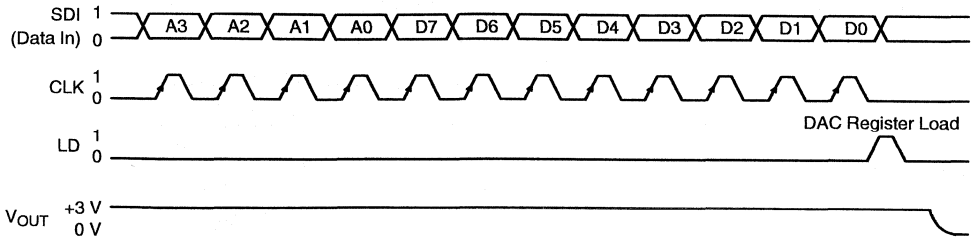


Figure 1. Serial Data Timing and Loading

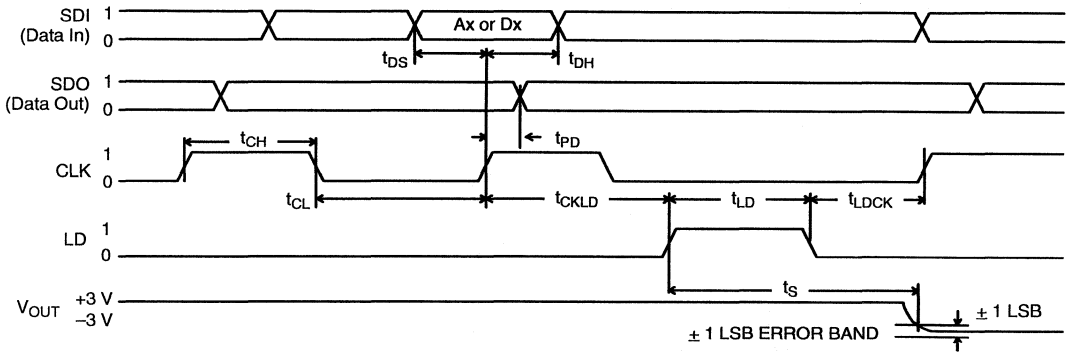


Figure 2. Detail Serial Data Input Timing ($\overline{PR}$ = "1")

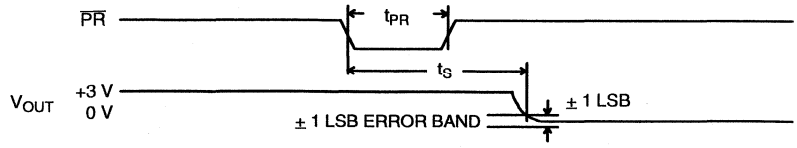
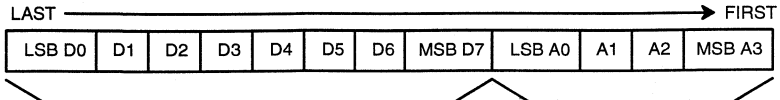


Figure 3. PRESET Operation



Data

Address

MSB A3	A2	A1	LSB A0	DAC Updated
0	0	0	0	No Operation
0	0	0	1	DAC A
0	0	1	0	DAC B
0	0	1	1	DAC C
0	1	0	0	DAC D
0	1	0	1	DAC E
0	1	1	0	DAC F
0	1	1	1	DAC G
1	0	0	0	DAC H
1	0	0	1	No Operation
1	1	1	1	No Operation

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	DAC Output Voltage $V_{OUT} = (D/128 - 1) \times V_{IN}$
0	0	0	0	0	0	0	0	$-V_{IN}$
0	0	0	0	0	0	0	1	$(1/128-1) \times V_{IN}$
0	1	1	1	1	1	1	1	$(127/128-1) \times V_{IN}$
1	0	0	0	0	0	0	0	$(128/128-1) \times V_{IN} = 0$ V, (Preset Value)
1	0	0	0	0	0	0	1	$(129/128-1) \times V_{IN}$
1	1	1	1	1	1	1	0	$(254/128-1) \times V_{IN}$
1	1	1	1	1	1	1	1	$(255/128-1) \times V_{IN} \approx V_{IN}$

Table 1. Serial Input Format

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X	↑	L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

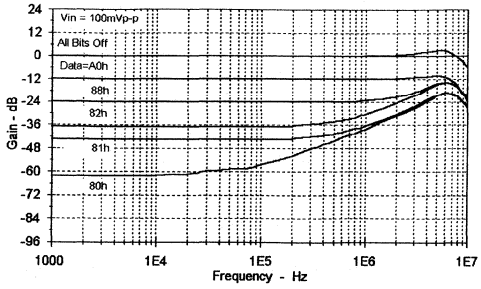
*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

Table 2. Control Logic Truth Table

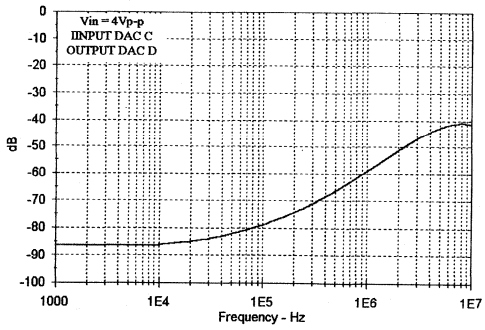
Decimal Input (D)	V_{OUT} (D)	Comments (V_{IN} = 3 V)
0	–3.00 V	Inverted FS
1	–2.98	
127	–0.02	
128	0.00	Zero Output
129	0.02	
254	2.95	
255	2.98	Full Scale (FS)

Table 3. DAC Transfer Function

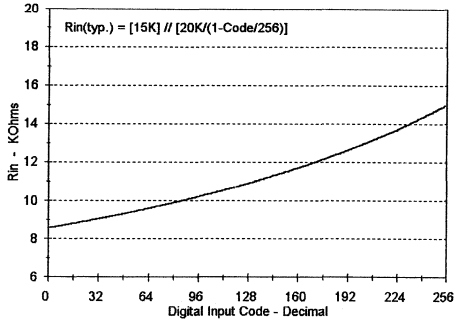
PERFORMANCE CHARACTERISTICS



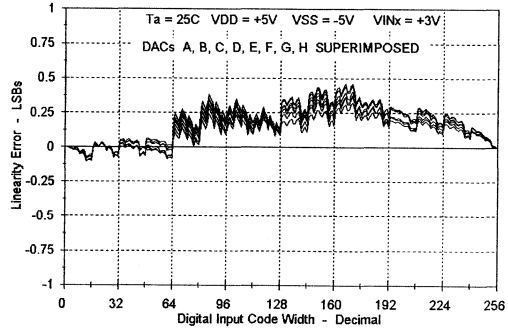
Graph 1. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency



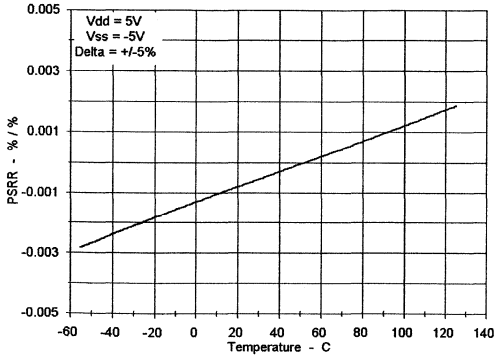
Graph 2. DAC Crosstalk vs. Frequency



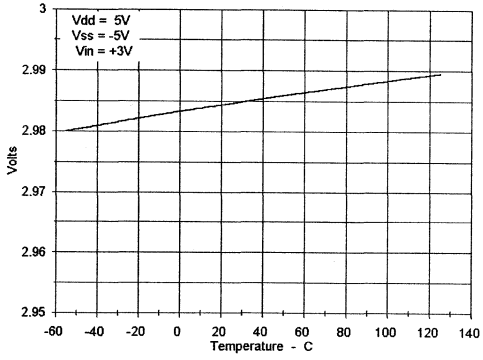
Graph 3. DAC Input Resistance vs. Digital Input Code



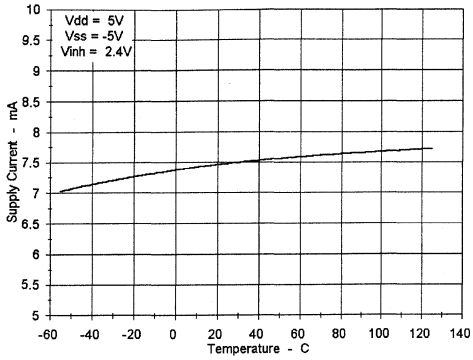
Graph 4. Linearity Error vs. Digital Input Code



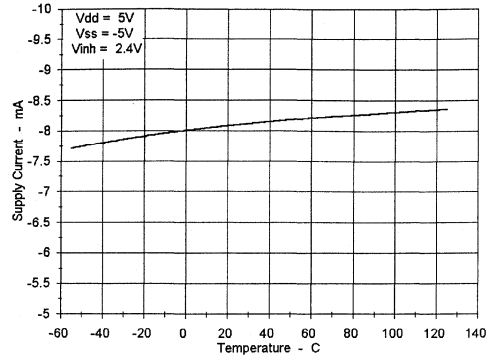
Graph 5. PSRR (DC) vs. Temperature



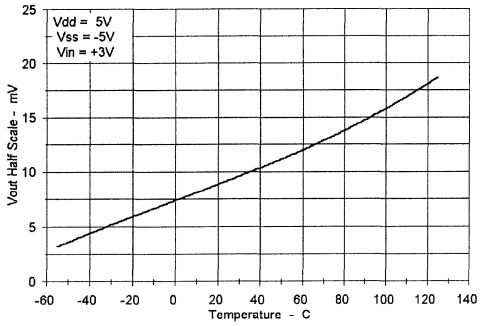
Graph 6. V_{OUT} Full Scale vs. Temperature



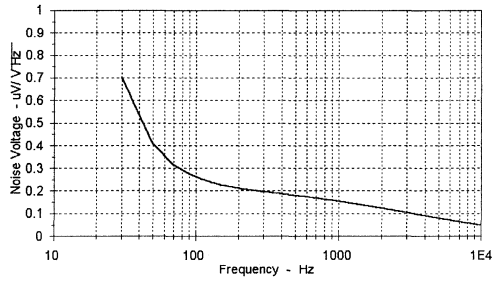
Graph 7. Supply Current (I_{DD}) vs. Temperature



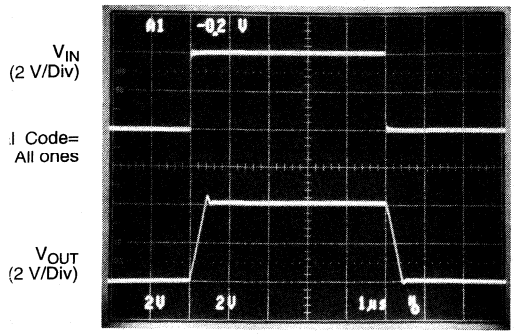
Graph 8. Supply Current (I_{SS}) vs. Temperature



Graph 9. V_{OUT} Offset Error vs. Temperature

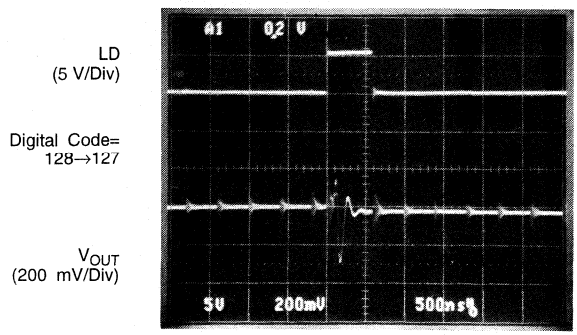


Graph 10. Voltage Noise Density vs. Frequency



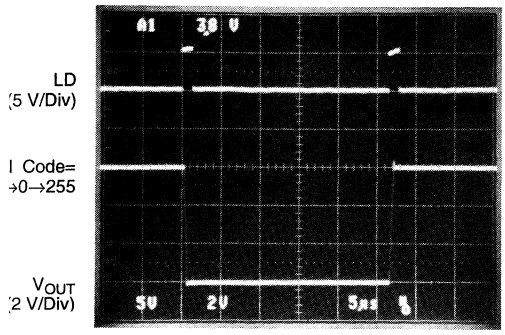
1 µs/Div

Graph 11. Pulse Response



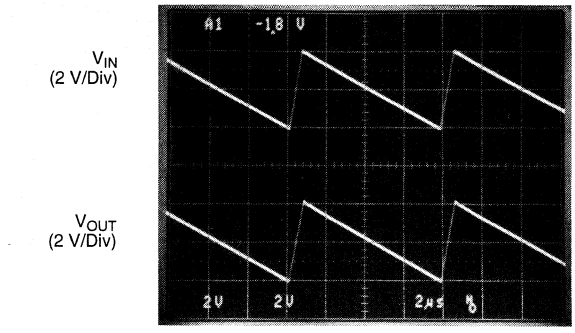
500 ns/Div

Graph 12. 1 LSB Digital Step Change



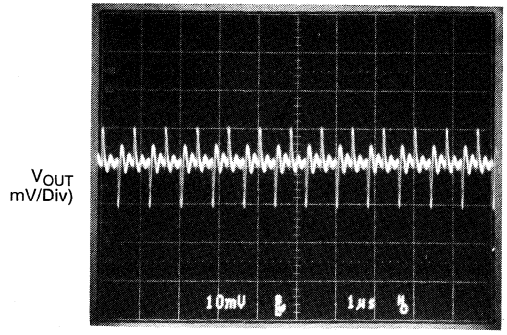
5 µs/Div

Graph 13. Settling Time



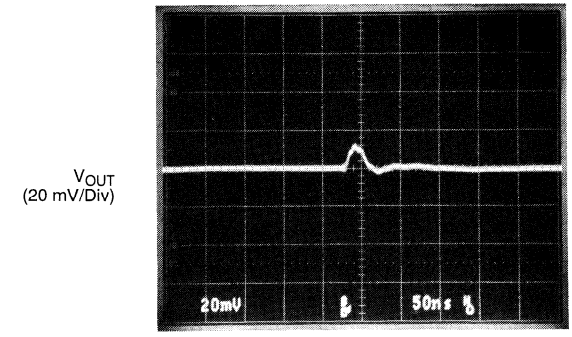
2 µs/Div

Graph 14. 128kHz Sawtooth Waveform Response



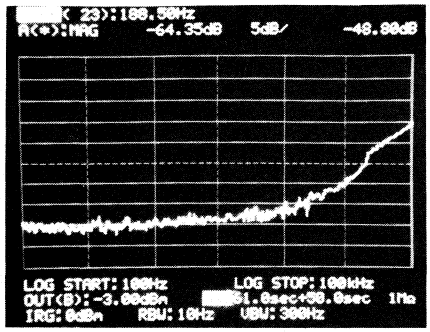
1 µs/Div

Graph 15. Clock Feedthrough



50 ns/Div

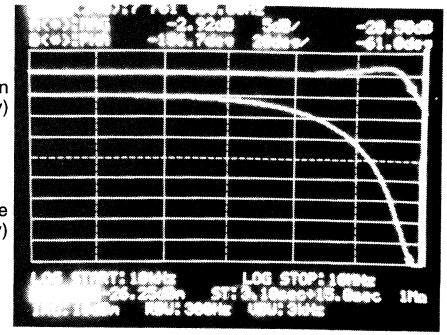
Graph 16. Digital Crosstalk



V_{OUT} (5 dB/Div)

kHz

Graph 17. PSRR vs. Frequency

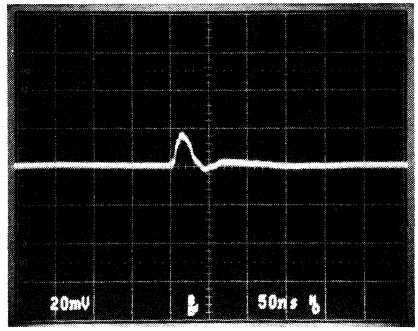


Gain (5 dB/Div)

Phase (20°/Div)

MHz

Graph 18. Gain and Phase vs. Frequency



V_{OUT} (20 mV/Div)

50 ns/Div

Graph 19. Digital Feedthrough

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Section 5

Low Voltage Converters

Listed Alpha-Numerically

EXAR Corporation

Low Voltage Converter Overview

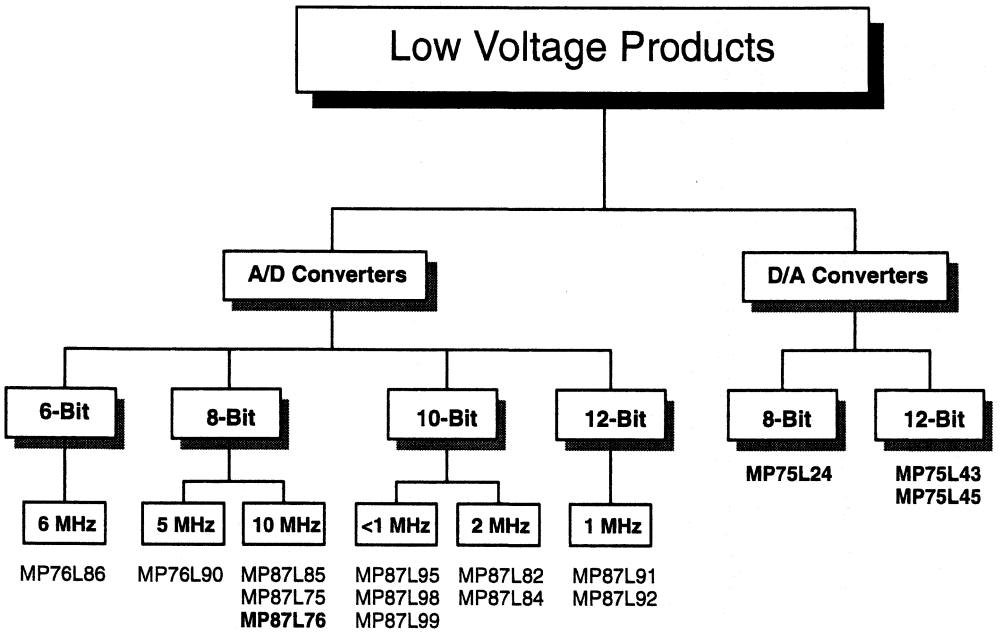
Low Voltage 3.3 V Digital-to-Analog Converters (3.0 to 3.6 V Operation, Tested at 3.0 V. For Performance at 2.7 V, Contact Local Sales Representative)

Part #	*Resolution (Bits)*	*# DACs*	*I or V/ FIX or MUL*	*Buffered or Double Buffered*	*Parallel or Serial*	*Operating Voltage Range*	*Pkg*
MP75L24	8	1	I/M 4Q	B	P	3.0 to 3.6 V	PDIP, SOIC
MP75L43	12	1	I/M 4Q		S	3.0 to 3.6 V	PDIP, SOIC
MP75L45	12	1	I/M 4Q	B	P	3.0 to 3.6 V	PDIP, SOIC, SSOP

Definitions
I = Current Output
M 4Q = Four Quadrant Multiplying

Low Voltage 3.3 V Analog-to-Digital Converters (3.0 to 3.6 V Operation, Tested at 3.0 V. For Performance at 2.7 V, Contact Local Sales Representative)

Part #	*Resolution (Bits)*	*Speed*	*Max Power*	*# Chan.*	*Track/ Hold*	*V_{REF} Range*	*µP Bus*	*Pkg*
MP87L91	12	1 MSPS	50	1	Y	1 to 3 V	12	PDIP, SOIC
MP87L92	12	0.5 MSPS	50	1	Y	1 to 3 V	12	PDIP, SOIC
MP87L82	10	2 MSPS	50	1	Y	1 to 3 V	10	PQFP
MP87L84	10	2 MSPS	50	1	Y	1 to 3 V	10	PDIP, SOIC
MP87L95	10	0.25 MSPS	10	1	Y	1 to 3 V	10	PDIP, SOIC
MP87L98	10	0.25 MSPS	10	4	Y	1 to 3 V	10	PDIP, SOIC, SSOP
MP87L99	10	0.25 MSPS	10	8	Y	1 to 3 V	10	PQFP
MP76L90	8	5 MSPS	45	1	Y	1 to 3 V	8	PDIP, SOIC
MP87L75	8	10 MSPS	35	1	Y	1 to 3 V	8	PDIP, SOIC, SSOP
MP87L85	8	10 MSPS	35	1	Y	1 to 3 V	8	PDIP, SOIC
MP87L76	8	10 MSPS	35	1	Y	1 to 3 V	8	PDIP, SOIC, SSOP
MP76L86	6	6 MSPS	25	1	Y	1 to 3 V	8	PDIP, SOIC



*Preliminary
Bold: New Product

New Product Highlights

Low Voltage Converters

MP75L24
Low Voltage CMOS Serial Input 12-Bit Digital-to-Analog Converter

- 3.3 V Operation
- 12-Bit DAC with Serial Digital Input Interface
- Full 4-Quadrant Multiplication
- Latch-Up Free
- Asynchronous CLEAR Input
- Serial Load On Positive or Negative Strobes
- Small Size and Low Cost

MP75L43
Low Voltage CMOS Serial Input 12-Bit Digital-to-Analog Converter

- 3.3 V Operation
- 12-Bit DAC with Serial Digital Input Interface
- Full 4-Quadrant Multiplication
- Latch-Up Free
- Asynchronous CLEAR Input
- Serial Load On Positive or Negative Strobes
- Small Size and Low Cost

MP87L76
CMOS 15 MSPS, 8-Bit High Speed, Low Power Analog-to-Digital Converter with Power Down

- 3.3 V Operation
- 8-Bit Resolution
- Sampling Rate to 15 MHz
- Low Power: 35 mW typ. (excluding reference)
- Power Down Mode: 100μA (typ)
- DNL = ±1/4 LSB, INL = ±1/2 LSB (typ)
- Rail-to-Rail Input Range
- Latch-Up Free
- ESD Protection: 2000 V Minimum
- 3 State Digital Outputs

MP87L92
12-Bit, 500 kHz Analog-to-Digital Converter

- 3.3 V Operation
- 12-Bit Resolution
- Sampling Rate to 0.75 MHz
- Low Power: 25 mW (typ.)
- Rail-to-rail Input Range
- Latch-Up Free
- ESD Protection: 2000 V Minimum
- Serial Interface

MP75L24

Low Voltage CMOS
Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- 3.3 V Operation
- I_{OUT} Pin Voltages are User Definable
- Improved Isolation of Analog from Digital Ground
- Full Four-Quadrant Multiplication
- On-chip Bus Interface Logic
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Use in Unipolar Supplies
- Extremely Low Power CMOS

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments
- Disk Drives

GENERAL DESCRIPTION

The MP75L24 is a low cost, 8-bit CMOS Digital-to-Analog Converter designed for direct interface to most microprocessors.

The MP75L24 is pin-to-pin compatible to the MP7524A. In addition, the $I_{OUT1,2}$ pins may be taken to a non-ground voltage. This allows its use in single supply circuits.

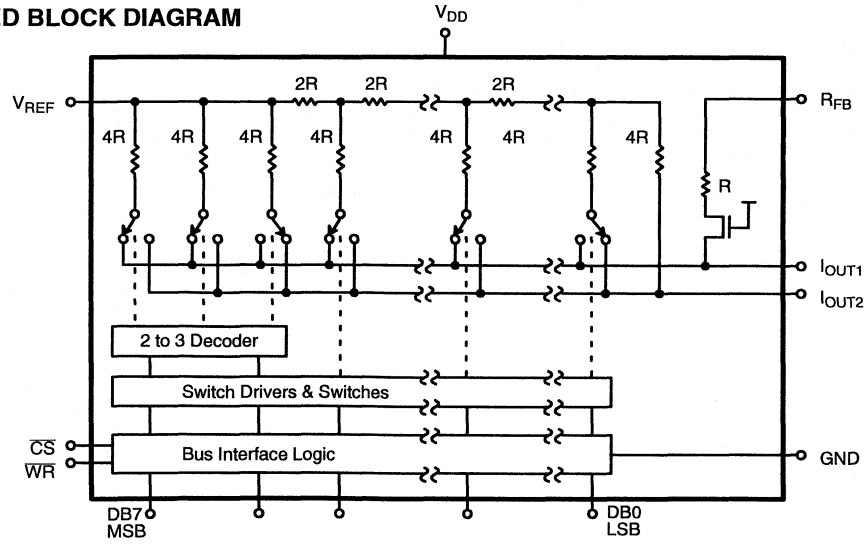
Basically an 8-bit DAC with input latches, the MP75L24's load cycle is similar to the "write" cycle of a random access memory.

Using an advanced thin-film on CMOS fabrication process, the MP75L24 provides accuracy to 1 LSB with power dissipation of only 0.3 mW.

Featuring operation from +3.0 V to +3.6 V, the MP75L24 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the MP75L24 an ideal choice for many microprocessor controlled gain setting and signal control applications.

5

SIMPLIFIED BLOCK DIAGRAM



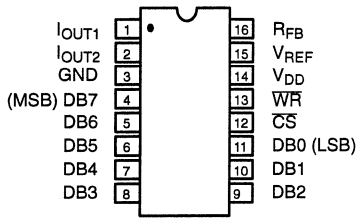
3 Segment D/A Converter with Termination to GND
Logical "1" at Digital Input Steers Current to IOUT1

ORDERING INFORMATION

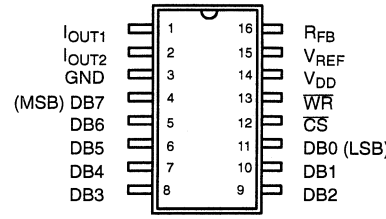
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP75L24AN	±1	±1	±3
SOIC	–40 to +85°C	MP75L24AR	±1	±1	±3

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



16 Pin PDIP (0.300")
N16



16 Pin SOIC (Jedec, 0.150")
SN16

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	DB7	Data Input Bit 7 (MSB)
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	DB3	Data Input Bit 3

PIN NO.	NAME	DESCRIPTION
9	DB2	Data Input Bit 2
10	DB1	Data Input Bit 1
11	DB0	Data Input Bit 0 (LSB)
12	$\overline{CS}$	Chip Select
13	$\overline{WR}$	Write
14	V_{DD}	Power Supply
15	V_{REF}	Reference Input
16	R_{FB}	Feedback Resistance

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 3.3 V, V_{REF} = +3 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]						FSR = Full Scale Range
Resolution (All Grades)	N	8			Bits	
Integral Non-Linearity (Relative Accuracy)	INL				LSB	End Point Linearity
A				±1		
Differential Non-Linearity	DNL				LSB	All grades monotonic over full temperature range.
A				±1		
Gain Error	GE			±3	LSB	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR		±100		ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current	I_{OUT1}			±50nA	nA	Digital Inputs = V_{INL}
DYNAMIC PERFORMANCE						RL = 100Ω, C_L = 10pF
Current Settling Time[2]	t_S		100		ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}[2]	F_T		±1/2		LSB	V_{REF}=100kHz, 20 Vp-p, sinewave
at I_{OUT2}			±1/2		LSB	DB0-DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT						
Input Resistance	R_{IN}	5		20	kΩ	
DIGITAL INPUTS[3]						
Logical "1" Voltage	V_{IH}	+2.0			V	
Logical "0" Voltage	V_{IL}			+0.8	V	
Input Leakage Current	I_{LKG}			±1	µA	
Input Capacitance[2]	C_{IN}			20	pF	V_{IN} = 0 V
ANALOG OUTPUTS[2]						
Output Capacitance						
	C_{OUT1}			70	pF	DAC Inputs all 1's
	C_{OUT1}			30	pF	DAC Inputs all 0's
	C_{OUT2}			20	pF	DAC Inputs all 1's
	C_{OUT2}			60	pF	DAC Inputs all 0's
POWER SUPPLY[5]						
Functional Voltage Range	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}		10	100	µA	All digital inputs = 0 V or all =V_{DD}

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ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]						
Chip Select to Write Set-Up Time	t_{CS}		170		ns	
Chip Select to Write Hold Time	t_{CH}		0		ns	
Data Valid to Write Set-Up Time	t_{DS}		135		ns	
Data Valid to Write Hold Time	t_{DH}		10		ns	
Write Pulse Width	t_{WR}		170		ns	
VOLTAGE MODE OPERATION[2, 6]						
Integral Nonlinearity Error @ V_{REF}	INL			1	LSB	I_{OUT1} = 1.2 V I_{OUT2} = 0 V

NOTES:

1 Full Scale Range (FSR) is 3 V for unipolar mode and ±3 V for bipolar.
2 Guaranteed but not production tested .
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.
6 Refer to *Figure 7.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... –0.5, +5 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... –0.5 to 5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC 700mW
Derates above 75°C ..... 10mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

Refer to Section 8 for Applications Information

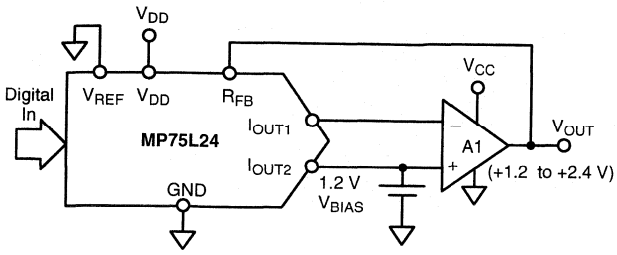


Figure 1. Single Supply Operation with 1.2 V to 2.4 V Swing

The R-2R ladder termination resistor on the MP75L24 is internally connected to I_{OUT2}. This configuration allows the use of the DAC in the single supply current steering mode, where I_{OUT2} is biased above ground level.

Figure 2. shows the generalized configuration.

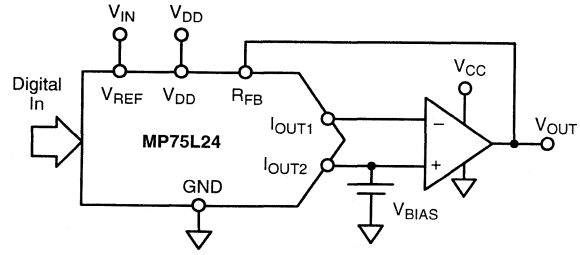


Figure 2. Single Supply Operation in Current Switching Mode

The advantage of this single supply configuration over the voltage switching mode is the greater flexibility with which the output voltage swing can be defined. A low impedance reference bias voltage is needed. Unlike the voltage switching mode which has a minimum output voltage of 0V, the current steering mode allows for output swings that do not have to approach the rail voltages. The equation for this configuration is:

$$V_{OUT} = \frac{D}{256}(V_{BIAS} - V_{IN}) + V_{BIAS}$$

where D=decimal equivalent of the DAC digital input code

V_{BIAS} is a voltage reference: $0\ V \leq V_{BIAS} \leq 1.2V$ for best linearity.

V_{IN} is a bipolar input voltage

By choosing the proper V_{BIAS} and V_{IN}, the output voltage can be set in the range between V_{BIAS} and $2V_{BIAS} - V_{IN}$. For example, for $V_{DD} = 3.3$, select $V_{IN} = 0$ V and $V_{BIAS} = 1.2$ V. This will result in a swing of 1.2 V to 2.4 V.

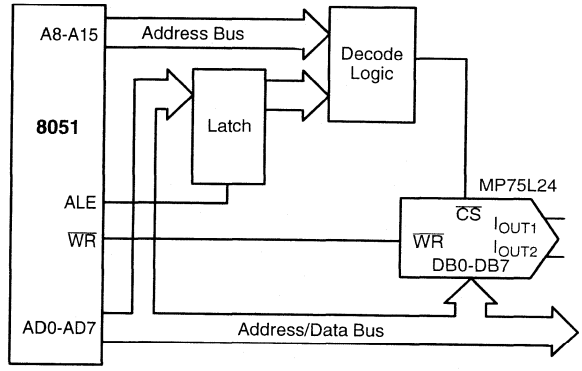


Figure 3. Microcontroller Interface

5

INTERFACE LOGIC INFORMATION

Mode Selection

MP75L24 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the MP75L24 is in the WRITE mode, and the MP75L24 analog circuit responds to data activity at the DB0-DB7 data bus inputs. In this mode, the MP75L24 acts like a non-latched input D/A converter.

Hold Mode

When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the MP75L24 is in the HOLD mode. The MP75L24 analog output holds the value corresponding to the last digital input present at DB0-DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the high state.

$\overline{CS}$	$\overline{WR}$	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0-DB7) inputs
H	X	Hold	Data Bus (DB0-DB7) is locked out
X	H	Hold	DAC holds last data present when $\overline{WR}$ assumed HIGH state

L = LOW state, H = HIGH state, X = Don't care state

Table 1. Mode Selection Table

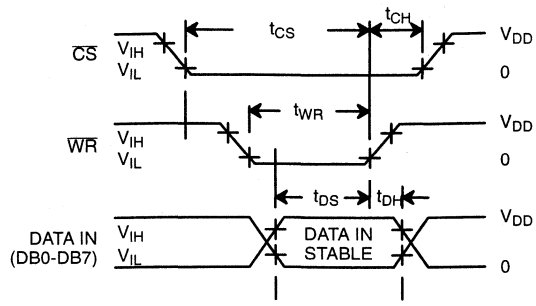


Figure 4. Write Cycle Timing Diagram

MICROPROCESSOR INTERFACE

MP75L24/8080A Interface

Figure 5. shows the MP75L24 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080A CPU, 8224 clock generator and 8228 system controller/bus driver. The MP75L24 $\overline{WR}$ input is connected to the 8228 system data bus outputs. The $\overline{CS}$ input is connected to the system address decoding logic. Note that pull-up resistors R3 and R4 are required to ensure that the $\overline{CS}$ and $\overline{WR}$ input HIGH states reach 3.0V min. Pull-ups are not required on the system data bus since the 8228 VOH is 3.6 V min for DB0-DB7.

System timing is shown in *Figure 6.* Data is loaded into the MP75L24 when the $\overline{WR}$ and $\overline{CS}$ inputs are both LOW. The data is latched into the MP75L24 when $\overline{WR}$ returns HIGH. MP75L24 updating is accomplished by using any of the 8080A memory write instructions.

The MP75L24 can also be addressed and loaded as an isolated Output Device by connecting the MP75L24 $\overline{WR}$ input to the 8228 $\overline{I/O\ W}$ terminal (instead of $\overline{MEMW}$).

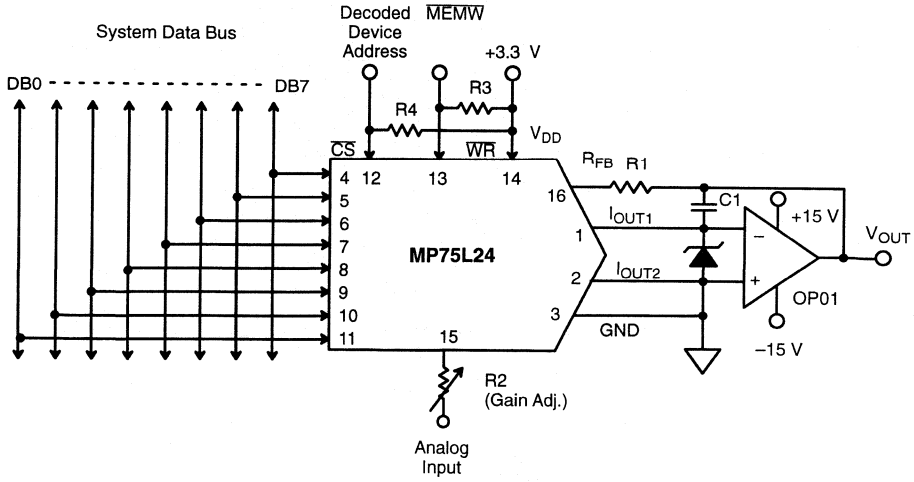


Figure 5. MP75L24/8080A Interface

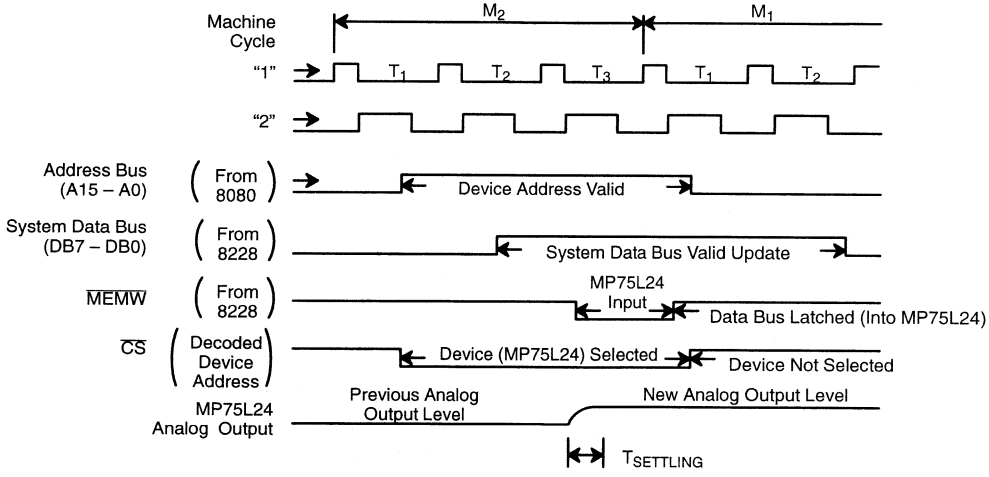


Figure 6. Timing Diagram

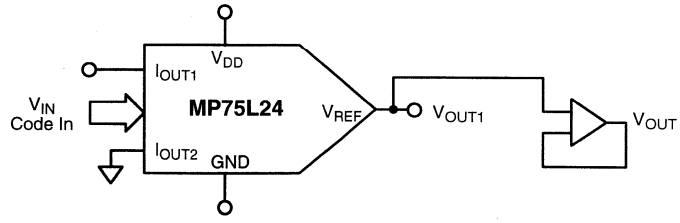
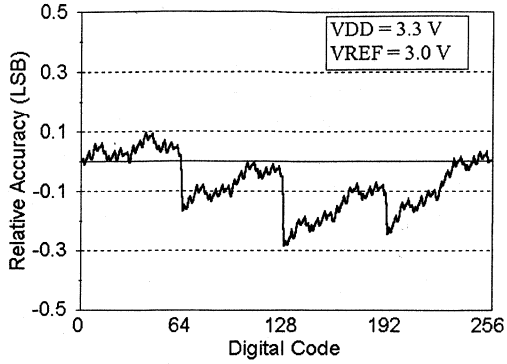


Figure 7. Voltage Mode Operation



Graph 1. Relative Accuracy vs. Digital Code

MP75L43

Low Voltage CMOS
Serial Input 12-Bit
Digital-to-Analog Converter

FEATURES

- 3.3 V Operation
- 12-Bit DAC with Serial Digital Input Interface
- Full 4-Quadrant Multiplication
- Latch-Up Free
- Asynchronous CLEAR Input
- Serial Load On Positive or Negative Strobes
- Small Size
- Low Cost

BENEFITS

- Lower Assembly Costs
- Compatible with Serial Addressing Systems

GENERAL DESCRIPTION

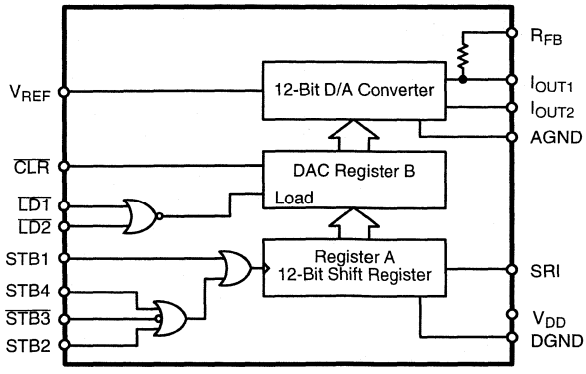
The MP75L43 is a precision, 12-bit CMOS 4-quadrant multiplying Digital-to-Analog Converter designed for serial interface applications.

The MP75L43 consists of two 12-bit registers, control logic and a 12-bit multiplying Digital-to-Analog Converter. The input register (register A) is a 12-bit serial-in parallel-out shift register. Serial data at the SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input, with the MSB loaded first. Register B is a 12-bit parallel-in parallel-out register that follows register A. The contents of register A are loaded into register B under control of the Load inputs.

A CLEAR input is provided for the asynchronous resetting of register B to all 0's.

The MP75L43 is manufactured using an advanced thin film monolithic CMOS fabrication process. A unique decoding technique is utilized yielding excellent accuracy and stability. 12-bit linearity is achieved without laser trimming.

SIMPLIFIED BLOCK DIAGRAM

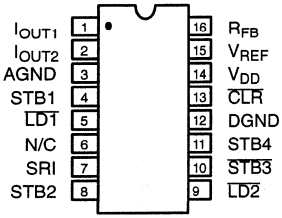


ORDERING INFORMATION

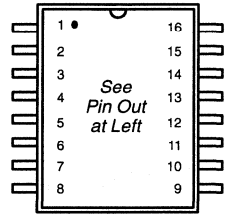
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP75L43JN	1	±1	±10
SOIC	–40 to +85°C	MP75L43JS	1	±1	±10

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



16 Pin PDIP (0.300")
N16



16 Pin SOIC (Jedec, 0.300")
S16

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	DAC current output pin. Normally terminated at op amp virtual ground.
2	I_{OUT2}	DAC current output pin. Normally terminated at AGND.
3	AGND	Analog Ground.
4	STB1	Register A Strobe 1 input, *See Table 1.*
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
6	N/C	No Connection.
7	SRI	Serial Data Input to Register A.
8	STB2	Register A Strobe 2 input, *See Table 1.*

PIN NO.	NAME	DESCRIPTION
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
10	$\overline{STB3}$	Register A Strobe 3 input, *See Table 1.*
11	STB4	Register A Strobe 4 input, *See Table 1.*
12	DGND	Digital Ground.
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000.
14	V_{DD}	Supply Input.
15	V_{REF}	Reference input. Can be positive or negative DC voltage or AC signal.
16	R_{FB}	DAC Feedback Resistor.

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 3 V, V_{REF} = +3 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J				±1		±1		
Differential Non-Linearity	DNL						LSB	Monotonicity: 12 Bits Guaranteed
J				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J				±10		±10		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
J				±10		±10		
DYNAMIC PERFORMANCE								
Current Output Settling Time[2]	t_S		2			2	µs	R_L=100Ω, C_L=13pF Full Scale Output Settles to 1/2 LSB of Final Value
AC Feedthrough at I_{OUT1}[2]	F_T		2.5			2.5	mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	2.5			3.0		V	
Logical "0" Voltage	V_{IL}			0.5		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			260		260	pF	DAC Inputs all 1's
	C_{OUT1}			100		100	pF	DAC Inputs all 0's
	C_{OUT2}			50		50	pF	DAC Inputs all 1's
	C_{OUT2}			210		210	pF	DAC Inputs all 0's
POWER SUPPLY								
Supply Voltage	V_{DD}	3	3.3	3.6			V	
Supply Current	I_{DD}			100			µA	All digital inputs = 0 V or all = 3 V

5

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Serial Input to Strobe Set-up Time	t_{DS1}		50				ns	STB1 used as a strobe
Serial Input to Strobe Set-up Time	t_{DS4}		0				ns	STB4 used as a strobe
Serial Input to Strobe Set-up Time	t_{DS3}		0				ns	$\overline{STB3}$ used as a strobe
Serial Input to Strobe Set-up Time	t_{DS2}		20				ns	STB2 used as a strobe
Serial Input to Strobe Hold Time	t_{DH1}		30				ns	STB1 used as a strobe
Serial Input to Strobe Hold Time	t_{DH4}		80				ns	STB4 used as a strobe
Serial Input to Strobe Hold Time	t_{DH3}		80				ns	$\overline{STB3}$ used as a strobe
Serial Input to Strobe Hold Time	t_{DH2}		60				ns	STB2 used as a strobe
SRI Data Pulse Width	t_{SRI}		80				ns	
STB1 Pulse Width	t_{STB1}		80				ns	
STB4 Pulse Width	t_{STB4}		100				ns	
$\overline{STB3}$ Pulse Width	t_{STB3}		100				ns	
STB2 Pulse Width	t_{STB2}		80				ns	
Load Pulse Width	$t_{LD1, 2}$		150				ns	
Minimum time between strobing Reg. A and loading Reg. B	t_{ASB}		0				ns	
$\overline{CLR}$ pulse width	t_{CLR}		200				ns	

NOTES:

1 Full Scale Range (FSR) is 3 V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +5 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
PDIP, SOIC 700mW
Derates above 75°C ..... 10mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

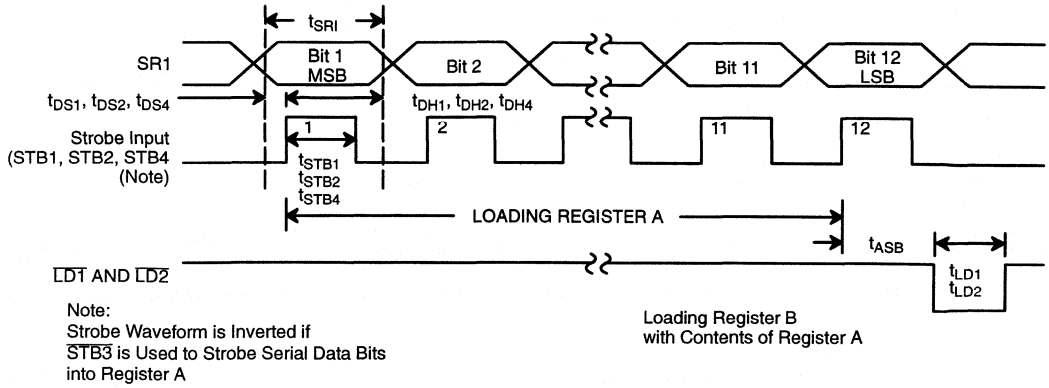


Figure 1. Timing Diagram

MP75L43 Logic Inputs							MP75L43 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	STB3	STB2	STB1	CLR	LD2	LD1		
0	1	0	↑	X	X	X	Data appearing at SRI strobed into Register A	2, 3
0	1	↑	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
0	↓	0	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
↑	1	0	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B to code 0000 0000 0000 (Asynchronous)	1, 3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B with the contents of Register A	3

NOTES
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↑ is positive edge, ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table 1. Truth Table

APPLICATION NOTES

Refer to Section 8 for Applications Information

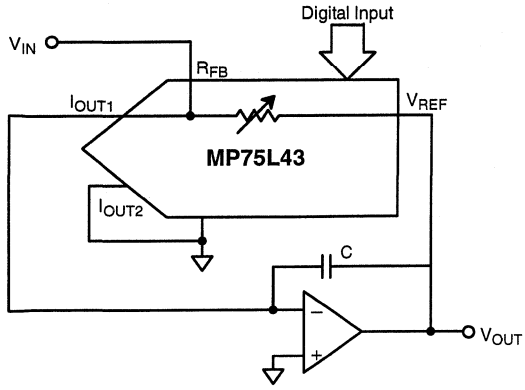
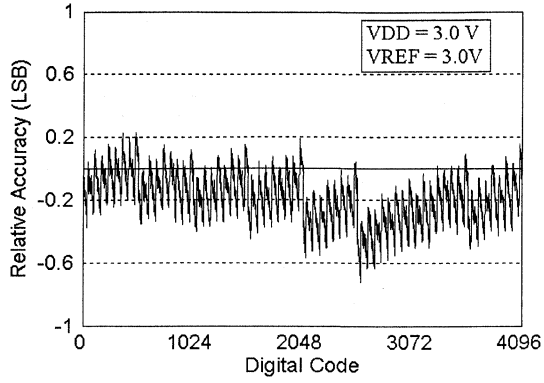


Figure 2. Digitally Programmable Gain Amplifier



Graph 1. Relative Accuracy vs. Digital Code

MP75L45

Low Voltage CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **3.3 V Operation**
- **Full Four Quadrant Multiplication**
- **12-Bit Resolution**
- **Latch-Up Free**
- **Extremely Low Power CMOS: 0.3 mW (typ.)**

APPLICATIONS

- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

GENERAL DESCRIPTION

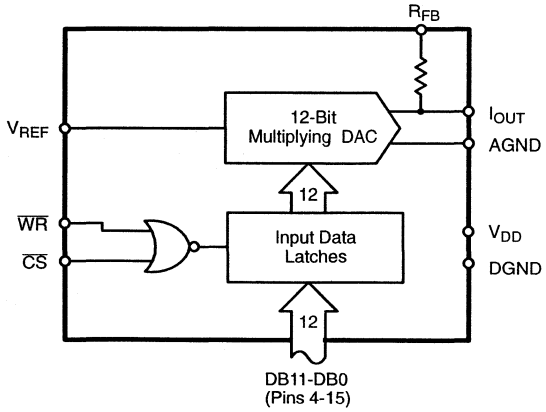
The MP75L45 is a 12-bit CMOS multiplying Digital-to-Analog Converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent, allowing direct unbuffered operation of the DAC.

The MP75L45 is particularly suitable for single supply operation and applications with wide temperature variations.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP75L45 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC), and Shrunk Small (SSOP) outline packages.

5

SIMPLIFIED BLOCK DIAGRAM

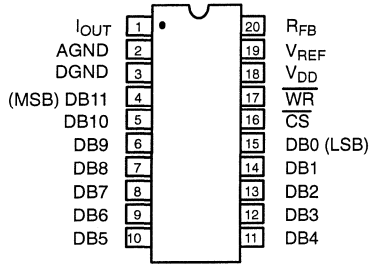


ORDERING INFORMATION

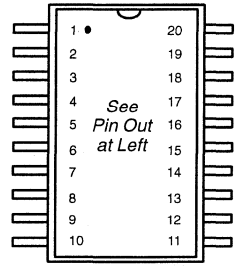
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP75L45KN	1	±1	±10
SOIC	–40 to +85°C	MP75L45KS	1	±1	±10
SSOP	–40 to +85°C	MP75L45KQ	1	±1	±10

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5

PIN NO.	NAME	DESCRIPTION
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	$\overline{WR}$	Write (Active Low)
18	V_{DD}	Digital Supply Voltage
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 3 V, V_{REF} = +3 V unless otherwise noted)

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]						
Resolution (All Grades)	N	12			Bits	
Integral Non-Linearity (Relative Accuracy)	INL			±1	LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
Differential Non-Linearity	DNL			±1	LSB	
Gain Error	GE		±5	±10	LSB	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		10		ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		±50		ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±10	nA	
REFERENCE INPUT						
Input Resistance	R_{IN}	7		25	KΩ	
DIGITAL INPUTS[3]						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
Input Leakage Current	I_{LKG}			±1	µA	
Input Capacitance[2]						
Data	C_{IN}			5	pF	
Control	C_{IN}			20	pF	
POWER SUPPLY[5]						
Functional Voltage Range	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}		10	100	µA	All digital inputs = 0 V or V_{DD}
SWITCHING CHARACTERISTICS[4]						
Chip Select to Write Set-Up Time	t_{CS}		200		ns	
Chip Select to Write Hold Time	t_{CH}		10		ns	
Data Valid to Write Set-Up Time	t_{DS}		100		ns	
Data Valid to Write Hold Time	t_{DH}		10		ns	
Write Pulse Width	t_{WR}		175		ns	

NOTES:

1. Full Scale Range (FSR) is 3 V for unipolar mode.
2. Guaranteed but not production tested.
3. Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4. See timing diagram.
5. Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +5 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC, SSOP 900mW
Derates above 75°C ..... 12mW/°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

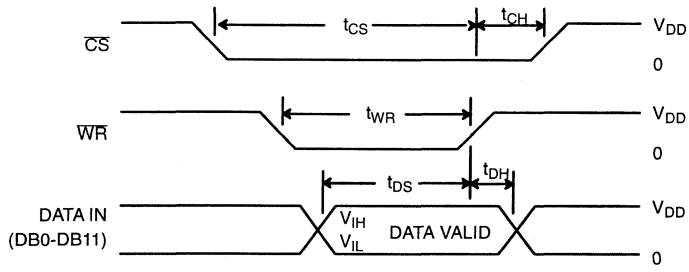
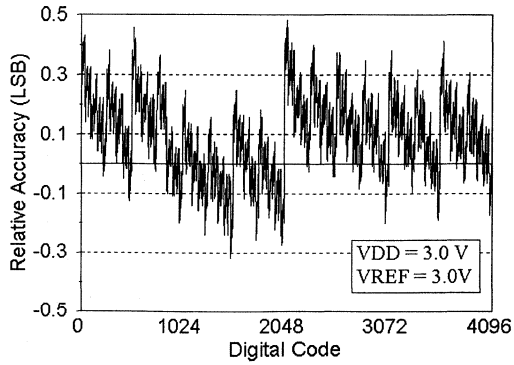


Figure 1. Write Cycle Timing Diagram



Graph 1. Relative Accuracy vs. Digital Code

MP76L86

Low Voltage CMOS
Programmable Input Range 6-Bit
High Speed Analog-to-Digital Converter

FEATURES

- **Single Power Supply (3.3 Volt)**
- **Sampling Rates from 1 kHz to 6.0 MHz**
- **Interface to any Input Range between GND and V_{DD}**
- **Input Op Amp Not Required**
- **Monotonic; No Missing Codes**
- **Low Power CMOS (20 mW)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

- **Reduced Board Space (small package)**
- **Excellent Accuracy Without High System Power**
- **Reduced External Parts, No Sample/Hold Needed**
- **Designer Can Adapt Input Range and Scaling**

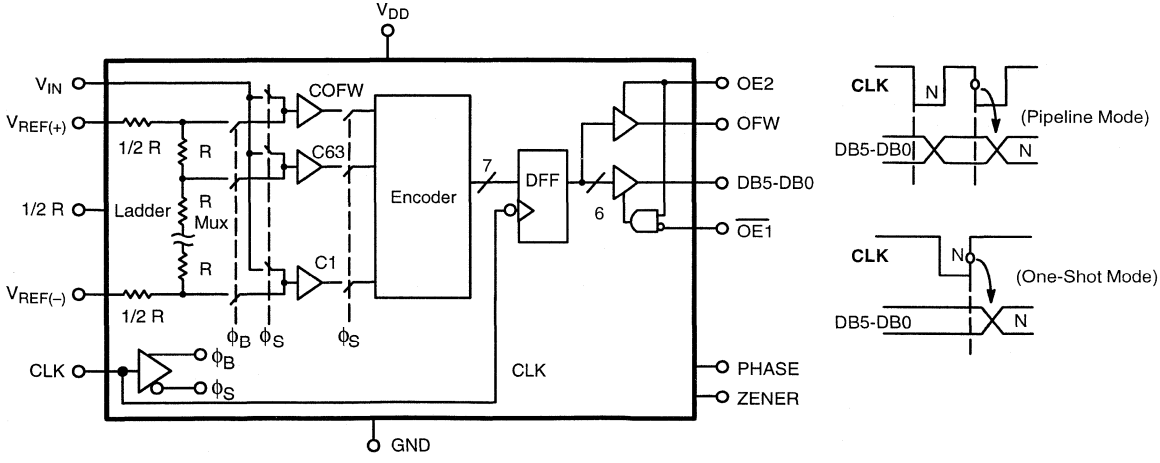
GENERAL DESCRIPTION

The MP76L86 is a 6-bit CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 6.0 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP76L86 allows direct interface to any analog input range between AGND and V_{DD} (of 50 mV to V_{DD}). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP76L86 includes 64 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

5

SIMPLIFIED BLOCK AND TIMING DIAGRAM

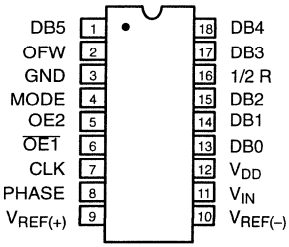


ORDERING INFORMATION

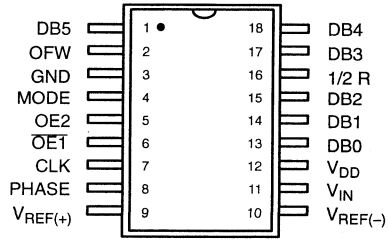
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP76L86AN	±1	1
SOIC	–40 to +85°C	MP76L86AS	±1	1

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin PDIP (0.300")
N18



18 Pin SOIC (Jedec, 0.300")
S18

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB5	Data Output Bit 5 (MSB)
2	OFW	Digital Output Overflow
3	GND	Ground
4	MODE	Mode Select
5	OE2	Output Enable Control (See Truth Table)
6	$\overline{OE1}$	Output Enable Control (See Truth Table)
7	CLK	Clock Input
8	PHASE	Sampling Clock Phase Control
9	$V_{REF(+)}$	Positive Reference Voltage Pin

PIN NO.	NAME	DESCRIPTION
10	$V_{REF(-)}$	Negative Reference Voltage Pin
11	V_{IN}	Analog Input
12	V_{DD}	Power Supply
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1
15	DB2	Data Output Bit 2
16	1/2 R	Center of Reference Ladder
17	DB3	Data Output Bit 3
18	DB4	Data Output Bit 4

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 3 V, F_S = 6.0 MHz (50% Duty Cycle), $V_{REF(+)}$ = 3, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		6			6		Bits	
Sampling Rate	F_S	0.001		6.0	0.001	6.0	MHz	
ACCURACY (A Grades)[1]								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	Best Fit Line (Max INL – Min INL)/2
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$	0.05		3			V	
Negative Ref. Voltage	$V_{REF(-)}$	GND					V	
Differential Ref. Voltage[3]	V_{REF}	50		V_{DD}-GND		V_{DD}-GND	mV	
Ladder Resistance	R_L	180		285	160	320	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance Sample[4]	C_{INA}		20				pF	
Aperture Delay	t_{AP}		25				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		60				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2.5			2.5		V	
Logical "0" Voltage	V_{IL}			0.5		0.5	V	
Leakage Currents[5]								V_{IN}=GND to V_{DD}
CLK	I_{IN}			±100			µA	
DIGITAL OUTPUTS								
Logical "1" Voltage	V_{OH}	2.5			2.5		V	
Logical "0" Voltage	V_{OL}			0.5		0.5	V	
3-state Leakage	I_{OZ}		±1				µA	
POWER SUPPLIES[6]								
Operating Voltage	V_{DD}	3	3.3	3.6		3	V	
Current	I_{DD}			7		10	mA	
AC PARAMETERS[2]								100 mV F_S
Signal Noise Ratio[6]	SNR		32				dB	F_S = 5 MHz, F_{IN} = 100 kHz
DYNAMIC ACCURACY								Histogram Test
Differential Non-Linearity[2]	DNL		0.3				LSB	F_{IN} = 0.1 MHz

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ELECTRICAL CHARACTERISTICS TABLE CONT'D

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width ($V_{REF}/64$) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to V_{DD} and GND. Input(s) $\overline{OET}$ has (have) internal pull down(s). Input(s) OE2 has(have) internal pull up(s). Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

6 SNR: Ratio of RMS signal to RMS noise, up to 1/2 F_S in dB.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND	+5.5 V
$V_{REF(+)}$ & $V_{REF(-)}$	GND –0.5 to V_{DD} +0.5 V
V_{IN}	GND –0.5 to V_{DD} +0.5 V
All Inputs	GND –0.5 to V_{DD} +0.5 V
All Outputs	GND –0.5 to V_{DD} +0.5 V
Storage Temperature	–65 to +150°C
Lead Temperature (Soldering 10 seconds)	+300°C
Package Power Dissipation Rating to 75°C	
PDIP, SOIC	850mW
Derates above 75°C	11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

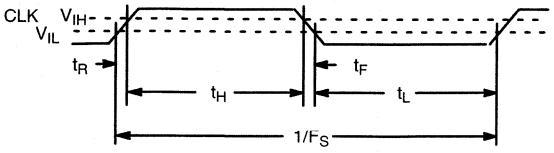


Figure 1. Clock Timing Specification

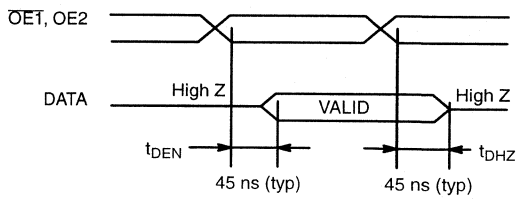


Figure 2. Data Line Enable Delay

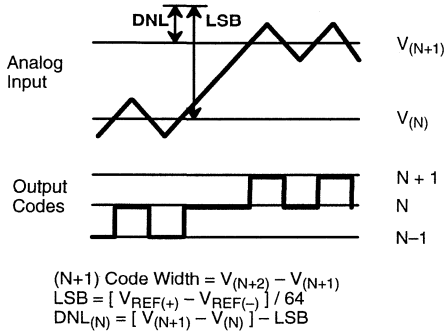


Figure 3. DNL Measurement

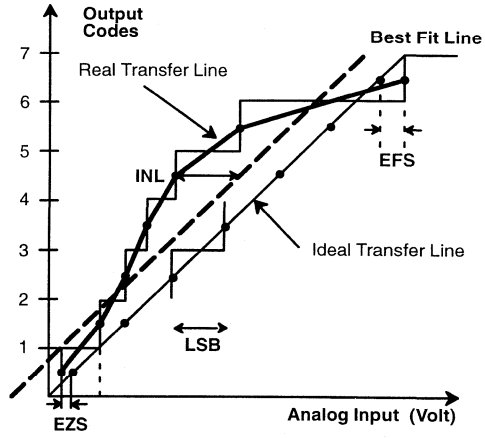


Figure 4. INL Error Calculation

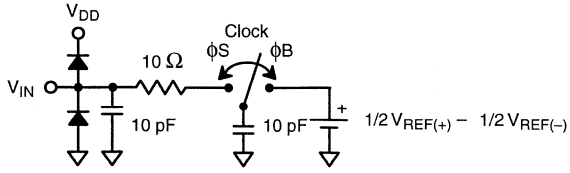


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

The MP76L86 has three operating modes. It has two pipelined modes (MP7682 compatible), and a one shot mode. The voltages applied to the Phase and Mode pins determine the operating mode. *Figures 1, 2, 6 and 7* show the timing specifications. Timing parameters are measured to and from valid logic levels (i.e. t_{DH} is the time from CLK = 0.8 V to DATA = 0.4 or 2.4V).

Pipeline Modes (Mode = High)

In this configuration, the MP76L86 works in a continuous fashion (MP7682 compatible). *Figure 6.* shows the timing with the Phase pin high and low. When Phase is low, "sampling" occurs during the low period of the clock, and "balancing" during the high period. When Phase is high, operation is reversed (see *Figure 7.*), "sampling" occurs during the high period and "balancing" during the low period. The actual time when the internal comparators are connected to V_{IN} is called the Acquisition Time. This time is equal to the sample phase of the external clock delayed by t_{AD} and t_{AP}.

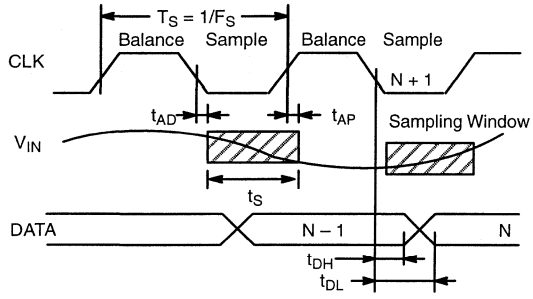


Figure 6. Pipeline Mode Timing (7682 compatible)
(Phase = 0, Mode = 1)

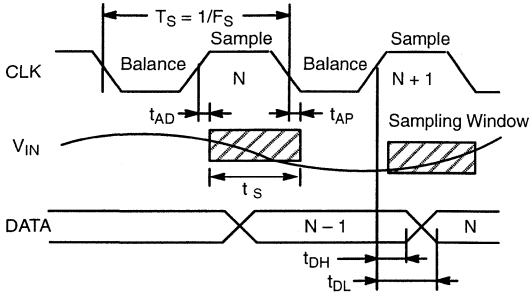


Figure 7. Pipeline Mode Timing (7682 compatible)
(Phase = 1, Mode = 1)

The MP76L86 converts analog voltages into 64 digital codes by encoding the outputs of comparators. A comparator is used to generate the overflow bit. The conversion is synchronous with the sample clock. A complete conversion cycle is accomplished in 1.5 cycles. Data is transferred from the comparator latches to the output register each cycle at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). Phase B connects the comparators to the reference tap points. Phase S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 65 resistors. The first and the last resistors of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = R \bullet 64 \qquad V_{REF} = V_{REF(+)} - V_{REF(-)} = 64 \bullet LSB$

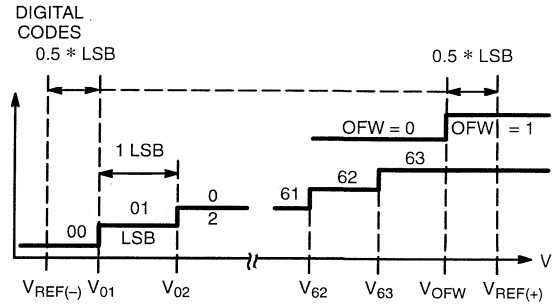


Figure 8. Ideal A/D Transfer Function

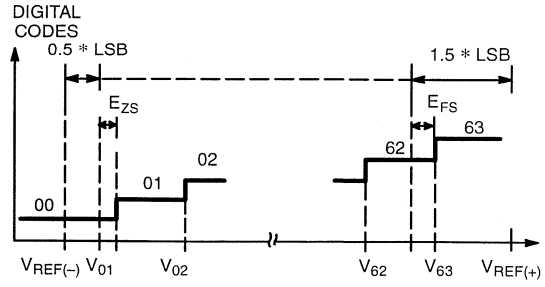


Figure 9. Real A/D Transfer Curve

For MP76L86 the overflow flag is ideally set at

$V_{OFW} = V_{REF(+)} - 0.5 * LSB$

Thus the first and last transition of the data bits take place at

$V_{IN} = V_{01} = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{63} = V_{REF(+)} - 1.5 * LSB$

$LSB = (V_{63} - V_{01}) / 62$

MP76L86 also has zero scale and full scale errors which indicate the deviations from the ideal initial and final transitions, thus

the various error relationships for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and the zero and full scale errors (E_{ZS} and E_{FS}) can be described as follows:

DNL (01) = $V_{02} - V_{01} - LSB$

: : :

DNL (62) = $V_{63} - V_{62} - LSB$

E_{FS} (full scale error) = $V_{63} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

INL (i) = Σ DNL (i)

Systems that adjust the V_{REF} voltages only increase the DNL accuracy at the two extreme points. In the MP76L86, such adjustments have little impact at frequencies lower than 2.5 MHz.

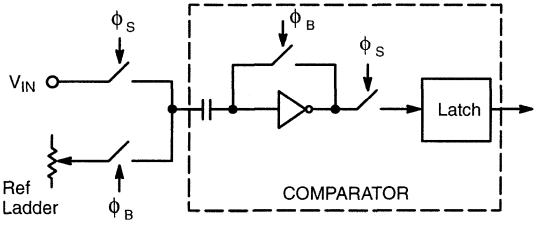


Figure 10. MP76L86 Comparator

The MP76L86 uses the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point and the other to the inverter/comparator trigger point (*Figure 10.*). During the sample phase (ϕ_S) one plate of the capacitor switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AP}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if (dv/dt) * $t_{AJ} \approx V_{REF}/64$, an internal 1 LSB of error results.

The logic encodes the 64 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

$\overline{OE1}$	OE2	OFW	DB5-DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

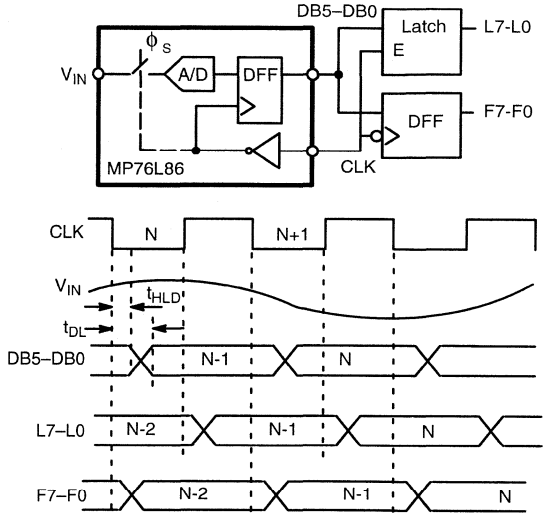


Figure 11. MP76L86 Functional Equivalent Circuit and Interface Timing (Pipeline Mode)

The MP76L86 functional equivalent circuit as shown is to help the designer to correctly design the timing of his system. The MP76L86 is equivalent to an A/D converter followed by a D-type flip-flop (DFF) with the hold and delay times specified in the electrical characteristics.

If another DFF is to follow the ADC, we recommend that the system latches the data at the negative going edge of the clock. If a latch follows the ADC, the positive half of the clock used as enable signal should guarantee stable output at the end of the enable pulse. At high sampling frequencies ($F_S > 2.5$ MHz), the user should verify in his system that the MP76L86 digital outputs do not change when the digital logic is trying to latch the data. If this problem occurs, it may be necessary to invert the logic state

5

of the input PHASE or to change the edge that latches the data into the external circuitry.

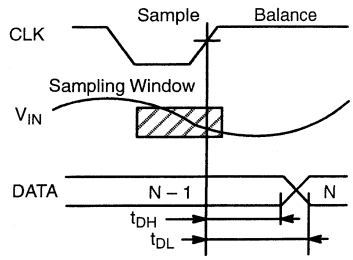


Figure 12. One Shot Mode Timing
(Phase = 0, Mode = 0)

One Shot Mode (Mode = Low, Phase = Low)

While the pipeline mode requires three clock edges (two clock pulses) to accomplish one A/D conversion, the One Shot mode (see *Figure 12.*) requires only two edges (one clock pulse) to complete a conversion.

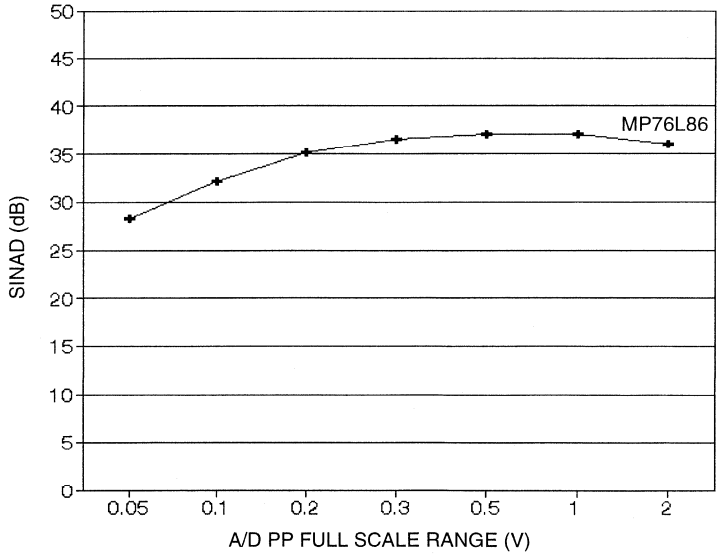
Reserved (Mode = Low, Phase = High)

This mode is not a valid operational mode.

Reference Voltages

If the input bandwidth is limited to the Nyquist region ($F_{IN} < F_S/2$), then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $F_S/2$, then it is recommended that V_{REF} be lower than $V_{DD}/2$.

PERFORMANCE CHARACTERISTICS



Graph 1. 6-Bit Low Level Input Performance
V_{DD} = 3 V, F_S = 5 MHz, F_{IN} = 100kHz

MP76L90

Low Voltage CMOS
Programmable Input Range 8-Bit
High Speed Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 1 kHz to 5 MHz**
- **Interface to any Input Range between GND and V_{DD}**
- **Input Op Amp Not Required**
- **Monotonic; No Missing Codes**
- **Single Power Supply (3.3 V)**
- **Low Power CMOS (45 mW)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

- **Reduced Board Space (small package)**
- **Excellent Accuracy Without High System Power**
- **Reduced External Parts, No Sample/Hold Needed**
- **Designer Can Adapt Input Range and Scaling**

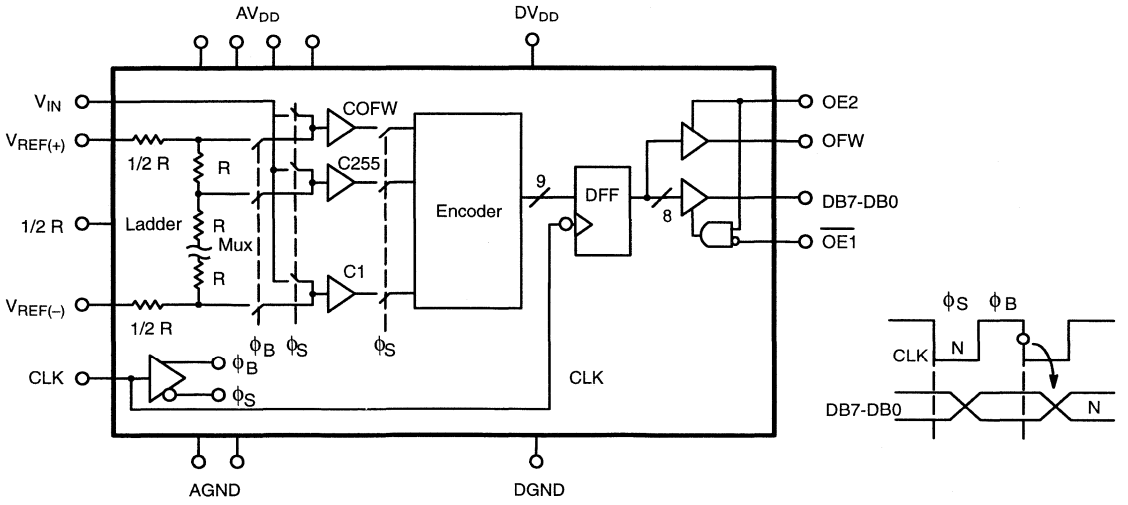
GENERAL DESCRIPTION

The MP76L90 is an 8-bit CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 5 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP76L90 allows direct interface to any analog input range between AGND and AV_{DD} (50 mV to AV_{DD}). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP76L90 includes 256 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

5

SIMPLIFIED BLOCK AND TIMING DIAGRAM

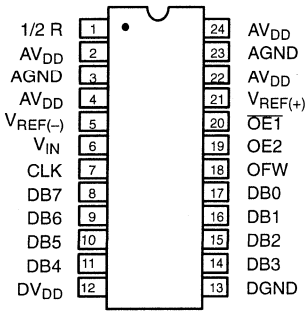


ORDERING INFORMATION

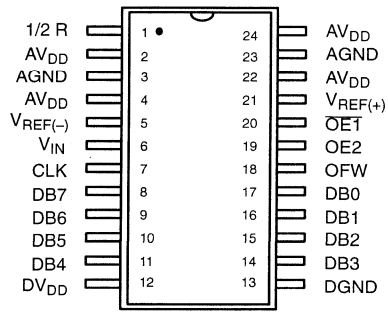
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP76L90AN	±1	1
SOIC	–40 to +85°C	MP76L90AS	±1	1

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	Center of Reference Ladder
2	AV_{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground Return
4	AV_{DD}	Analog Power Supply Voltage
5	$V_{REF(-)}$	Lower Reference Voltage Input
6	V_{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Output Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV_{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground Return
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow flag
19	OE2	Output Enable Control Pin
20	$\overline{OE1}$	Output Enable Control Pin
21	$V_{REF(+)}$	Upper Reference Voltage Input
22	AV_{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground Return
24	AV_{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3$ V, $F_S =$ 5 MHz (50% Duty Cycle), $V_{REF(+)} = 3$, $V_{REF(-)} = AGND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	F_S	0.001		5	0.001	5	MHz	For Specified Accuracy
ACCURACY (A Grades)[1]								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			1		1	LSB	Best Fit Line (Min INL – Max INL)/2
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$	0.05		3			V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND					V	
Differential Ref. Voltage[3]	V_{REF}	50	AV_{DD}-AGND		AV_{DD}-AGND		mV	
Ladder Resistance	R_L	180		285	165	305	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					2000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Capacitance Sample[4]	C_{INA}		50				pF	
Aperture Delay	t_{AP}		25				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		60				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2.5			2.5		V	
Logical "0" Voltage	V_{IL}			0.5		0.5	V	
Leakage Currents[5]								V_{IN}=DGND to DV_{DD}
CLK	I_{IN}	–100		100			µA	
DIGITAL OUTPUTS								
Logical "1" Voltage	V_{OH}	2.5			2.5		V	
Logical "0" Voltage	V_{OL}			0.5		0.5	V	
Tristate Leakage	I_{OZ}			±10		±15	µA	
POWER SUPPLIES[6]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6		3.3	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			15		20	mA	
AC PARAMETERS[2]								
Signal Noise Ratio[7]	SNR		40				dB	
Harmonic Distortion								100 mV F_S
Total Harmonic Distortion[8]	THD		–38				dB	F_S = 5 MHz, F_{IN} = 100 kHz
DYNAMIC ACCURACY								Histogram Test
Differential Non-Linearity[2]	DNL		0.3				LSB	F_{IN} = 0.1 MHz

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ELECTRICAL CHARACTERISTICS TABLE CONT'D

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (VIN). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).
2. Guaranteed. Not tested.
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.
5. All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE1}$ has (have) internal pull down(s). Input(s) OE2 has(have) internal pull up(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
6. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply.
7. SNR: Ratio of RMS signal to RMS noise, up to 1/2 F_S in dB.
8. THD: Ratio of total RMS of harmonics (2nd to 5th) over RMS of signal, in dB.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND	+7 V
$V_{REF(+)}$ & $V_{REF(-)}$	GND –0.5 to V_{DD} +0.5 V
V_{IN}	GND –0.5 to V_{DD} +0.5 V
All Inputs	GND –0.5 to V_{DD} +0.5 V
All Outputs	GND –0.5 to V_{DD} +0.5 V
Storage Temperature	–65 to +150°C
Lead Temperature (Soldering 10 seconds)	+300°C
Package Power Dissipation Rating to 75°C	
PDIP, SOIC	1000mW
Derates above 75°C	13mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

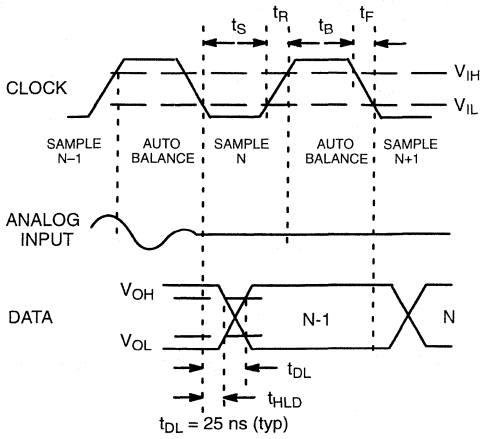


Figure 1. MP76L90 Timing Diagram

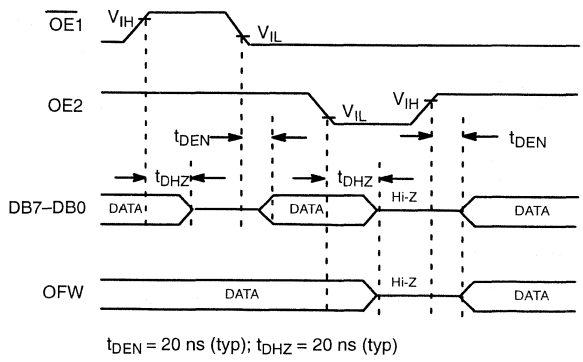
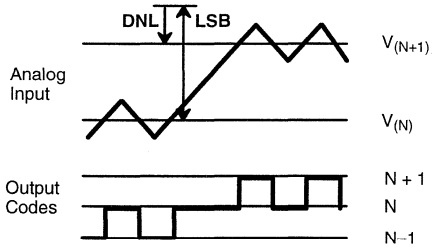


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

DNL(N) = [$V_{(N+1)} - V_{(N)}$] – LSB

Figure 3. DNL Measurement

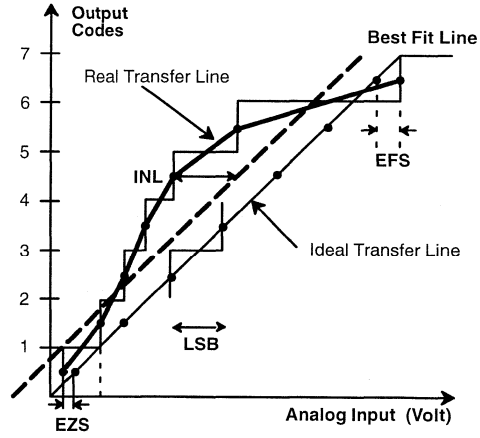


Figure 4. INL Error Calculation

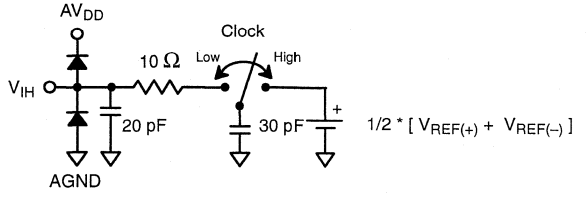


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP76L90 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R \qquad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

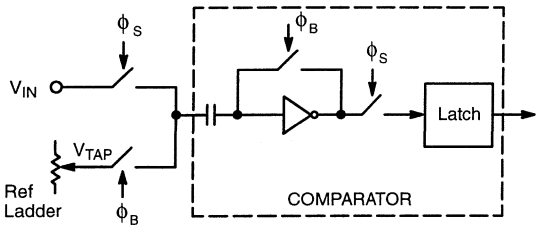


Figure 6. MP76L90 Comparator

The MP76L90 comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitors and forces the inverters into one of the two possible logic states. Latches (connected to the comparators during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The aperture delay may vary from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is if $(dv/dt) * t_{AJ} \approx V_{REF}/256$ an internal error of 1 LSB results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

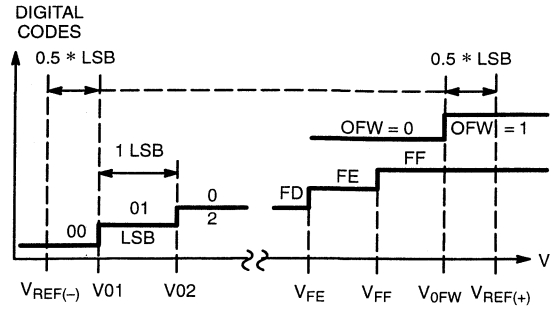


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V01 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = (V_{REF(+)} - V_{REF(-)}) / 256 = (V_{FF} - V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

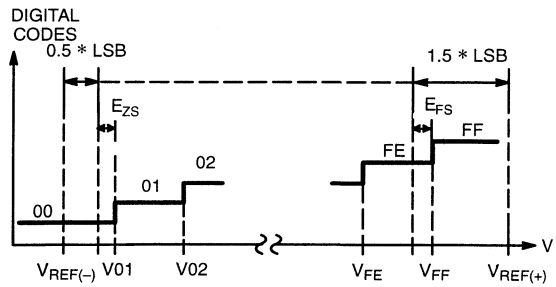


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every $(V_{REF(+)} - V_{REF(-)}) / 256$ volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than or less than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

EZS (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

Figure 8. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP76L90, such adjustments have little impact at frequencies lower than 10 MHz and generally are not required. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

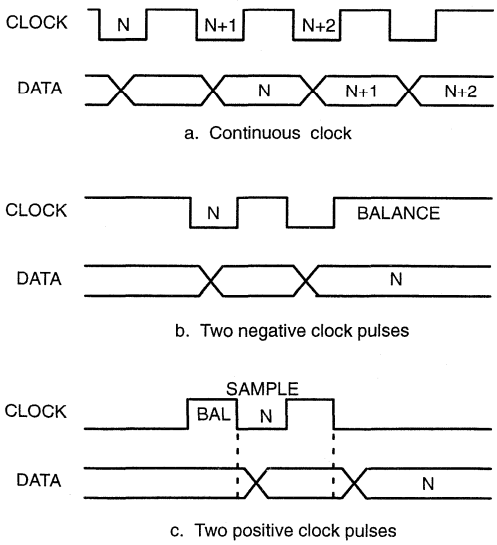


Figure 9. Relationship of Data to Clock

Clock and Conversion Timing

A system will clock the MP76L90 continuously (*Figure 9a*) or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b* keeps the MP76L90 comparators in balance and ready to sample the analog input. This mode draws the most current from AV_{DD}. The timing of *Figure 9c* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP76L90's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

5

Reference Voltages

If the input bandwidth is limited to the Nyquist region (F_{IN}) < (F_S) /2 then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds (F_S) /2, then it is recommended that V_{REF} is lower than $V_{DD}/2$.

At V_{REF} = 1.5 V the LSB is reduced to 6mV. Further reductions show an increased error in terms of LSB (which is getting smaller) even if the error in terms of mV is about constant.

The input/output relationship as a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 256 * (A_{IN}/V_{REF})$$
$$0 \le V_{IN} \le V_{REF} - 1\ LSB,\ DATA = 255\ if\ V_{IN} = V_{REF}$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range**. A system can increase dynamic range by using DAC's to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner), a first digitization would point to the input range in which most of the output codes fall. The system then would adjust the DACs to generate $V_{REF(+)}$ and $V_{REF(-)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution.** Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merging of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

The functional equivalent of the MP76L90 (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An A/D which tracks and converts V_{IN} with no delay.
3) A DFF with specified hold (t_{HLD}) and delay (t_{DL}) times.

$\overline{OE1}$	OE2	OFW	DB7 – DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If an external DFF is to follow the MP76L90, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

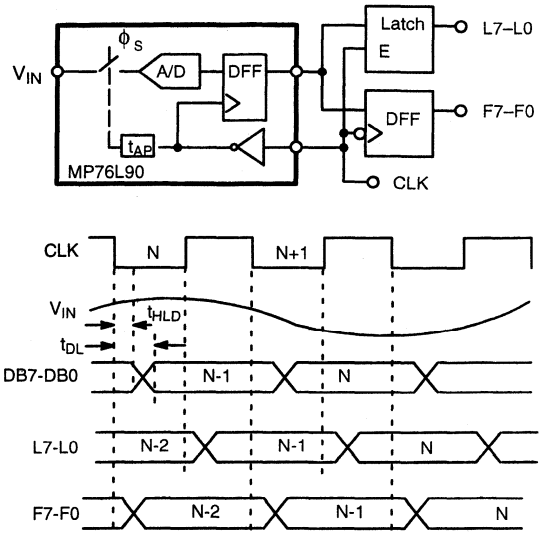
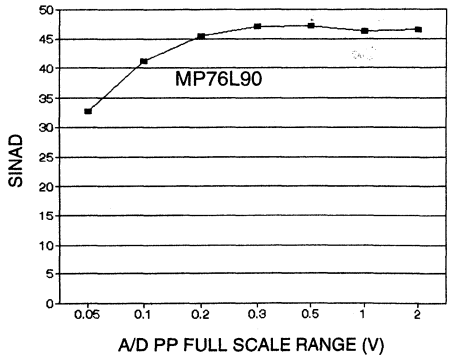


Figure 10. MP76L90 Functional Equivalent Circuit and Interface Timing

PERFORMANCE CHARACTERISTICS



Graph 1. 8-Bit Low Level Input Performance
AV_{DD} = DV_{DD} = 3 V, F_S = 5 MHz, F_{IN} = 100kHz

MP87L75

Low Voltage CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **3.3 Volt Operation**
- **8-Bit Resolution**
- **Small 20 Pin SOIC, PDIP & SSOP Packages**
- **DNL = ±1/2 LSB, INL = ±1 LSB (typ)**
- **Internal S/H Function**
- **V_{IN} DC Range: 0 V to V_{DD}**
- **V_{REF} DC Range: 1 V to V_{DD}**
- **Low Power: 20 mW typ. (excluding reference)**
- **Latch-Up Free**

APPLICATIONS

- **Digital Radio**
- **Cellular Telephones**
- **CCD's and Scanners**
- **Hand Held and Battery Powered Data Acquisition**

GENERAL DESCRIPTION

The MP87L75 is an 8-bit Analog-to-Digital Converter in a small 20 pin SOIC package that operates at 3.3 V. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP87L75 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP87L75.

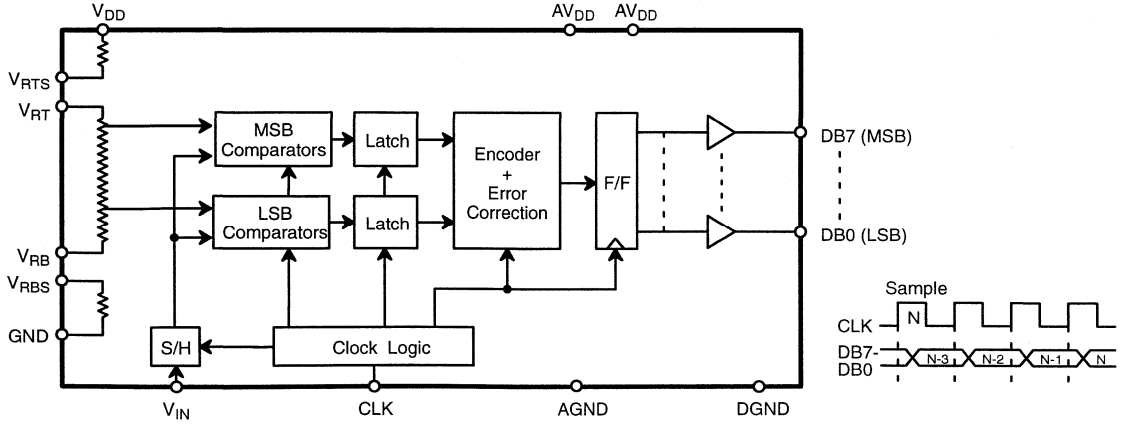
The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.4 V at V_{RB} and 1.72 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +3.3 V supply ±10%. Power consumption is 20 mW at FS = 10 MHz.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP87L75 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC), and Shrunk small outline (SSOP) packages.

5

SIMPLIFIED BLOCK AND TIMING DIAGRAM

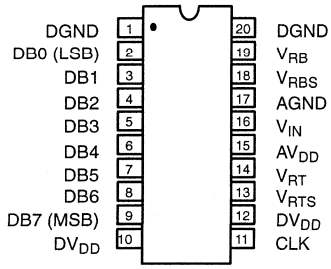


ORDERING INFORMATION

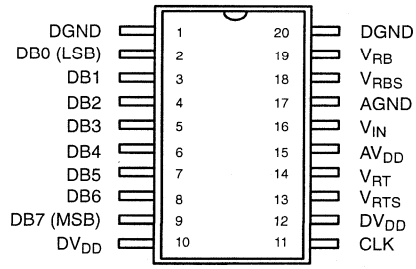
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP87L75AS	±1/2	1 1/2
SSOP	–40 to +85°C	MP87L75AQ	±1/2	1 1/2
PDIP	–40 to +85°C	MP87L75AN	±1/2	1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV_{DD}	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV_{DD}	Digital Power Supply
13	V_{RTS}	Internal Top Ladder Bias
14	V_{RT}	Top Reference
15	AV_{DD}	Analog Power Supply
16	V_{IN}	Analog Input
17	AGND	Analog Ground
18	V_{RBS}	Internal Bottom Ladder Bias
19	V_{RB}	Bottom Reference
20	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3.3 V, FS = 6 MHz (50% Duty Cycle), V_{RT} = 2.5 V, V_{RB} = 0.5 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS			10	MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±1/2	LSB	
Integral Non-Linearity	INL			1 1/2	LSB	Best Fit Line (Min INL – Max INL)/2
REFERENCE VOLTAGES						
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L		350		Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.4		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		1.32		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		1.52		V	
ANALOG INPUT						
Input Bandwidth (–1 dB)[4]	BW		5		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance[5]	C_{IN}		16		pF	
Aperture Delay	t_{AP}		30		ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[7]						
Clock Period	1/FS		100		ns	
High Pulse Width	t_{PWH}		50		ns	
Low Pulse Width	t_{PWL}		50		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	2.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
Data Valid Delay	t_{DL}		30		ns	

5

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current	I_{DD}		6	12	mA	Does not include ref. current

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 2.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 3.*). Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} input equivalent circuit (*Figure 4.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to V_{DD} and GND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

7 t_R, t_F should be limited to >5 ns for best results.

8 AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 5.5 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
SOIC, SSOP, PDIP ..... 700 mW
Derates above 75°C ..... 9mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

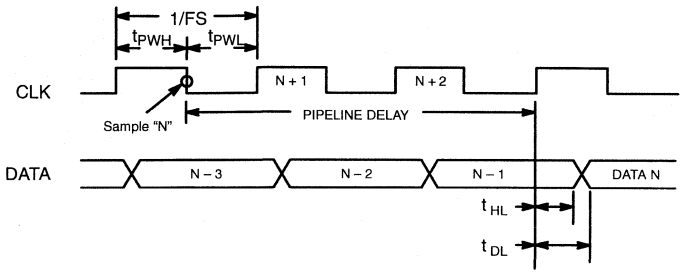
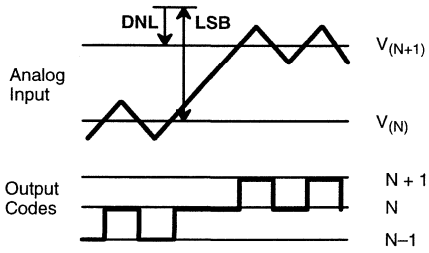


Figure 1. MP87L75 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 256

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 2. DNL Measurement

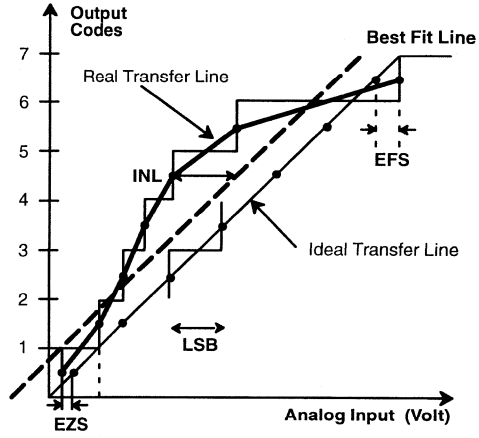


Figure 3. INL Error Calculation

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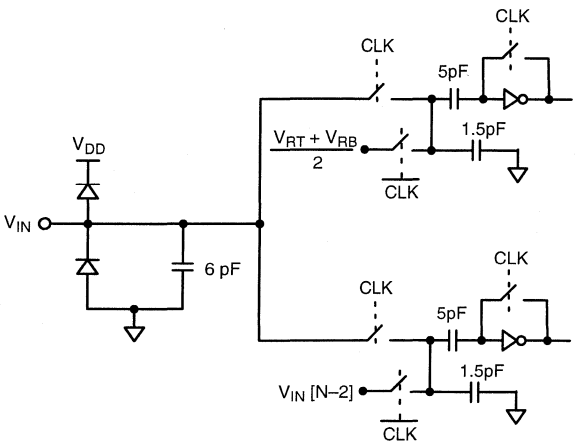


Figure 4. Equivalent Input Circuit

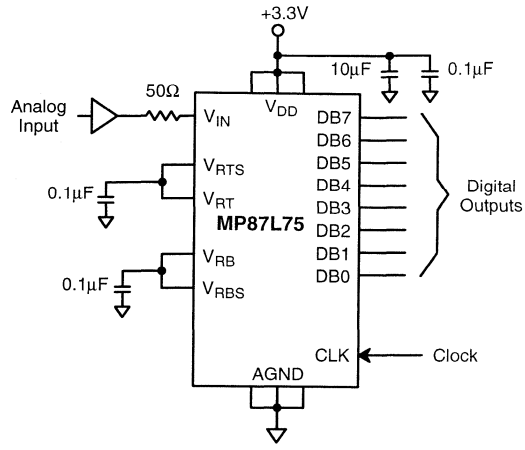


Figure 5. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed AV_{DD} or DV_{DD} +0.5V or go below AV_{DD} or DV_{DD} –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P–substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

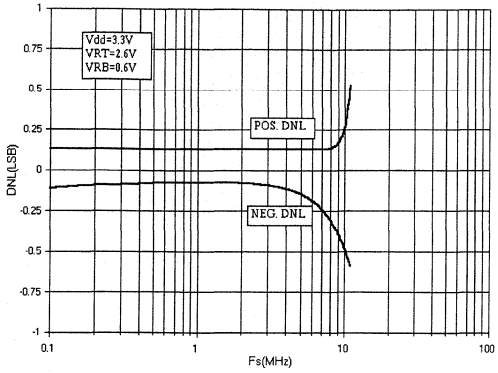
The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

It is possible for the data valid delay (t_{DL}) to be equal to or greater than the high pulse width of the sampling clock (t_{PWH}), See *Figure 1.* This can cause timing related errors. For sample rates above 8 MSPS use only the rising edge of the sample clock (CLK) to latch data from the MP87L75 to other parts of the system.

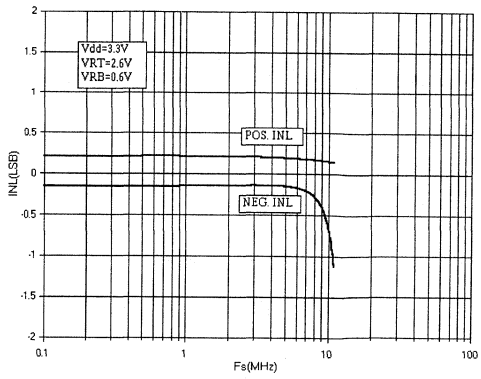
The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.36 V at V_{RB} and 1.56 V at V_{RT} (see *Figure 5.).*

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

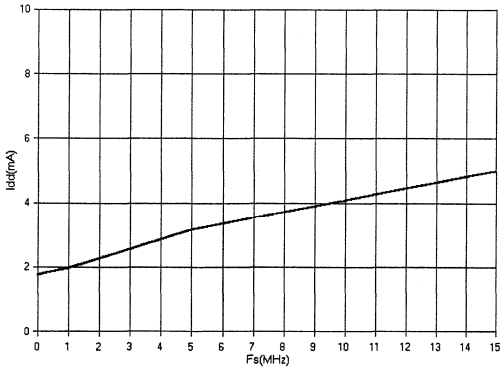
PERFORMANCE CHARACTERISTICS



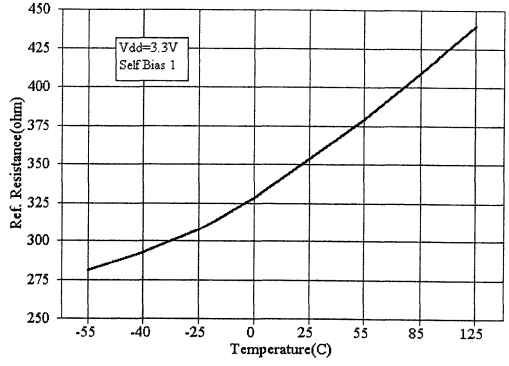
Graph 1. DNL vs. Sampling Frequency



Graph 2. INL vs. Sampling Frequency

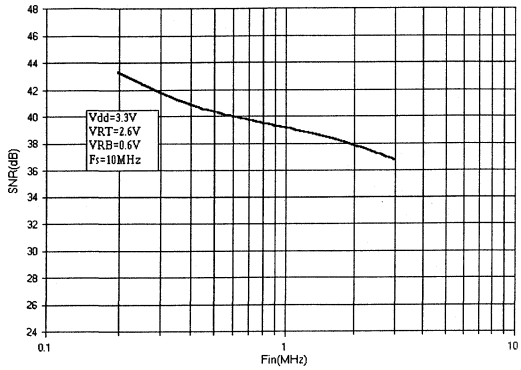


Graph 3. Supply Current vs. Sampling Frequency

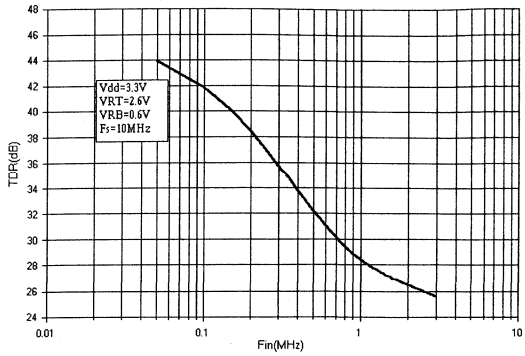


Graph 4. Reference Resistance vs. Temperature

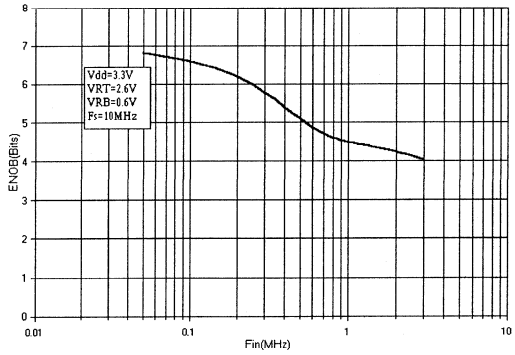
5



Graph 5. SNR vs. Input Frequency



Graph 6. SINAD vs. Input Frequency



Graph 7. ENOB vs. Input Frequency

MP87L76

CMOS
10 MSPS, 8-Bit High Speed, Low Power
Analog-to-Digital Converter with Power Down

FEATURES

- **8-Bit Resolution**
- **Sampling Rate to 15 MHz**
- **Low Power: 35 mW typ. (excluding reference)**
- **Power Down Mode: 100µA (typ)**
- **DNL = ±1/4 LSB, INL = ±1/2 LSB (typ)**
- **Internal S/H Function**
- **Single Supply: 3 V**
- **V_{IN} Range: 0 V to V_{DD}**
- **V_{REF} Range: 1 V to V_{DD}**
- **Latch-Up Tolerant**
- **ESD Protection: 2000 V Minimum**
- **3 State Digital Outputs**
- **20 Pin PDIP, SOIC and SSOP Packages**
- **24 Pin Package Available: MP87L86**
- **Improved Version of MP87L75**

APPLICATIONS

- **Wireless Communications**
- **Digital Cellular Telephones**
- **Telecommunications**
- **CCD's and Scanners**
- **Video Boards**
- **Digital Color Copiers**
- **Battery Powered Devices**

GENERAL DESCRIPTION

The MP87L76 is an 8-bit Analog-to-Digital Converter designed for high speed digitizing applications requiring low power. The MP87L76 offers exceptional performance, flexible input architecture, low power consumption, power down capability, latch-up tolerant operation and is manufactured using an advanced 5 volt CMOS process.

This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP87L76 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP87L76.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.36 V at V_{RB} and 1.56 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 volt supply. Power consumption is 35 mW (typ) at FS = 15 MHz. Power down is accomplished by dropping V_{RT} below 0.55 V.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP87L76 is available in surface mount (SOIC), shrink small outline (SSOP) and plastic dual-in-line (PDIP) packages.

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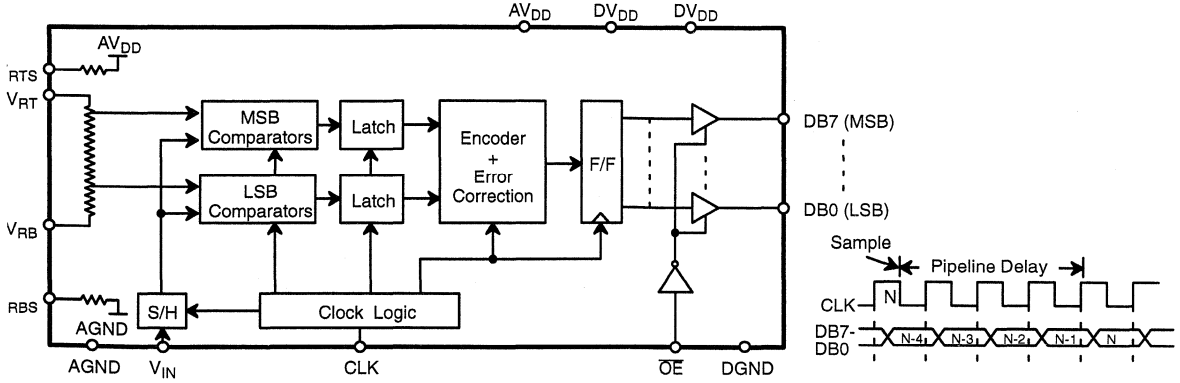
SIMPLIFIED BLOCK AND TIMING DIAGRAM

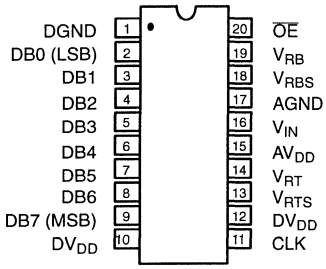


ORDERING INFORMATION

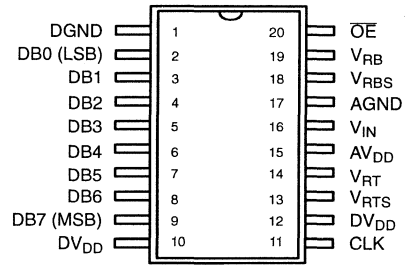
Package Type	Temperature Range	Part No.
SOIC	–40 to +85°C	MP87L76AS
PDIP	–40 to +85°C	MP87L76AN
SSOP	–40 to +85°C	MP87L76AQ

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV_{DD}	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV_{DD}	Digital Power Supply
13	V_{RTS}	Generates 1.56 V if tied to V_{RT}
14	V_{RT}	Top Reference
15	AV_{DD}	Analog Power Supply
16	V_{IN}	Analog Input
17	AGND	Analog Ground
18	V_{RBS}	Generates 0.36 V if tied to V_{RB}
19	V_{RB}	Bottom Reference
20	$\overline{OE}$ or DGND	Output Enable or DGND

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3 V, FS = 10 MHz (50% Duty Cycle), V_{RT} = 1.56 V, V_{RB} = 0.36 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS	0.01		15	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL		±1/4	±1/2	LSB	
Integral Non-Linearity	INL		±1/2	1	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±35		mV	
Full Scale Error	EFS		±35		mV	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		1.56	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.36		V	
Differential Ref. Voltage[3]	V_{REF}	0.75		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	455	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1	V_{RB}		0.36		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
	V_{REF}		1.20		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
Self Bias 2	V_{RT}		1.38		V	V_{RB} = AGND, Short V_{RT} and V_{RTS}
ANALOG INPUT[2]						
Bandwidth (–1 dB)[4]	BW		14		MHz	
Input Voltage Range	V_{IN}	0		AV_{DD}	V	
Input Capacitance Sample[5]	C_{IN}		22		pF	Clock High
Input Capacitance Convert[5]	C_{IN}		7		pF	Clock Low
Aperture Delay	t_{AP}		20		ns	
Aperture Jitter	t_{AJ}		30		ps	
DYNAMIC PERFORMANCE[2]						F_{IN} = 1 MHz
Signal to Noise Ratio	SNR		46		dB	
Signal to Noise plus Distortion	SINAD		42		dB	
Harmonic Distortion	THD		–46		dB	
Effective No. of Bits	ENOB		6.8		Bits	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 6.*)[7]						
Clock Period	1/FS	66.6			ns	For Specified Performance
High Pulse Width	t_{PWH}	33.3			ns	For Specified Performance
Low Pulse Width	t_{PWL}	33.3			ns	For Specified Performance

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ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	V_{DD}–0.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=GND to DV_{DD}
Data Valid Delay[2, 8]	t_{DL}		25	30	ns	
Data Enable Delay[2, 8]	t_{DEN}		27	30	ns	
Data 3-state Delay[2, 8]	t_{DHZ}		13	15	ns	
Pipeline Delay				3.5	clock cycles	Constant relationship between clock and output
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}		3		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		8	12	mA	Does not include ref. current
POWER DOWN						
Power Down Point	VRT_{PD}	0.4	0.55		V	Chip goes to power down mode
Power Up Point				0.9	V	when V_{RT} < 0.55 V
Power Down Current	I_{DDPD}			100	µA	Does not include ref. current
Power Control Delay	PDD			200	ns	V_{RT} @ 0.4→0.9 V

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 10.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 11.*) Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 The bandwidth represents the gain of the ADC and does not imply accuracy

5 See V_{IN} input equivalent circuit (*Figure 2.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to V_{DD} and GND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

7 t_R, t_F should be limited to >5 ns for best results.

8 Depends on the RC load connected to the output pin.

9 AGND and DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted) [1, 2, 3]

V_{DD} to GND ..... 5.5 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP, SSOP ..... 680 mW
Derates above 75°C ..... 9 mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

THEORY OF OPERATION

Analog to Digital Conversion

The MP87L76 uses a two step, sub-ranging architecture to convert analog voltages into 256 digital codes.

A full conversion (sampling V_{IN}, converting MSB & LSB, and performing any error correction) requires 3 1/2 clock cycles to complete (*see Figure 6.*) The pipelined architecture allows the chip to maintain a one conversion per cycle sample rate. Digital logic combines the MSB and LSB data and performs error correction to produce 8-bit output codes.

Internal Reference Bias

The MP87L76 includes two on-chip resistors that can be used to bias the reference ladder without external circuitry. These two resistors are designed to track the reference ladder and are used to create a voltage divider between the supplies (AV_{DD} and AGND).

To use this feature simply connect V_{RT} to V_{RTS} and connect V_{RB} to V_{RBS}. This will nominally generate:

AV_{DD} x (0.3/2.5) at V_{RB}, and

AV_{DD} x (1.3/2.5) at V_{RT}

This will generate 0.36 V at V_{RB} and 1.56 V at V_{RT} (see *Figure 1.)* Bypass capacitors on V_{RT} and V_{RB} are suggested to stabilize the ladder.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

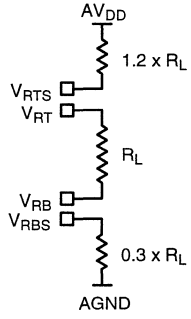


Figure 1. Internal Reference Bias

Transfer Characteristics

The ideal ADC is a linear building block that has infinite bandwidth and no phase distortion. A real ADC, however, exhibits finite bandwidth and non-constant group delay characteristics as well as non-linear behavior due to the non-zero INL characteristic. When modeling the ADC as a linear element and a quantizer, the circuit shown in *Figure 2.* can be used in order to represent the ADC's bandwidth.

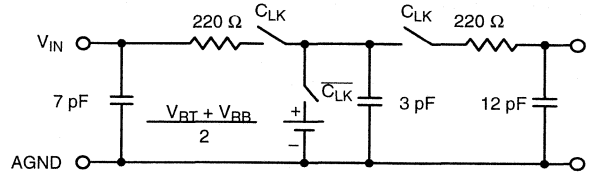


Figure 2. Input Equivalent Circuit

Sample and Hold Timing

The ADC's internal sample and hold tracks the input signal when CLK is high. t_{AP} after the falling clock edge, the analog signal is sampled and held for conversion as seen in *Figure 3.*

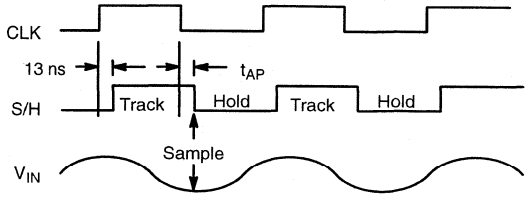


Figure 3. Sample and Hold Timing

Output Enable ($\overline{OE}$)

The $\overline{OE}$ pin controls the state of the digital output drivers. When forced low, the drivers are active. When pulled high the drivers are 3-stated. Please note that the $\overline{OE}$ pin only controls the output drivers; the rest of the chip is still active. Therefore if the clock is running, the internal registers are updated even if the digital outputs are 3-stated (*Figure 4.).*

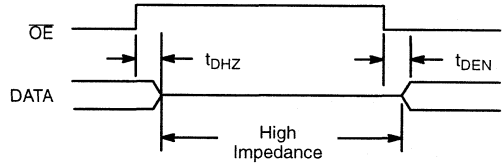


Figure 4. Output Enable/Disable Timing Diagram

Power Down Mode

For systems that are battery powered, the MP87L76 has a power down feature to help extend battery life. When the voltage at the V_{RT} pin drops below 0.43 V, the chip goes into power down mode. In this state, conversions are halted, the outputs are 3-stated and I_{DD} drops to less than 100 µA. Then, when the voltage at the V_{RT} pin rises above 0.8 V, the chip will power up. Note that after power up, four clock cycles are required to get valid data at the digital outputs (see *Figure 6.*) One way to achieve power down is to disconnect or disable the buffer/amp driving V_{RT}, and let the internal reference resistance pull V_{RT} down. Remember, any bypass capacitors at V_{RT} will increase the time for V_{RT} to drop below 0.4 V.

5

APPLICATION NOTES

Power Supplies and Grounding

AV_{DD} and DV_{DD} should be connected to the sample power supply source (*Figure 5.*). The power supply (AV_{DD} and DV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to GND, placed as close to the chip as possible.

AGND and DGND pins are connected internally through the P-substrate. AGND and DGND pins should be connected together as close to the chip as possible.

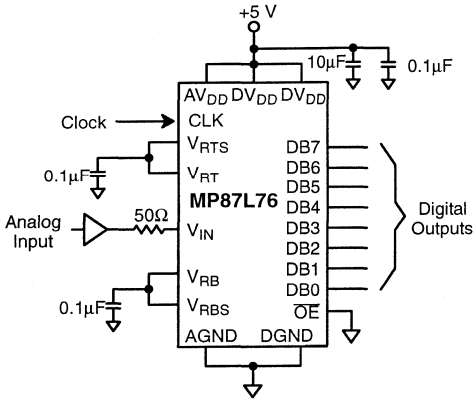


Figure 5. Typical Circuit Connections

The Analog Input

When designing with the MP87L76, the following points can help optimize performance.

1. Driving the analog input – The input impedance can be represented as a switched capacitor type input circuit, ie. the input impedance changes with the phase of the input clock. *Figure 2.* shows an equivalent input circuit. In many applications, the input impedance can be treated as capacitive. For fast signals and a high driving impedance, a wide bandwidth op amp is recommended.
2. It is important to note that op amps have inductive output impedances at high frequencies which is a consequence of the emitter impedance of the typical push-pull output stage. The resulting transient ringing should be damped by inserting a resistor in series with the ADC input – typically about 50Ω. See *Figure 5.* The exact value may be obtained from the op amp manufacturer's data sheet.
3. Signals should not exceed V_{DD} +0.5V or go below GND –0.5V. All pins have internal protection diodes that will protect them from short transients (*See Note 2, Absolute Maximum Ratings*) outside the supply range.

Digital Outputs

Refer to *Figure 6.* for details on the data availability timing. The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion. The output enable pin ($\overline{OE}$) should not be left unconnected. If it is not controlled by an active signal, it must be tied to ground.

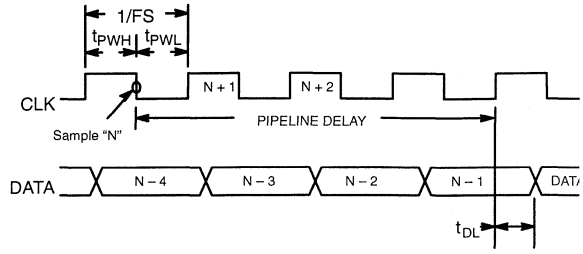


Figure 6. Data Available Timing

Dynamic Reference Control

The MP87L76 allows for dynamically adjusted V_{RT} and V_{RB}. When this is done, V_{RT} and V_{RB} have to be kept static during a certain period.

The A/D conversion is done in a two-step method. During the first clock period, the MSB comparator bank compares the V_{IN} with the reference voltage string in order to determine in which subrange the exact V_{IN} lies. During the subsequent clock period, an LSB comparator bank compares a subrange of the V_{REF} to the V_{IN}. Thus, the reference inputs have to be stable during two compare cycles. This implies that while the ADC is clocked with FS, the conversion only occurs at a rate of FS/2. Every second sample and resulting data must be discarded because the reference changes during its conversion.

The reference inputs V_{RT} and V_{RB} have to have settled to within 1 LSB, at least 50 ns before the rising edge which occurs after the sampling instant. The reference has to be kept constant until (t_{AP} + 10 ns) after the second rising edge. See *Figure 7.* for timing details. The digital data of the N + 1, N +3, N + 5 etc. samples are invalid if the reference is changed every second clock cycle. The data for the N, N + 2, N + 4 etc. samples are valid.

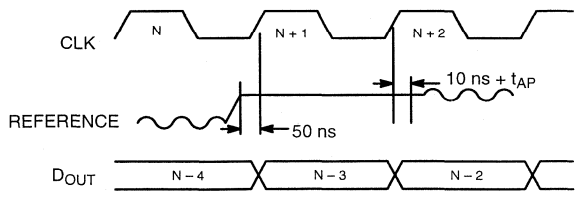


Figure 7. Dynamic Reference Control

LINEARITY DEFINITION

The Ideal ADC

The transfer function for an ideal A/D converter is shown in *Figure 8.*

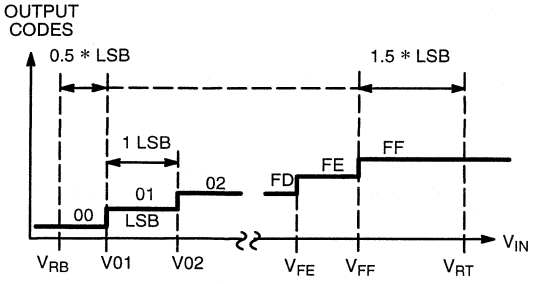


Figure 8. Ideal A/D Transfer Function

The first transition for the data bits takes place when:

$V_{IN} = V01 = V_{RB} + 0.5 * LSB$

The last transition of the data bits takes place when:

$V_{IN} = V_{FF} = V_{RT} - 1.5 * LSB$

where: $LSB = V_{REF} / 256$
$= (V_{FF} - V01) / 254$

and $V_{REF} = (V_{RT} - V_{RB})$

The Real ADC

In a "real" converter, the code-to-code transitions do not fall exactly every $V_{REF}/256$ volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A specification of Max DNL = ± 0.5 LSB means that all codes are within 0.5 LSB and 1.5 LSB. For example, if $V_{REF} = 4.096$ V then 1 LSB = 16mV and every code width is between 8 and 24 mV.

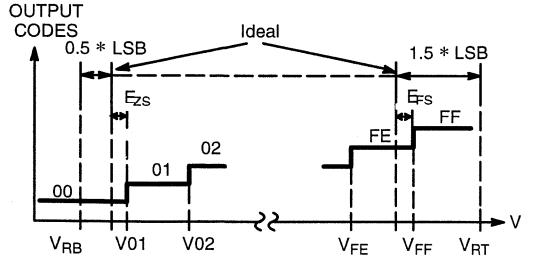


Figure 9. Real A/D Transfer Curve

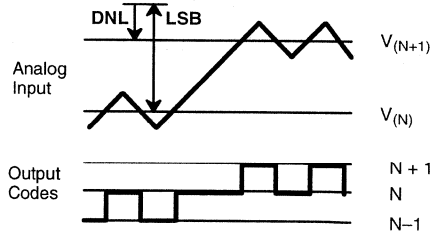


Figure 10. DNL Measurement

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) are:

DNL (01) = V02 – V01 – LSB
: : :
DNL (FE) = $V_{FF} - V_{FE}$ – LSB
Thus $DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$
Code Width (N) = $V_{(N+1)} - V_{(N)}$

Similarly, the zero scale and full scale errors are defined as:

EFS (full scale error) = $V_{FF} - (V_{RT} - 1.5 * LSB)$
EZS (zero scale error) = $V01 - (V_{RB} + 0.5 * LSB)$
where: $LSB = [V_{RT} - V_{RB}] / 256$

Figure 9. shows the zero scale and full scale error terms while *Figure 10.* shows the definition of DNL.

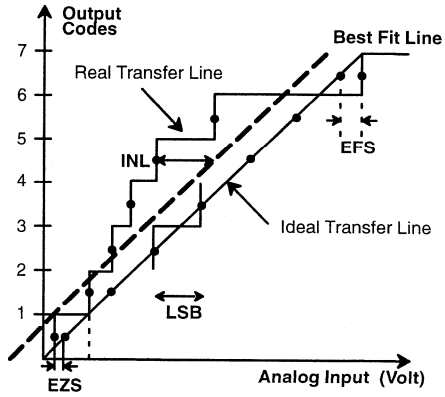


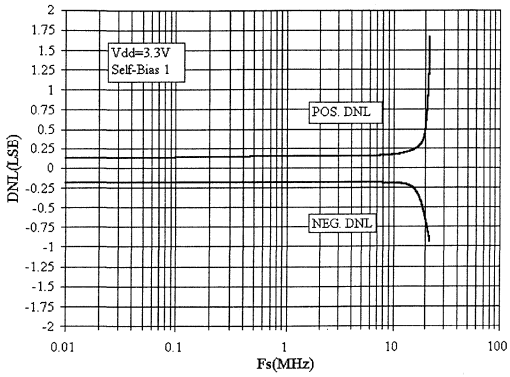
Figure 11. INL Error Calculation (3-Bit)

Figure 11. gives a visual definition of the INL error. The graph shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

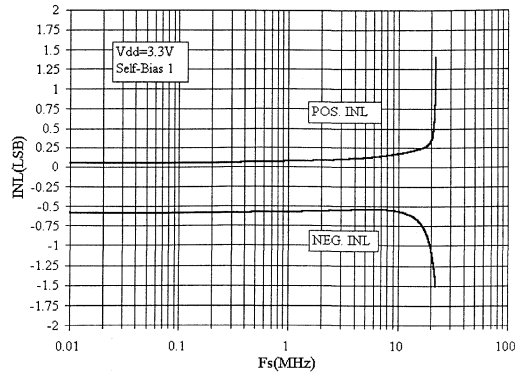
After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the best fit line makes equal the positive and the negative INL errors. This may change an INL of –1 to +2 LSB's relative to the ideal line into a ±1.5 relative to the best fit line.

5

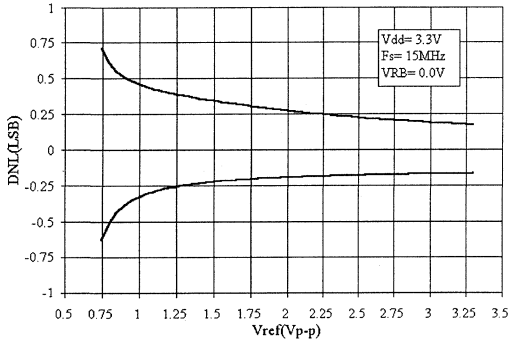
PERFORMANCE CHARACTERISTICS



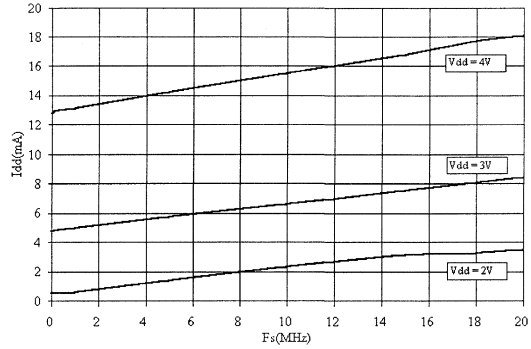
Graph 1. DNL vs. Sampling Frequency



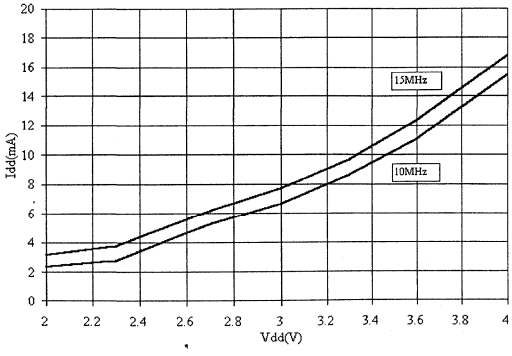
Graph 2. INL vs. Sampling Frequency



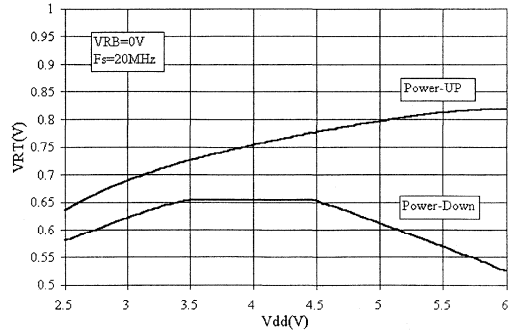
Graph 3. DNL vs. Reference Voltage



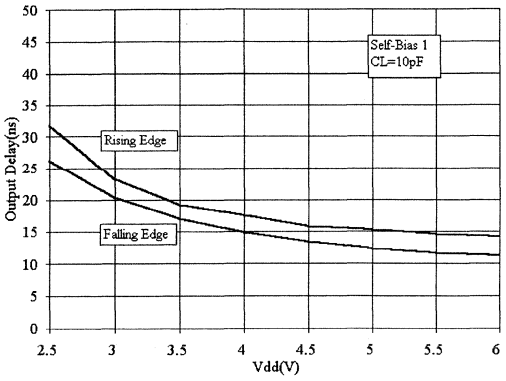
Graph 4. Supply Current vs. Sampling Frequency



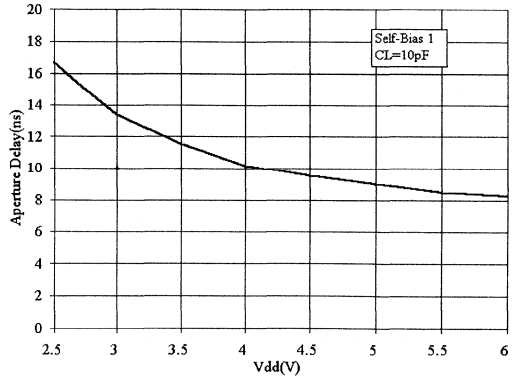
Graph 5. Supply Current vs. Supply Voltage



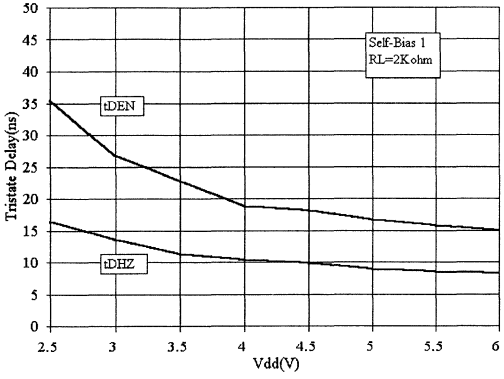
Graph 6. Power Up/Down Voltage vs. Supply Voltage



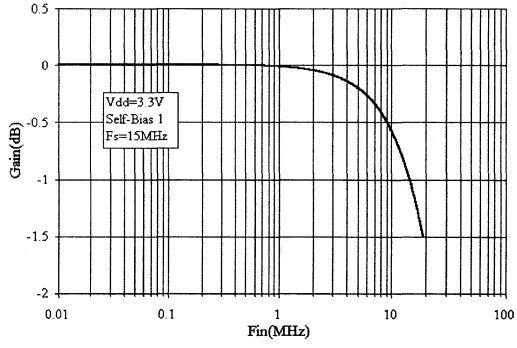
Graph 7. Output Delay vs. Supply Voltage



Graph 8. Aperture Delay vs. Supply Voltage



Graph 9. 3-State/Enable Delay vs. Supply Voltage



Graph 10. Gain vs. Input Frequency

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MP87L82

Low Voltage CMOS
10-Bit 2 MHz
Analog-to-Digital Converter

FEATURES

- 3.3 V Operation
- 10-Bit Resolution
- 2 MHz Sampling Rate
- DNL = ±1 LSB, INL = ±2 LSB
- Internal S/H Function
- V_{IN} DC Range: 0 V to V_{DD}
- V_{REF} DC Range: 1 V to V_{DD}
- Low Power: 25 mW (typ)
- Bipolar Range using RTS & RBS; +1.4 V to –1.4 V
- R1 - R7 Reference Ladder Taps (1/8th – 7/8th points)
- Aperture Delay Sync Signal
- MINV & LINV Digital Output Format Controls
- PHASE Control
- Overflow and Underflow bits
- Dual 3-State Controls ($\overline{OE1}$ & OE2)
- Three-State Digital Outputs
- Latch-Up Free

APPLICATIONS

- Digital Color Copiers
- Digital Cellular Telephones
- Precision CCDs and Scanners
- Medical Scanners
- Ultrasonics
- Digital Radio

BENEFITS

- Simplified Analog Design
- Rugged
- Few External Components, no S/H Needed
- Reduced Board Space

5

GENERAL DESCRIPTION

The MP87L82 is a full featured 10 bit, 2 MSPS, Analog-to-Digital Converter for applications which require high speed and high accuracy and operate at 3.3 V. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The MP87L82 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the MP87L82 includes a S/H function and internal resistors that allow this part to digitize analog input signals between – V_{RT} to V_{DD} using a single supply. (Unipolar and Bipolar Conversion capability)

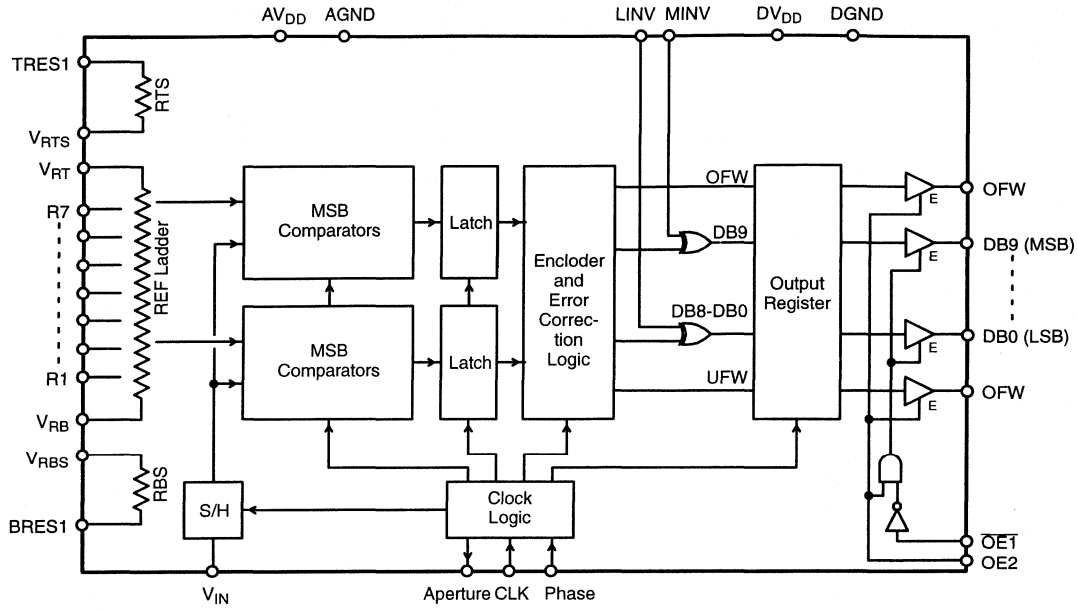
The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.4 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R7) can be used to externally trim any INL errors, or to shape the A/D converter transfer function.

This device operates from a single 3.3 V supply ±10%. Power consumption from a 5 V supply is typically 25 mW at F_S=5MHz.

ORDERING INFORMATION

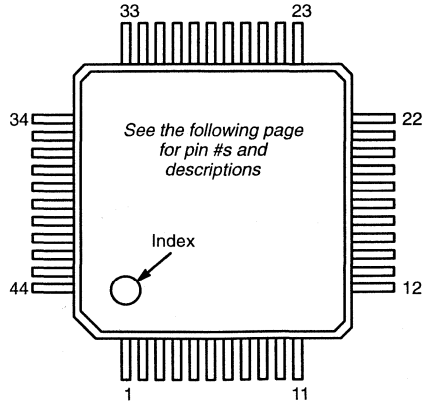
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP87L82AE	±1	2

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



44 Pin PQFP (14 mm x 14 mm)
Q44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{RT}	Top of Ladder
2	R7	Reference Ladder Tap @ 7/8
3	R6	Reference Ladder Tap @ 3/4
4	R5	Reference Ladder Tap @ 5/8
5	R4	Reference Ladder Tap @ 1/2
6	AV_{DD}	Analog Power Supply
7	A_{IN}	Analog Input
8	AGND	Analog Ground
9	R3	Reference Ladder Tap @ 3/8
10	R2	Reference Ladder Tap @ 1/4
11	R1	Reference Ladder Tap @ 1/8
12	V_{RBS}	Bottom Bias Resistor Terminal 2
13	N/C	No Connection
14	V_{RB}	Bottom of Ladder
15	Bres1	Bottom Bias Resistor Terminal 1
16	DGND	Digital Ground
17	OE2	Output Enable 2 (Input, Active High)
18	$\overline{OE1}$	Output Enable 1 (Input, Active Low)
19	UFW	Underflow (Output)
20	DB0	Data Output Bit 0 (LSB)
21	DB1	Data Output Bit 1
22	N/C	No Connection
23	DB2	Data Output Bit 2
24	DB3	Data Output Bit 3
25	DB4	Data Output Bit 4
26	N/C	No Connection
27	PHASE	Clock Polarity Control (Input)
28	LINV	Non MSB Digital Output Format (Input)
29	MINV	MSB Digital Output Format (Input)
30	N/C	No Connection
31	DB5	Data Output Bit 5
32	DB6	Data Output Bit 6
33	DB7	Data Output Bit 7
34	N/C	No Connection
35	N/C	No Connection
36	DB8	Data Output Bit 8
37	DB9	Data Output Bit 9 (MSB)
38	OFW	Overflow (Output)
39	CLK	Clock Input
40	Aperture	Aperture Delay Sync (Output)
41	DV_{DD}	Digital Power Supply
42	Tres1	Top Bias Resistor Terminal 1
43	V_{RTS}	Top Bias Resistor Terminal 2
44	N/C	No Connection

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3$ V, FS = 2 MHz (50% Duty Cycle), $V_{RT} = 2.4$, $V_{RB} = 0.6$, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	FS			2	MHz	
ACCURACY (A, S Grades)[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		10		LSB	
Full Scale Error	EFS		6		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}			AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L		375		Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Top Internal Reference	V_{RTS}		4		V	V_{RT} connected to V_{RTS} &
Bottom Internal Reference	V_{RBS}		1		V	V_{RB} connected to V_{RBS}
ANALOG INPUT[2]						
Input Bandwidth (–1 dB)[4]	BW		5		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance Sample[5]	C_{IN}		25		pF	
Input Capacitance Convert[5]			5		pF	
Aperture Delay	t_{AP}		40		ns	
Aperture Delay from Aperture Out			0		ns	5pF Load
Aperture Uncertainty (Jitter)	t_{AJ}		50		ps	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE1}$, MINV, LINV (Internal Res to DGND)[7]			15		µA	
$\overline{OE2}$, Phase (Internal Res to DV_{DD})[7]			15		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1*)						
Clock Period	1/FS		500		ns	
Rise & Fall Time[8]	t_R, t_F		5		ns	
"High" Pulse Width	t_{PWH}		250		ns	
"Low" Pulse Width	t_{PWL}		250		ns	
Duty Cycle			50		%	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	2.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		75		ns	
Data Enable Delay	t_{DEN}		45		ns	
Data 3-state Delay	t_{DHZ}		45		ns	
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}	3	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			12	mA	

NOTES
1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (FS).
2 Guaranteed. Not tested.
3 Specified values guarantee functionality. Refer to other parameters for accuracy.
4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5 See V_{IN} equivalent circuit (*Figure 8.*). Switched capacitor analog input requires driver with low output resistance.
6 All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE}$ has internal pull down. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7 Internal resistor to DGND biases unconnected input to active low logical level.
8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
9 The AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.
10 DV_{DD} and AV_{DD} pins should go to the same voltage and be separately decoupled.

Specifications are subject to change without notice

5

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +5.5 V
RTS & RBS terminals ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Package Power Dissipation Rating @ 75°C
PQFP ..... 800 mW
Derates above 75°C ..... 11mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

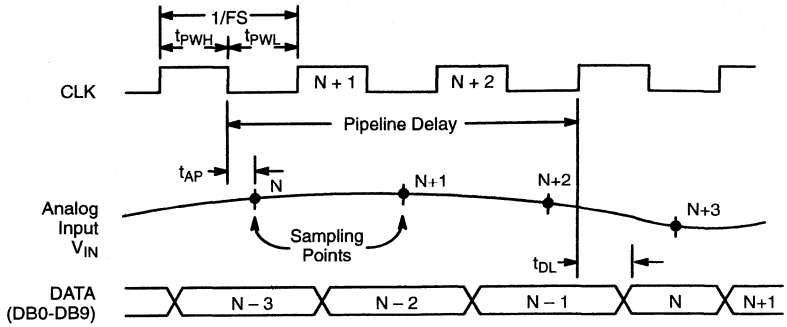


Figure 1. MP87L82 Timing Diagram

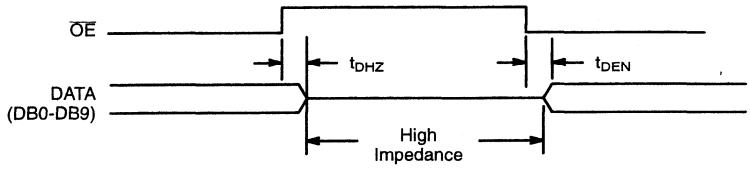
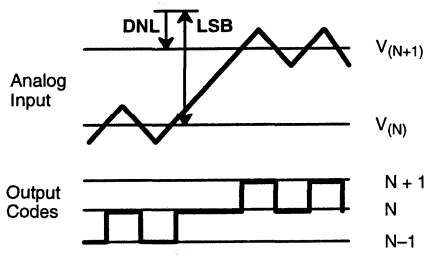


Figure 2. 3-State Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 1024

$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$

Figure 3. DNL Measurement

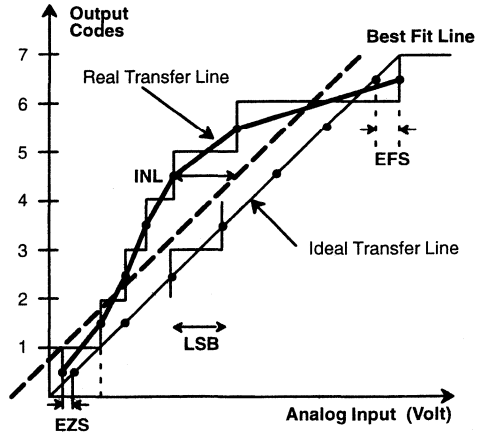


Figure 4. INL Error Calculation

APPLICATION NOTES

V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGNE and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

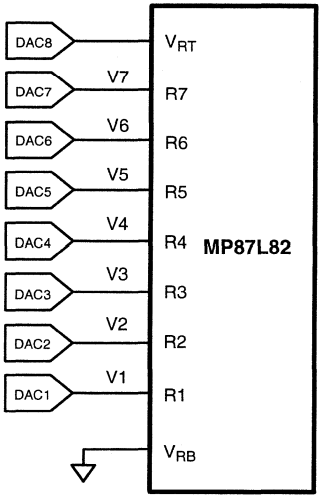
The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

The application resistors, RTS and RBS, protection allows for applied voltages in the range of AV_{DD} + 5 V to AGND – 5V. If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

The reference tap pins (R1-R7) should be decoupled with 0.1µF to 1µF capacitors. This will help stabilize the internal reference voltages thus reducing any INL errors.

The reference tap pins (R1-R7) can be used to create piecewise-linear transfer functions. By forcing custom voltages on these pins, an eight segment transfer function can be made. See *Figure 5. and Figure 6.*



DAC MP7228

Only the Ladder detail shown.

Figure 5. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

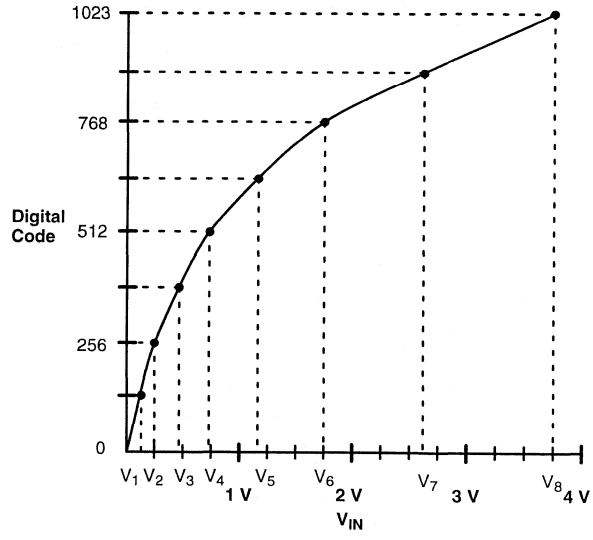


Figure 6. A Piecewise Linear, Logarithmic Transfer Function

5

OPTIONS on the MP87L82 DIE & OPERATION NOTES:

OFW & UFW Overflow & Underflow (outputs)

These signals indicate when the Analog Input (V_{IN}) goes outside the V_{RB} to V_{RT} range. Both pins are normally at low logic levels. When $V_{IN} > V_{RT}$, OFW will go high and the data bits (DB0 – DB9) will show full scale (i.e. all 1s if MINV & LINV are low). When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0s if MINV & LINV are low).

$\overline{OE1}$ & OE2 Output Enable (inputs)

These signals control the 3-state drivers on the digital outputs DB0 – DB9, OFW and UFW. During normal operation $\overline{OE1}$ should be held low and OE2 should be held high so that all outputs are enabled (NOTE: internal resistors will pull $\overline{OE1}$ and OE2 to these levels if they are not connected). When $\overline{OE1}$ is driven high DB0 – DB9 go into high impedance mode. When OE2 is driven low DB0 – DB9, OFW and UFW all go into high impedance mode (please refer to the truth table below). These controls operate asynchronous to the clock and they only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode.

$\overline{OE1}$	OE2	DBO-DB9	OFW & UFW
0	1	enabled	enabled
1	1	3-state	enabled
X	0	3-state	3-state

PHASE Clock Polarity Control (input)

This signal controls the phase relationship between the signal applied at the CLK pin and the internal clock signals. When PHASE is high, V_{IN} is sampled at the high to low CLK transition and the digital data changes after a low to high CLK transition. When PHASE is low, V_{IN} is sampled at the low to high CLK transition and the digital data changes after a high to low CLK transition. See timing diagram *Figure 7.* PHASE has an internal pull up device.

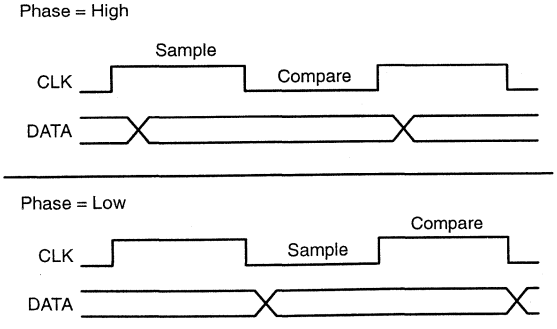


Figure 7. Clock Phase Relationship

APERTURE Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event.

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. The diagram *Figure 8.* shows an equivalent input circuit.

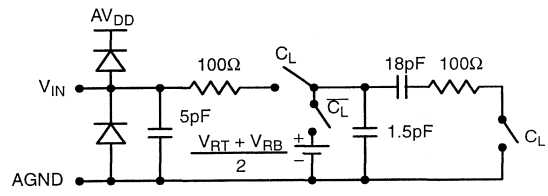


Figure 8. Equivalent Input Circuit

MINV & LINV Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB9 (*see Table 1.)* Normally both pins are held low so the data is in straight binary format (all 0s when $V_{IN}=V_{RB}$; all 1s when $V_{IN}=V_{RT}$). If MINV is pulled high then the MSB (DB9) will be inverted. If LINV is pulled high, then the LSB's (DB0 – DB8) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV LINV	0 0	0 1	1 0	1 1
V_{IN}	V_{RT} 111 . . . 11 111 . . . 10 ⋮ 100 . . . 01 100 . . . 00 (mid scale) 011 . . . 11 ⋮ 000 . . . 01 V_{RB} 000 . . . 00	100 . . . 00 100 . . . 01 ⋮ 111 . . . 10 111 . . . 11 000 . . . 00 ⋮ 011 . . . 10 011 . . . 11	011 . . . 11 011 . . . 10 ⋮ 000 . . . 01 000 . . . 00 111 . . . 11 ⋮ 100 . . . 01 100 . . . 00	000 . . . 00 000 . . . 01 ⋮ 011 . . . 10 011 . . . 11 100 . . . 00 ⋮ 111 . . . 10 111 . . . 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

MINV & LINV are meant to be static digital signals. If they are to change during operation they should only change when the CLK is low (assuming PHASE is high, if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. Please see the simplified logic circuit *Figure 9.* MINV and LINV have internal pull down devices.

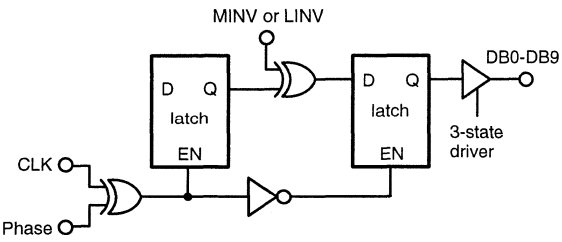


Figure 9. MINV, LINV Simplified Logic Circuit

RTS & RBS Internal Bias Resistors

Two matched resistors are provided on the chip. These resistors can be used to generate on chip reference voltages, or to extend the analog input range. Each resistor has a value equal to 1/3 of the reference ladder resistor. By connecting RTS between AV_{DD} (3 V) and V_{RT}, and connecting RBS between AGND and V_{RB}, the reference ladder will be biased to 0.6 V at V_{RB} and 2.4 V at V_{RT}.

A bipolar input range ($+V_{RT}$ to $-V_{RT}$) can be achieved by connecting RTS and RBS as shown in *Figure 10.* Due to current density limitations for RTS and RBS, V_{RT} should be limited to +1.4 volts in this configuration. The protection pads used for the resistor terminals are designed to allow voltages that go beyond the supply rails.

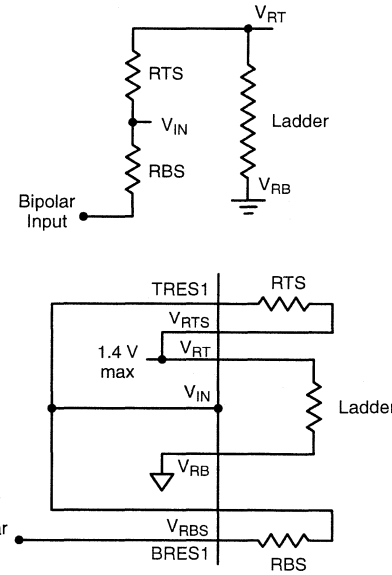
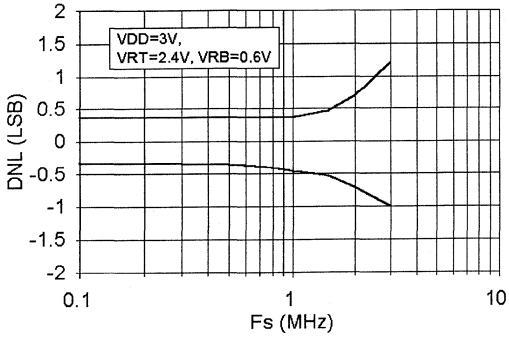


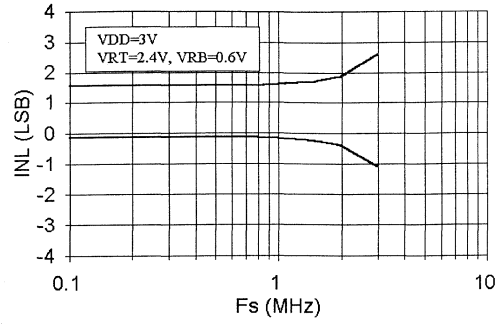
Figure 10. Bipolar Input Configuration

R1 thru R7 Reference Ladder Taps. These taps connect to every eighth point along the reference ladder; R1 is 1/8th up from V_{RB}, R7 is 7/8ths up from V_{RB} (or 1/8th down from V_{RT}). Normally these pins should have 0.1 µF capacitors to AGND, this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. An eight segment, piece wise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

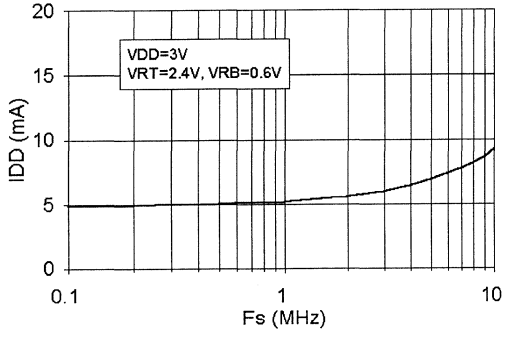
PERFORMANCE CHARACTERISTICS



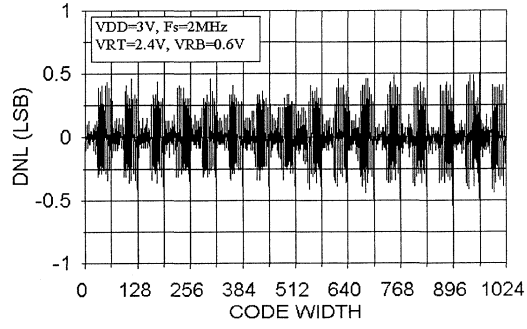
Graph 1. DNL vs. Sampling Frequency



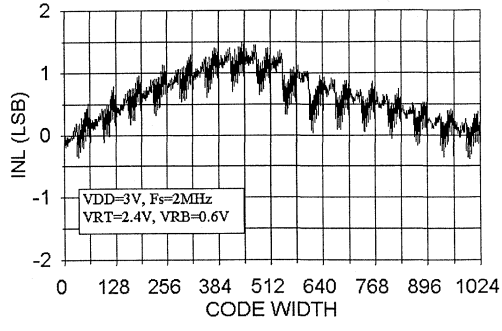
Graph 2. INL vs. Sampling Frequency



Graph 3. Power Supply Current vs. Sampling Frequency



Graph 4. DNL Error Plot



Graph 5. INL Error Plot

MP87L84

Low Voltage CMOS
10-Bit 2 MHz
Analog-to-Digital Converter

FEATURES

- 3.3 V Operation
- 10-Bit Resolution
- 2 MHz Sampling Rate
- DNL = ±1 LSB, INL = ±2 LSB
- Internal S/H Function
- V_{IN} DC Range: 0 V to V_{DD}
- V_{REF} DC Range: 1 V to V_{DD}
- Low Power: 25 mW (typ)
- Three-State Digital Outputs
- Latch-Up Free

APPLICATIONS

- Digital Color Copiers
- Digital Cellular Telephones
- Precision CCDs and Scanners
- Medical Scanners
- Ultrasonics
- Digital Radio

BENEFITS

- Simplified Analog Design
- Rugged
- Few External Components, no S/H Needed
- Reduced Board Space

GENERAL DESCRIPTION

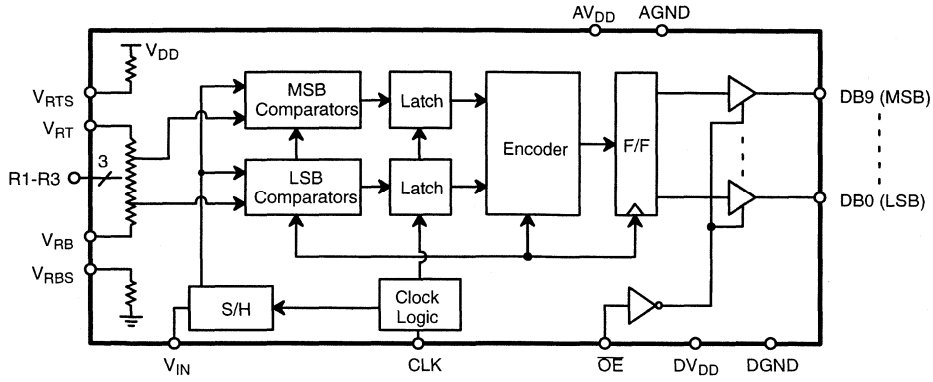
The MP87L84 is a 10-bit, 2 MSPS Analog-to-Digital Converter for applications that require high speed and high accuracy. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The MP87L84 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the MP87L84 includes an on-chip S/H function that allows this part to digitize analog input signals between AGND and AV_{DD}.

The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.4 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R3) can be used to externally trim any INL errors.

This device operates from a single 3.3 V supply. Power consumption from a 3.3 V supply is typically 25 mW at F_S=2 MHz.

SIMPLIFIED BLOCK DIAGRAM

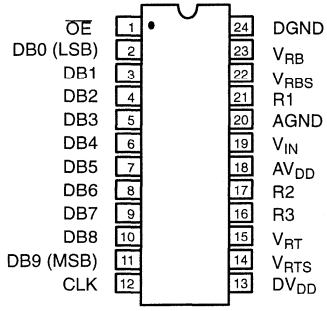


ORDERING INFORMATION

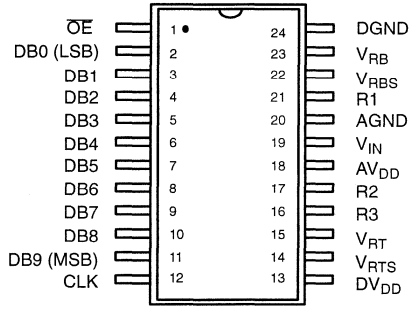
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP87L84AN	⊥1	2
SOIC	–40 to +85°C	MP87L84AS	±1	2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	CLK	Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV_{DD}	Digital Power Supply
14	V_{RTS}	Top Internal Reference
15	V_{RT}	Top of Reference
16	R3	3/4 Reference Tap Point
17	R2	1/2 Reference Tap Point
18	AV_{DD}	Analog Power Supply
19	V_{IN}	Analog Input Voltage
20	AGND	Analog Ground
21	R1	1/4 Reference Tap Point
22	V_{RBS}	Bottom Internal Reference
23	V_{RB}	Bottom of Reference
24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3 V, FS = 2 MHz (50% Duty Cycle), V_{RT} = 2.4, V_{RB} = 0.6, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	FS			2	MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		10		LSB	
Full Scale Error	EFS		6		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}			AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L		375		Ω	
Ladder Temp. Coefficient[2]	R_{TCO}		2000		ppm/°C	
Top Internal Reference	V_{RTS}		4		V	V_{RT} connected to V_{RTS} &
Bottom Internal Reference	V_{RBS}		1		V	V_{RB} connected to V_{RBS}
ANALOG INPUT						
Input Bandwidth (–1 dB)[4]	BW		5		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance Sample[5]	C_{IN}		25		pF	
Input Capacitance Convert[5]			5		pF	
Aperture Delay	t_{AP}		40		ns	
Aperture Uncertainty (Jitter)	t_{AJ}		50		ps	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$ (Internal Res to DGND)[7]			15		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1*)						
Clock Period	1/FS	500			ns	
Rise & Fall Time[8]	t_R, t_F		5		ns	
"High" Pulse Width	t_{PWH}		250		ns	
"Low" Pulse Width	t_{PWL}		250		ns	
Duty Cycle			50		%	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	2.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		75		ns	
Data Enable Delay	t_{DEN}		45		ns	
Data 3-state Delay	t_{DHZ}		45		ns	

5

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}	3.0	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			12	mA	

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (FS).
2. Guaranteed. Not tested.
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5. See V_{IN} equivalent circuit (*Figure 8.*). Switched capacitor analog input requires driver with low output resistance.
6. All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE}$ has internal pull down. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7. Internal resistor to GND biases unconnected input to active low logical level.
8. Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
9. The AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +5.5 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC ..... 1000 mW
Derating above 75°C ..... 13mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

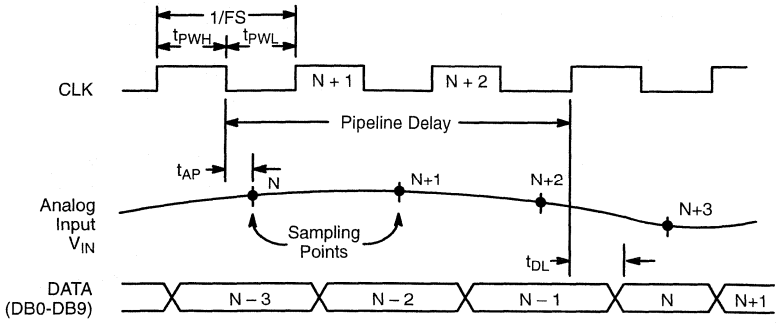


Figure 1. MP87L84 Timing Diagram

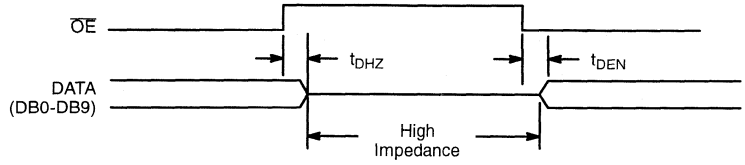


Figure 2. 3-State Timing Diagram

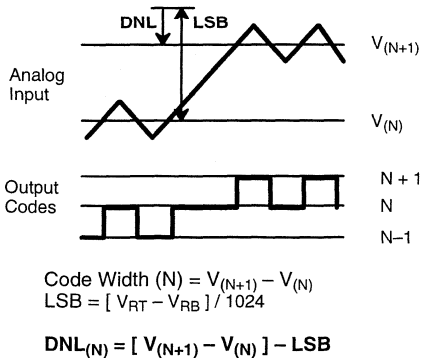


Figure 3. DNL Measurement

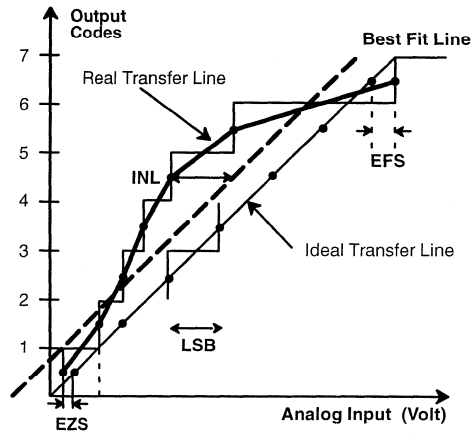


Figure 4. INL Error Calculation

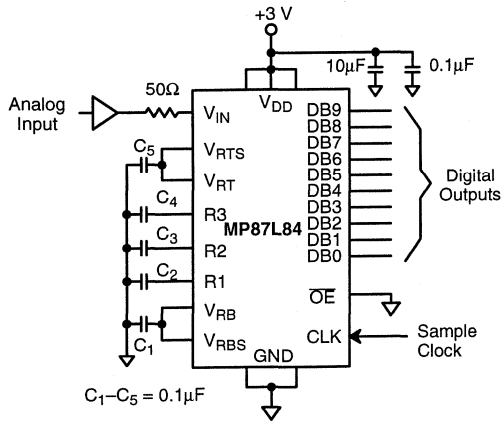


Figure 5. Typical Circuit Connections

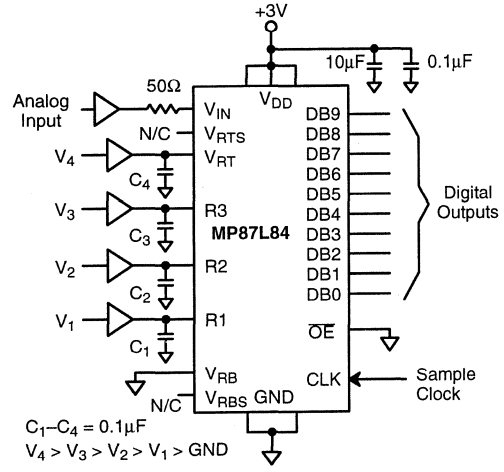


Figure 6. Creating a Piecewise Linear Transfer Function

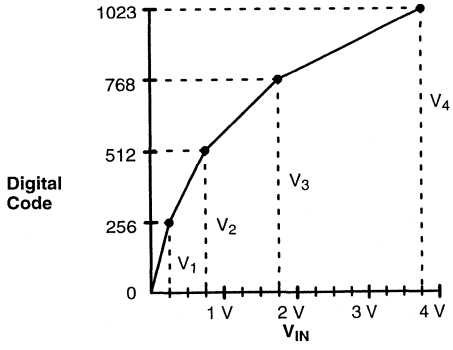


Figure 7. A Piecewise Linear, Logarithmic Transfer Function

APPLICATION NOTES

Signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. *Figure 8.* shows an equivalent input circuit.

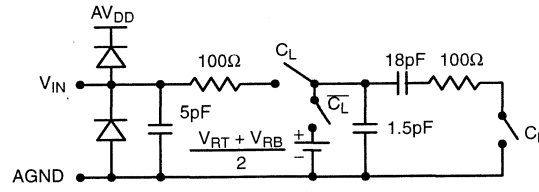


Figure 8. Equivalent Input Circuit

RTS & RBS Internal Bias Resistors

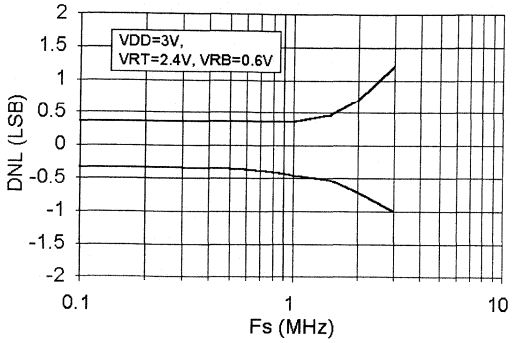
Two matched resistors are provided on the chip. These resistors can be used to generate on chip reference voltages. Each resistor has a value equal to 1/3 of the reference ladder resistor. By connecting RTS to V_{RT}, and connecting RBS to V_{RB}, the reference ladder will be biased to 0.6 V at V_{RB} and 2.4 V at V_{RT}.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

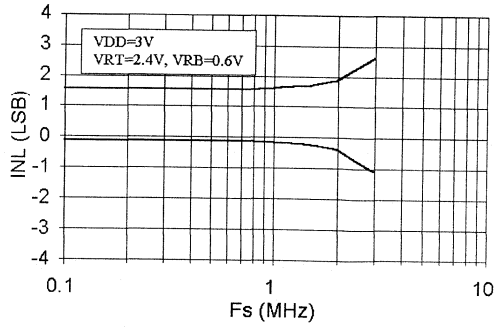
R1 thru R3 Reference Ladder Taps

These taps connect to every eighth point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 micro farad capacitors to V_{SS}, this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. A four segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

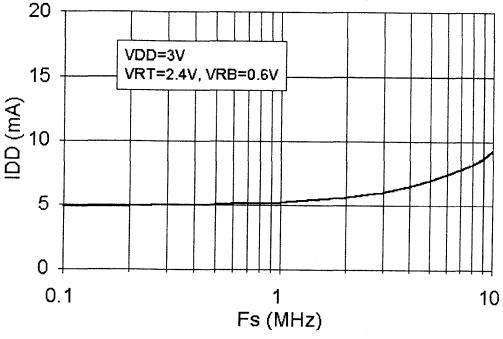
PERFORMANCE CHARACTERISTICS



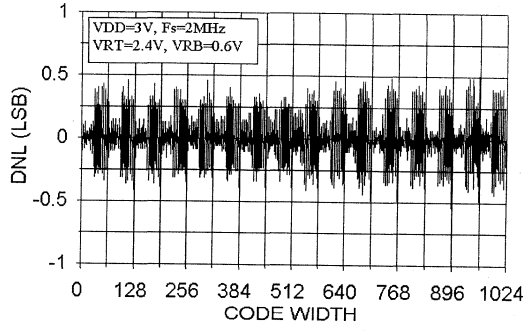
Graph 1. DNL vs. Sampling Frequency



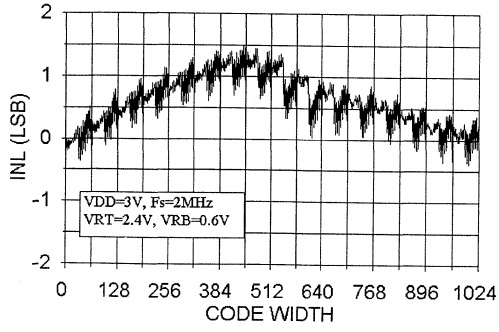
Graph 2. INL vs. Sampling Frequency



Graph 3. Power Supply Current vs. Sampling Frequency



Graph 4. DNL Error Plot



Graph 5. INL Error Plot

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MP87L85

Low Voltage CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **3.3 Volt Operation**
- **8-Bit Resolution**
- **DNL = ±1/2 LSB, INL = ±1 LSB (typ)**
- **Internal S/H Function**
- **V_{IN} DC Range: 0 V to V_{DD}**
- **V_{REF} DC Range: 1 V to V_{DD}**
- **Low Power: 25 mW typ. (excluding reference)**
- **Latch-Up Free**

APPLICATIONS

- **Digital Radio**
- **Cellular Telephones**
- **CCD's and Scanners**
- **Hand Held and Battery Powered Data Acquisition**

GENERAL DESCRIPTION

The MP87L85 is an 8-bit Analog-to-Digital Converter that operates at 3.3 V. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

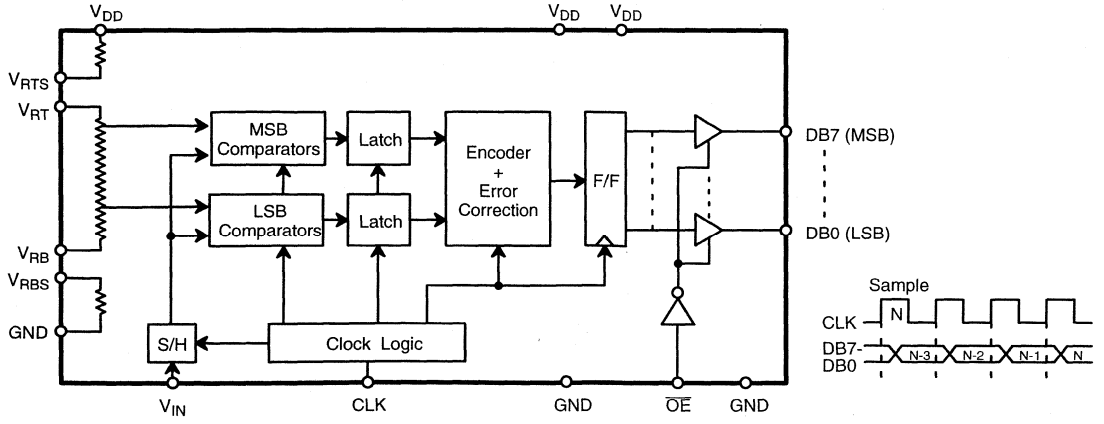
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP87L85 includes an on-chip S/H function which allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP87L85.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.4 V at V_{RB} and 1.72 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +3.3 V supply ±10%. Power consumption is 35 mW maximum at FS = 10 MHz.

5

SIMPLIFIED BLOCK AND TIMING DIAGRAM

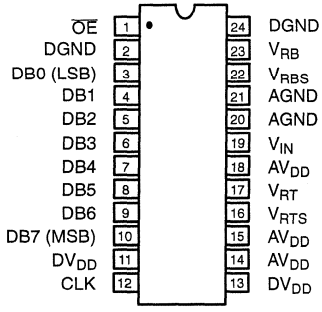


ORDERING INFORMATION

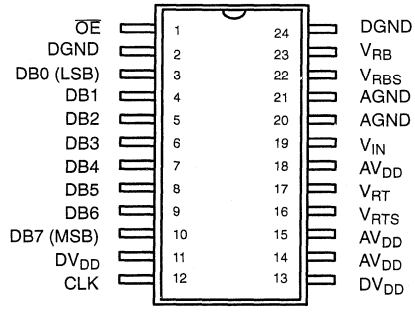
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC (EIAJ)	–40 to +85°C	MP87L85AR	±1/2	1 1/2
SOIC (Jedec)	–40 to +85°C	MP87L85AS	±1/2	1 1/2
Plastic Dip (0.300")	–40 to +85°C	MP87L85AN	±1/2	1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC EIAJ (0.300") – RN24
& Jedec (0.300") – S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DGND	Digital Ground
3	DB0	Data Output Bit 0 (LSB)
4	DB1	Data Output Bit 1
5	DB2	Data Output Bit 2
6	DB3	Data Output Bit 3
7	DB4	Data Output Bit 4
8	DB5	Data Output Bit 5
9	DB6	Data Output Bit 6
10	DB7	Data Output Bit 7 (MSB)
11	DV_{DD}	Digital Power Supply
12	CLK	Sampling Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV_{DD}	Digital Power Supply
14	AV_{DD}	Analog Power Supply
15	AV_{DD}	Analog Power Supply
16	V_{RTS}	Generates 1.72 V if tied to V_{RT}
17	V_{RT}	Top Reference
18	AV_{DD}	Analog Power Supply
19	V_{IN}	Analog Input
20	AGND	Analog Ground
21	AGND	Analog Ground
22	V_{RBS}	Generates 0.4 V if tied to V_{RB}
23	V_{RB}	Bottom Reference
24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3.3 V, FS = 6 MHz (50% Duty Cycle), V_{RT} = 2.5 V, V_{RB} = 0.5 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS	0.1		10	MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±1/2	LSB	
Integral Non-Linearity	INL			1 1/2	LSB	Best Fit Line (Max INL – Min INL)/2
REFERENCE VOLTAGES						
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L		350		Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.36		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		1.32		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		1.52		V	
ANALOG INPUT						
Input Bandwidth (–1 dB)[4]	BW		5		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance[5]	C_{IN}		16		pF	
Aperture Delay	t_{AP}		30		ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[7]						
Clock Period	1/FS		100		ns	
High Pulse Width	t_{PWH}		50		ns	
Low Pulse Width	t_{PWL}		50		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	2.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		30		ns	
Data Enable Delay	t_{DEN}		35		ns	
Data 3-state Delay	t_{DHZ}		17		ns	

5

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
POWER SUPPLIES						
Operating Voltage	V_{DD}	3	3.3	3.6	V	
Current	I_{DD}		6	12	mA	Does not include ref. current

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width ($V_{REF}/256$) is the DNL error (*Figure 2.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 3.*). Accuracy is a function of the sampling rate (FS).
2. Guaranteed. Not tested.
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5. See V_{IN} input equivalent circuit (*Figure 4.*). Switched capacitor analog input requires driver with low output resistance.
6. All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7. t_R, t_F should be limited to >5 ns for best results.
8. AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 5.5 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP ..... 850 mW
Derates above 75°C ..... 11 mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

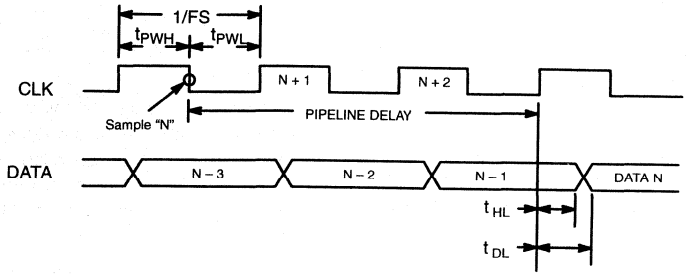
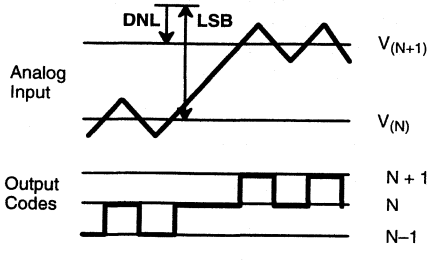


Figure 1. MP87L85 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 256

$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$

Figure 2. DNL Measurement

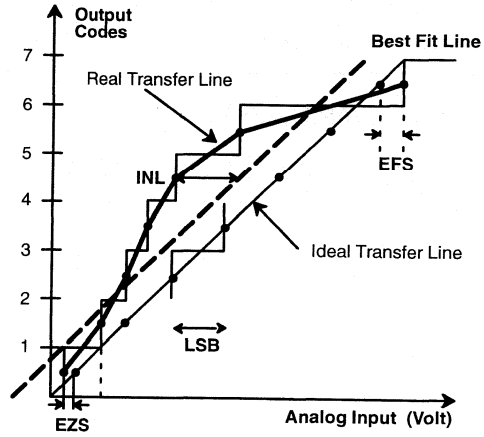


Figure 3. INL Error Calculation

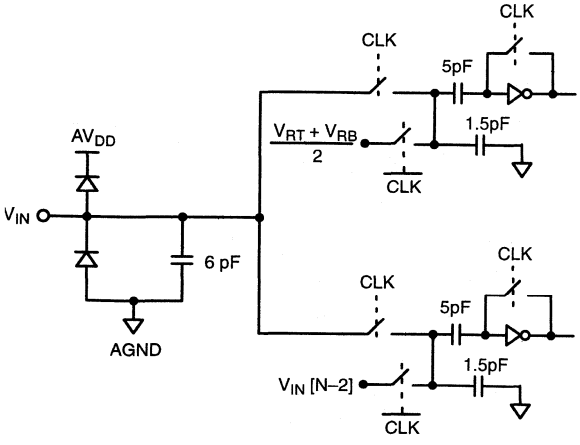


Figure 4. Equivalent Input Circuit

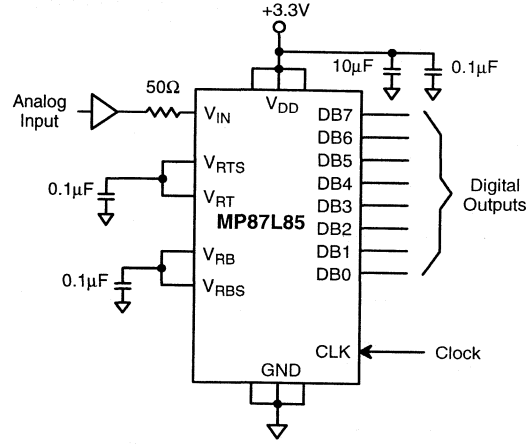


Figure 5. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V or DV_{DD} +0.5 V or DGND –0.5 V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

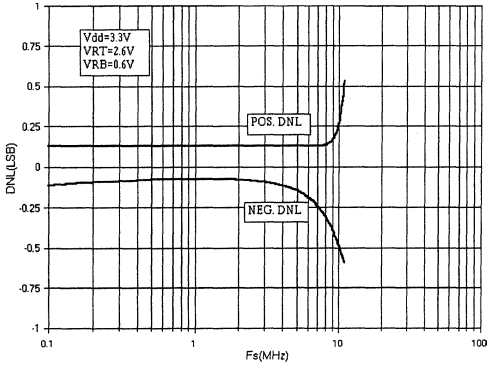
The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

It is possible for the data valid delay (t_{DL}) to be equal to or greater than the high pulse width of the sampling clock (t_{PWH}), See *Figure 1.* This can cause timing related errors. For sample rates above 14 MSPS use only the rising edge of the sample clock (CLK) to latch data from the MP87L85 to other parts of the system.

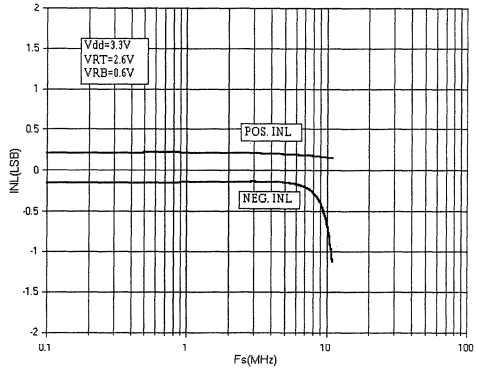
The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.36 V at V_{RB} and 1.56 V at V_{RT} (see *Figure 5.).*

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

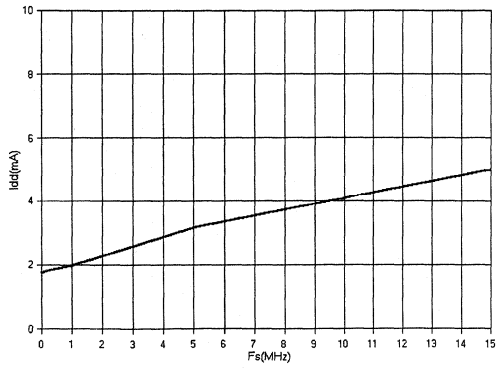
PERFORMANCE CHARACTERISTICS



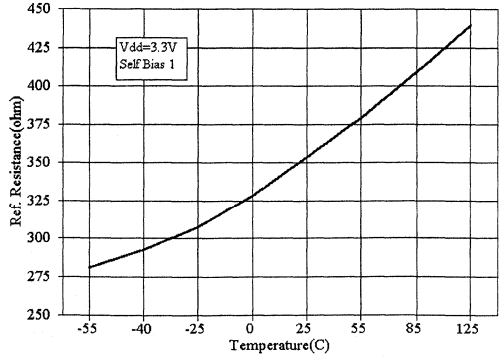
Graph 1. DNL vs. Sampling Frequency



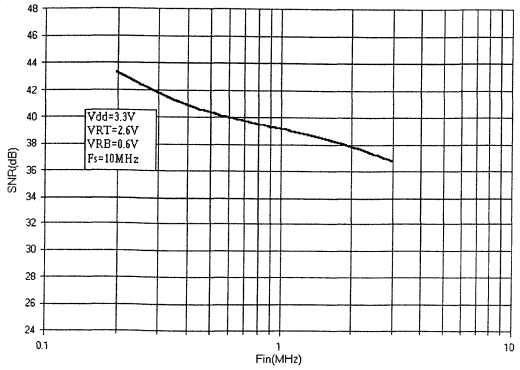
Graph 2. INL vs. Sampling Frequency



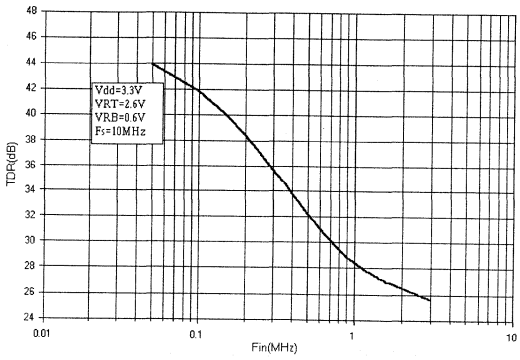
Graph 3. Supply Current vs. Sampling Frequency



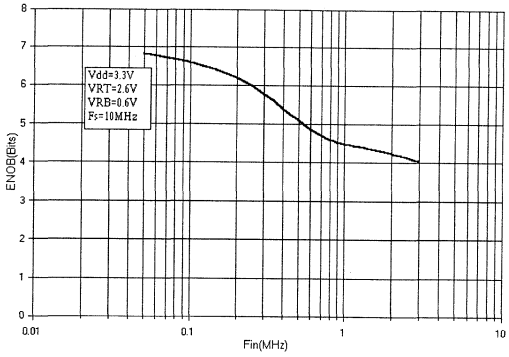
Graph 4. Reference Resistance vs. Temperature



Graph 5. SNR vs. Input Frequency



Graph 6. SINAD vs. Input Frequency



Graph 7. ENOB vs. Input Frequency

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MP87L91

Low Voltage CMOS 12-Bit High Speed Analog-to-Digital Converter with Parallel Logic Interface Port

FEATURES

- **3.3 V Operation**
- **12-Bit ADC with DNL = ±1 LSB, INL = ±2 LSB**
- **Sampling Frequency 1 MHz (typ)**
- **Rail-to-Rail Input Range**
- **V_{REF} Range: 1.5 V to V_{DD}**
- **CMOS Low Power: 25 mW (typ)**
- **1/4, 1/2 and 3/4 Scale Reference Resistor Taps**
- **Three-State Outputs**
- **Binary and Two's Complement Digital Output Mode**

APPLICATIONS

- **Instrumentation**
- **Medical Imaging**
- **Ultrasound**
- **Magnetic Resonance Signal Acquisition**
- **Digital Oscilloscopes**
- **Spectrum Analysis**

GENERAL DESCRIPTION

The MP87L91 is a monolithic 1 MSPS 12-bit 2-step flash Analog-to-Digital Converter with DNL = ±1 LSB and INL = ±2 LSB. The MP87L91 contains an internal track and hold.

The MP87L91 operates with a single 3.3 V supply while consuming less than 25 mW of power (typical). Separate pins for reference ladder terminals and power supplies allow flexibility for various A_{IN}, ΔV_{REF}, and power supply ranges.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. Also, the digital output port is equipped with a 3-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment, linearity, and speed enhancement can be accommodated.

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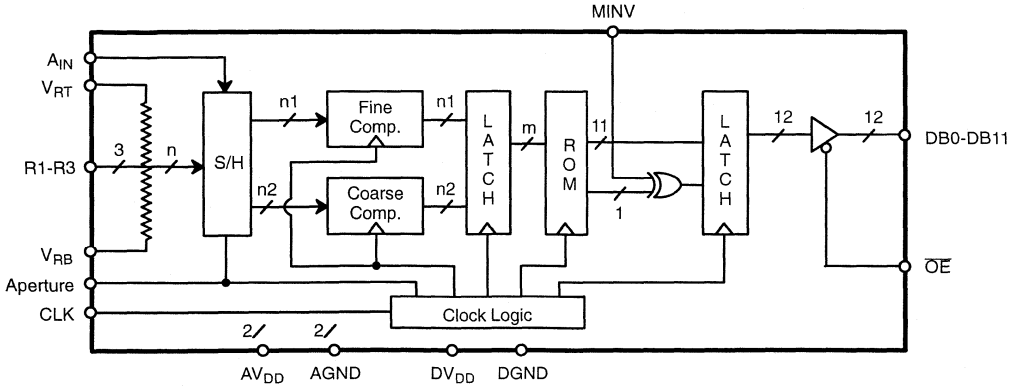
SIMPLIFIED BLOCK DIAGRAM

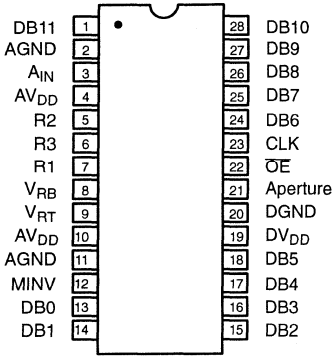


ORDERING INFORMATION

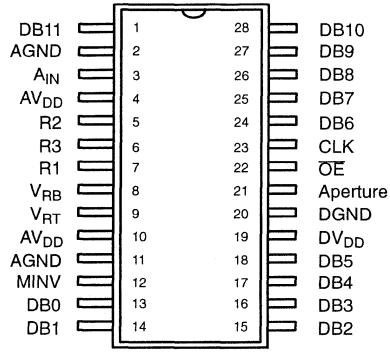
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	MP87L91AN	±1	2 1/2
SOIC	–40 to +85°C	MP87L91AS	±1	2 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB11	Data Output Bit 11 (MSB)
2	AGND	Analog Negative Supply
3	A_{IN}	Analog Input
4	AV_{DD}	Analog Positive Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{RB}	Negative Reference
9	V_{RT}	Positive Reference
10	AV_{DD}	Analog Positive Supply
11	AGND	Analog Negative Supply
12	MINV	Invert MSB (Active High)
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1

PIN NO.	NAME	DESCRIPTION
15	DB2	Data Output Bit 2
16	DB3	Data Output Bit 3
17	DB4	Data Output Bit 4
18	DB5	Data Output Bit 5
19	DV_{DD}	Digital Positive Supply
20	DGND	Digital Negative Supply
21	Aperture	Delayed Clock, indicates sample point
22	$\overline{OE}$	Output Enable (Active Low)
23	CLK	Clock
24	DB6	Data Output Bit 6
25	DB7	Data Output Bit 7
26	DB8	Data Output Bit 8
27	DB9	Data Output Bit 9
28	DB10	Data Output Bit 10

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3 V, FS = 1 MHz (50% Duty Cycle), V_{RT} = 3.0 V, V_{RB} = AGND, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		12			Bits	
Sampling Rate	FS			1	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			2 1/2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$	0.5		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		V_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		55	60	ns	
Aperture Delay from Aperture Signal	t_{AP}		0		ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE}$, MINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S		1		µs	
Rise & Fall Time[7]	t_R, t_F		15		ns	
"High" Time	t_{PWH}		500		ns	
"Low" Time	t_{PWL}		500		ns	
Duty Cycle			50		%	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		65	75	ns	
Data Enable Delay	t_{DEN}		60	75	ns	
Data 3-state Delay	t_{DHZ}		60		ns	

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ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
POWER SUPPLIES[8] (Tmin to Tmax)						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			12	mA	
AC PARAMETERS						
Signal Noise Ratio	SNR		66		dB	

NOTES

1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).
2. Guaranteed. Not tested.
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5. Switched capacitor analog input requires driver with low output resistance.
6. All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7. Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
8. AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 5.5 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

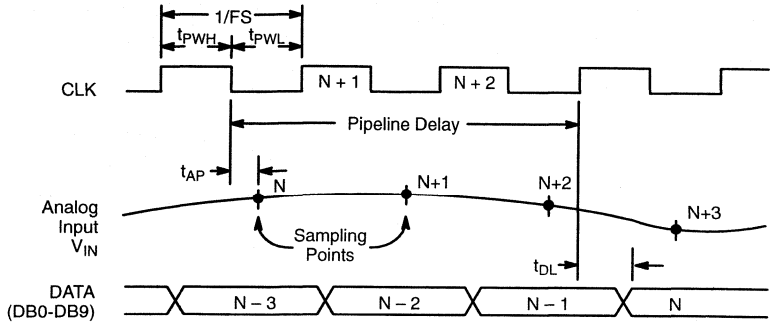

Figure 1. Timing Diagram

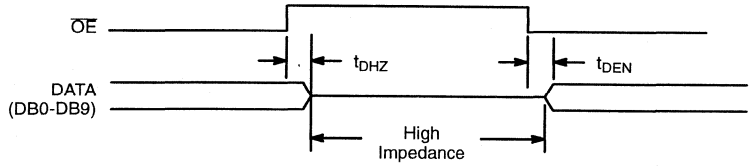

Figure 2. 3-State Timing Diagram

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OVERVIEW OF THE MP87L91 PINS & OPERATION NOTES

$\overline{OE}$: Output Enable (Input)

This signal controls the 3-state drivers on the digital outputs DB0 - DB11. During normal operation $\overline{OE}$ should be held low so that all outputs are enabled (NOTE: an internal resistor will pull $\overline{OE}$ to this level if it is not connected). When $\overline{OE}$ is driven high DB0 - DB11 goes into high impedance mode. This control operates asynchronously to the clock and only controls the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. If possible, $\overline{OE}$ should be in 3-state during Clock = 1 to reduce digital noise coupling into A_{IN} during the sample time. Aperature provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

APERTURE: Aperture Delay Sync (Output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperature pin may also be used to control the $\overline{OE}$ (outputs between 3-state and active mode). This will reduce the errors introducted by digital output coupling during the A_{IN} sample time.

MINV: Digital Output Format (Input)

This signal controls the format of the digital output data bits DB0 – DB11. Normally it is held low so the data is in straight binary format (all 0's when $V_{IN} = V_{RB}$; all 1's when $V_{IN} = V_{RT}$). If MINV is pulled high then the MSB (DB11) will be inverted.

MINV is meant to be a static digital signal. If it is to change during operation it should only change when the CLK is low. Changing MINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV has a internal pull down device. This function is not available in the engineering sidebraze samples. For these samples, this pin must be tied to GND.

V_{IN}: Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock.

R1, R2, R3: Reference Ladder Taps

These taps connect to every 1/4 point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS}, this helps reduce the INL errors by stabilizing the reference ladder voltages.

These taps can also be used to alter the transfer curve of the ADC. A 4 segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

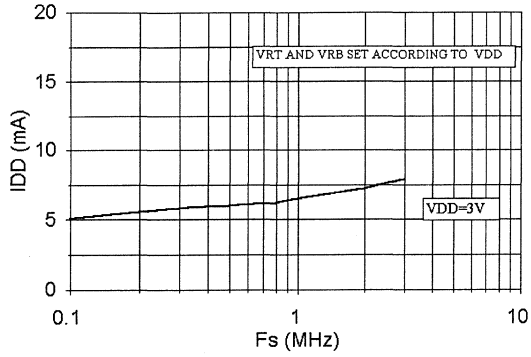
This may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

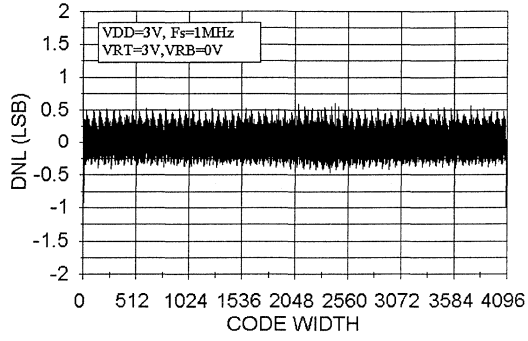
The internal interconnect resistance from each of the t_{AP} pins to the ladder is less than 3Ω.

1.6V maximum per tap is recommended for applications above 85°C. For operation less than 85°C up to 3.2 V per tap can be utilized.

PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. FS



Graph 2. DNL Error Plot

MP87L92

Low Voltage CMOS 12-Bit High Speed Analog-to-Digital Converter with Serial Logic Interface Port

FEATURES

- 3.3 V Operation
- 12-Bit ADC with DNL = ±1 LSB, INL = ±2 LSB
- Sampling Frequency 1 MHz (typ)
- Rail-to-Rail Input Range
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 25 mW (typ)
- Spaced Ladder Taps for Non-Linear Transfer Function Creation
- Binary and Two's Complement Digital Output Mode
- Serial Port
- Underflow Outputs
- Precision Aperture Output
- Latch-Up Proof

APPLICATIONS

- Instrumentation
- DAS
- Radar
- Medical Imaging
- Ultrasound
- Broadcast and Studio Video
- Magnetic Resonance Signal Acquisition
- Digital Oscilloscopes
- Spectrum Analysis
- Digital Radio

5

GENERAL DESCRIPTION

The MP87L92 is a 12-bit 2-step high speed Analog-to-Digital Converter with DNL = ±1 LSB and INL = ±2 LSB. The MP87L92 contains an internal track and hold which allows for analog input signals as fast as 1 MHz and can convert signals at a 1 MSPS rate.

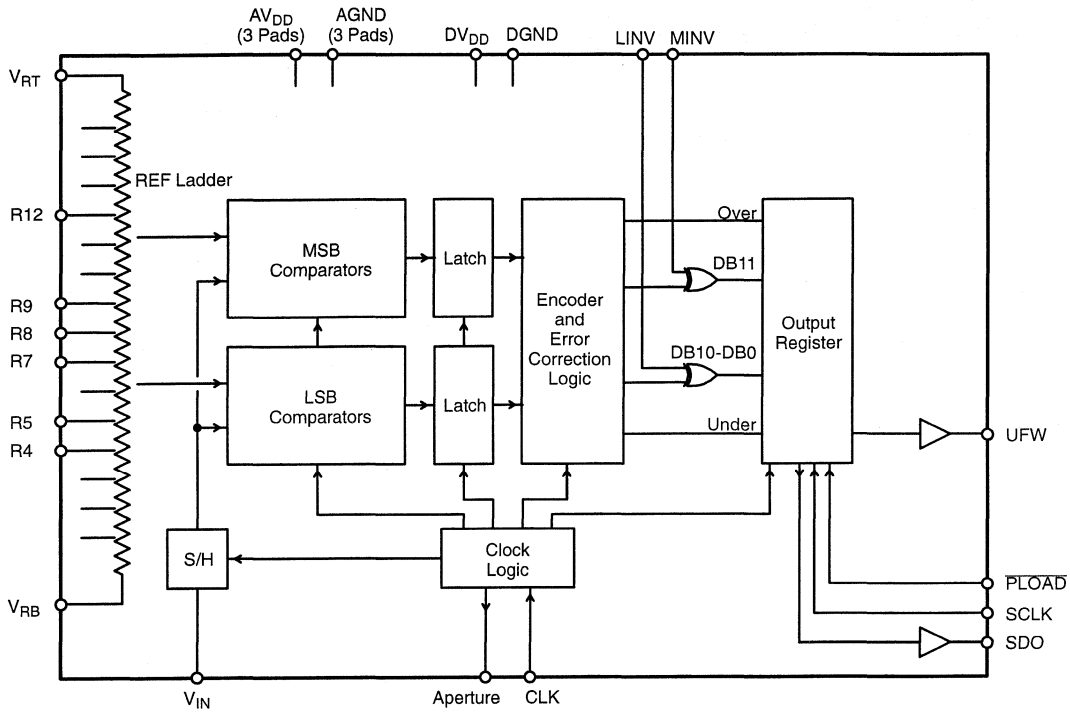
The MP87L92 operates with a single supply at +3.3 V. Separate pins for reference ladder terminals and power supplies allow flexibility for various A_{IN}, ΔV_{REF}, and power supply ranges.

Data is presented at the output port every clock cycle after a 2.5 cycle pipeline delay. The digital output port is equipped with a serial data port. LINV and MINV enable binary and 2's complement data formatting. Through the 6 ladder tap pins, transfer function adjustment, linearity, and speed enhancement can be accommodated.

ORDERING INFORMATION

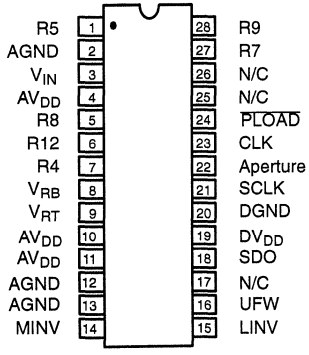
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP87L92AS	±1	±2
PDIP	–40 to +85°C	MP87L92AN	±1	±2

SIMPLIFIED BLOCK DIAGRAM

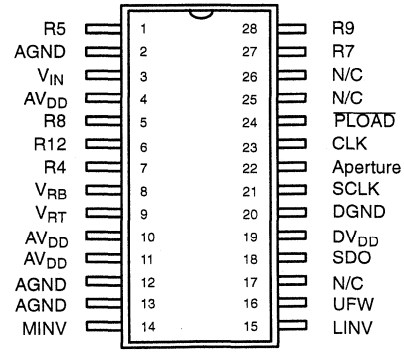


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28



28 Pin SOIC (EIAJ 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	R5	Ref. Resistor Ladder Tap (5/16 V_{REF})
2	AGND	Analog Ground
3	V_{IN}	Analog Input
4	AV_{DD}	Analog Positive Supply
5	R8	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R12	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R4	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{RB}	Negative Reference
9	V_{RT}	Positive Reference
10	AV_{DD}	Analog Positive Supply
11	AV_{DD}	Analog Positive Supply
12	AGND	Analog Ground
13	AGND	Analog Ground
14	MINV	Invert MSB (Active High)
15	LINV	Invert LSB (Active High)
16	UFW	Underflow Bit
17	N/C	No Connection
18	SDO	Serial Data Out
19	DV_{DD}	Digital Positive Supply
20	DGND	Digital Ground
21	SCLK	Serial Clock
22	Aperture	Aperture Delay Sync
23	CLK	Clock
24	$\overline{PLOAD}$	Serial Shift Register Data Load
25	N/C	No Connection
26	N/C	No Connection
27	R7	Ref. Resistor Ladder Tap (7/16 V_{REF})
28	R9	Ref. Resistor Ladder Tap (9/16 V_{REF})

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 3 V, FS = 500 kHz (50% Duty Cycle), V_{RT} = 3.0 V, V_{RB} = AGND, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		12			Bits	
Sampling Rate	FS			1	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±3	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$	1.5		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Bandwidth (–3 dB)[4]	BW		5		MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		30		ns	
Aperture Delay from Aperture Signal	t_{AP}		0		ns	Aperture pin load 5 pF Measured at 50% point
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OET}$, OE2, MINV, LINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	1000			ns	
Rise & Fall Time[7]	t_R, t_F		15		ns	
"High" Time	t_{PWH}	500			ns	
"Low" Time	t_{PWL}	500			ns	
Duty Cycle			50		%	
Serial Register Timing						
Shift Clock Period	t_{SC}	80	50		ns	
Shift Clock to Data Delay	t_{SD}		30		ns	
Minimum Pulse Width $\overline{PLOAD}$	t_S		50		ns	
Clock↑ to $\overline{PLOAD}$↓ For Valid D11	t_{CP}		0		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
Tristate Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		100		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
POWER SUPPLIES[8] (Tmin to Tmax)						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		8	12	mA	
AC PARAMETERS						
Signal Noise Ratio	SNR		66		dB	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to DV_{DD} and DGND. Input(s) LINV and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

8 AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

5

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 5.5 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

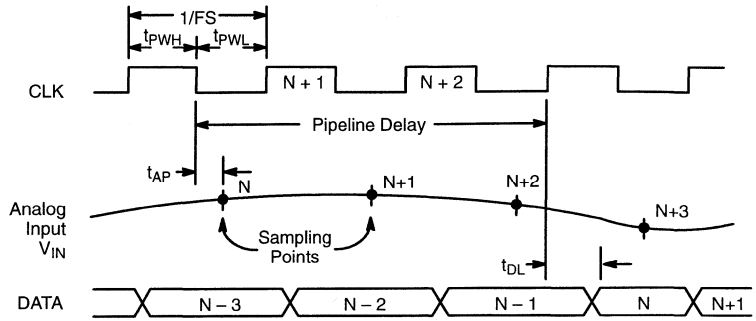
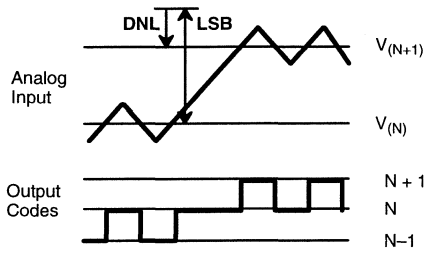


Figure 1. MP87L92 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 1024

$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$

Figure 2. DNL Measurement

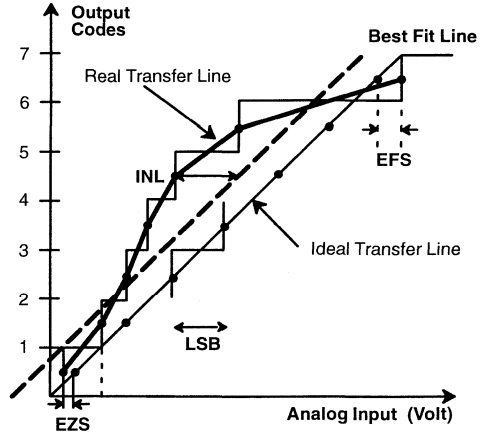


Figure 3. INL Error Calculation

UFW: Underflow (Output)

This signal indicates when the Analog Input (V_{IN}) goes outside the V_{RB} range, and is normally at a low logic level. When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0's if MINV & LINV are low).

SDO: Serial Data Output

After the internal shift register is updated using the $\overline{\text{PLOAD}}$ signal, the SDO pin outputs the A/D result starting with the MSB (which appears just after the $\overline{\text{PLOAD}}$ strobe). Each bit is output on the rising edge of SCLK.

SCLK: Serial Data Port Clock

The SCLK controls the output of the serial port through SDO. SDO is updated on every rising edge of SCLK. The $\overline{\text{PLOAD}}$ signal will override the SCLK signal.

$\overline{\text{PLOAD}}$

Serial data port shift register load: When $\overline{\text{PLOAD}}$ is low (i.e. level triggered not edge triggered), the current parallel data will be loaded into the shift register. $\overline{\text{PLOAD}}$ overrides SCLK. When $\overline{\text{PLOAD}}$ is high, the data can be shifted out through the SDO pin with SCLK.

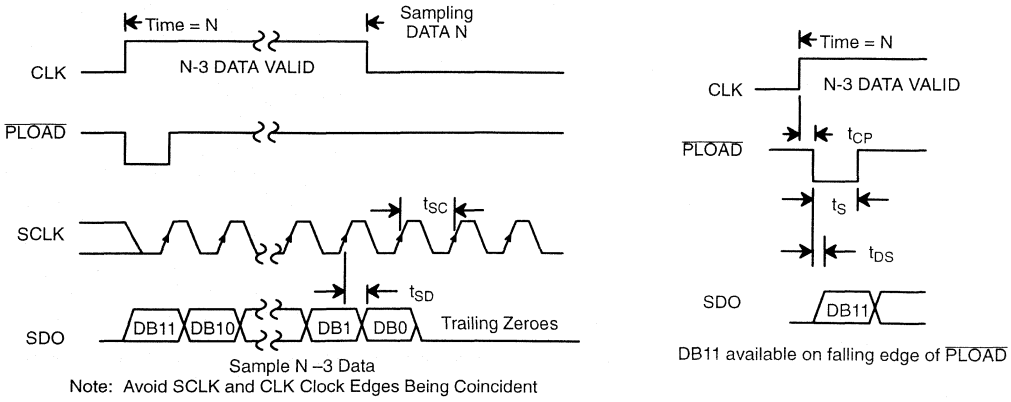


Figure 4. Serial Port Timing Chart
PHASE = 1

APERTURE: Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event.

5

MINV LINV	0 0	0 1	1 0	1 1
V_{RT}	111 . . . 11 111 . . . 10	100 . . . 00 100 . . . 01	011 . . . 11 011 . . . 10	000 . . . 00 000 . . . 01
V_{IN} mid scale	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11
	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
V_{RB}	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

MINV & LINV: Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB11. Normally both pins are held low so the data is in straight binary format (all 0's when V_{IN}=V_{RB}; all 1's when V_{IN}=V_{RT}). If MINV is pulled high then the MSB (DB11) will be inverted. If LINV is pulled high then the LSBs (DB0 – DB10) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV & LINV are meant to be static digital signals. If they are to change during operation they should only change when the CLK is low (assuming PHASE is high; if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV and LINV have internal pull down devices. Please see the simplified logic circuit *(Figure 5.)*

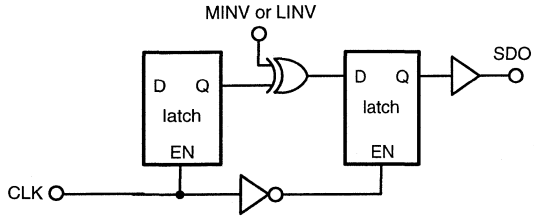


Figure 5. MINV, LINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *(Figure 6.)* shows an equivalent input circuit.

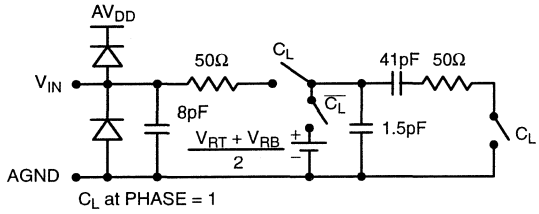


Figure 6. Equivalent Input Circuit

Reference Ladder Taps

These taps connect to every sixteenth point along the reference ladder; R4 is 4/16th up from V_{RB}, R7 is 7/16ths up from V_{RB}. Normally R4, R8 and R12 should have 0.1 microfarad capacitors to GND; this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. The internal interconnect resistance from the pin to the ladder is less than 3Ω for the even numbered taps, (i.e. R4,R6, etc.) and is approximately 10Ω for the odd numbered taps.

Alternating the transfer curve may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

For Log shapes, the MP8790 is ideal since it provides 16 segments.

0.8 V maximum per tap is recommended for applications above 85°C.

APPLICATION NOTES

V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

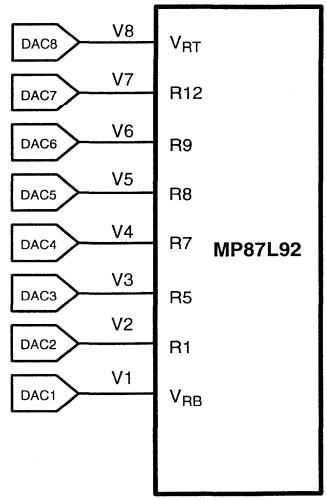
AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

At least three of the reference tap pins (R4, R8, R12) should be decoupled with 0.1µF to 1µF capacitors. This will help stabilize the internal reference voltages thus reducing any INL errors.

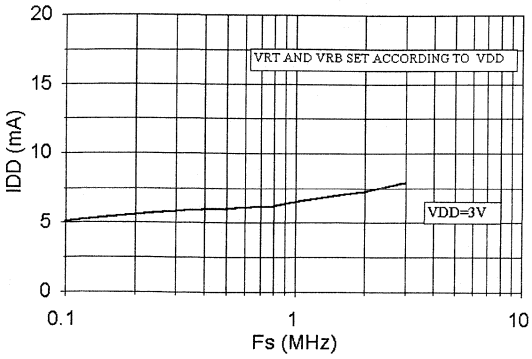
The reference tap pins (R1-R16) can be used to create piecewise linear transfer functions. By forcing custom voltages on these pins, a 16-segment transfer function can be made. See *Figure 7.*



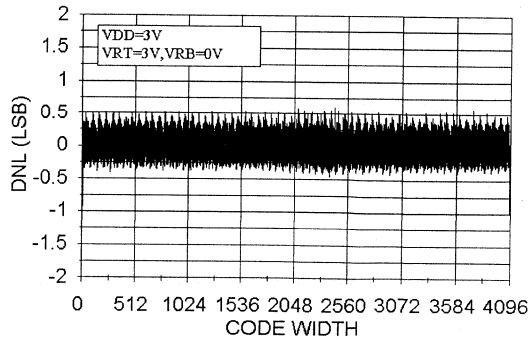
Only the Ladder detail shown.

Figure 7. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. FS



Graph 2. DNL Error Plot

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MP87L95

Low Voltage CMOS
Very Low Power 10-Bit
Analog-to-Digital Converter

FEATURES

- **3.3 V Operation**
- **10-Bit Resolution**
- **Sampling Rates from <1 kHz to 500 kHz**
- **DNL better than 1/2 LSB (typ) up to 250 kHz**
- **Very Low Power CMOS - 5 mW (typ)**
- **Power Down; Lower Consumption – 1 mW (typ)**
- **Interface to any Input Range between GND and V_{DD}**
- **No S/H Required for CCD Signals less than 250 kHz**
- **Latch-Up Free**
- **ESD Protection: 4000 Volts Minimum**

BENEFITS

- **Reliable Operation**
- **Reduced Board Space (Small Package)**
- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer Can Adapt Input Range & Scaling**

APPLICATIONS

- **µP/DSP Interface and Control Applications**
- **High Resolution Imaging – Scanners, Copiers, Facsimile**
- **Multiplexed Data Acquisition**
- **Radar Pulse Analysis**
- **Low Power A/D Applications**

GENERAL DESCRIPTION

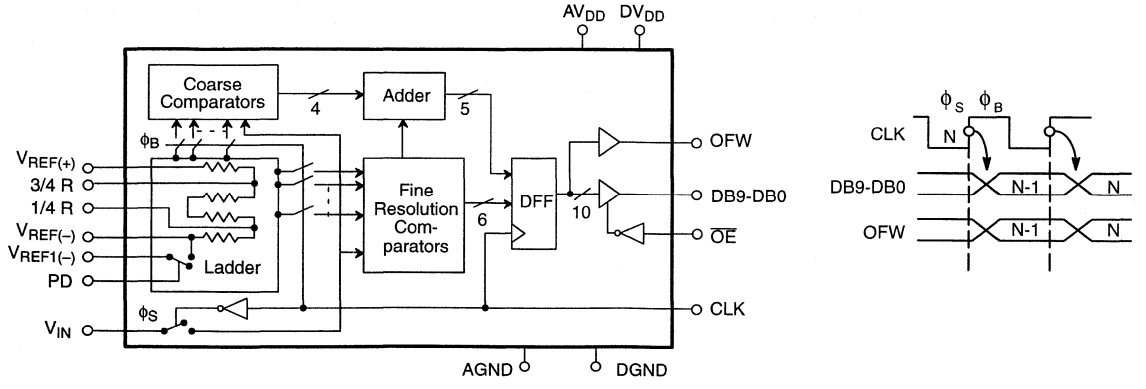
The MP87L95 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter that operates over a wide range of input and sampling conditions. The MP87L95 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 250 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 250 kHz, or multiplexed input applications when the signal source bandwidth is limited to 20 kHz. The input architecture of the MP87L95 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 3 V). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor taps 1/4 R and 3/4 R allow for customizing the transfer curve. Digital outputs offer 3-state operation.

The MP87L95 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 1mW.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

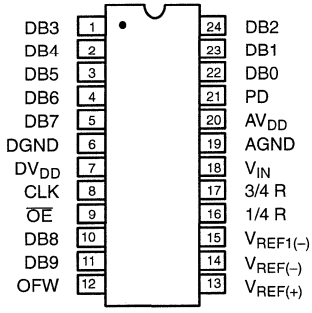


ORDERING INFORMATION

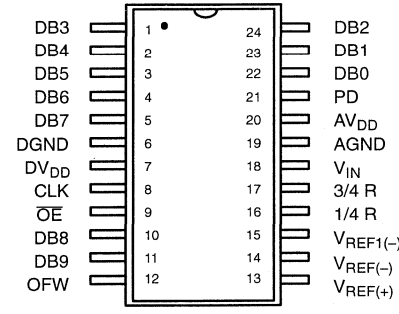
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP87L95AN	1	2
SOIC	–40 to +85°C	MP87L95AS	1	2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(-)}$	Lower Reference Voltage
15	$V_{REF1(-)}$	Lower Reference Voltage
16	1/4 R	Reference Ladder Tap @ 1/4 FS
17	3/4 R	Reference Ladder Tap @ 3/4 FS
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	PD	Power Down
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3$ V, $F_S =$ 250 KHz (50% Duty Cycle), $V_{REF(+)} = 2.6$, $V_{REF(-)} = AGND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S			0.25	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL			±1	LSB	Best Fit Line (Max INL – Min INL)/2
Integral Non-Linearity	INL			±2	LSB	
Zero Scale Error	EZS		+1.00		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance[1]			12		Ω	
Ladder Switch Off Leakage	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		60	70	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, $\overline{OE}$ (Internal Res to DGND		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	4			µs	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	2		1000	µs	
"Low" Time[6]	t_S	2		1000	µs	Functional
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	V_{DD}-0.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}			±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		50	60	ns	
Data Valid Delay[1]	t_{DL}		60	70	ns	

5

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C_{OUT}=15 pF
Data Enable Delay[1]	t_{DEN}		35	40	ns	
Data 3-state Delay[1]	t_{DHZ}		30	40	ns	
Clock to PD Set-up Time	t_{CLKS1}			400	ns	
Clock to PD Hold Time	t_{CLKH1}			600	ns	
Power Down Delay	t_{PD}			300	ns	
Power Up Delay	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{DDOWN}		0.3	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			3	mA	V_{IN} = 2 V

NOTES:
1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 5.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP87L95 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +5.5 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

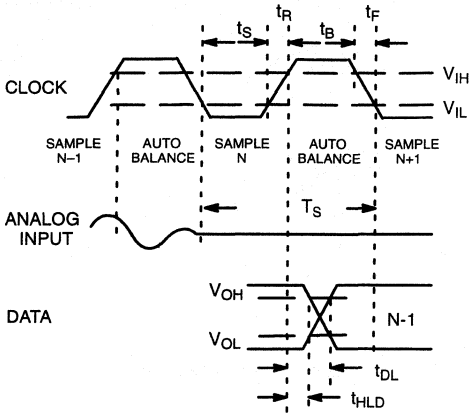


Figure 1. MP87L95 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87L95 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

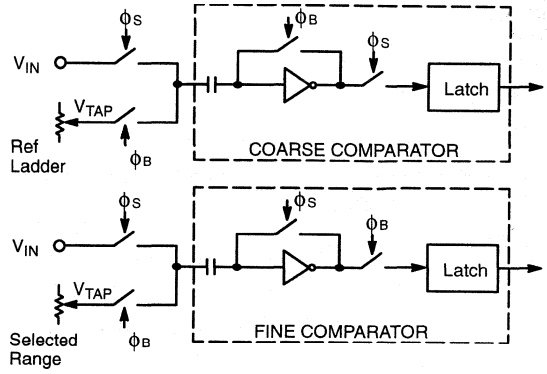


Figure 2. MP87L95 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

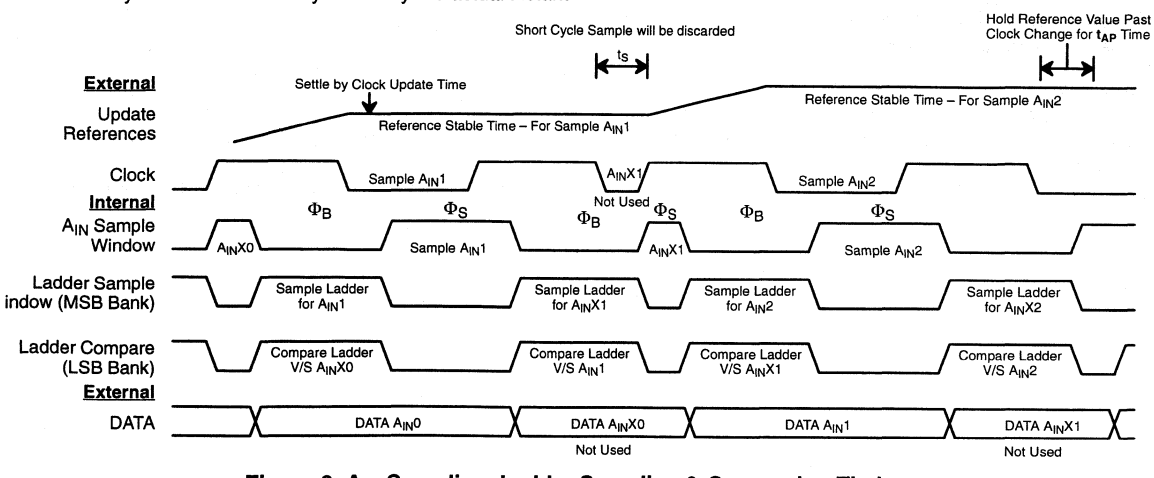


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

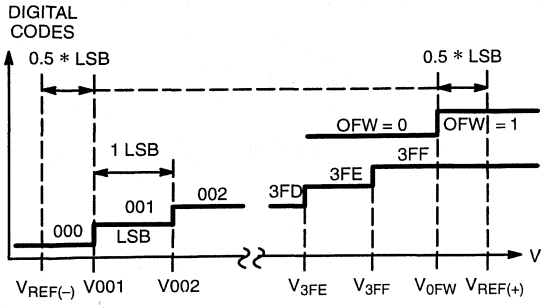


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(-)} - 1.5 * LSB$

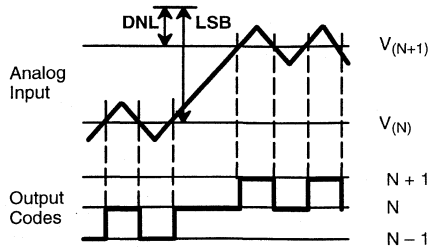
$LSB = V_{REF} / 1024 = (V_{3FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

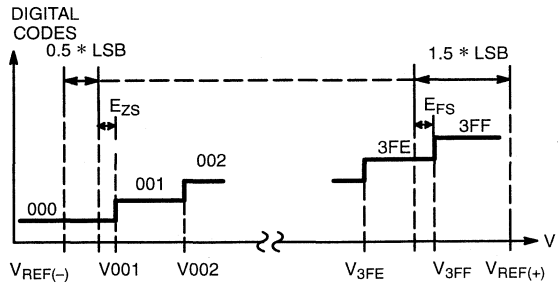


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSBs relative to the Ideal Line would be ±1.5 LSB's relative to the best fit line.

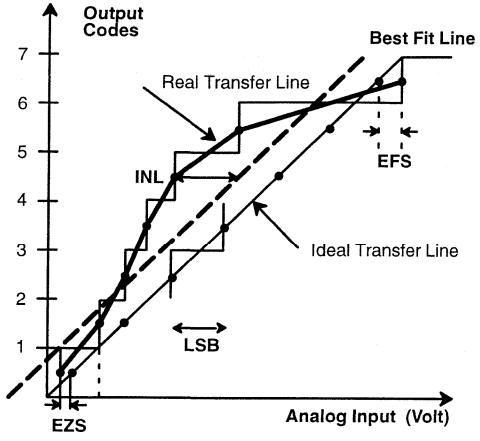


Figure 7. INL Error Calculation

Clock and Conversion Timing

A system will clock the MP87L95 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87L95 in balance and ready to sample the analog input.

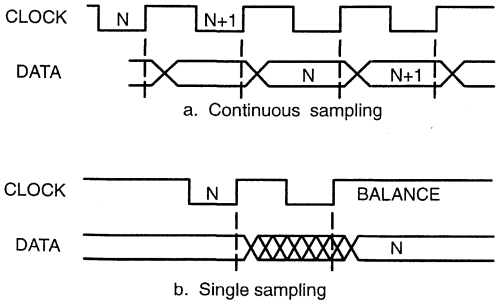


Figure 8. Relationship of Data to Clock

Analog Input

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87L95's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

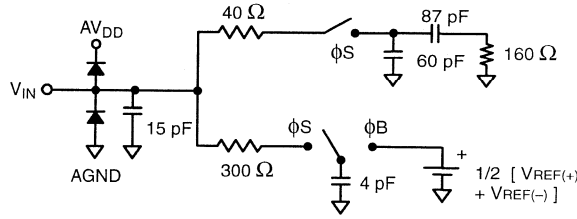


Figure 9. Analog Input Equivalent Circuit

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE}$ controls the output buffers in an asynchronous mode.

$\overline{OE}$	OFW	DB9 – DB0
1	Valid	High Z
0	Valid	Valid

Table 1. Output Enable Logic

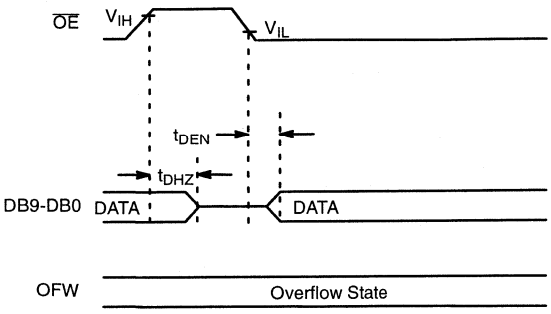


Figure 10. Output Enable/Disable Timing Diagram

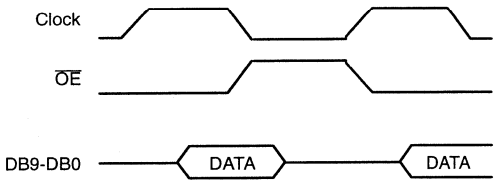


Figure 11. Preferred Output Control

Figure 11. shows the preferred output control where $\overline{OE}$ and clock are opposite phase. This provides a quiet time at the end of the A_{IN} sample phase.

The functional equivalent of the MP87L95 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

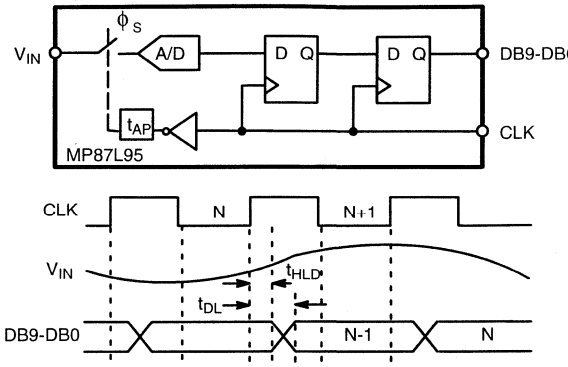


Figure 12. MP87L95 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

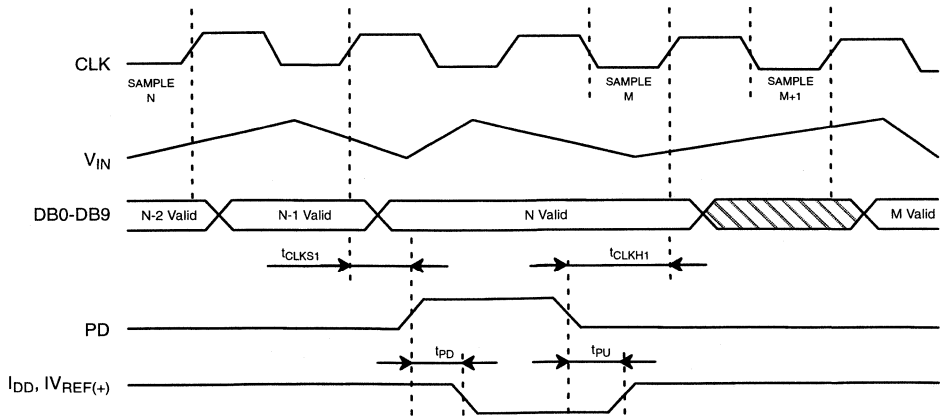


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance cap
R_T = Clock Transmission Line Termination

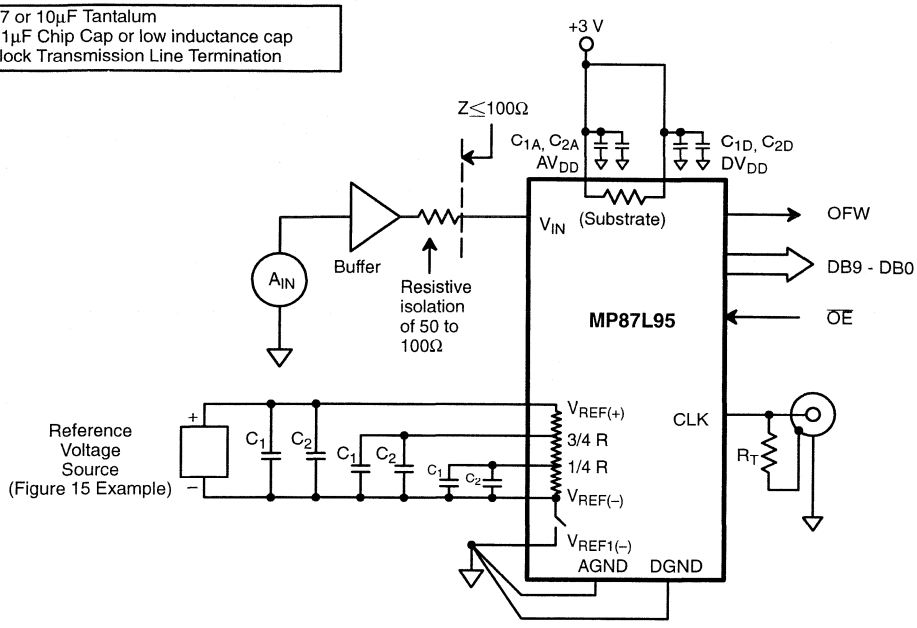


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87L95.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP87L95 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87L95. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87L95.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87L95 should be connected to AV_{DD} next to the MP87L95.
8. DV_{DD} and AV_{DD} are connected inside the MP87L95 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

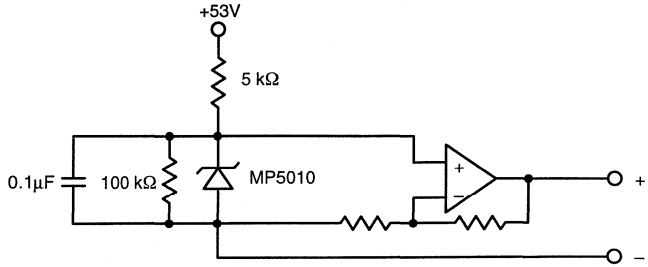
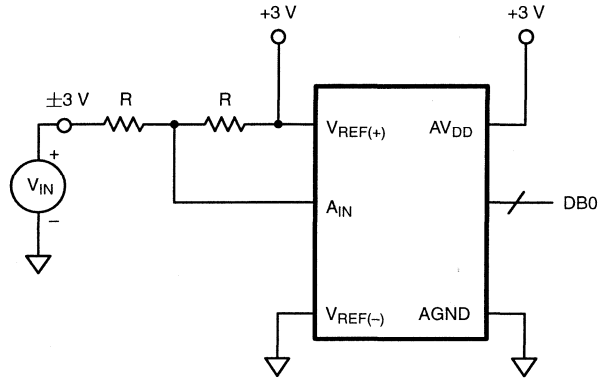


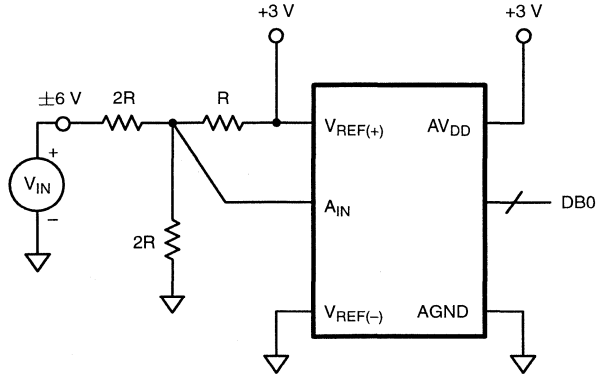
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

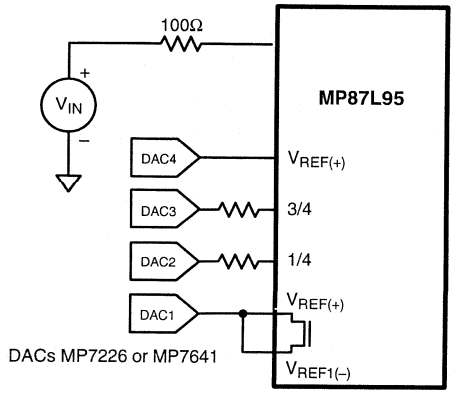
Figure 16. ±3 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 17. ±6 V Analog Input

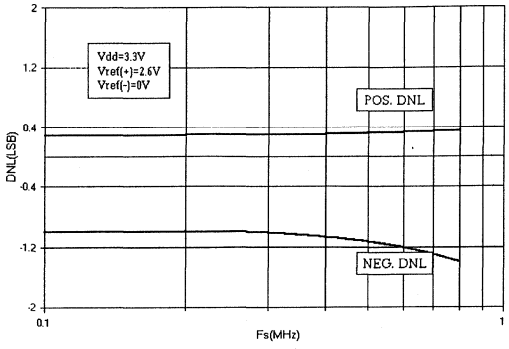


@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

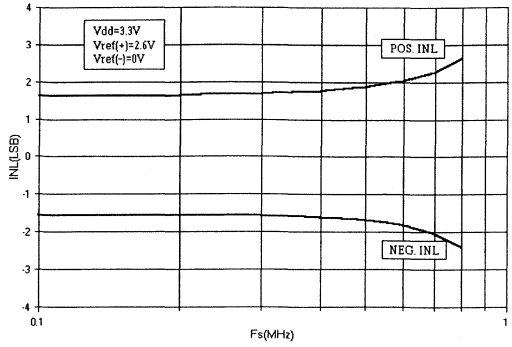
Figure 18. A/D Ladder with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/4 and 3/4 TAP.)

5

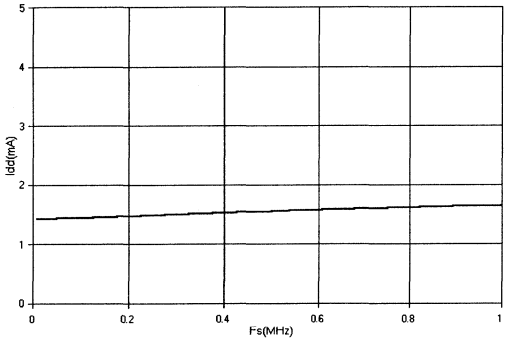
PERFORMANCE CHARACTERISTICS



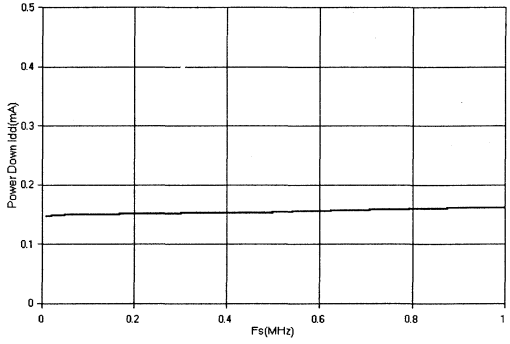
Graph 1. DNL vs. Sampling Frequency



Graph 2. INL vs. Sampling Frequency



Graph 3. Supply Current vs. Sampling Frequency



Graph 4. Power Down Current vs. Sampling Frequency

MP87L98

Low Voltage CMOS
Very Low Power 10-Bit, Analog-to-Digital
Converter with 4-Channel Mux

FEATURES

- 3.3 V Operation
- 10-Bit Resolution
- Sampling Rates from <1 kHz to 500 kHz
- DNL better than 1/2 LSB (typ) up to 250 kHz
- Very Low Power CMOS - 5 mW (typ)
- Power Down; Lower Consumption – 1 mW (typ)
- Interface to any Input Range between GND and V_{DD}
- 4-Channel Mux
- No S/H Required for CCD Signals less than 250 kHz
- Latch-Up Free
- ESD Protection: 4000 Volts Minimum

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- High Resolution Imaging – Scanners, Copiers, Facsimile
- Multiplexed Data Acquisition
- Radar Pulse Analysis

GENERAL DESCRIPTION

The MP87L98 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with 4-channel mux that operates over a wide range of input and sampling conditions. The MP87L98 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 250 kHz. The elimination of the S/H, requirements, very low power, and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 250 kHz, or multiplexed input applications when the signal source bandwidth is limited to 25 kHz. The input architecture of the MP87L98 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 3 V etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap at 1/2 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage.

The MP87L98 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 1mW.

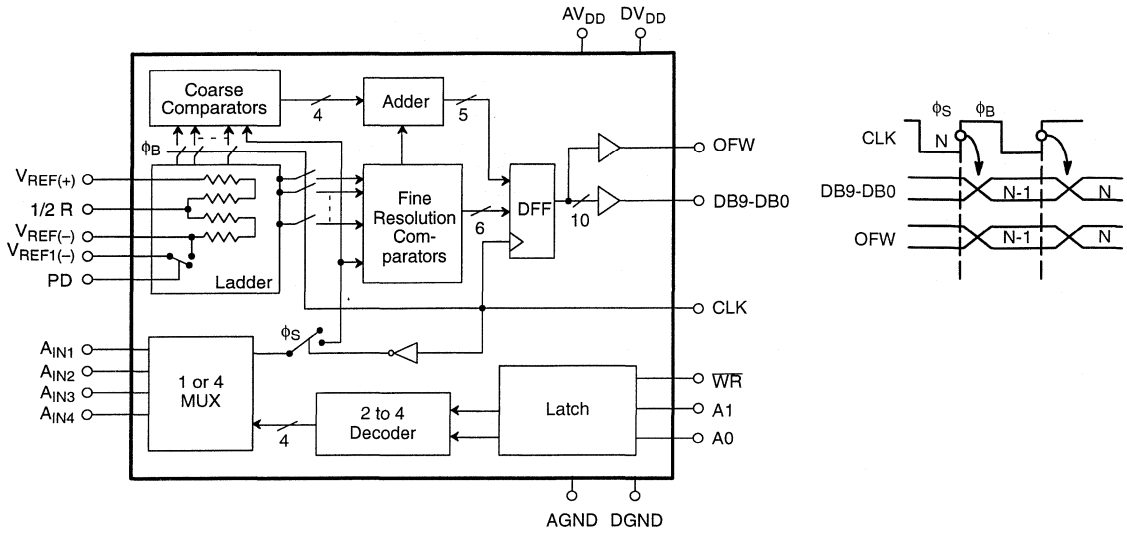
Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP87L98 is available in Plastic Dual-in-Line (PDIP), Surface Mount (SOIC), and Shrunk Small Outline (SSOP) packages.

5

ORDERING INFORMATION

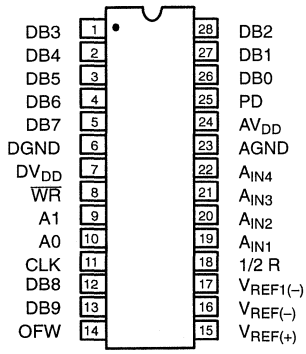
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP87L98AS	±1	2
PDIP	–40 to +85°C	MP87L98AN	±1	2
SSOP	–40 to +85°C	MP87L98AQ	±1	2

SIMPLIFIED BLOCK AND TIMING DIAGRAM

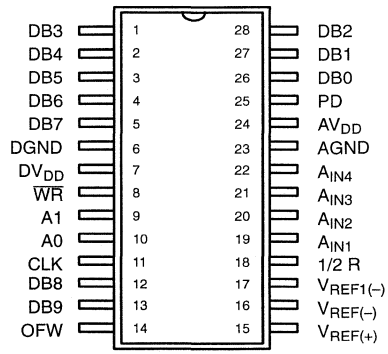


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (Jedec, 0.300") – S28
28 Pin SSOP – A28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	$\overline{WR}$	Write (Active Low)
9	A1	Address 1 Input
10	A0	Address 0 Input
11	CLK	Clock Input
12	DB8	Data Output Bit 8
13	DB9	Data Output Bit 9 (MSB)
14	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
15	$V_{REF(+)}$	Upper Reference Voltage
16	$V_{REF(-)}$	Lower Reference Voltage
17	$V_{REF1(-)}$	Lower Reference Voltage
18	1/2 R	Reference Ladder Tap
19	A_{IN1}	Analog Signal Input 1
20	A_{IN2}	Analog Signal Input 2
21	A_{IN3}	Analog Signal Input 3
22	A_{IN4}	Analog Signal Input 4
23	AGND	Analog Ground
24	AV_{DD}	Analog V_{DD}
25	PD	Power Down
26	DB0	Data Output Bit 0 (LSB)
27	DB1	Data Output Bit 1
28	DB2	Data Output Bit 2

TRUTH TABLE FOR INPUT CHANNEL SELECTION

$\overline{WR}$	A1	A0	SELECTED ANALOG INPUT
0	0	0	A_{IN1}
0	0	1	A_{IN2}
0	1	0	A_{IN3}
0	1	1	A_{IN4}
1	X	X	Previous selection

Note: $\overline{WR}$, A1, A0 are internally connected to GND through 500kΩ resistance.

5

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3$ V, $F_S =$ 250 kHz (50% Duty Cycle), $V_{REF(+)} = 2.6$, $V_{REF(-)} =$ AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		0.25	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		1.0		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	ΔV_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance			12		Ω	
Ladder Switch Off Leakage	I_{LKG-SW}		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			25		kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		60	70	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, (Internal Res to GND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	4			µs	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	2		1000	µs	
"Low" Time[6]	t_S	2		1000	µs	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}			±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		50	60	ns	
Data Valid Delay[1]	t_{DL}		60	70	ns	
Write Pulse Width	t_{WR}	40			ns	
Multiplexer Address Setup Time	t_{AS}	80			ns	
Multiplexer Address Hold Time	t_{AH}	0			ns	
Delay from $\overline{WR}$ to Multiplexer Enable	t_{MUXEN1}			80	ns	
Power Down Time	t_{PD}			300	ns	
Power Up Time	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{PD-DD}		0.3		mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			3	mA	V_{IN} = 2 V

NOTES:
1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 5.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP87L98 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

5

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +5.5 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
SOIC, PDIP 1050mW
Derates above 75°C ..... 14mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

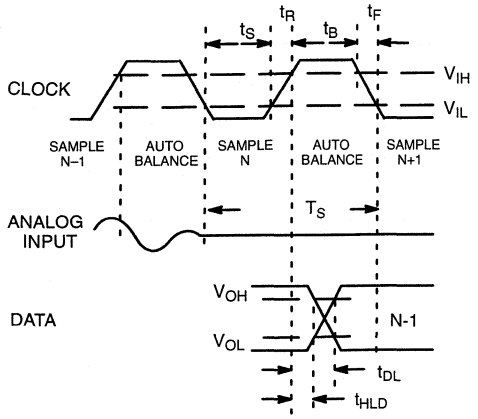


Figure 1. MP87L98 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87L98 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

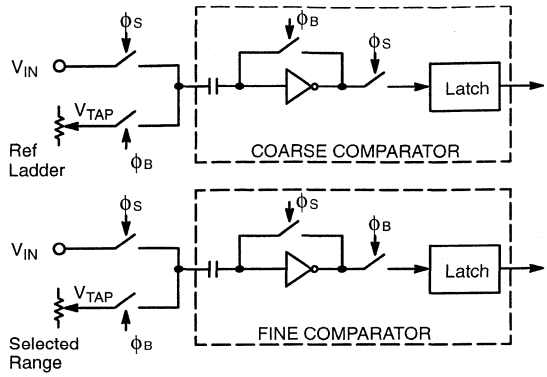


Figure 2. MP87L98 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

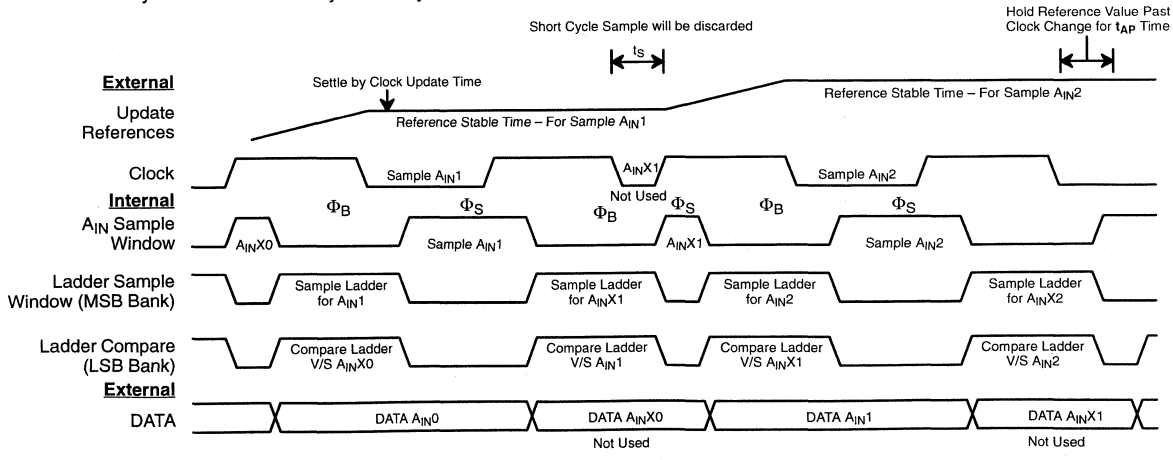


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

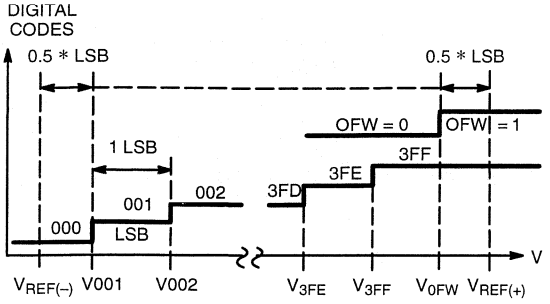


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 1024 = (V_{3FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.

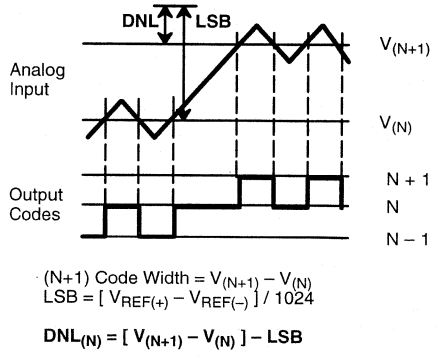


Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

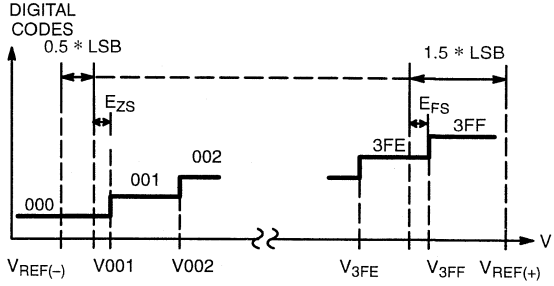


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

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Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the best fit line.

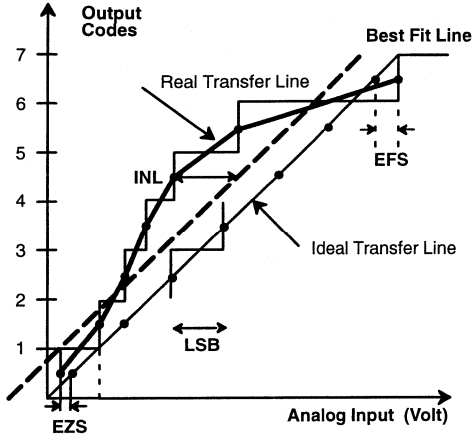

Figure 7. INL Error Calculation

Clock and Conversion Timing

A system will clock the MP87L98 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87L98 in balance and ready to sample the analog input.

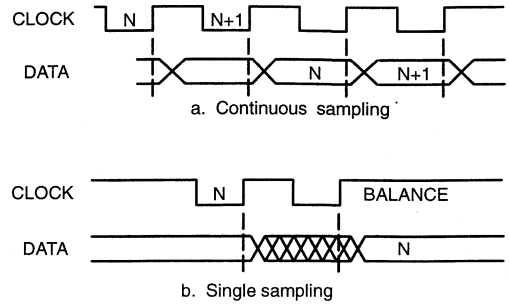

Figure 8. Relationship of Data to Clock

Analog Input

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87L98's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

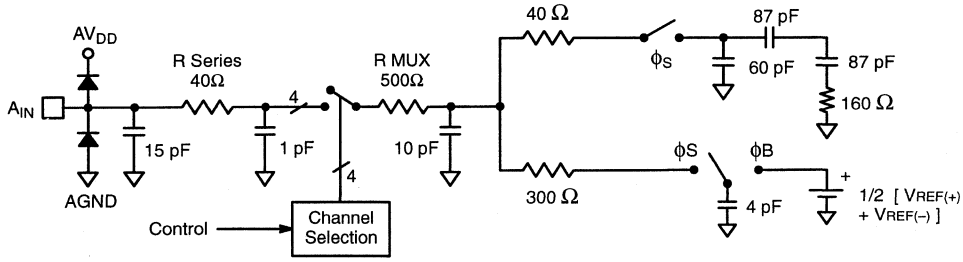

Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP87L98 includes a 4-channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 11.*

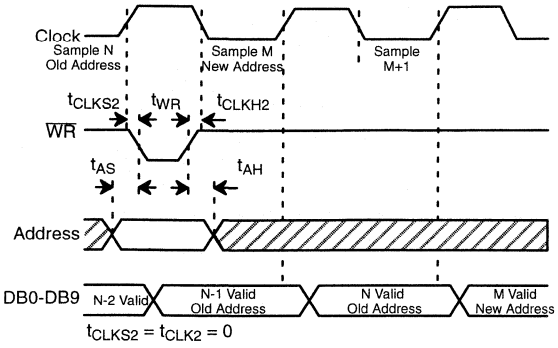

Figure 10. MUX Address Timing

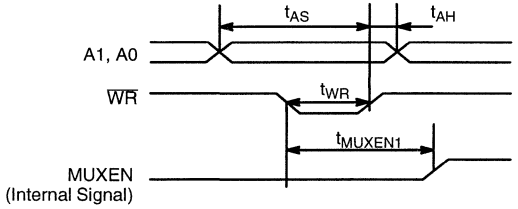

Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP87L98 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

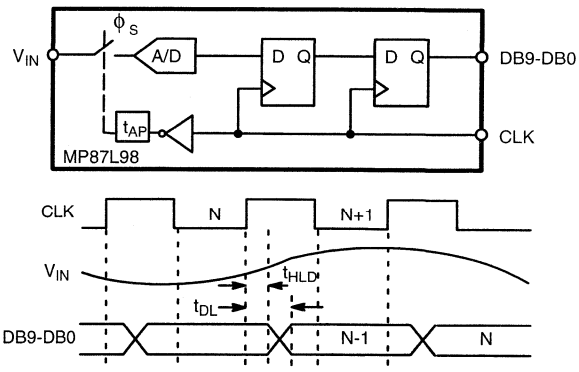

Figure 12. MP87L98 Functional Equivalent Circuit and Interface Timing

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Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

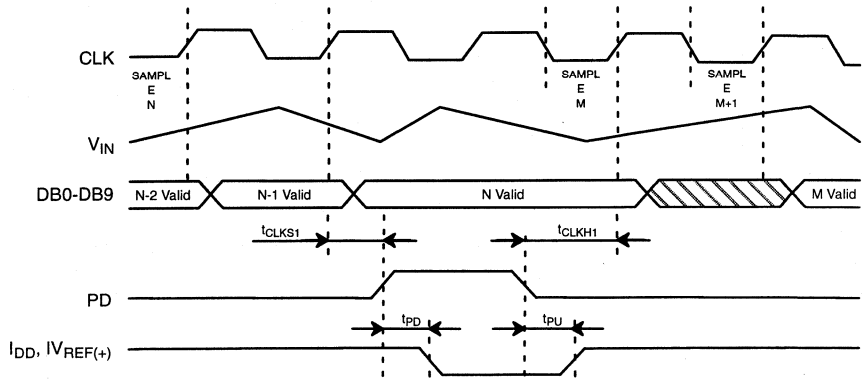


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance capacitor
L_1 = 100nH or larger
R_T = Clock Transmission Line Termination

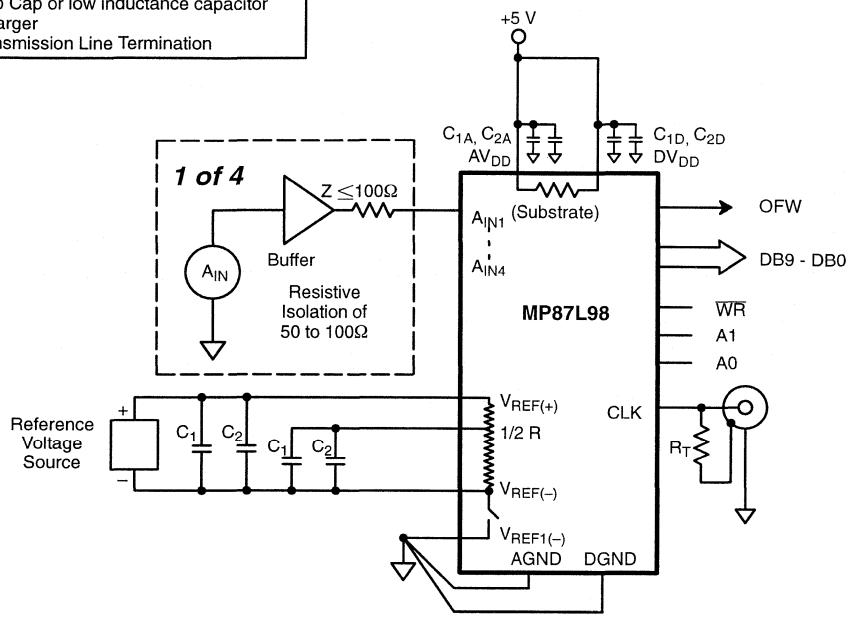


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87L98.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP87L98 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87L98. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87L98.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87L98 should be connected to AV_{DD} next to the MP87L98.
8. DV_{DD} and AV_{DD} are connected inside the MP87L98 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

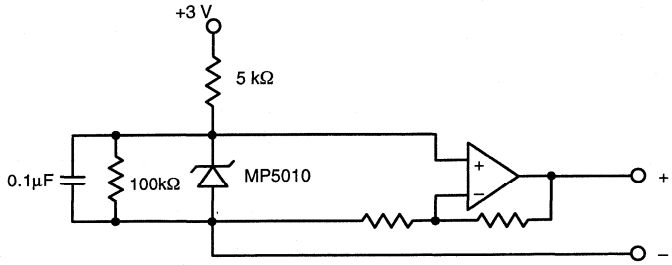
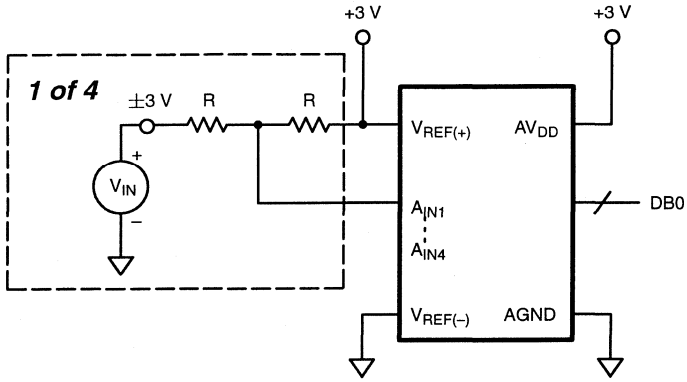


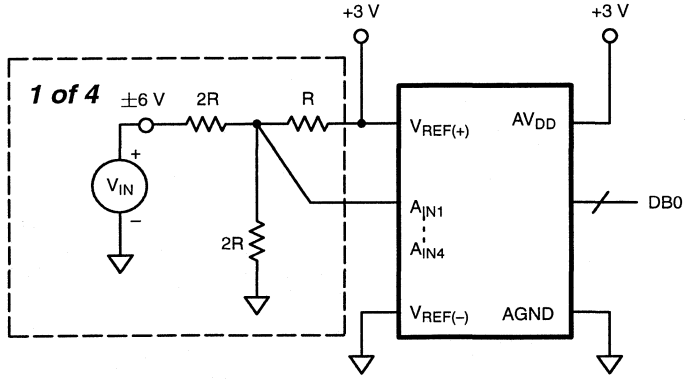
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

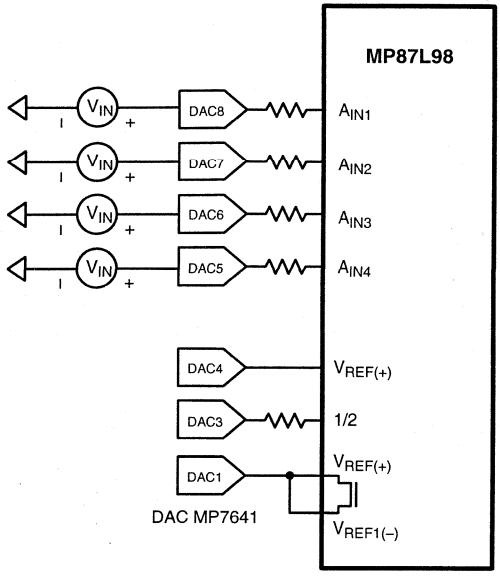
Figure 16. ±3 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the ($R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

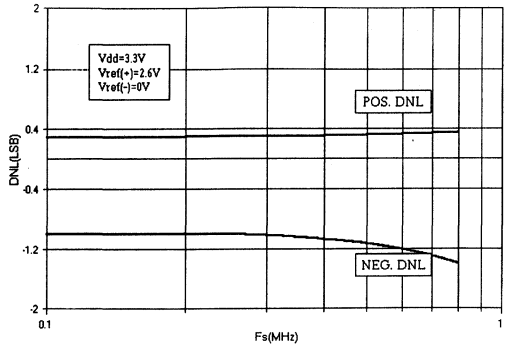
Figure 17. ±6 V Analog Input



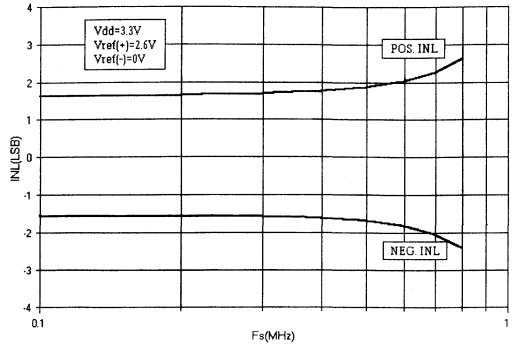
@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder and A_{IN} with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/2 TAP.)

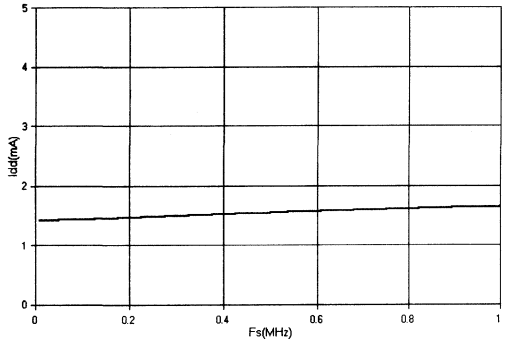
PERFORMANCE CHARACTERISTICS



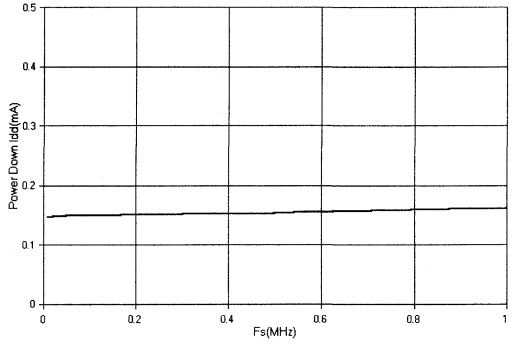
Graph 1. DNL vs. Sampling Frequency



Graph 2. INL vs. Sampling Frequency



Graph 3. Supply Current vs. Sampling Frequency



Graph 4. Power Down Current vs. Sampling Frequency

MP87L99

Low Voltage CMOS Very Low Power 10-Bit, Analog-to-Digital Converter with 8-Channel Mux

FEATURES

- 3.3 V Operation
- 10-Bit Resolution
- Sampling Rates from <1 kHz to 500 kHz
- DNL better than 1/2 LSB (typ) up to 250 kHz
- Very Low Power CMOS - 5 mW (typ)
- Power Down; Lower Consumption – 1 mW (typ)
- Interface to any Input Range between GND and V_{DD}
- 8-Channel Mux
- No S/H Required for CCD Signals less than 250 kHz
- Latch-Up Free
- ESD Protection: 4000 Volts Minimum

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- High Resolution Imaging – Scanners, Copiers, Facsimile
- Multiplexed Data Acquisition
- Radar Pulse Analysis
- Low Power A/D Applications

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GENERAL DESCRIPTION

The MP87L99 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with 8-channel mux that operates over a wide range of input and sampling conditions. The MP87L99 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 250 kHz. The elimination of the S/H, requirements, very low power, and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 250 kHz, or multiplexed input applications when the signal source bandwidth is limited to 25 kHz. The input architecture of the MP87L99 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 3 V.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap at 1/4 R, 1/2 R, and 3/4 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage.

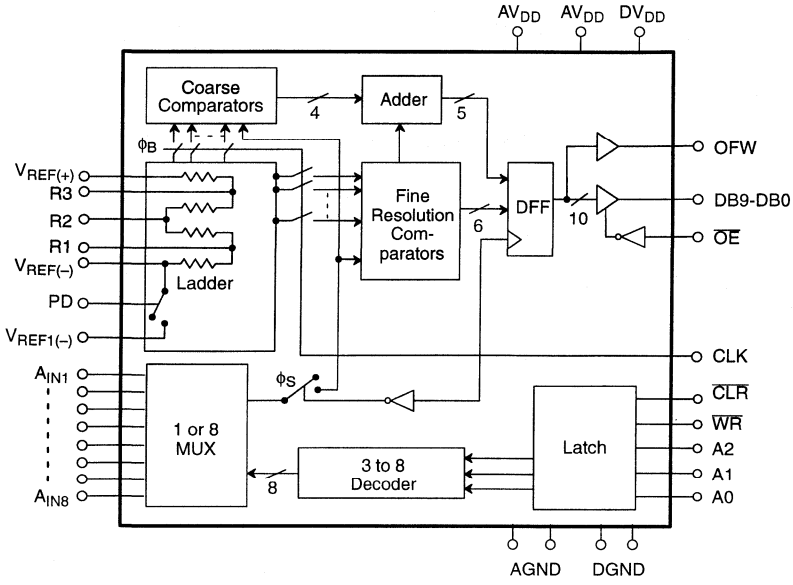
The MP87L99 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

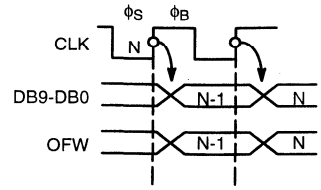
When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 1 mW.

ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP87L99AE	±1	2

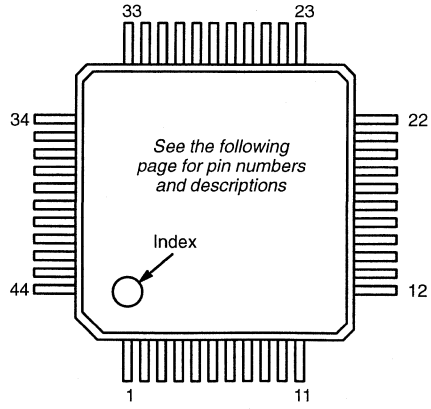
SIMPLIFIED BLOCK AND TIMING DIAGRAM





PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



44-Pin PQFP (10 mm x 10 mm)
QN44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB6	Data Output Bit 6 Output
2	DB7	Data Output Bit 7 Output
3	DGND	Digital Ground
4	DGND	Digital Ground
5	DV_{DD}	Digital V_{DD}
6	$\overline{CLR}$	Clear (Active Low)
7	$\overline{WR}$	Write (Active Low)
8	A2	Address 2
9	A1	Address 1
10	A0	Address 0
11	CLK	Clock Input
12	$\overline{OE}$	Output Enable (Active Low)
13	N/C	No Connect
14	DB8	Data Output Bit 8 Output
15	DB9	Data Output Bit 9 Output (MSB)
16	OFW	Overflow Output
17	$V_{REF(+)}$	Upper Reference Voltage
18	$V_{REF(-)}$	Lower Reference Voltage
19	$V_{REF1(-)}$	Lower Reference Voltage
20	R1	Reference Ladder Tap
21	R2	Reference Ladder Tap
22	A_{IN8}	Analog Signal Input 8

PIN NO.	NAME	DESCRIPTION
23	R3	Reference Ladder Tap
24	N/C	No Connect
25	A_{IN1}	Analog Signal Input 1
26	A_{IN2}	Analog Signal Input 2
27	A_{IN3}	Analog Signal Input 3
28	A_{IN4}	Analog Signal Input 4
29	A_{IN5}	Analog Signal Input 5
30	AGND	Analog Ground
31	AV_{DD}	Analog V_{DD}
32	AV_{DD}	Analog V_{DD}
33	A_{IN6}	Analog Signal Input 6
34	AGND	Analog Ground
35	PD	Power Down
36	A_{IN7}	Analog Signal Input 7
37	DB0	Data Output Bit 0 (LSB)
38	DB1	Data Output Bit 1
39	DB2	Data Output Bit 2
40	DB3	Data Output Bit 3
41	DB4	Data Output Bit 4
42	DB5	Data Output Bit 5
43	N/C	No Connect
44	N/C	No Connect

5

$\overline{CLR}$	$\overline{WR}$	A2	A1	A0	Selected Analog Input
L	X	X	X	X	A_{IN1}
H	L	L	L	L	A_{IN1}
H	L	L	L	H	A_{IN2}
H	L	L	H	L	A_{IN3}
H	L	L	H	H	A_{IN4}
H	L	H	L	L	A_{IN5}
H	L	H	L	H	A_{IN6}
H	L	H	H	L	A_{IN7}
H	L	H	H	H	A_{IN8}
H	H	X	X	X	Previous Selection

Note: $\overline{CLR}$, $\overline{WR}$, A2, A1, A0 are internally connected to ground through 500k Ω resistance.

Table 1. Truth Table For Input Channel Selection

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3$ V, F_S = 250 kHz (50% Duty Cycle), $V_{REF(+)} = 2.6$, $V_{REF(-)}$ = AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S	.001		0.25	MHz	For Rated Performance
ACCURACY (A Grade)[2]						
Differential Non-Linearity	DNL			±1	LSB	LSB
Integral Non-Linearity	INL			2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±1		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance[1]			12		Ω	
Ladder Switch Off Leakage	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Bandwidth			25		kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		60	70	ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, $\overline{OE}$ (Internal Res to GND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	4			µs	
Rise & Fall Time[4]	t_R, t_F			10	ns	
"High" Time[6]	t_B	2		1000	µs	
"Low" Time[6]	t_S	2		1000	µs	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			V	I_{LOAD} = 1 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
Tristate Leakage	I_{OZ}	0		±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		50	60	ns	
Data Valid Delay[1]	t_{DL}		60	70	ns	
Write Pulse Width[1]	t_{WR}	40			ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C_{OUT}=15 pF
Multiplexer Address Setup Time[1]	t_{AS}	80			ns	
Multiplexer Address Hold Time[1]	t_{AS}	0			ns	
Delay from $\overline{WR}$ to Multiplexer[1] Enable	t_{MUXEN1}			80	ns	
Power Down Time[1]	t_{PD}			300	ns	
Power Up Time[1]	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{PD-DD}		0.3		mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			3	mA	V_{IN} = 2 V

NOTES:
1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 5.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP87L99 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

5

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +5.5 V
$V_{REF(+)}$, $V_{REF(-)}$, $V_{REF1(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
All A_{INs} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PQFP 650mW
Derates above 75°C ..... 9mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

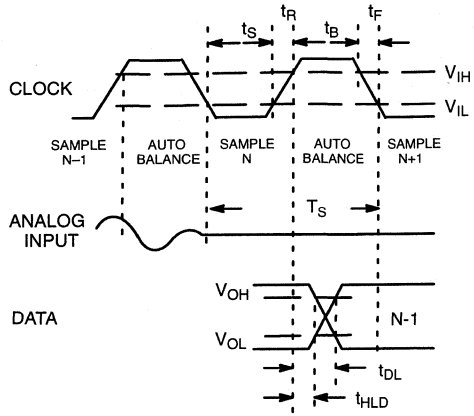


Figure 1. MP87L99 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87L99 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R$ $V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

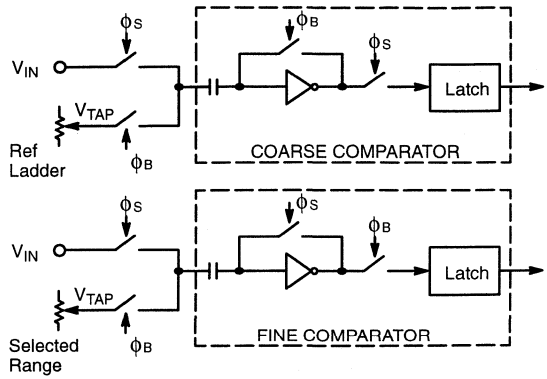


Figure 2. MP87L99 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

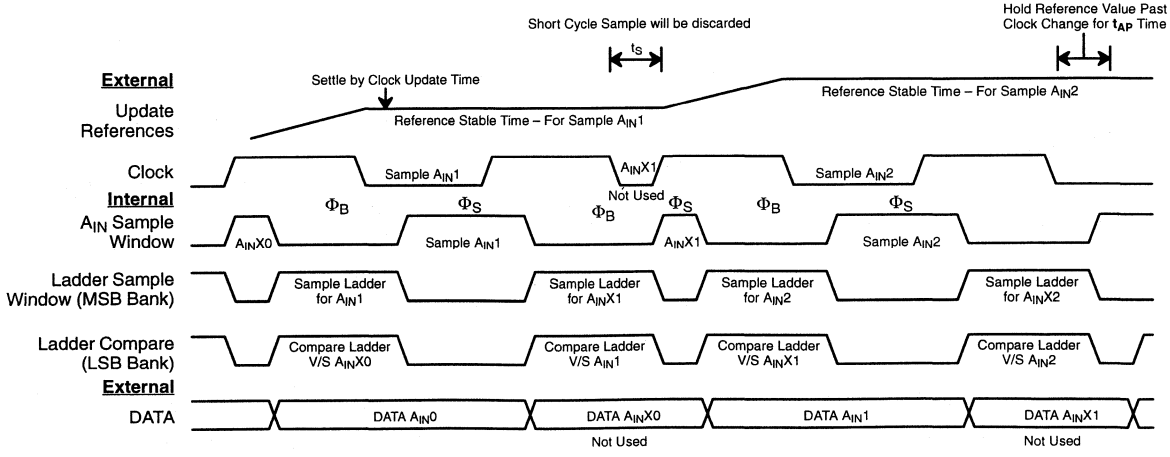


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

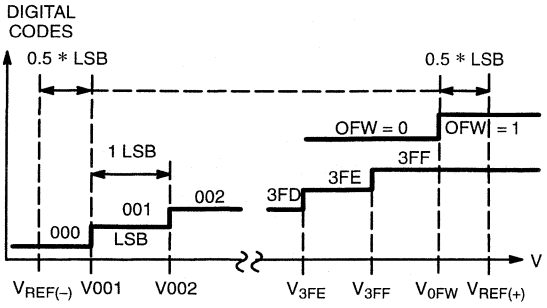


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(+)} - 1.5 * LSB$

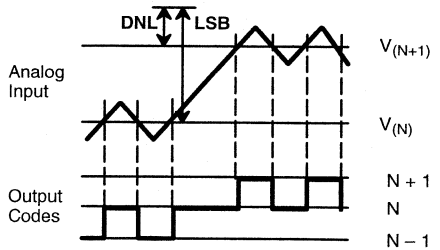
$LSB = V_{REF} / 1024 = (V_{3FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V, then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} - V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

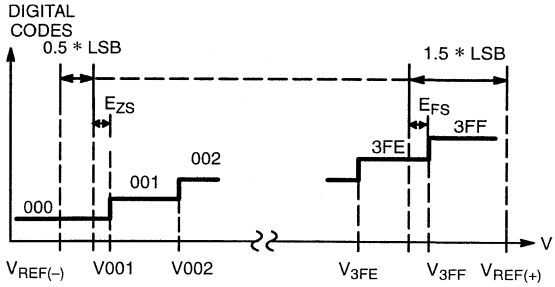


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the best fit line.

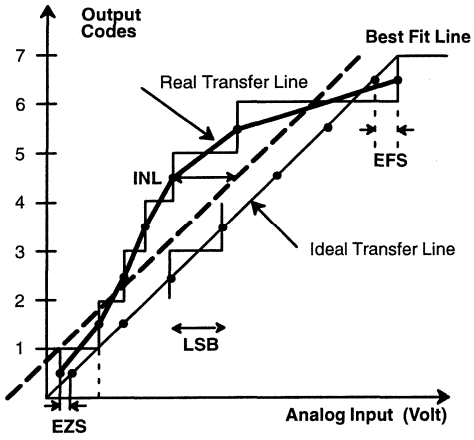


Figure 7. INL Error Calculation

Clock and Conversion Timing

A system will clock the MP87L99 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87L99 in balance and ready to sample the analog input.

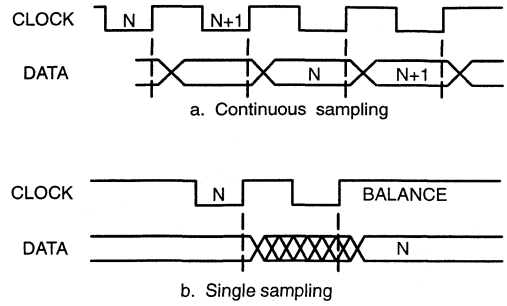


Figure 8. Relationship of Data to Clock

Analog Input

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87L99's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

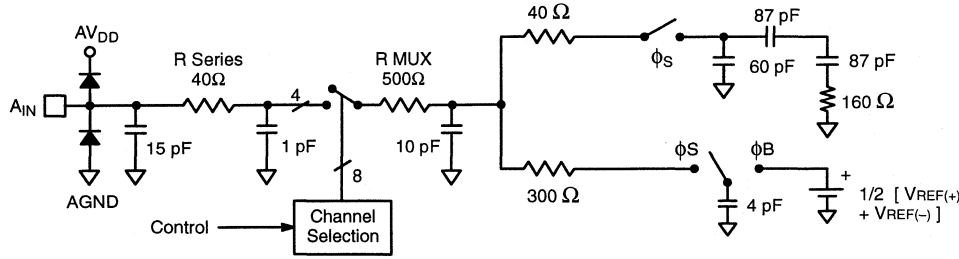


Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP87L99 includes a 8-Channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 11.*

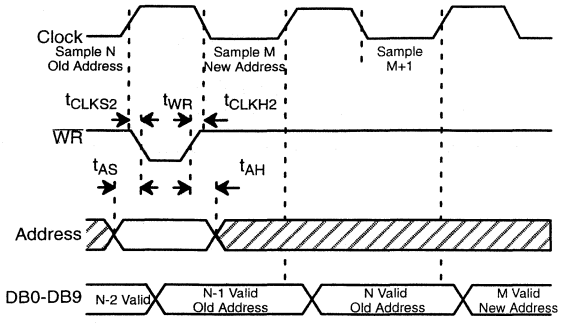


Figure 10. MUX Address Timing

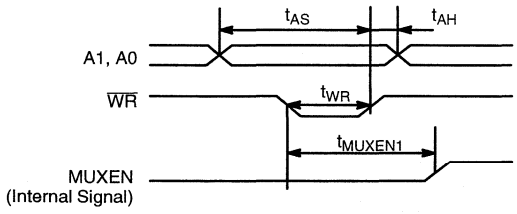


Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP87L99 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

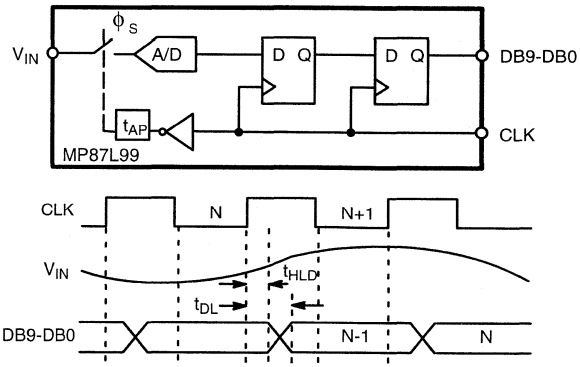


Figure 12. MP87L99 Functional Equivalent Circuit and Interface Timing

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Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

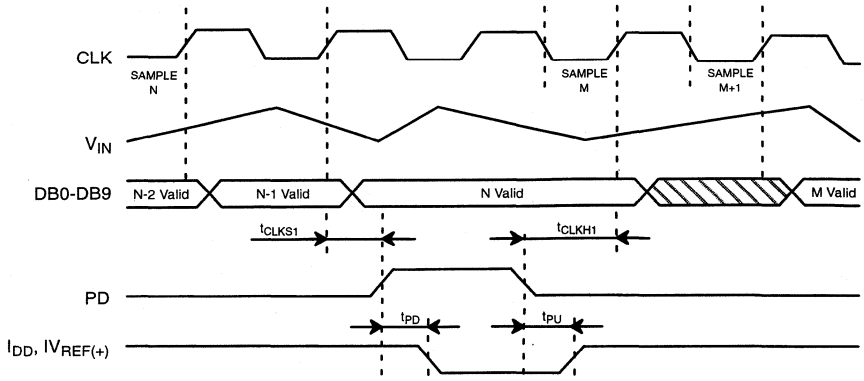


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance cap
R_T = Clock Transmission Line Termination

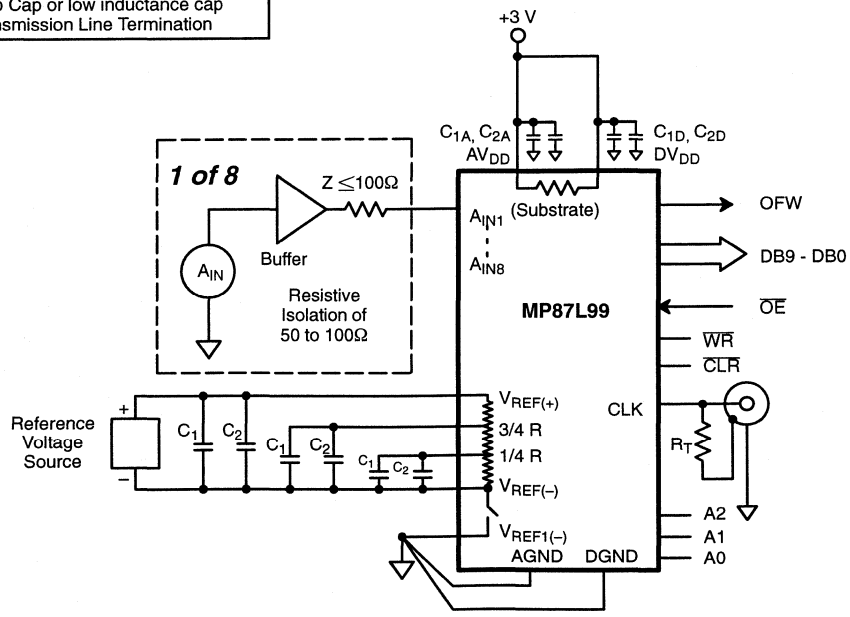


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87L99.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP87L99 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87L99. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87L99.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87L99 should be connected to AV_{DD} next to the MP87L99.
8. DV_{DD} and AV_{DD} are connected inside the MP87L99 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

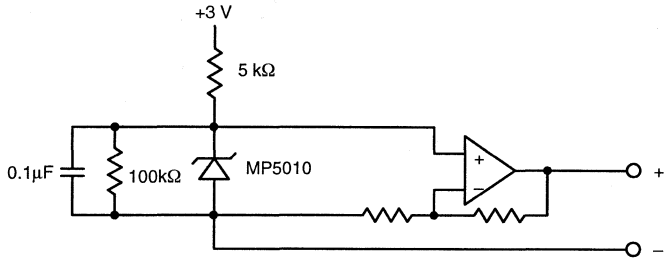
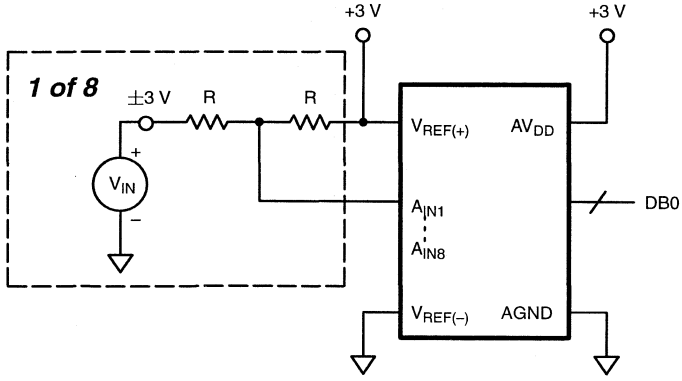


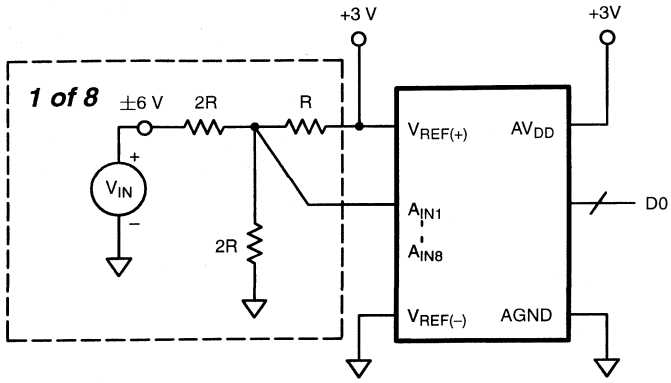
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

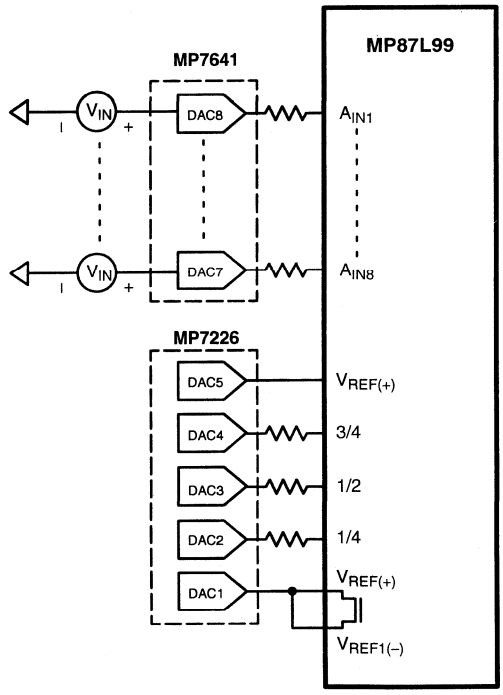
Figure 16. ±3 V Analog Input



For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 17. ±6 V Analog Input

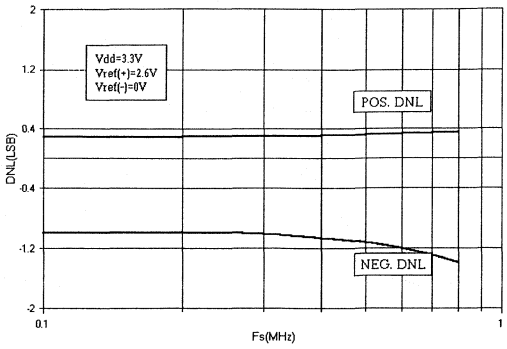


@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.

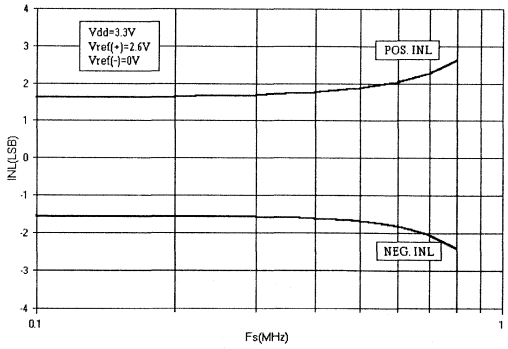
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder and A_{IN} with Programmed Control (of $V_{REF(+)}$, $V_{REF(-)}$, 1/4, 1/2 and 3/4 TAP.)

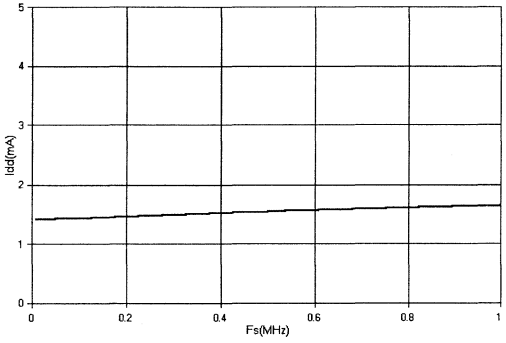
PERFORMANCE CHARACTERISTICS



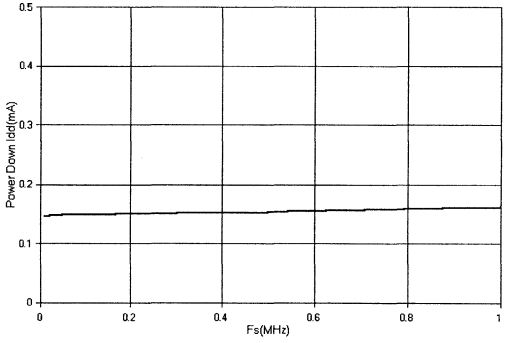
Graph 1. DNL vs. Sampling Frequency



Graph 2. INL vs. Sampling Frequency



Graph 3. Supply Current vs. Sampling Frequency



Graph 4. Power Down Current vs. Sampling Frequency

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Section 6

Voltage References

Listed Alpha-Numerically

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MP5010

Very Low Tempco
1.2 Volt Reference

FEATURES

- **Tested and Guaranteed as low as 5 ppm/°C Max Tempco**
- **Wide Operating Range: 50 μA - 5 mA**
- **Low Output Impedance: 0.6 Ω Typical**

BENEFITS

- **Lower Sensitivity to Capacitive Loading**
- **No Frequency Compensation Required**
- **Accurate Stable Reference over Temp**

APPLICATIONS

- **Building Block for Custom References**
- **Low Current Voltage Reference for Hand Held Multimeters**
- **Voltage Reference for Video Flash Converters**
- **Voltage Reference for D/A and A/D Converters**
- **Precision Analog Control Circuits**

GENERAL DESCRIPTION

The MP5010 is a 2 terminal, band-gap voltage reference which provides a fixed 1.2 V nominal output voltage. The design and process enables us to provide guaranteed tempcos as low as 5 ppm/°C max. We provide this with a wide input current range of 50μA to 5mA, lower sensitivity to load capacitances, and a low output impedance of 0.6Ω (typ).

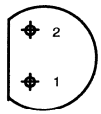
Specified for operation over the commercial (0 to +70°C), industrial (–40 to +85°C), and military (–55 to +125°C) temperature ranges, the MP5010 is available in Plastic TO-92, Metal Can TO-52, and Surface Mount (SOIC) packages.

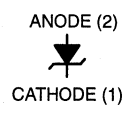
6

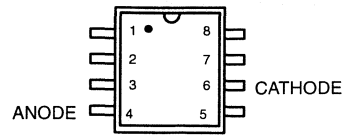
ORDERING INFORMATION

Part No.	Max Tempco	Temperature Range	Package Type
MP5010GN	100	–40 to +85°C	Plastic TO-92
MP5010HN	50	–40 to +85°C	Plastic TO-92
MP5010LN	25	–40 to +85°C	Plastic TO-92
MP5010MN	10	0 to 70°C	Plastic TO-92
MP5010JT	100	–55 to +125°C	TO-52
MP5010KT	50	–55 to +125°C	TO-52
MP5010LT	25	–55 to +125°C	TO-52
MP5010MT	10	–40 to +85°C	TO-52
MP5010NT	5	–40 to +85°C	TO-52
MP5010JR	100	–40 to +85°C	SO-8
MP5010MR	10	–40 to +85°C	SO-8

PIN CONFIGURATIONS







TO-92 PLASTIC **TO-52 (Metal Can)** **8 Lead SOIC (0.150")**

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
Reference Current	I_R	50		5000			µA	
Reference Voltage	V_{REF}	1.200	1.220	1.250			V	I_R = 500µA
Output Impedance[1]	Z_{OUT}		.6	2			Ω	I_R = 500µA
RMS Noise Voltage[1]			5				µV	10Hz ≤ f ≤ 10 kHz, I_R = 500µA
BREAKDOWN VOLTAGE TEMPERATURE COEFFICIENT								
G-S			30	100			ppm/°C	I_R = 500µA
H-K			25	50				Tmin ≤ T_A ≤ Tmax
L			10	25				
M			5	10				
N			3	5				
Reverse Current		50		5000			µA	To rated specs

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

Maximum Temperature
- Storage (JT, KT, LT, MT, NT) ..... –65 to +200°C
- Storage (GN, HN, LN, JR, GR, RR, LR) –65 to +125°C
- Operating Range (JT, KT, LT) ..... –55 to +125°C
- Operating Range (GN, HN, LN, NT, MT, JR, RR, LR) ..... –40 to +85°C
- Operating Range (MN, GR) ..... 0 to 70°C

Lead Temperature (soldering, 10 sec) ..... +260°C

Maximum Power Dissipation (all packages) (2)
- Power Dissipation (25°C) 13mW

Maximum Current
- Forward Current 10mA
- Reverse Current 10mA

NOTES:
1. Guaranteed, not tested.
2. Limited by max forward/reverse current.
3. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

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Section 7

Die Specifications

Listed Alpha-Numerically

Die Specifications

Die Information

EXAR offers a wide variety of standard products in die form. This new section contains a data sheet for each product available in die form, with specific ordering information, electrical specifications, and physical characteristics useful to the end user.

In addition to the layout of the die, the data sheets provide relevant information about die dimensions, pad designation, pad size (defined as the dimensions of the oxide opening), wafer thickness, backside electrical potential and material.

The die are electrically tested in wafer form (*see Figure 1, Process Flow for Plated Die*). The Electrical Parameter and Test Conditions Table describes the electrical tests performed and the guaranteed limits. Each die is tested to those limits at room temperature. No other static or dynamic electrical test is implied or guaranteed. The wafer goes then through the wafer saw process and the good die are plated (loaded in compartmentalized waffle packs) under clean room conditions. Each plated die is inspected for visual defects according to a commercial standard to a 2% LTPD as defined in Appendix D of MIL-I-38535.

Each waffle pack is labeled with the product name, die quantity, and lot number for full identification and traceability. The waffle packs are vacuum packed in antistatic bags before shipment. During the entire flow, the product is processed using strict ESD handling procedures. Wafers and die are packaged in antistatic material and handled only by personnel wearing proper antistatic attire and grounded wrist straps which are checked daily. All work is performed on antistatic work surfaces.

EXAR makes no guarantee on yield after assembly by the user. Packaged device performance depends on proper assembly by the user. Packaged device performance depends on proper assembly procedures, package thermal impedance and selection of materials not under EXAR control.

The die grades included in this section represent EXAR standard products. Please contact the factory for information concerning non-standard die requirements.

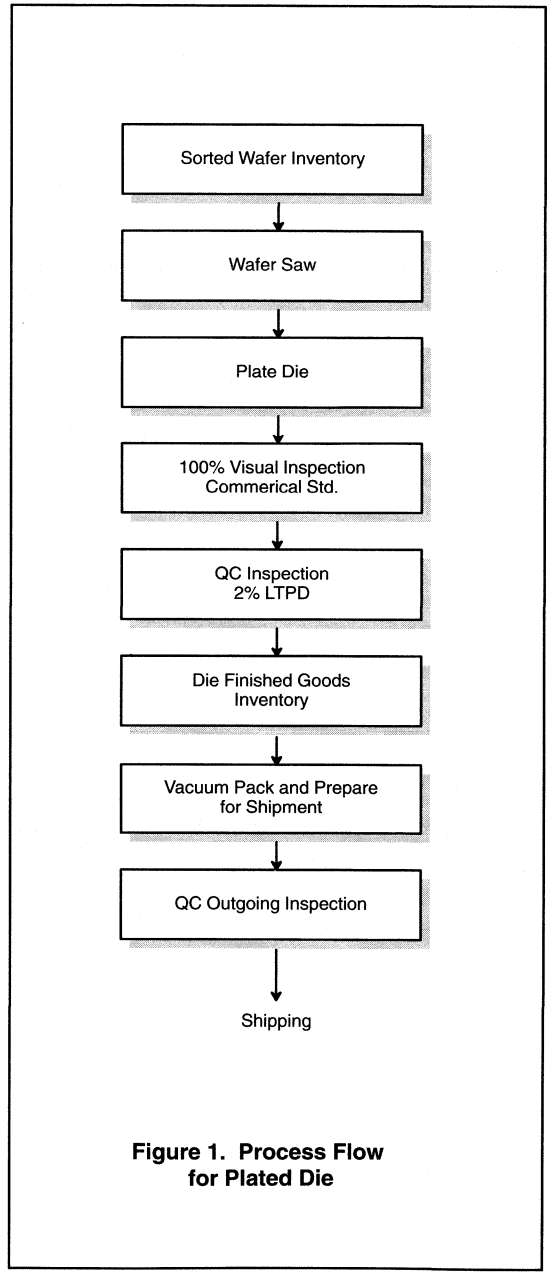


Figure 1. Process Flow for Plated Die

MP1208/09 DIE

12-Bit, Microprocessor Compatible
Double-Buffered Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... −0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. −0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

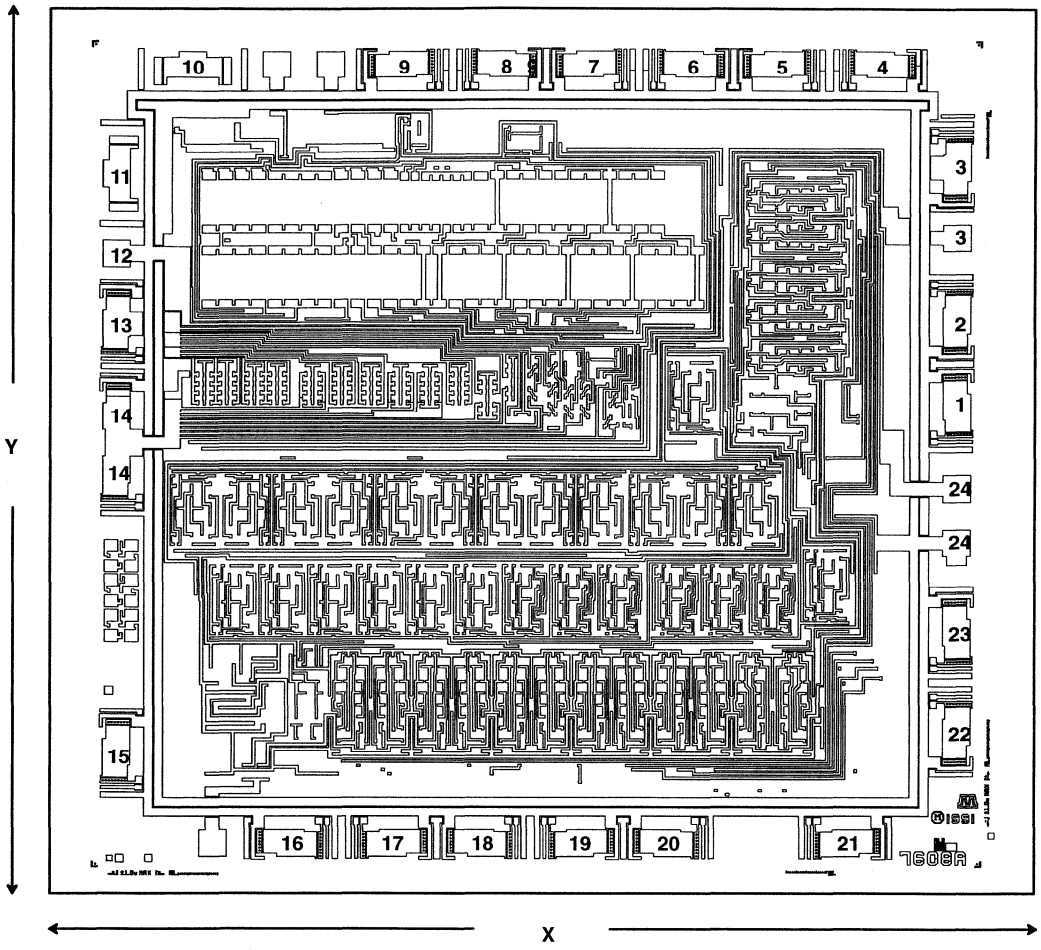
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP1208K-DIE	0.5	1.0	16.0
MP1209J-DIE	1.0	1.0	16.0

Electrical Parameters And Test Conditions (T_A = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		0.5	LSB	Best Straight Line
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		16.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		20	ppm / %	
I_{OUT}	Output Leakage Current		10.0	nA	
R_{IN}	Input Resistance	5	20	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.0	mA	V_{IN} = 0, 15 V

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 129 mils, Y = 136 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. $\overline{CS}$
2. $\overline{WR1}$
3. AGND
4. DB5
5. DB4
6. DB3
7. DB2
8. DB1
9. DB0 (LSB)
10. V_{REF}
11. R_{FB}
12. DGND
13. I_{OUT1}
14. I_{OUT2}
15. DB11 (MSB)
16. DB10
17. DB9
18. DB8
19. DB7
20. DB6
21. $\overline{XFER}$
22. $\overline{WR2}$
23. BYTE 1/$\overline{BYTE\ 2}$
24. V_{DD}*

*Connect pin 24 first

MP1230A/31A DIE

12-Bit Microprocessor Compatible
Double-Buffered Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... –0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

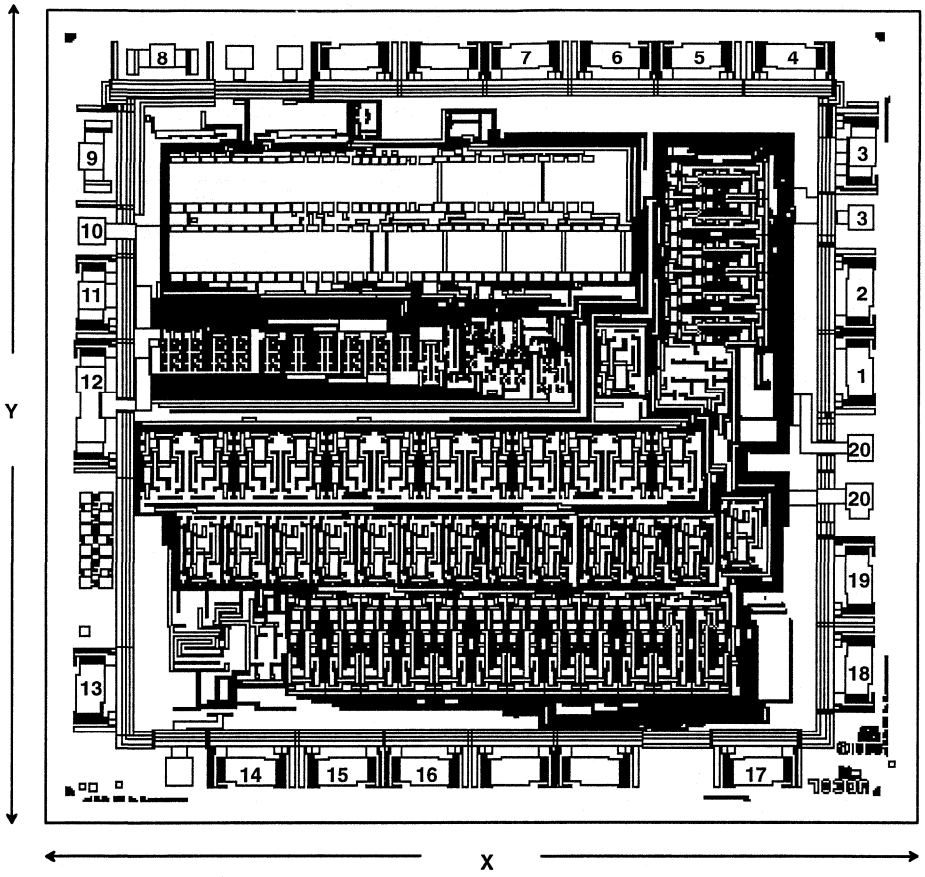
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP1230AB-DIE	0.5	0.75	16.0
MP1231AB-DIE	1.0	1.0	16.0

Electrical Parameters And Test Conditions (TA = 25°C, VDD = 15 V, VREF = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		0.5	LSB	Best Straight Line
DNL	Differential Non-Linearity		0.75	LSB	
GE	Gain Error		16.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		20	ppm / %	
I_{OUT}	Output Leakage Current		10	nA	
R_{IN}	Input Resistance	5	20	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.0	mA	V_{IN} = 0, 5 V

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 136 mils, Y = 129 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. $\overline{CS}$
2. $\overline{WR1}$
3. AGND
4. DB7
5. DB6
6. DB5
7. DB4
8. V_{REF}
9. R_{FB}
10. DGND
11. I_{OUT1}
12. I_{OUT2}
13. DB11 (MSB) (DB3)
14. DB10 (DB2)
15. DB9 (DB1)
16. DB8 (DB0)
17. $\overline{XFER}$
18. $\overline{WR2}$
19. BYTE1/$\overline{BYTE2}$
20. V_{DD}*

*Connect Pin 20 First

MP3274 DIE

Complete 32 Channel, 12-Bit
Data Acquisition Subsystem
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{CC} to DGND ..... 0 to +16.5 V
V_{EE} to DGND ..... 0 to –16.5 V
V_{DD} to DGND ..... 0 to +7 V
AGND to DGND ..... ±1 V
Digital Inputs/Outputs
to DGND ..... –0.5 V to V_{LOGIC} +0.5 V
Analog Inputs ($A_{IN}0 - A_{IN}31$, GND REF)
to AGND ..... ±16.5 V
20 V_{IN} to AGND ..... ±60 V
REF OUT ..... Indefinite short to DGND,
Momentary short to V_{CC}
T_J (Maximum) ..... 150°C

Ordering Information

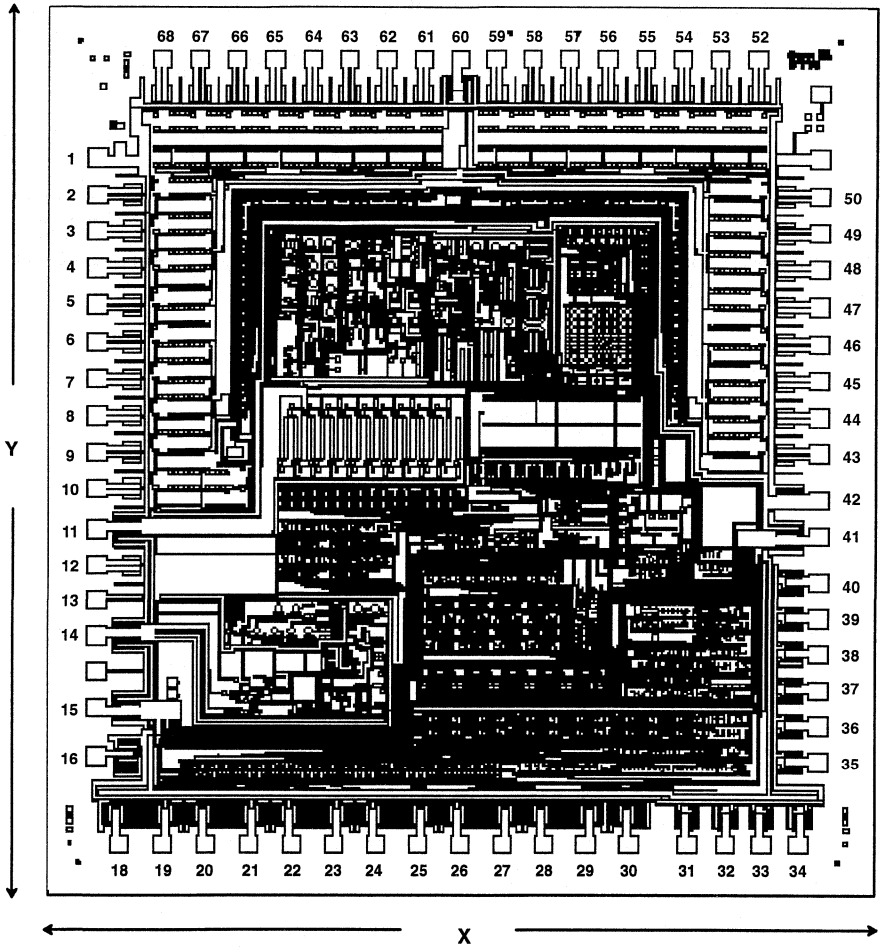
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (% FS)
MP3274K-DIE	2	1	±1

Electrical Parameters And Test Conditions (TA = 25°C, V_{CC} = +15 V, V_{DD} = +5 V, V_{EE} = –15 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		±2	LSB	
DNL	Differential Non-Linearity		±1	LSB	
GE	Gain Error		±1	% FS	
PSRR	Power Supply Rejection Ratio		±2	LSB	
I_{LKG}	Output Leakage Current		±5	µA	
R_{IN}	Input Resistance	100	300	KΩ	
V_{IN}	Logic "1"	2.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		±5	µA	
I_{DD}	Supply Current		7	mA	
I_{EE}	Supply Current		3	mA	
I_{CC}	Supply Current		8	mA	
V_{OH}	Logical "1" Voltage	2.4		V	$I_{SOURCE} \leq 500\mu A$
V_{OL}	Logical "0" Voltage		0.4	V	$I_{SINK} \leq 1.6mA$
V_{REF}	Reference Output Voltage	3.95	4.05	V	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.
7. Electrical parameters above are for laser trimmed die.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 212.2 mils, Y = 232.68 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{EE}

*Bond pin 1 first.

Pad Designations

1*	V_{EE}	14	AGND3	27	DB10	41	V_{DD}	55	$A_{IN}11$
2	$A_{IN}24$	15	DGND	28	DB11/SDO	42	V_{CC}	56	$A_{IN}12$
3	$A_{IN}25$	16	DB0/SDC	29	STS	43	$A_{IN}0$	57	$A_{IN}13$
4	$A_{IN}26$	17	N/C	30	STL	44	$A_{IN}1$	58	$A_{IN}14$
5	$A_{IN}27$	18	DB1	31	PXS	45	$A_{IN}2$	59	$A_{IN}15$
6	$A_{IN}28$	19	DB2	32	$\overline{RD}$	46	$A_{IN}3$	60	AGND2
7	$A_{IN}29$	20	DB3	33	$\overline{CS}$	47	$A_{IN}4$	61	$A_{IN}16$
8	$A_{IN}30$	21	DB4	34	$\overline{WR}$	48	$A_{IN}5$	62	$A_{IN}17$
9	$A_{IN}31$	22	DB5	35	ADEN	49	$A_{IN}6$	63	$A_{IN}18$
10	GND Ref.	23	DB6	36	AB4	50	$A_{IN}7$	64	$A_{IN}19$
11	AGND	24	DB7	37	AB3	51	N/C	65	$A_{IN}20$
12	REF IN	25	DB8	38	AB2	52	$A_{IN}8$	66	$A_{IN}21$
13	REF OUT	26	DB9	39	AB1	53	$A_{IN}9$	67	$A_{IN}22$
				40	AB0	54	$A_{IN}10$	68	$A_{IN}23$

MP7226 DIE

Quad 8-Bit
Digital-to-Analog Converter
BiCMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to AGND, DGND ..... 0 to +17 V
Digital Input Voltage to DGND .... –0.5 to V_{DD} +0.5 V
V_{REF} to AGND, DGND ..... –0.5 to V_{DD} +0.5 V
V_{SS} to AGND, DGND ..... +0.5 to –7 V
T_J (maximum) ..... 150°C

Ordering Information

Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7226K-DIE*	±1	±1	±1

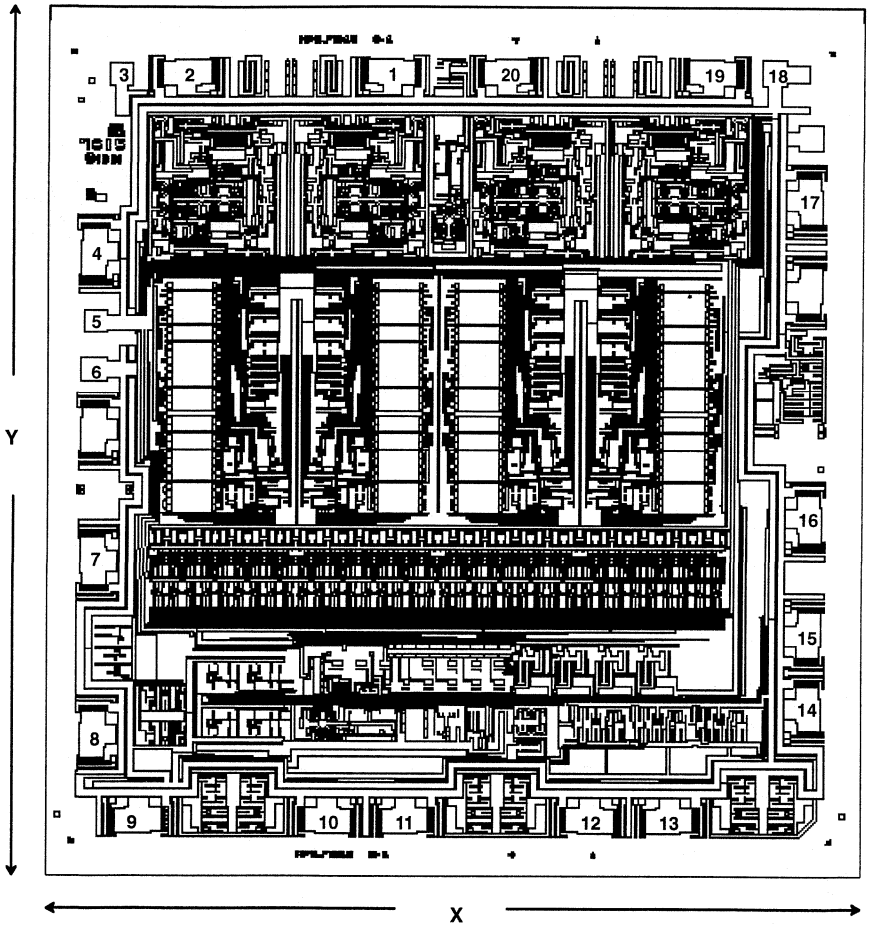
*Note Limitation for product $V_{REF} - V_{SS}$ <11 V

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{SS} = –5 v, V_{REF} = 5 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		±1	LSB	Endpoint Linearity Spec
DNL	Differential Non-Linearity		±1	LSB	
GE	Gain Error		±1	LSB	
R_{IN}	Input Resistance	2		KΩ	Min R_{IN} at code 149_{10}
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		±1	µA	
I_{DD}	Supply Current		12	mA	
I_{SS}	Supply Current		–10	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 3440µ, Y = 3640µ
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. V_{OUT2}
2. V_{OUT1}
3. V_{SS}
4. V_{REF}
5. AGND
6. DGND
7. DB7 (MSB)
8. DB6
9. DB5
10. DB4
11. DB3
12. DB2
13. DB1
14. DB0 (LSB)
15. $\overline{WR}$
16. A1
17. A0
18. V_{DD}*
19. V_{OUT4}
20. V_{OUT3}

*Connect pin 18 first

7

MP7228 DIE

Octal 8-Bit
Digital-to-Analog Converter
BiCMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND ..... –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... –0.5 to V_{DD} +0.5 V
V_{SS} to GND ..... +0.5 to –7 V
T_J (maximum) ..... 150°C

Ordering Information

Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7228K-DIE*	±1	±1	±1

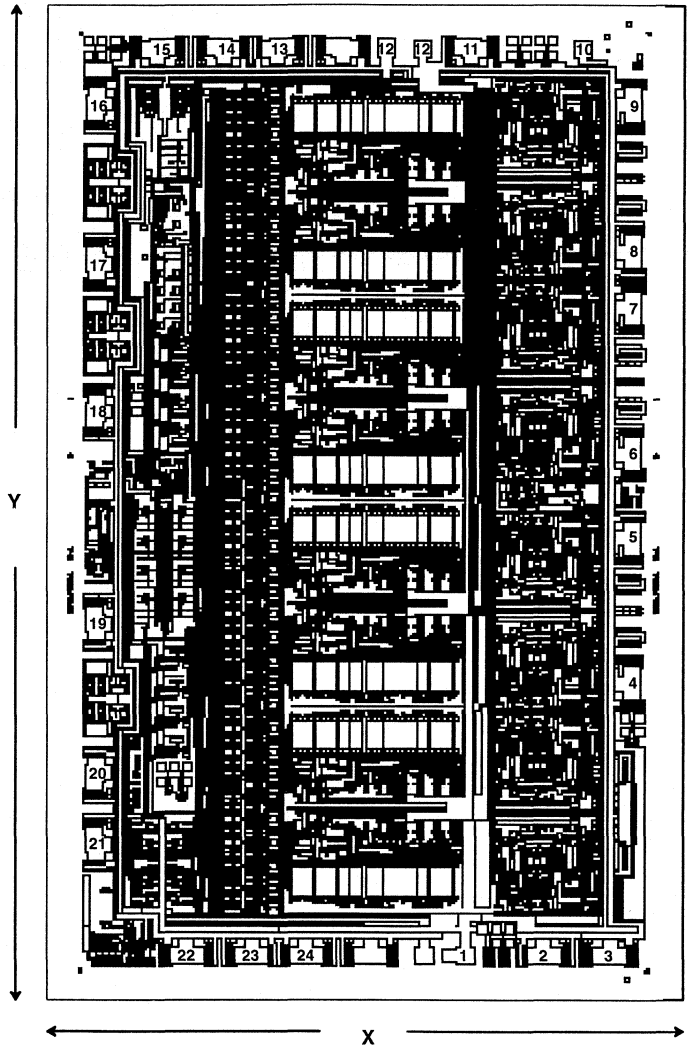
*Note Limitation for product $V_{REF} - V_{SS}$ <11 V

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{SS} = –5 V, V_{REF} = 5 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		±1	LSB	End Point Linearity Spec
DNL	Differential Non-Linearity		±1	LSB	
GE	Full Scale Error		±1	LSB	
R_{IN}	Input Resistance	2		KΩ	Min R_{IN} at code 149_{10}
V_{INH}	Logic "1"	2.4		V	
V_{INL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		±1	µA	
I_{DD}	Supply Current		16	mA	
I_{SS}	Supply Current		–14	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 5880µ, Y = 3560µ
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. V_{DD}*
2. $V_{OUT}8$
3. $V_{OUT}7$
4. $V_{OUT}6$
5. $V_{OUT}5$
6. $V_{OUT}4$
7. $V_{OUT}3$
8. $V_{OUT}2$
9. $V_{OUT}1$
10. V_{SS}
11. V_{REF}
12. GND
13. DB7 (MSB)
14. DB6
15. DB5
16. DB4
17. DB3
18. DB2
19. DB1
20. DB0 (LSB)
21. $\overline{WR}$
22. A2
23. A1
24. A0

*Connect pin 1 first

7

MP7523 DIE

8-Bit Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

EXAR

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND .... −0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND ..... −0.5 V to +6.5 V
T_J (maximum) ..... 150°C

Ordering Information

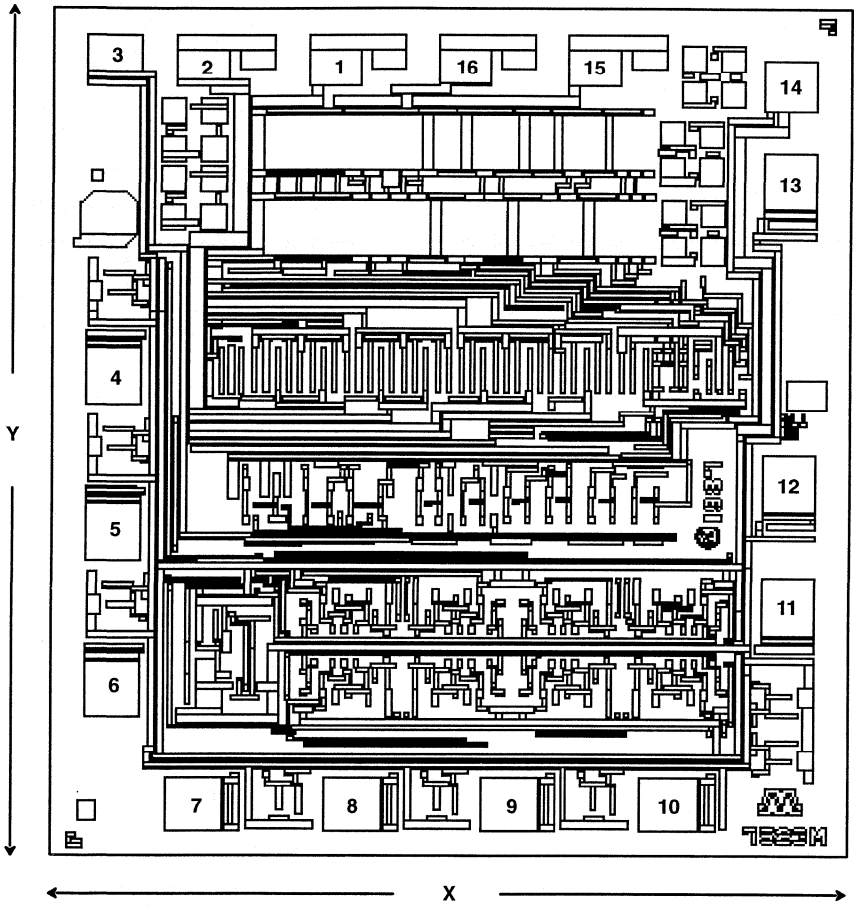
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7523A-DIE	0.5	1.0	4.0
MP7523B-DIE	0.25	1.0	4.0

Electrical Parameters And Test Conditions
(T_A = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		0.5	LSB	Best Straight Line
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		4.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		200	ppm / %	Using Internal R_{FB}
I_{OUT}	Output Leakage Current		50	nA	
R_{IN}	Input Resistance	5	20	K Ω	
V_{IN}	Logic "1"	13.5		Volts	V_{DD} = 15 V
V_{IL}	Logic "0"		1.5	Volts	V_{DD} = 15 V
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.0	mA	Inputs 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 63 mils, Y = 69 mils
Pad Size	4 x 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. GND
4. BIT 1 (MSB)
5. BIT 2
6. BIT 3
7. BIT 4
8. BIT 5
9. BIT 6
10. BIT 7
11. BIT 8 (LSB)
12. N/C
13. N/C
14. $V_{DD(+)}$*
15. V_{REF} (IN)
16. R_{FB}

* Bond Pin 14 First

7

MP7524 DIE

8-Bit Buffered Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

EXAR

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... −0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND ..... −0.5 V to +6.5 V
T_J (maximum) ..... 150°C

Ordering Information

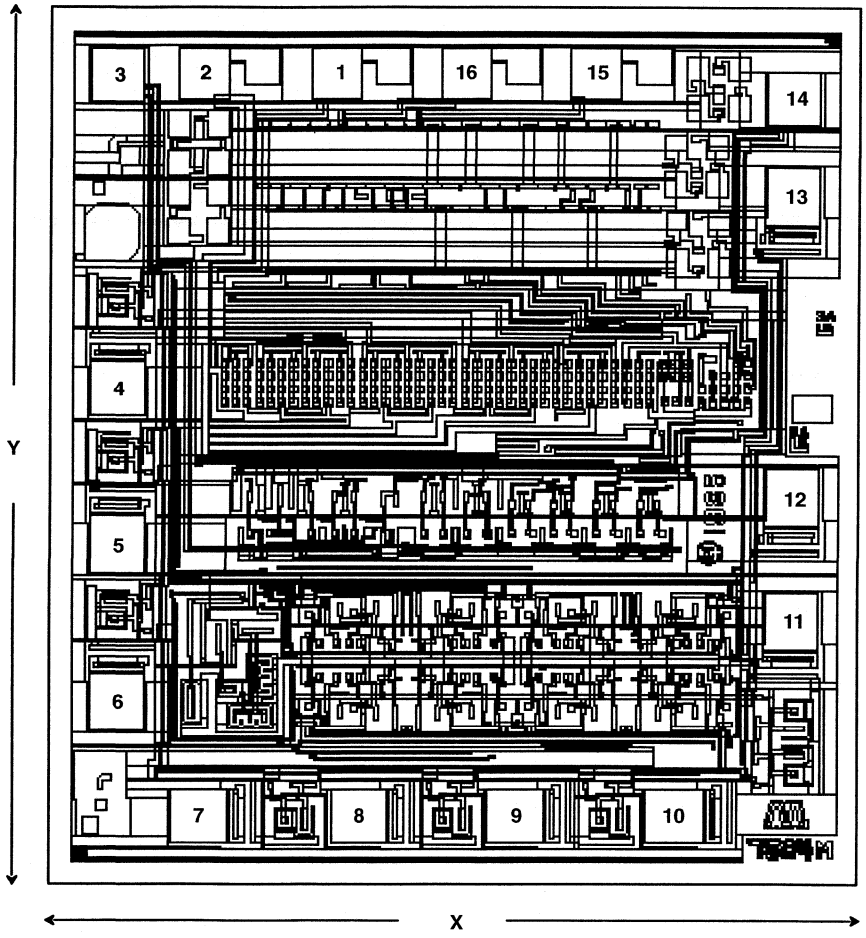
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7524J-DIE	0.5	1.0	2.5
MP7524K-DIE	0.25	1.0	2.5

Electrical Parameters And Test Conditions
(T_A = 25°C, V_{DD} = 5 V & 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		0.5	LSB	End Point Linearity
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		2.5	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		800 200	ppm / % ppm / %	V_{DD} = 5 V V_{DD} = 15 V
I_{OUT}	Output Leakage Current		50	nA	
R_{IN}	Input Resistance	5	20	KΩ	
V_{IH}	Logic "1"	2.4 13.5		V V	V_{DD} = 5 V V_{DD} = 15 V
V_{IL}	Logic "0"		0.8 1.5	V V	V_{DD} = 5 V V_{DD} = 15 V
I_{LKG}	Input Leakage Current		1	µA	
I_{DD}	Supply Current		2	mA	Inputs 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 63 mils, Y = 69 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. GND
4. DB7 (MSB)
5. DB6
6. DB5
7. DB4
8. DB3
9. DB2
10. DB1
11. DB0 (LSB)
12. $\overline{CS}$
13. $\overline{WR}$
14. V_{DD}*
15. V_{REF}
16. R_{FB}

* Bond #14 first

MP7524A DIE

8-Bit Buffered Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... –0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND ..... –0.5 V to +6.5 V
T_J (maximum) ..... 150°C

Ordering Information

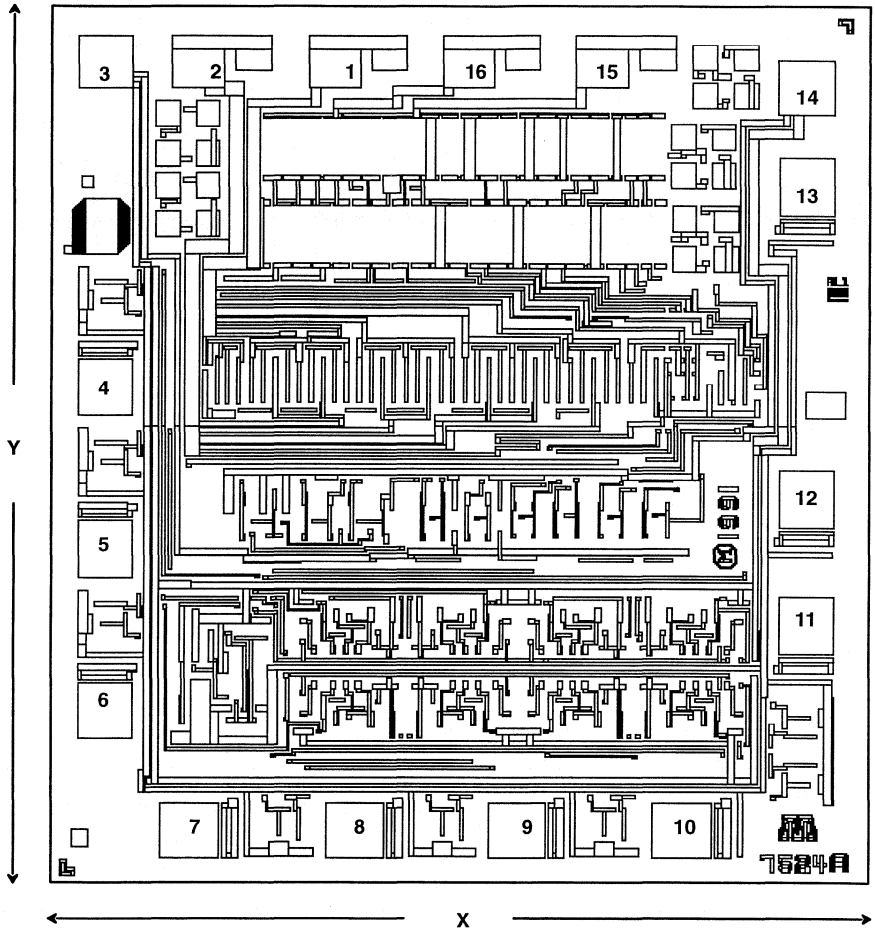
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7524AA-DIE	0.5	1.0	2.5
MP7524AB-DIE	0.25	1.0	2.5

Electrical Parameters And Test Conditions
(T_A = 25°C, V_{DD} = 5 V & 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		0.5	LSB	End Point Linearity
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		2.5	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		800 200	ppm / % ppm / %	V_{DD} = 5 V V_{DD} = 15 V
I_{OUT}	Output Leakage Current		50	nA	I_{OUT1} only
R_{IN}	Input Resistance	5	20	KΩ	
V_{IH}	Logic "1"	2.4 13.5		V V	V_{DD} = 5 V V_{DD} = 15 V
V_{IL}	Logic "0"		0.8 1.5	V V	V_{DD} = 5 V V_{DD} = 15 V
I_{LKG}	Input Leakage Current		1	µA	
I_{DD}	Supply Current		2	mA	Inputs 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 63 mils, Y = 69 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. GND
4. DB7 (MSB)
5. DB6
6. DB5
7. DB4
8. DB3
9. DB2
10. DB1
11. DB0 (LSB)
12. $\overline{CS}$
13. $\overline{WR}$
14. V_{DD}*
15. V_{REF}
16. R_{FB}

* Bond #14 first

7

MP7528 DIE

8-Bit Dual Buffered Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ...–0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND ..–0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

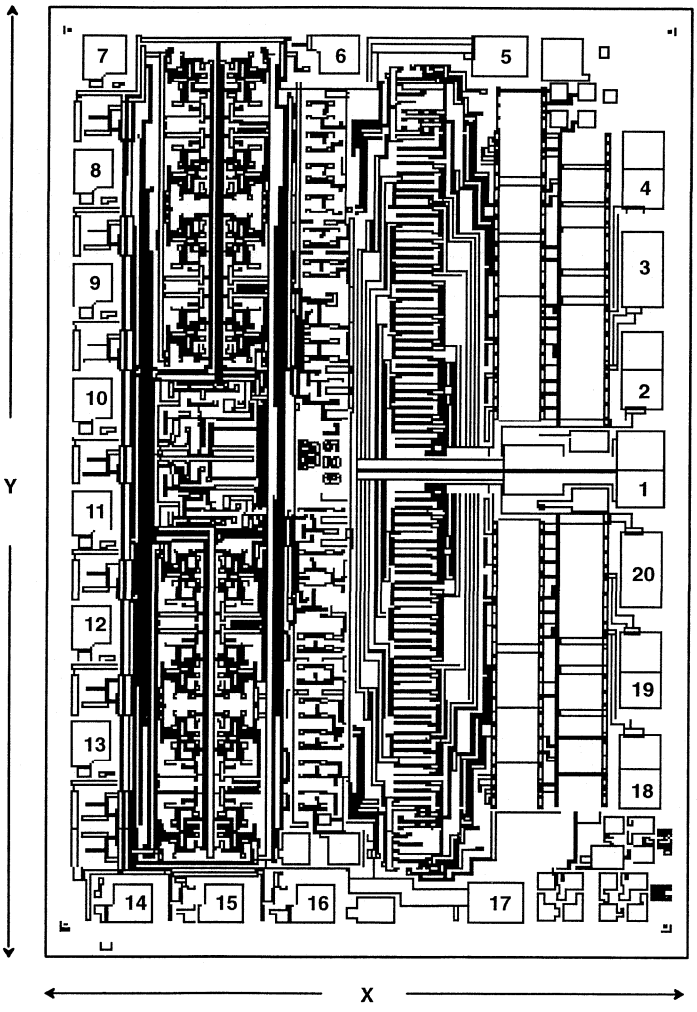
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7528J-DIE	1.0	1.0	4.0
MP7528K-DIE	0.5	1.0	2.0

Electrical Parameters And Test Conditions (TA = 25°C, VDD = 5 & 15 V, VREF = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		1.0	LSB	End Point Linearity
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		4.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		400	ppm / %	$\Delta V_{DD} = \pm 5\%$
I_{OUT}	Output Leakage Current		50	nA	
R_{IN}	Input Resistance DAC A/DAC B Resistance Match	8	15 1	KΩ %	
V_{IH}	Logic "1"	2.4 13.5		V V	V_{DD} = 5 V V_{DD} = 15 V
V_{IL}	Logic "0"		0.8 1.5	V V	V_{DD} = 5 V V_{DD} = 15 V
I_{LKG}	Input Leakage Current		1	µA	
I_{DD}	Supply Current		2	mA	Inputs 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 69 mils, Y = 101 mils
Pad Size	4 x 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. AGND
2. I_{OUTA}
3. R_{FB} A
4. V_{REF} A
5. DGND
6. $\overline{DAC\ A}$ /DAC B
7. DB7 (MSB)
8. DB6
9. DB5
10. DB4
11. DB3
12. DB2
13. DB1
14. DB0 (LSB)
15. $\overline{CS}$
16. $\overline{WR}$
17. V_{DD}*
18. V_{REF} B
19. R_{FB} B
20. I_{OUT} B

* Bond #17 first

MP7529A DIE

8-Bit Dual Buffered Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ..... –0.5 to +7.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND ..... –0.5 to +6.5 V
T_J (maximum) ..... 150°C

Ordering Information

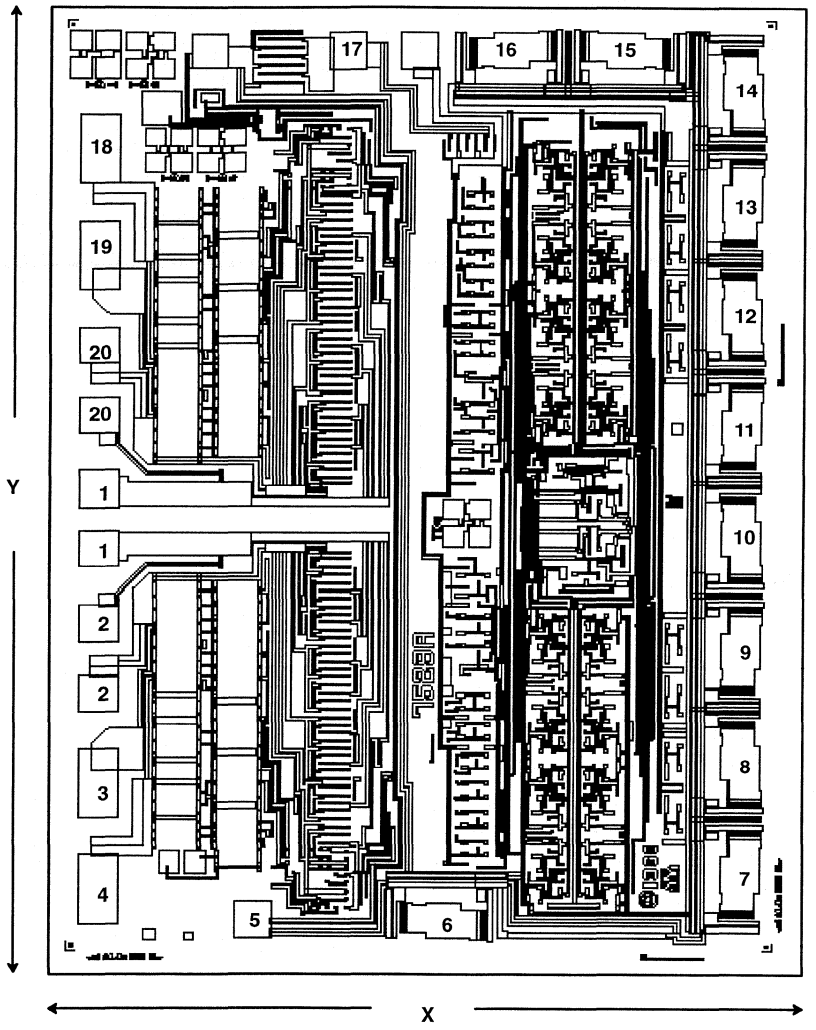
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7529AJ-DIE	1.0	1.0	4.0

Electrical Parameters And Test Conditions (T_A = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		1.0	LSB	End Point Linearity
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		4.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		100	ppm / %	
I_{OUT}	Output Leakage Current		50.0	nA	
R_{IN}	Input Resistance	8.0	15.0	KΩ	
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		1.0	mA	V_{IN} = 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 83 mils, Y = 110 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. AGND
2. I_{OUTA}
3. R_{FBA}
4. V_{REFA}
5. DGND
6. $\overline{DACA}$/DACB
7. DB7 (MSB)
8. DB6
9. DB5
10. DB4
11. DB3
12. DB2
13. DB1
14. DB0 (LSB)
15. $\overline{CS}$
16. $\overline{WR}$
17. V_{DD}*
18. V_{REFB}
19. R_{FBB}
20. I_{OUTB}

*Connect Pin 17 First

MP7529B DIE

8-Bit Dual Buffered Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +7 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ..... –0.5 to +7.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND ..... –0.5 to +6.5 V
T_J (maximum) ..... 150°C

Ordering Information

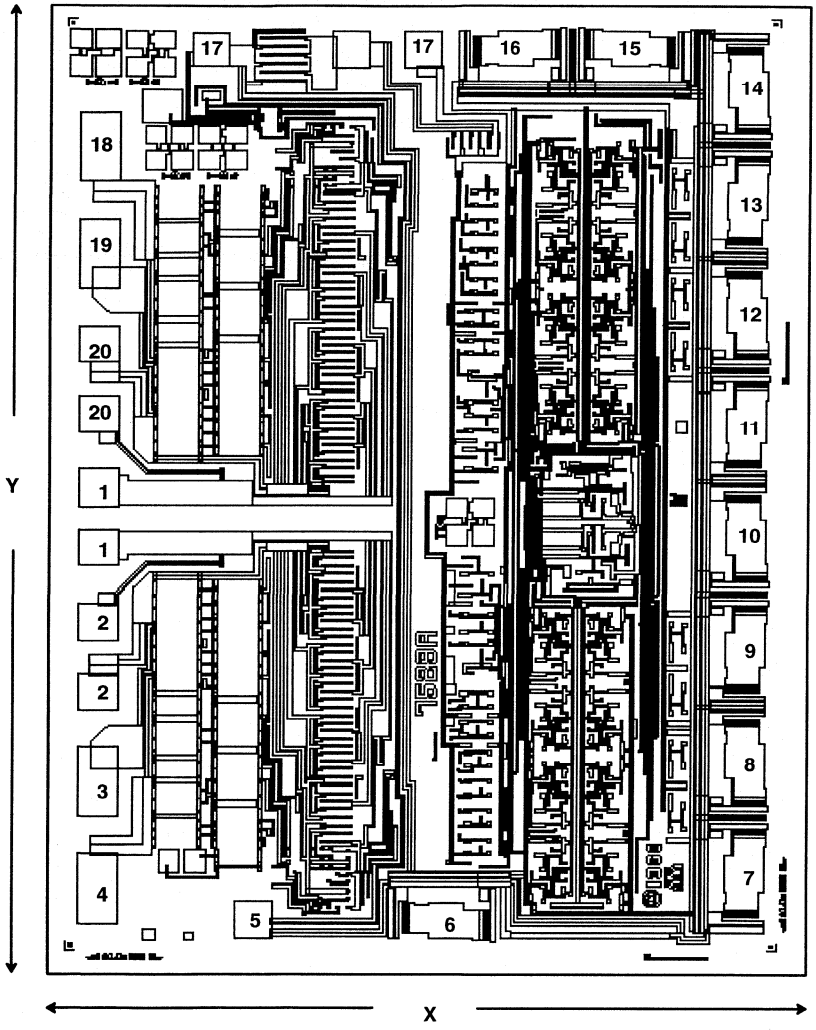
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7529BJ-DIE	1.0	1.0	4.0

Electrical Parameters And Test Conditions (T_A = 25°C, V_{DD} = 5 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		1.0	LSB	End Point Linearity
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		4.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		100	ppm / %	
I_{OUT}	Output Leakage Current		50.0	nA	
R_{IN}	Input Resistance	8.0	15.0	KΩ	
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		1.0	mA	V_{IN} = 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 83 mils, Y = 110 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. AGND
2. I_{OUTA}
3. R_{FBA}
4. V_{REFA}
5. DGND
6. $\overline{DACA}$/DACB
7. DB7 (MSB)
8. DB6
9. DB5
10. DB4
11. DB3
12. DB2
13. DB1
14. DB0 (LSB)
15. $\overline{CS}$
16. $\overline{WR}$
17. V_{DD}*
18. V_{REFB}
19. R_{FBB}
20. I_{OUTB}

*Connect Pin 17 First

MP7541B DIE

Multiplying 12-Bit
Digital-to-Analog Converter
CMOS Die Specifications

EXAR

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... ±17 V
V_{REF} to GND ..... ±25 V
Digital Input Voltage (V_{IN}) to GND
..... GND –0.5 V to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND
..... GND –0.5 V to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

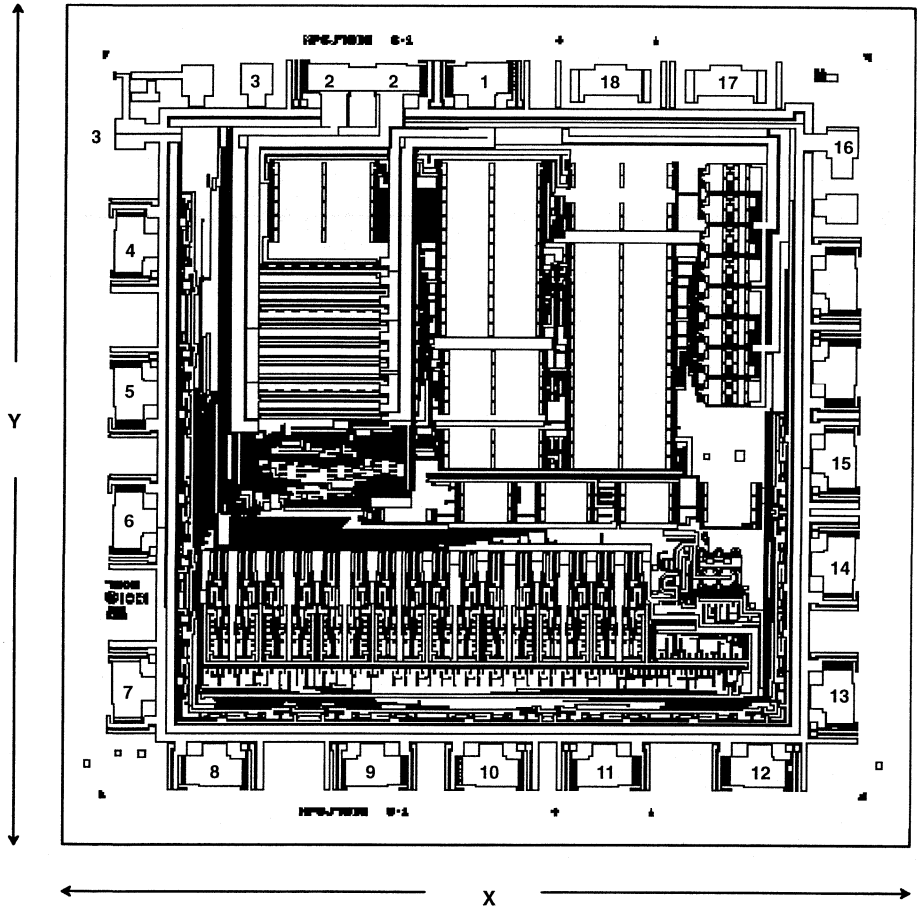
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7541BK-DIE	0.5	1.0	6

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{REF} = +10 V, I_{OUT1} = I_{OUT2} = GND = 0 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		±0.5	LSB	End Point Linearity
DNL	Differential Non-Linearity		±1	LSB	
GE	Gain Error		±6	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		±50	ppm / %	Using Internal R_{FB}
I_{LKG}	Output Leakage Current		±10	nA	
R_{IN}	Input Resistance	5	20	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		±1	µA	
I_{DD}	Supply Current		1	mA	Inputs 0, 5 V

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 115.75 mils, Y = 114.57 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. GND
4. BIT 1 (MSB)
5. BIT 2
6. BIT 3
7. BIT 4
8. BIT 5
9. BIT 6
10. BIT 7
11. BIT 8
12. BIT 9
13. BIT 10
14. BIT 11
15. BIT 12 (LSB)
16. V_{DD}*
17. V_{REF}
18. R_{FB}

*Bond pin 16 first

MP7542 DIE

12-Bit Microprocessor Compatible
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +7 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... −0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. −0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

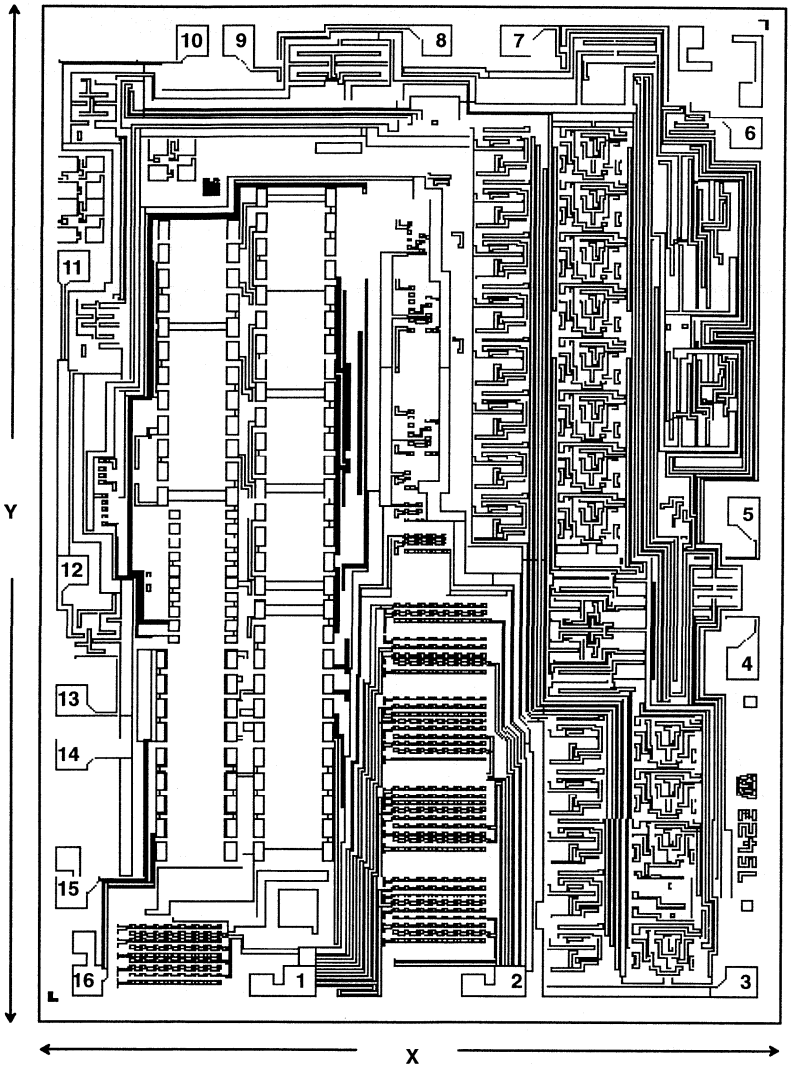
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7542J-DIE	1.0	2.0	11.0
MP7542K-DIE	0.5	1.0	11.0

Electrical Parameters And Test Conditions (T_A = 25°C, V_{DD} = 5 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		0.5	LSB	Best Straight Line
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		11.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		50	ppm / %	
I_{OUT}	Output Leakage Current		10.0	nA	
R_{IN}	Input Resistance	5	20	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		1.0	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.5	mA	V_{IN} = 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 97 mils, Y = 134 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. AGND
4. D3
5. D2
6. D1
7. D0
8. $\overline{CS}$
9. $\overline{WR}$
10. A0
11. A1
12. DGND
13. $\overline{CLR}$
14. V_{DD}*
15. V_{REF}
16. R_{FB}

*Connect Pin 14 first

MP7543 DIE

12-Bit Serial Input
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +7 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... −0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. −0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

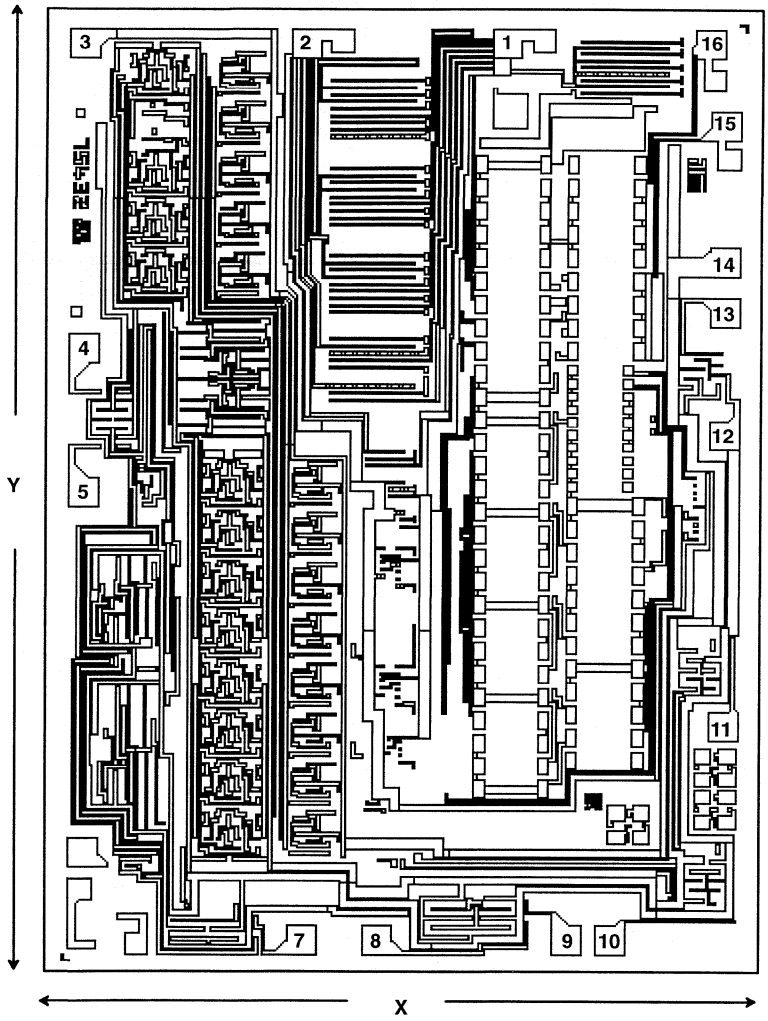
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7543J-DIE	1.0	2.0	12.0
MP7543K-DIE	0.5	1.0	12.0

Electrical Parameters And Test Conditions (T_A = 25°C, V_{DD} = 5 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		1.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		2.0	LSB	
GE	Gain Error		12.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		50	ppm / %	
I_{OUT}	Output Leakage Current		10.0	nA	
R_{IN}	Input Resistance	5.0	20.0	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.5	mA	V_{IN} = 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 97 mils, Y = 134 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. AGND
4. STB1
5. $\overline{LD1}$
6. NC
7. SRI
8. STB2
9. $\overline{LD2}$
10. $\overline{STB3}$
11. STB4
12. DGND
13. $\overline{CLR}$
14. V_{DD}*
15. V_{REF}
16. R_{FB}

*Connect pin 14 first

MP7545B DIE

Buffered Multiplying 12-Bit
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 to +17 V
V_{REF} to GND ..... ±25 V
Digital Input Voltage (V_{IN}) to GND
..... GND –0.5 to V_{DD} +0.5 V
V_{OUT} to GND ..... GND –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

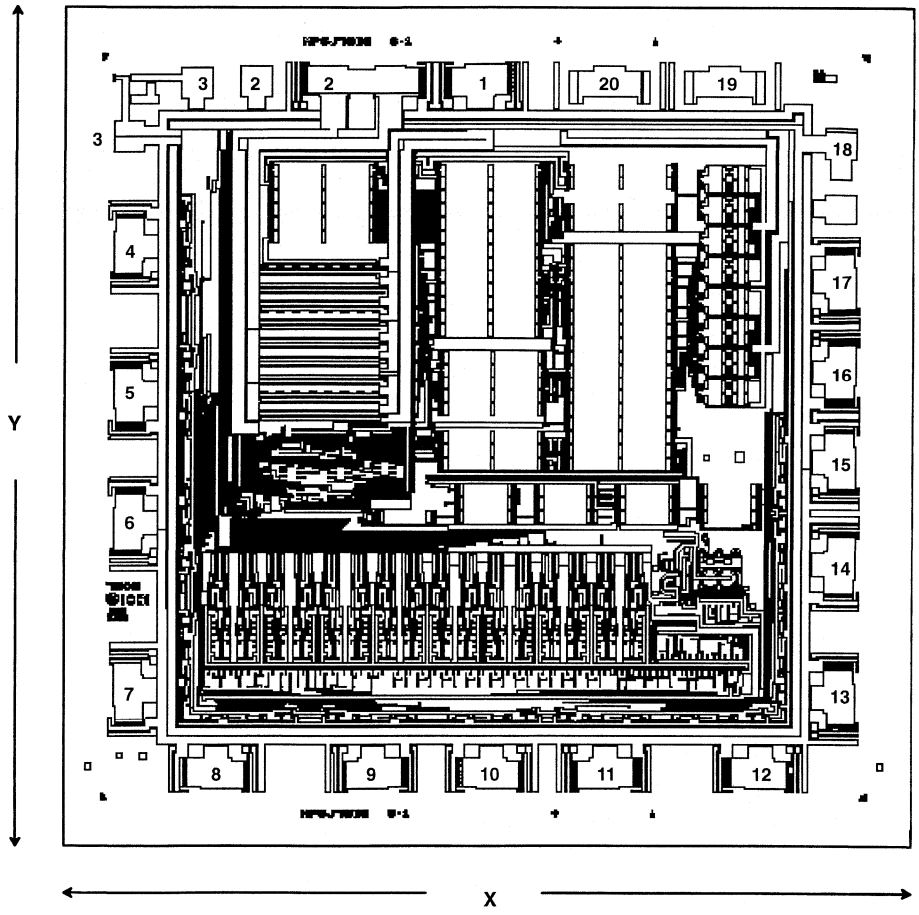
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7545BK-DIE	0.5	1.0	6

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 & 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		±0.5	LSB	End Point Linearity
DNL	Differential Non-Linearity		±1.0	LSB	
GE	Gain Error		±6	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		±50	ppm / %	Using Internal R_{FB}
I_{LKG}	Output Leakage Current		±10	nA	
R_{IN}	Input Resistance	7	25	KΩ	
V_{IN}	Logic "1"	2.4 13.5		V	V_{DD} = 5 V V_{DD} = 15 V
V_{IL}	Logic "0"		0.8 1.5	V	V_{DD} = 5 V V_{DD} = 15 V
I_{LKG}	Input Leakage Current		±1	µA	
I_{DD}	Supply Current		1	mA	Input 0 to V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 115.75 mils, Y = 114.57 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT}
2. AGND
3. DGND
4. DB11 (MSB)
5. DB1
6. DB9
7. DB8
8. DB7
9. DB6
10. DB5
11. DB4
12. DB3
13. DB2
14. DB1
15. DB0
16. $\overline{CS}$
17. $\overline{WR}$
18. V_{DD}*
19. V_{REF}
20. R_{FB}

*Bond pin 18 first

MP7610 DIE

Octal 14-Bit DAC Array™
Digital-to-Analog Converter with Output Amplifier
and Serial Data/Address µP Control Logic
BiCMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{CC} to AGND ..... +16.5 V
V_{EE} to AGND ..... –16.5 V
DV_{DD} to DGND ..... 6.5 V
V_{REF} to GND ..... 6 V
T_J (maximum) ..... 150°C

Ordering Information

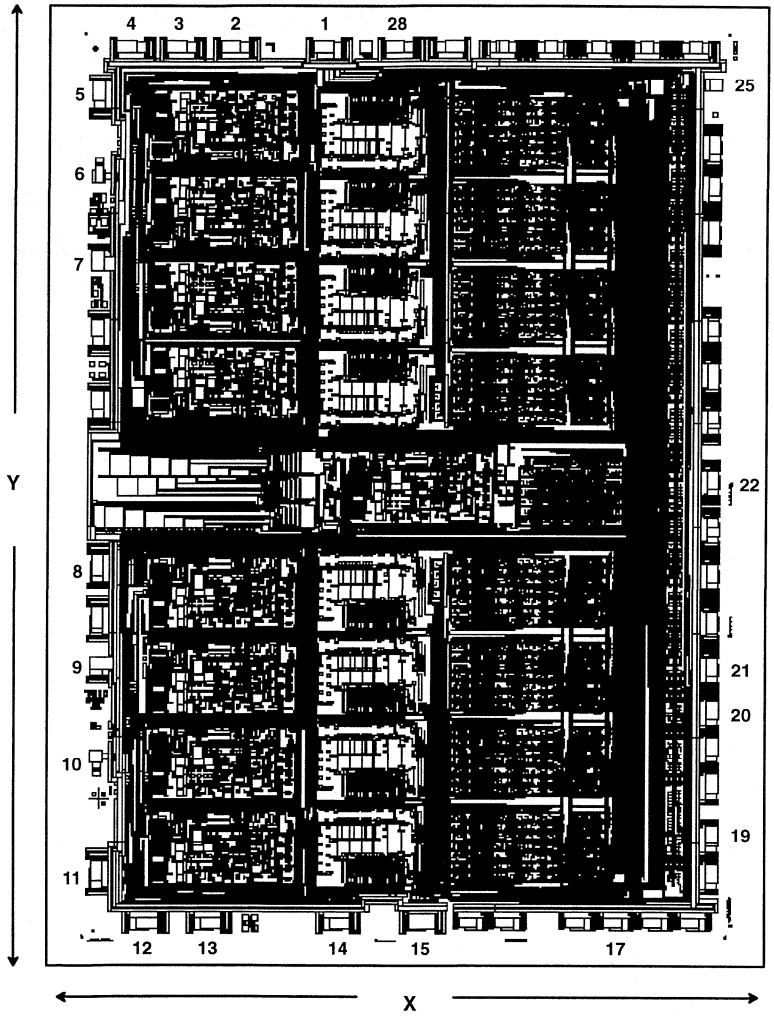
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7610A-DIE	8.0	4.0	32

Electrical Parameters And Test Conditions (TA = 25°C, V_{CC} = +12, V_{EE} = –12 V_{DD} = 5 V, V_{REF} =5 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	14		Bits	
INL	Relative Accuracy		8	LSB	Best Straight Line
DNL	Differential Non-Linearity		4	LSB	
GE	Gain Error		32	LSB	
PSRR	Power Supply Rejection Ratio		0.05	ppm / %	
I_{LKG}	Output Leakage Current			nA	
R_{IN}	Input Resistance	0.35	1.4	KΩ	
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		400	µA	
I_{DD}	Supply Current		1.0	mA	
I_{CC}	Supply Current		10	mA	
I_{EE}	Supply Current		20	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 225 mils, Y = 317 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{EE}

Pad Designations

1. AGND0
2. V_{O0}
3. V_{O1}
4. V_{O2}
5. V_{O3}
6. V_{EE0}*
7. V_{CC0}
8. V_{REF}
9. V_{CC1}
10. V_{EE1}*
11. V_{O4}
12. V_{O5}
13. V_{O6}
14. V_{O7}
15. AGND1
16. N/C
17. $\overline{RST}$
18. N/C
19. $\overline{LD}$
20. CLK
21. SLK
22. SDO
23. N/C
24. N/C
25. DV_{DD}
26. N/C
27. N/C
28. DGND

*Bond pins 6 & 10 first

7

MP7611 DIE

Octal 14-Bit DAC Array™
Digital-to-Analog Converter with Output Amplifier
and Parallel Data/Address µP Control Logic
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{CC} to AGND ..... +16.5 V
V_{EE} to AGND ..... –16.5 V
DV_{DD} to DGND ..... 6.5 V
V_{REF} to GND ..... 6 V
T_J (maximum) ..... 150°C

Ordering Information

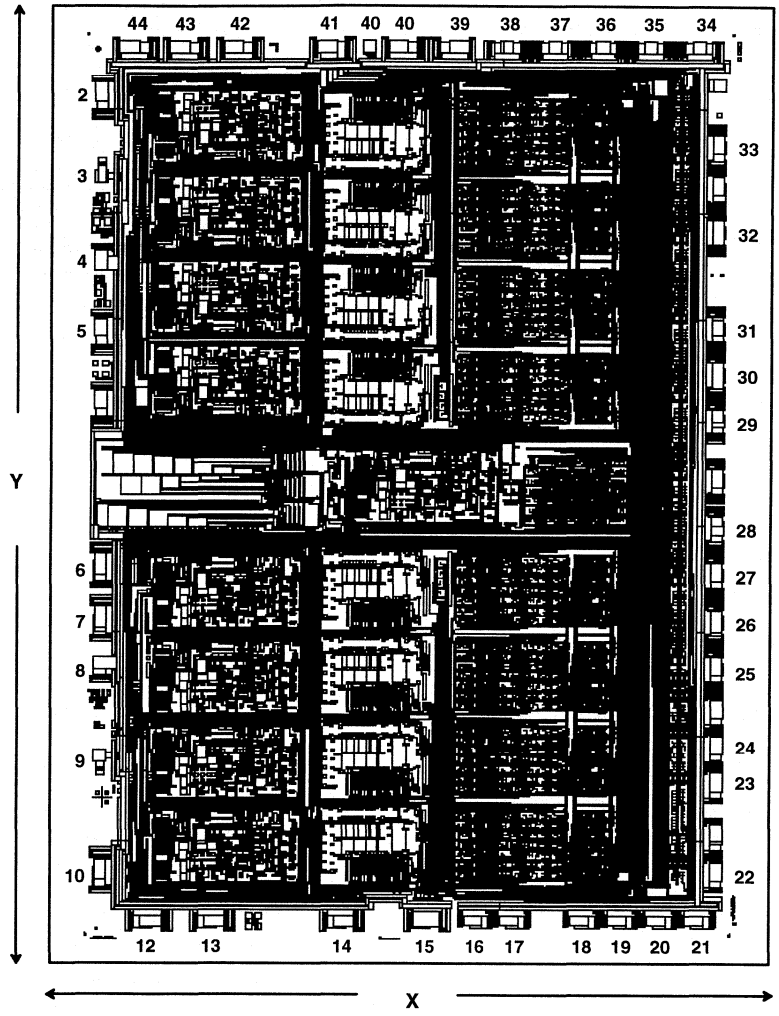
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7611A-DIE	8.0	4.0	32

Electrical Parameters And Test Conditions (TA = 25°C, V_{CC} = +12, V_{EE} = –12 V_{DD} = 5 V, V_{REF} =5 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	14		Bits	
INL	Relative Accuracy		8	LSB	Best Straight Line
DNL	Differential Non-Linearity		4	LSB	
GE	Gain Error		32	LSB	
PSRR	Power Supply Rejection Ratio		0.05	ppm / %	
I_{LKG}	Output Leakage Current			nA	
R_{IN}	Input Resistance	0.35	1.4	KΩ	
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		400	µA	
I_{DD}	Supply Current		1.0	mA	
I_{CC}	Supply Current		10	mA	
I_{EE}	Supply Current		20	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 225 mils, Y = 317 mils
Pad Size	4 X 4 mils nominal
Pad Metal	A1
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{EE}

*Bond pins 3 and 9 first

Pad Designations

1. N/C	12. VO5	23. A1	34. D9
2. V_{OS}	13. VO6	24. A0	35. D10
3. V_{EE0}*	14. VO7	25. D0	36. D11
4. V_{CC0}	15. AGND1	26. D1	37. D12
5. N/C	16. $\overline{CS}$	27. D2	38. D13
6. V_{REFP}	17. $\overline{RD}$	28. D3	39. V_{DD}
7. V_{REFN}	18. $\overline{R2}$	29. D4	40. DGND
8. V_{CC1}	19. $\overline{R1}$	30. D5	41. AGND
9. V_{EE1}*	20. $\overline{LD2}$	31. D6	42. V_{O0}
10. V_{O4}	21. $\overline{LD1}$	32. D7	43. V_{O1}
11. N/C	22. A2	33. D8	44. V_{O2}

MP7614 DIE

14-Bit Monolithic Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... –0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

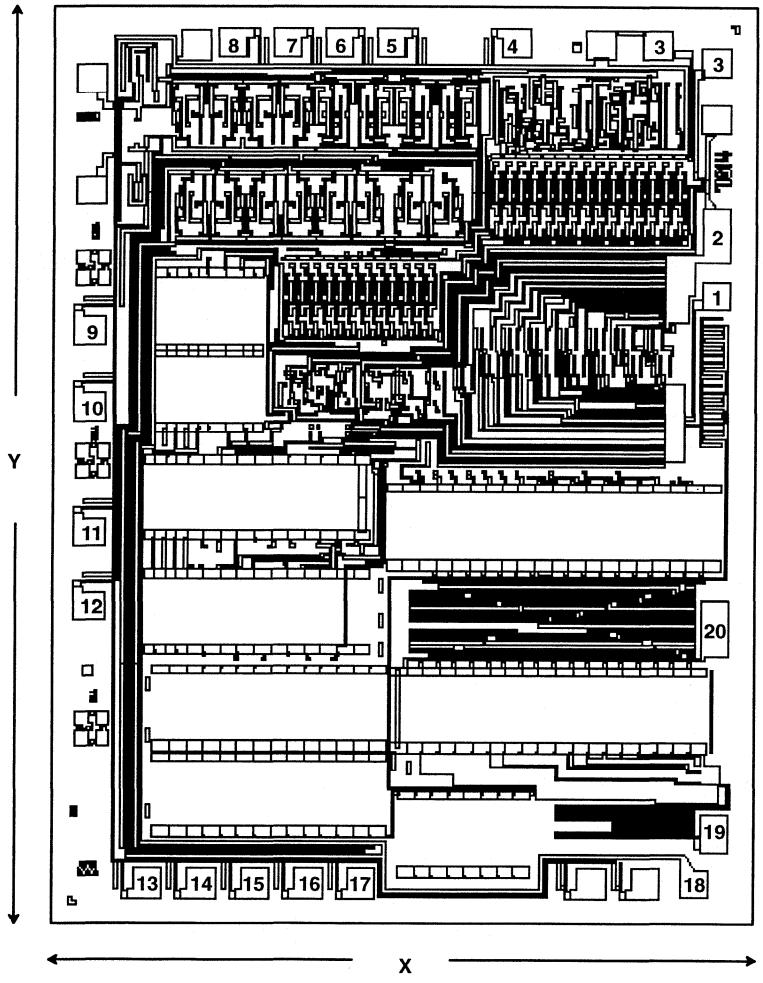
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (% FSR)
MP7614J-DIE	3.3	4.0	0.8
MP7614K-DIE	1.6	2.0	0.8

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	14		Bits	
INL	Relative Accuracy		3.3	LSB	Best Straight Line
DNL	Differential Non-Linearity		4.0	LSB	
GE	Gain Error		0.8	% FSR	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		0.005	% / %	
I_{OUT}	Output Leakage Current		10.0	nA	I_{OUT1} Leakage
R_{IN}	Input Resistance	1	10	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		4.0	mA	V_{IN} = 0, 5 V

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 101 mils, Y = 134 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. GND
4. BIT 1 (MSB)
5. BIT 2
6. BIT 3
7. BIT 4
8. BIT 5
9. BIT 6
10. BIT 7
11. BIT 8
12. BIT 9
13. BIT 10
14. BIT 11
15. BIT 12
16. BIT 13
17. BIT 14
18. V_{DD}*
19. V_{REF}
20. R_{FD}

*Connect pin 18 first

MP7616 DIE

16-Bit Monolithic Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

EXAR

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND .. −0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND . −0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

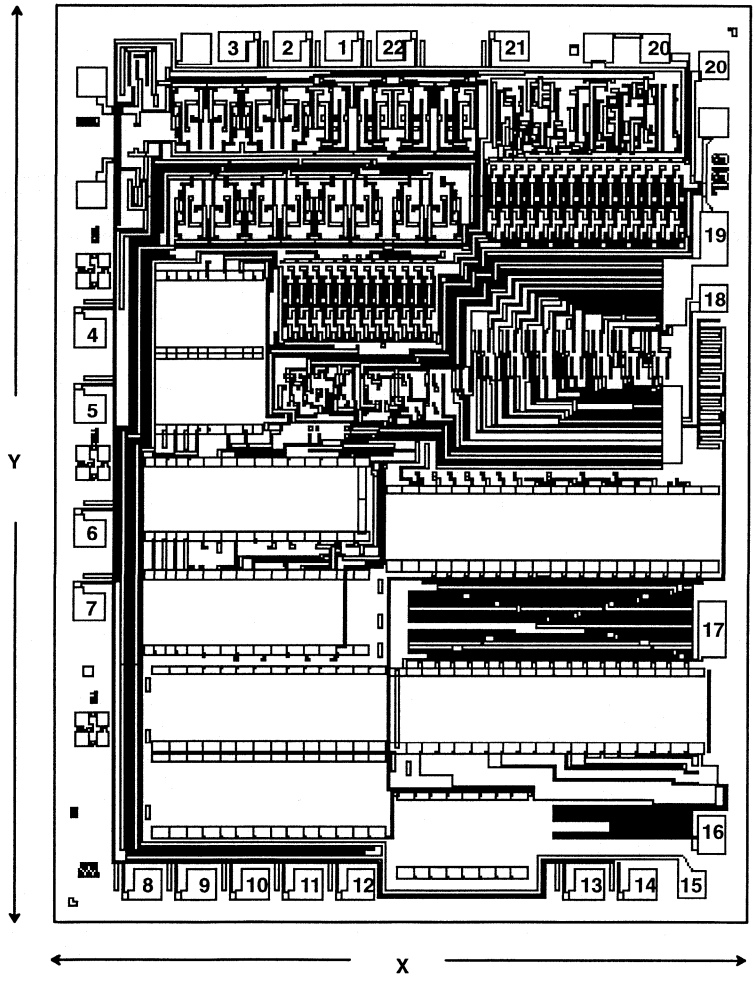
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (% FSR)
MP7616J-DIE	13.3	16.0	0.8
MP7616K-DIE	6.6	8.0	0.8

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	16		Bits	
INL	Relative Accuracy		13.3	LSB	Best Straight Line
DNL	Differential Non-Linearity		16.0	LSB	
GE	Gain Error		0.8	% FSR	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		0.005	% / %	
I_{OUT}	Output Leakage Current		10	nA	I_{OUT1} Leakage
R_{IN}	Input Resistance	1	10	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		4.0	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 101 mils, Y = 134 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. BIT 3
2. BIT 4
3. BIT 5
4. BIT 6
5. BIT 7
6. BIT 8
7. BIT 9
8. BIT 10
9. BIT 11
10. BIT 12
11. BIT 13
12. BIT 14
13. BIT 15
14. BIT 16 (LSB)
15. V_{DD}*
16. V_{REF}
17. R_{FB}
18. I_{OUT1}
19. I_{OUT2}
20. V_{SS}
21. BIT 1 (MSB)
22. BIT 2

*Bond pin 15 first.

7

MP7626 DIE

16-Bit Microprocessor Compatible Buffered Multiplying Digital-to-Analog Converter CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... –0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

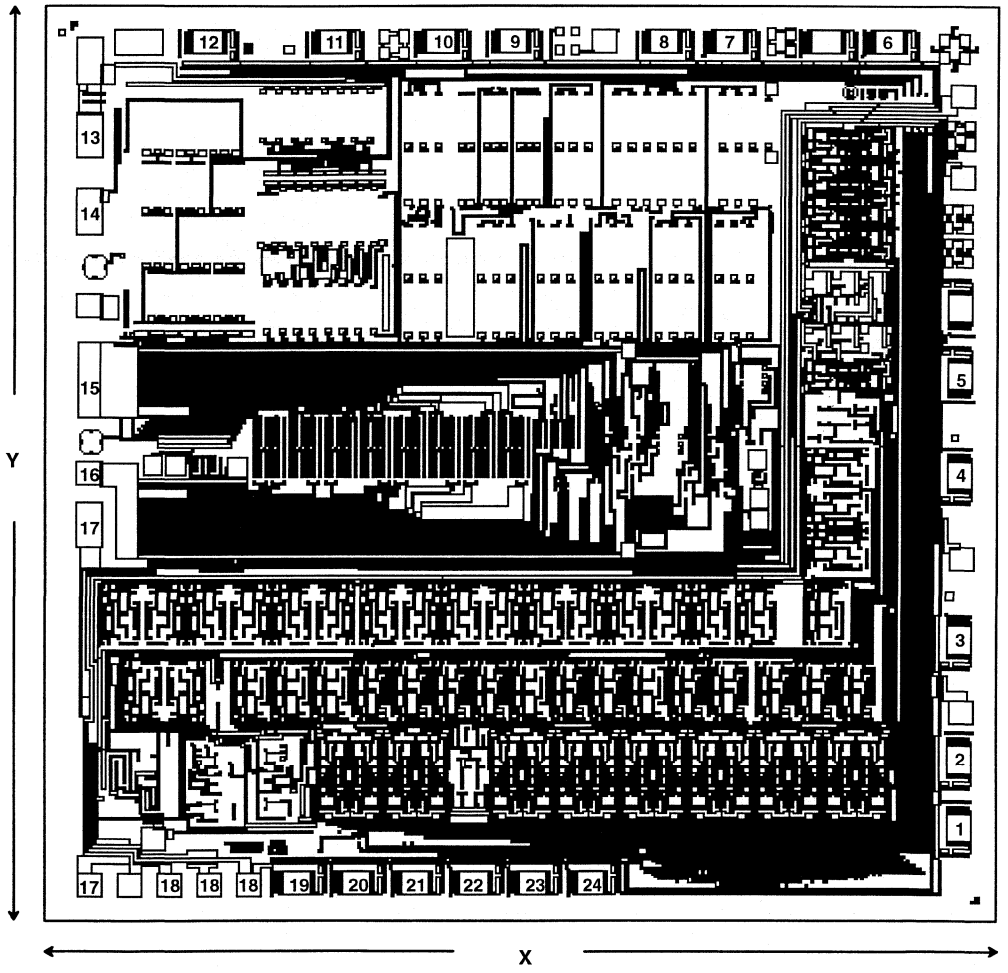
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (%)
MP7626J-DIE	4.0	4.0	0.025

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	16		Bits	
INL	Relative Accuracy		4.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		4.0	LSB	
GE	Gain Error		0.025	%	
PSRR	Power Supply Rejection Ratio		50	ppm / %	
I_{OUT}	Output Leakage Current		10.0	nA	I_{OUT1} only
R_{IN}	Input Resistance	2.5	7.5	KΩ	
V_{IH}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.0	mA	V_{IN} = V_{IL} or V_{IH}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 165 mils, Y = 167 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. DB4	9. DB12	17. V_{DD}*
2. DB5	10. DB13	18. AGND
3. DB6	11. DB14	19. LSB LATCH
4. DB7	12. DB15	20. MSB LATCH
5. DB8	13. V_{REF}	21. DB0 (LSB)
6. DB9	14. R_{FB}	22. DB1
7. DB10	15. I_{OUT2}	23. DB2
8. DB11	16. I_{OUT1}	24. DB3

*Connect pin 17 first

MP7628 DIE

8-Bit Multiplying Quad
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
V_{DD} to AGND ..... 0 V, +7 V
V_{DD} to DGND ..... 0 V, +7 V
Digital Input Voltage to DGND ..... –0.5 V, +7 V
V_{PIN2}, V_{PIN20} to AGND ..... –0.5 V, +7 V
$V_{REFA,B,C,D}$ to AGND ..... ±25 V
$VR_{FBA,B,C,D}$ to AGND ..... ±25 V
T_J (maximum) ..... +150°C

Ordering Information

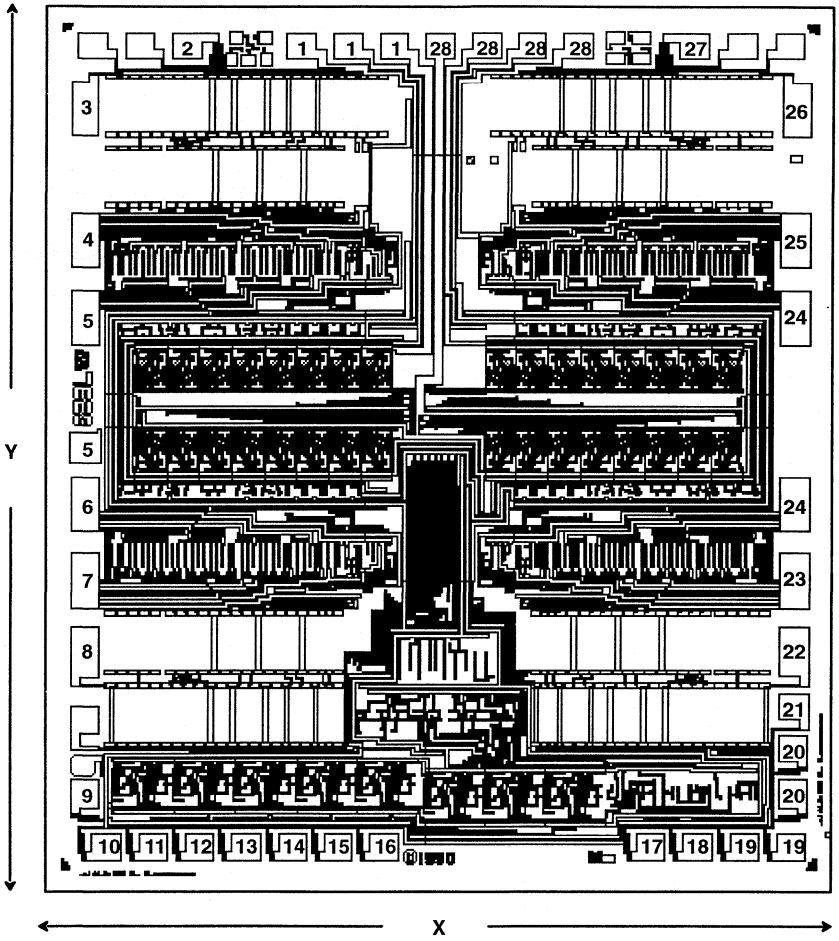
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7628J-DIE	0.5	0.5	4
MP7628K-DIE	0.25	0.25	2

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		0.5	LSB	End Point Linearity
DNL	Differential Non-Linearity		0.5	LSB	
GE	Gain Error		4	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		200	ppm / %	Using Internal R_{FB}
I_{OUT}	Output Leakage Current		50	nA	
R_{IN}	Input Resistance	12	28	K Ω	
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1	µA	
I_{DD}	Supply Current		50	µA	Inputs @ 0 V, 5 V

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 127 mils, Y = 144 mils
Pad Size	4 x 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. V_{DD}*
2. V_{REFA}
3. R_{FBA}
4. I_{OUT1A}
5. $I_{OUT2A/2B}$
6. I_{OUT1B}
7. R_{FBB}
8. V_{REFB}
9. DB0 (LSB)
10. DB1
11. DB2
12. DB3
13. DB4
14. DB5
15. DB6
16. DB7 (MSB)
17. A/$\overline{B}$
18. R/$\overline{W}$
19. $\overline{DS1}$
20. $\overline{DS2}$
21. V_{REFD}
22. R_{FBD}
23. I_{OUT1D}
24. $I_{OUT2C/2D}$
25. I_{OUT1C}
26. R_{FBC}
27. V_{REFC}
28. V_{SS}

* Bond Pin #1 First

MP7633 DIE

10-Bit Multiplying
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND .. −0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND . −0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

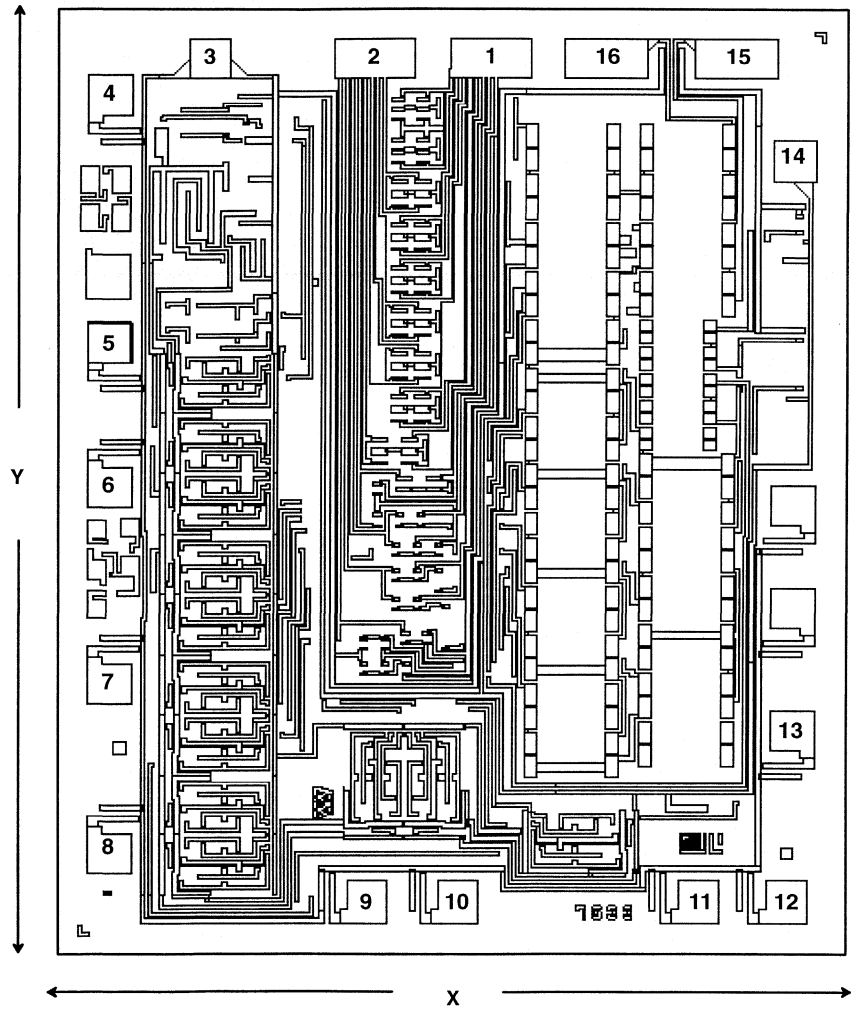
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7633K-DIE	1.0	1.0	16.0

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	10		Bits	
INL	Relative Accuracy		1.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		1.0	LSB	
GE	Gain Error		16.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		50	ppm / %	
I_{OUT}	Output Leakage Current		10.0	nA	
R_{IN}	Input Resistance	5.0	20.0	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.0	mA	V_{IN} = 0, 5 V

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 86 mils, Y = 105 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT1}
2. I_{OUT2}
3. V_{SS}
4. BIT 1 (MSB)
5. BIT 2
6. BIT 3
7. BIT 4
8. BIT 5
9. BIT 6
10. BIT 7
11. BIT 8
12. BIT 9
13. BIT 10 (LSB)
14. $V_{DD(+)}$*
15. V_{REF}
16. R_{FB}

*Connect Pin 14 First

MP7636A DIE

16-Bit Microprocessor Compatible, Double-Buffered
Multiplying Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +17 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... –0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

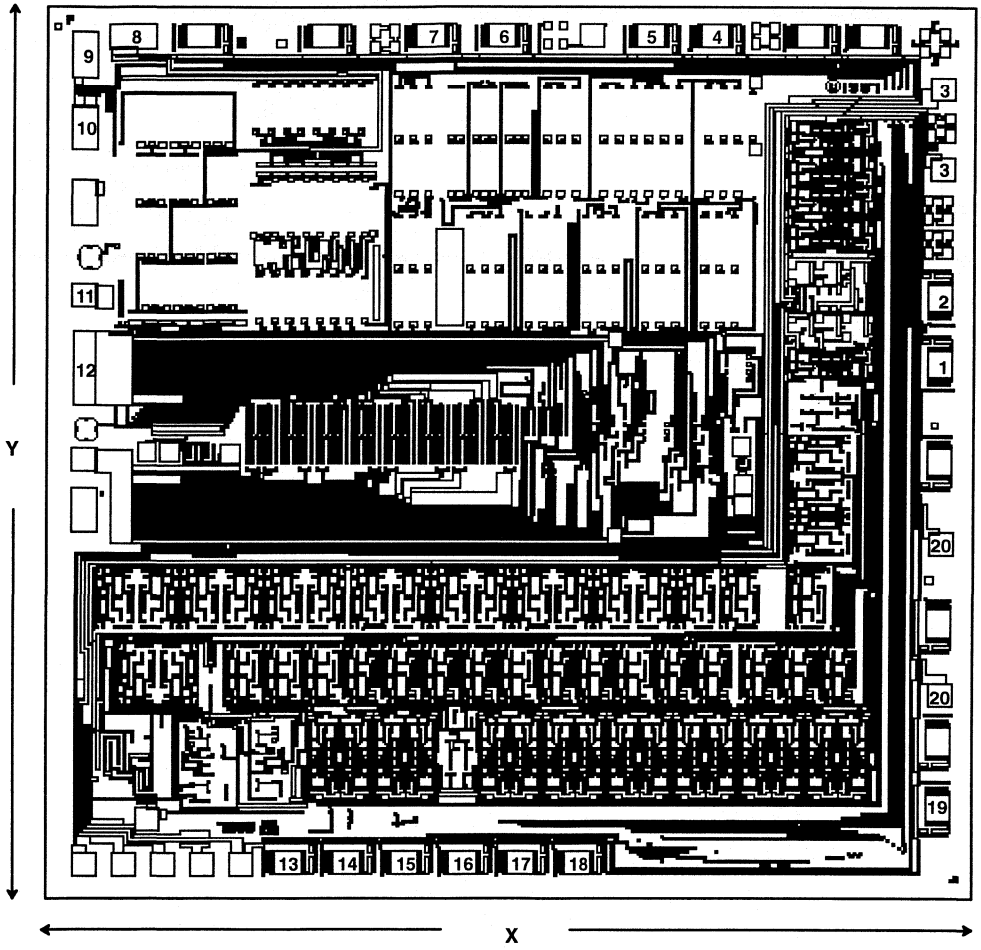
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (%)
MP7636AJ-DIE	4.0	4.0	1.0

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	16		Bits	
INL	Relative Accuracy		4.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		4.0	LSB	
GE	Gain Error		0.025	%	
PSRR	Power Supply Rejection Ratio		50	ppm / %	
I_{OUT}	Output Leakage Current		10.0	nA	I_{OUT1} only
R_{IN}	Input Resistance	2.5	7.5	KΩ	
V_{IH}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		2.0	mA	V_{IN} = V_{IL} or V_{IH}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 165 mils, Y = 167 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. $\overline{CS}$
2. $\overline{WR1}$
3. AGND
4. DB11 (DB3)
5. DB10 (DB2)
6. DB9 (DB1)
7. DB8 (DB0)
8. V_{REF}
9. R_{FB}
10. DGND
11. I_{OUT1}
12. I_{OUT2}
13. DB15 (DB7)
14. DB14 (DB6)
15. DB13 (DB5)
16. DB12 (DB4)
17. $\overline{XFER}$
18. $\overline{WR2}$
19. BYTE1/$\overline{BYTE2}$
20. V_{DD}*

*Bond pin 20 first

MP7641 DIE

8-Channel High-Speed Non-Linearity
10 MHz Input Bandwidth 8-Bit
DACs with Output Buffer and Serial Digital
Data Port, BiCMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{CC} to AGND ..... +6.5 V
V_{EE} to AGND ..... –6.5 V
V_{CC} to DGND ..... +13.0 V
V_{EE} to DGND ..... –6.5 V
V_{Ri} to GND ..... V_{CC} to V_{EE}
V_{Oi} to GND ..... V_{CC} to V_{EE}
Digital Input & Output Voltage to DGND –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

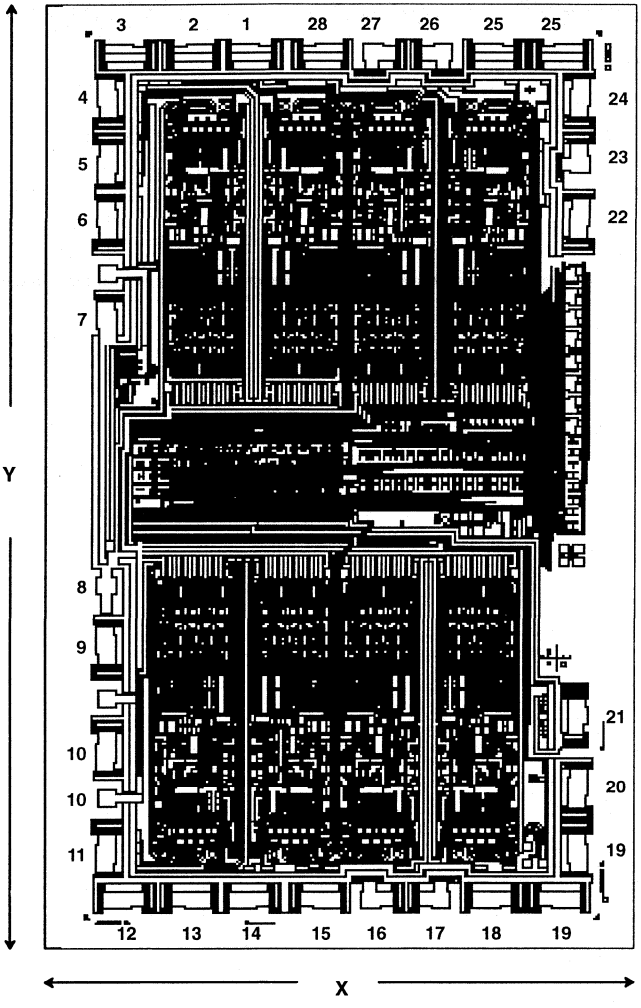
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (% FSR)
MP7641A-DIE	1.0	0.8	1.5

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{CC} = 5 V, V_{EE} = –5 V, V_{REF} = 3 V, Output Load Open, AGND = DGND = 0 V

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		±1	LSB	Best Straight Line
DNL	Differential Non-Linearity		±0.8	LSB	
GE	Gain Error		±1.5	% FSR	
PSRR	Power Supply Rejection Ratio		0.02	% / %	
R_{IN}	Input Resistance	6	18	KΩ	
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		±10	µA	
I_{CC}	Supply Current		30	mA	
I_{EE}	Supply Current		–30	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 127 mils, Y = 223 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{EE}

Pad Designations

1.	V_{O1}	8.	V_{EE}	15.	V_{O6}	22.	CLK
2.	V_{O2}	9.	AGND	16.	V_{R6}	23.	$\overline{LD}$
3.	V_{R2}	10.	DGND	17.	V_{R7}	24.	$\overline{RST}$
4.	V_{R3}	11.	V_{O4}	18.	V_{O7}	25.	AGND
5.	V_{O3}	12.	V_{R4}	19.	AGND	26.	V_{O0}
6.	V_{DD}	13.	V_{R5}	20.	SDI	27.	V_{R0}
7.	V_{CC}	14.	V_{O6}	21.	SDO	28.	V_{R1}

*Bond Pin 8 first

MP7645B DIE

Buffered Multiplying 12-Bit
Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... ±17 V
V_{REF} to GND ..... ±25 V
Digital Input Voltage (V_{IN}) to GND
..... GND –0.5 V to V_{DD} +0.5 V
V_{OUT} to GND ..... GND –0.5 V to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

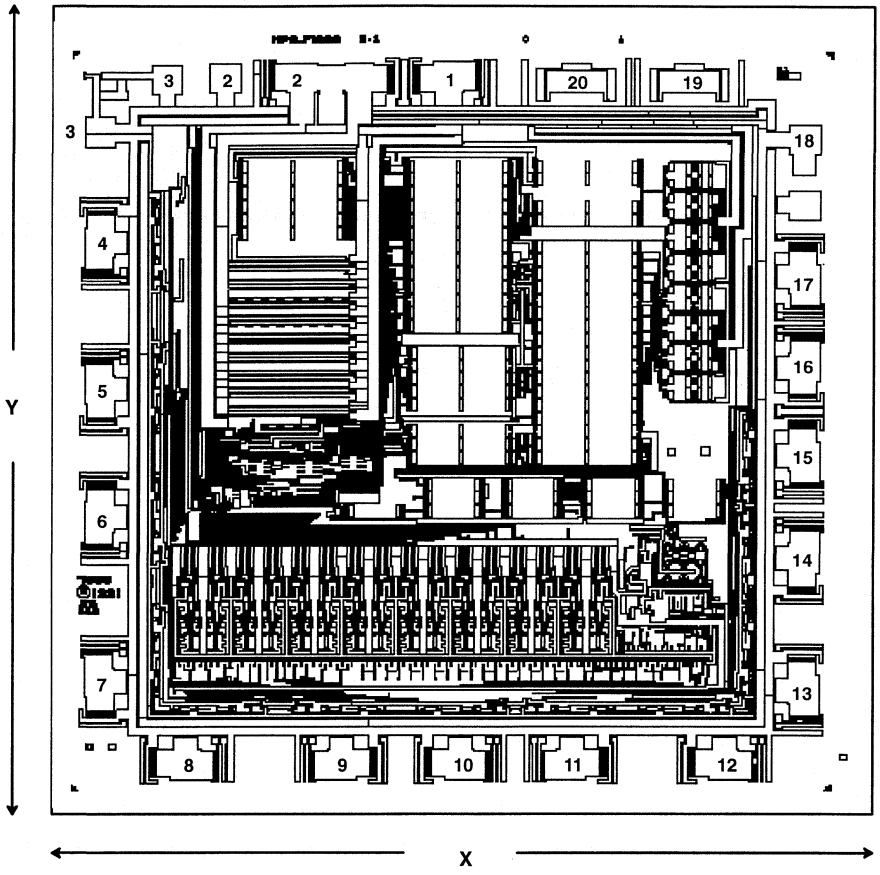
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7645BK-DIE	1	1	8

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 15 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		1	LSB	
DNL	Differential Non-Linearity		1	LSB	
GE	Gain Error		8	LSB	
PSRR	Power Supply Rejection Ratio		±50	ppm / %	
I_{LKG}	Output Leakage Current		±10	nA	
R_{IN}	Input Resistance	7	25	KΩ	
V_{IN}	Logic "1"	3.0		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		±1	µA	
I_{DD}	Supply Current		1	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 115.75 mils, Y = 114.57 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. I_{OUT}
2. AGND
3. DGND
4. DB11 (MSB)
5. DB10
6. DB9
7. DB8
8. DB7
9. DB6
10. DB5
11. DB4
12. DB3
13. DB2
14. DB1
15. DB0
16. $\overline{CS}$
17. $\overline{WR}$
18. V_{DD}*
19. V_{REF}
20. R_{FB}

*Bond pin 18 first

MP7680 DIE

12-Bit Quad Double-Buffered
Multiplying Digital-to-Analog Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +7 V
V_{REF} to GND ..... +25 V
Digital Input Voltage (V_{IN}) to GND ... –0.5 to V_{DD} +0.5 V
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND .. –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

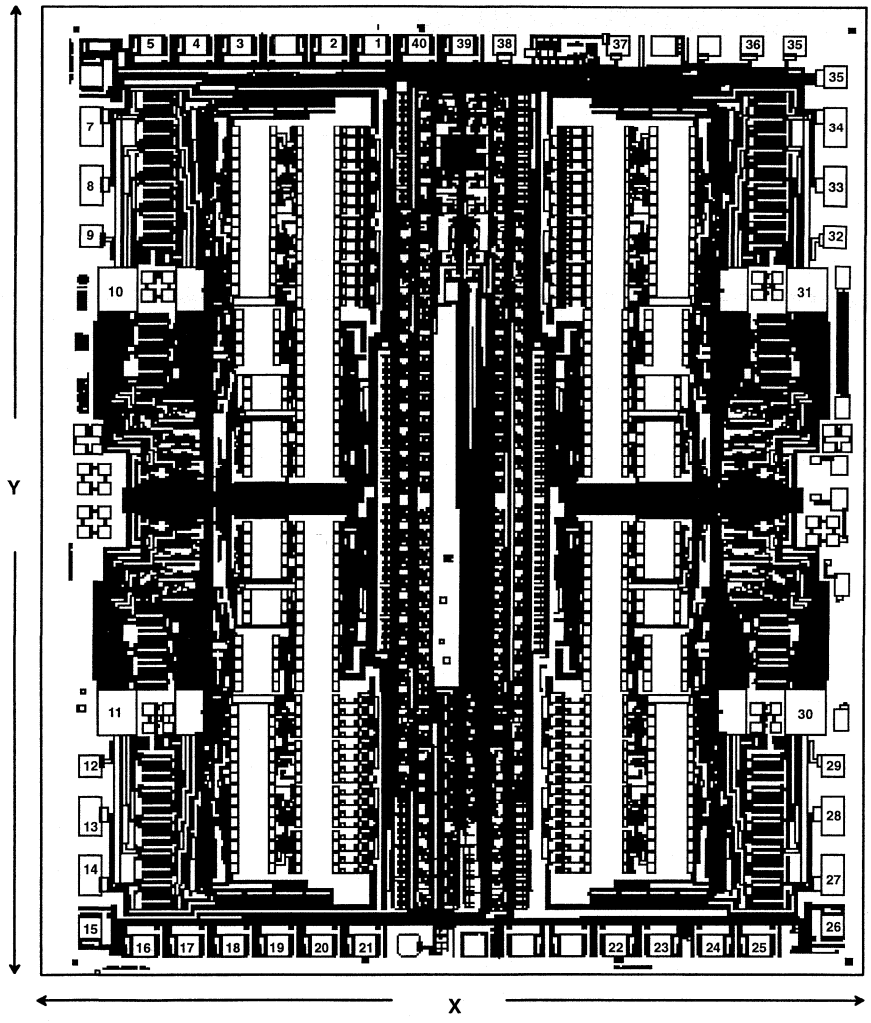
Part No.	Parameters		
	INL (LSB)	DNL (LSB)	GE (LSB)
MP7680J-DIE	2.0	4.0	16.0
MP7680K-DIE	1.0	2.0	16.0

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 10 V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		2.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		4.0	LSB	
GE	Gain Error		16.0	LSB	Using Internal R_{FB}
PSRR	Power Supply Rejection Ratio		50	ppm / %	
I_{OUT}	Output Leakage Current		50.0	nA	
R_{IN}	Input Resistance	3.0	7.0	KΩ	
V_{IN}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
I_{LKG}	Input Leakage Current		1.0	µA	
I_{DD}	Supply Current		1.0	mA	Inputs 0 V or V_{DD}

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 169 mils, Y = 206 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. A1
2. $\overline{XFER}$
3. $\overline{WR2}$
4. $\overline{WR1}$
5. $\overline{CS}$
6. NC
7. V_{REFA}
8. R_{FBA}
9. I_{OUT1A}
10. I_{OUT2A}
11. I_{OUT2B}
12. I_{OUT1B}
13. R_{FBB}
14. V_{REFB}
15. DB11 (MSB)
16. DB10
17. DB9
18. DB8
19. DB7
20. DB6
21. DB5
22. DB4
23. DB3
24. DB2
25. DB1
26. DB0 (LSB)
27. V_{REFC}
28. R_{FBC}
29. I_{OUT1C}
30. I_{OUT2C}
31. I_{OUT2C}
32. I_{OUT2D}
33. R_{FBD}
34. V_{REFD}
35. AGND
36. DGND
37. AV_{DD}*
38. DV_{DD}
39. B1/$\overline{B2}$
40. A0

*Connect Pin 37 First

MP7683 DIE

8-Bit Flash
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 0 V, +7 V
V_{REF} to GND ..... +7 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65 to +150°C

Ordering Information

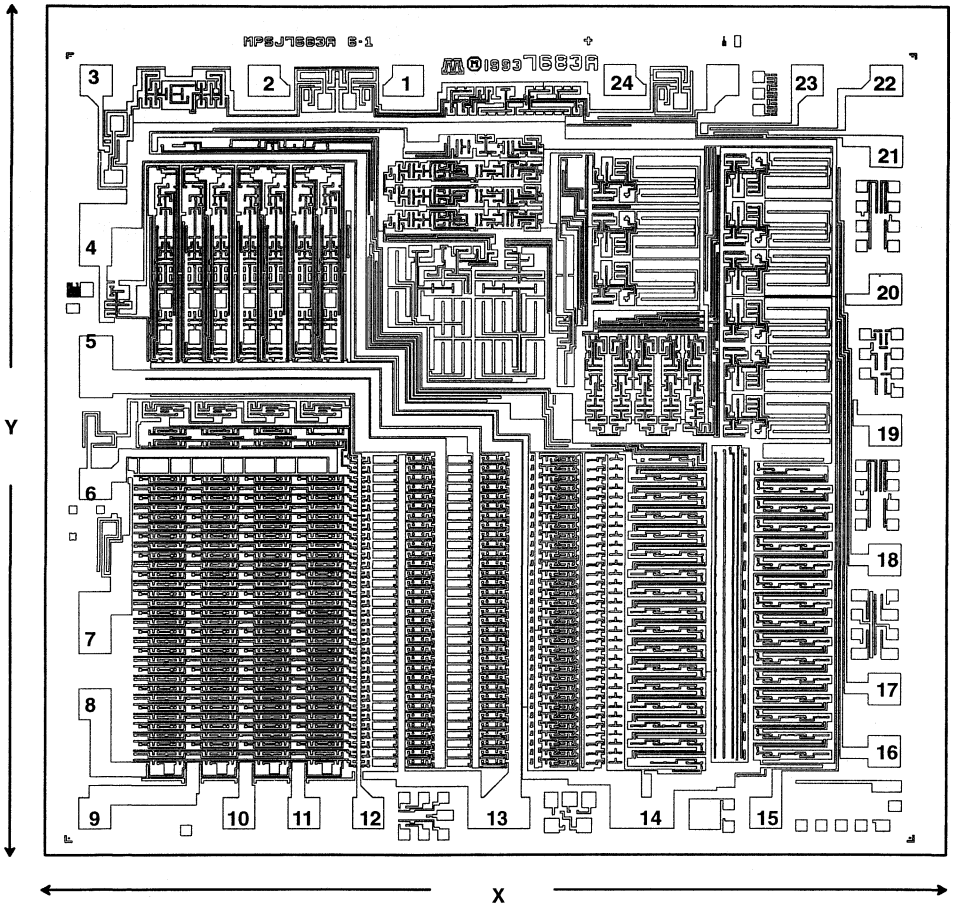
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP7683J-DIE	1.0	1.0

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 4.1 V, F_S = 3 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		1.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		1.0	LSB	
I_{O2}	Output Leakage Current	–50.0	+50.0	µA	
R_{IN}	Ref. Resistance	500	1500	Ω	
V_{IN}	Logic "1"	3.5		V	
V_{IL}	Logic "0"		1.5	V	
V_{OH}	Digital o/p, Logic "1"	V_{DD}-.4		V	I_L = 1 mA
V_{OL}	Digital o/p, Logic "0"		0.4	V	I_L = 2 mA
I_{DD}	Supply Current		20.0	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 104 mils, Y = 110 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. OE2	9. R2	17. DB2
2. ϕ	10. R3	18. DB3
3. CLK	11. R4	19. DB4
4. V_{DD}*	12. V_{IN}	20. DB5
5. AV_{DD}	13. AGND	21. DB6
6. $V_{REF(+)}$	14. DGND	22. DB7
7. $V_{REF(-)}$	15. DB0	23. OFW
8. R1	16. DB1	24. $\overline{OE1}$

*Connect pin 4 first

MP7684A DIE

8-Bit Flash
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... +8 V
$V_{REF(+)}$ and $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
VIN ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
T_J (maximum) ..... 150°C

Ordering Information

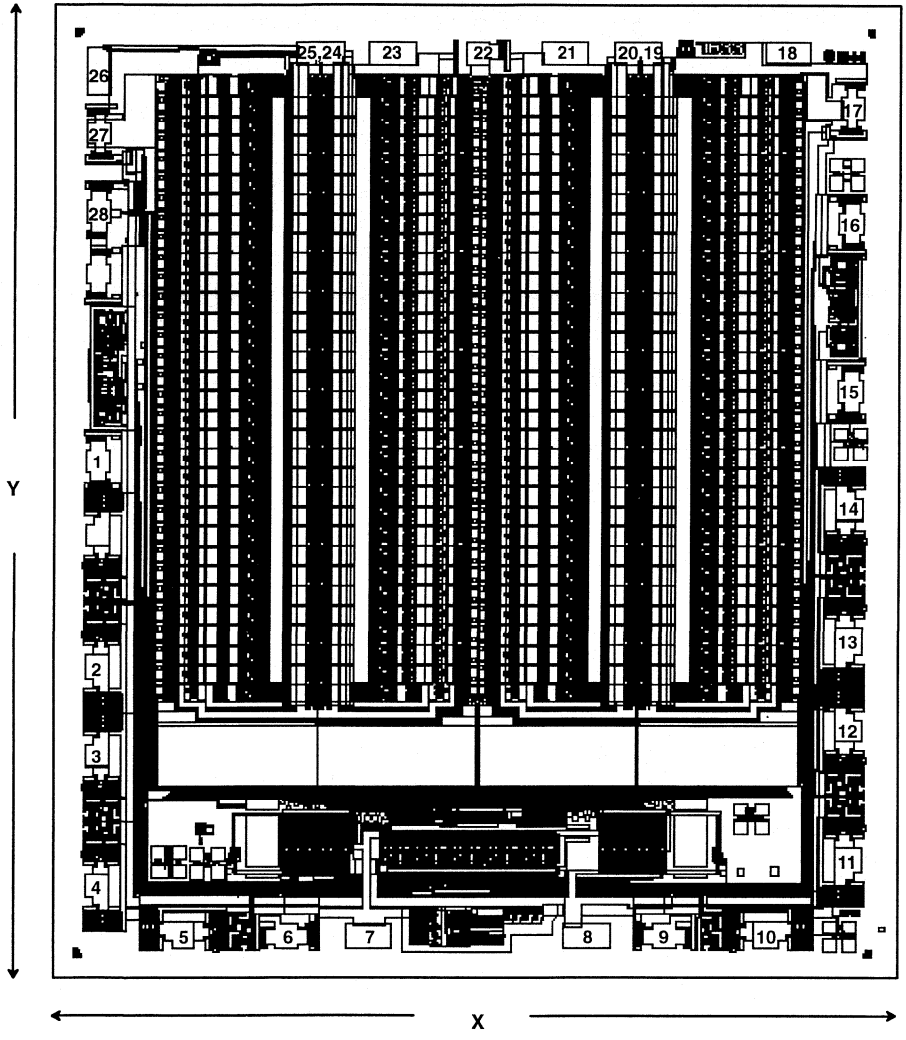
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP7684AJ-DIE	2.0	2.0

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 4.1 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		2.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		2.0	LSB	
I_{O2}	Output Leakage Current	–10.0	10.0	µA	
R_{IN}	Input Resistance	170	300	Ω	
V_{IH}	Logic "1"	2		V	
V_{IL}	Logic "0"	0.8		V	
V_{OH}	Digital o/p, Logic "1"	V_{DD}–0.5		V	I_L = 4 mA
V_{OL}	Digital o/p, Logic "0"		0.4	V	I_L = 4 mA
I_{DD}	Supply Current		70	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 158 mils, Y = 186 mils
Pad Size	4 x 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. CLK	8. DGND	15. OE2	22. 1/2 R
2. DB7	9. 3/4 R	16. $\overline{OE1}$	23. AV_{DD}
3. DB6	10. DB3	17. $V_{REF(+)}$	24. AGND
4. DB5	11. DB2	18. AV_{DD}	25. AGND
5. DB4	12. DB1	19. AGND	26. AV_{DD}
6. 1/4 R	13. DB0	20. AGND	27. $V_{REF(-)}$
7. DV_{DD}*	14. OFW	21. AV_{DD}	28. V_{IN}

* Bond pin #7 first

MP7686 DIE

6-Bit Flash
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... +7 V
$V_{REF(+)}$ and $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
TJ (maximum) ..... 150°C

Ordering Information

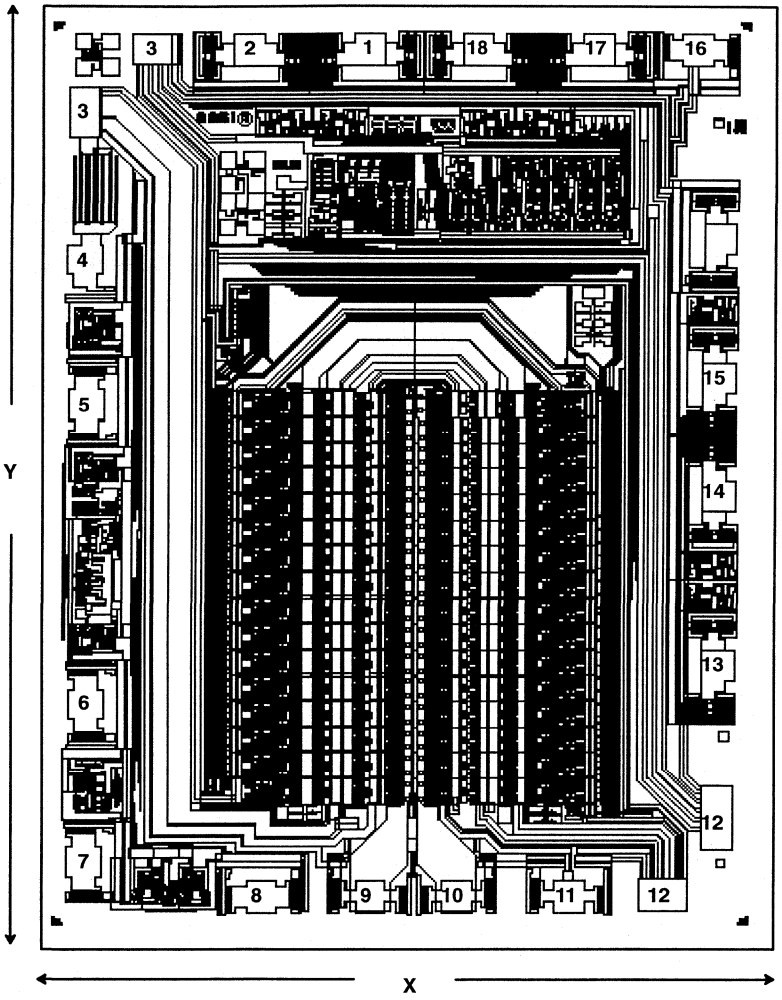
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP7686J-DIE	1.5	0.75

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 4.6 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	6		Bits	
INL	Relative Accuracy		1.5	LSB	Best Straight Line
DNL	Differential Non-Linearity		0.75	LSB	
I_{O2}	Output Leakage Current	–10.0	10.0	µA	
R_{IN}	Ref. Resistance	170	265	Ω	
V_{IH}	Logic "1"	2.4		V	
V_{IL}	Logic "0"		0.8	V	
V_{OH}	Digital o/p, Logic "1"	V_{DD}-.5		V	I_L = 4.0 mA
V_{OL}	Digital o/p, Logic "0"		0.4	V	I_L = 4.0 mA
I_{DD}	Supply Current		40.0	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 105.1 mils, Y = 138.6 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. DB5
2. OFW
3. GND
4. MODE/ZENER
5. OE2
6. $\overline{OET}$
7. CLK
8. PHASE
9. $V_{REF(+)}$
10. $V_{REF(-)}$
11. V_{IN}
12. V_{DD}*
13. DB0
14. DB1
15. DB2
16. $V_{REF\ (CTR)}$
17. DB3
18. DB4

*Connect pin 12 first

MP7690A DIE

8-Bit Flash
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... +8 V
$V_{REF(+)}$ and $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
T_J (maximum) ..... 150°C

Ordering Information

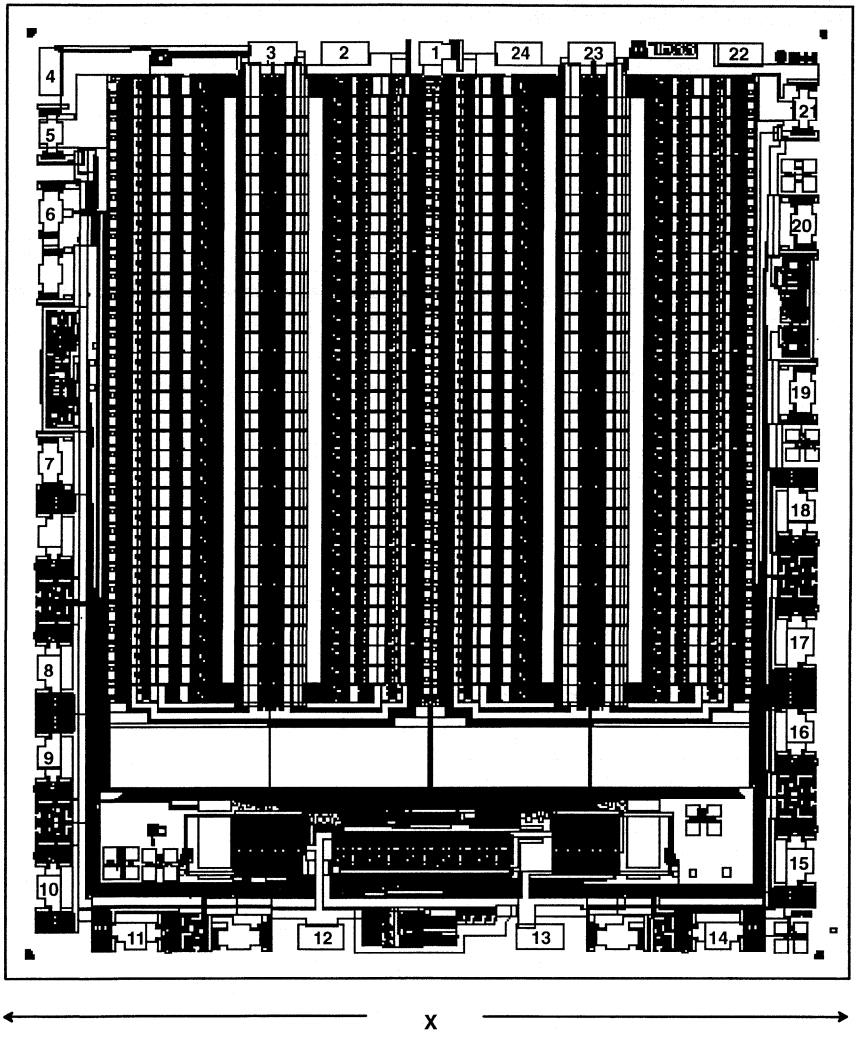
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP7690AJ-DIE	2.0	2.0

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 4.1 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		2.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		2.0	LSB	
I_{O2}	Output Leakage Current	–10.0	10.0	µA	
R_{IN}	Input Resistance	170	300	Ω	
V_{IH}	Logic "1"	2		V	
V_{IL}	Logic "0"	0.8		V	
V_{OH}	Digital o/p, Logic "1"	V_{DD}–0.5		V	I_L = 4 mA
V_{OL}	Digital o/p, Logic "0"		0.4	V	I_L = 4 mA
I_{DD}	Supply Current		70	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 158 mils, Y = 186 mils
Pad Size	4 x 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. 1/2 R
2. AV_{DD}
3. AGND
4. AV_{DD}
5. $V_{REF(-)}$
6. V_{IN}
7. CLOCK
8. DB7
9. DB6
10. DB5
11. DB4
12. DV_{DD}
13. DGND
14. DB3
15. DB2
16. DB1
17. DB0
18. OFW
19. OE2
20. $\overline{OE1}$
21. $V_{REF(+)}$
22. AV_{DD}
23. AGND
24. AV_{DD}

*Connect Pin 12 first

MP7695 DIE

10-Bit Low Power
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} (to GND) ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
T_J (maximum) ..... +150°C

Ordering Information

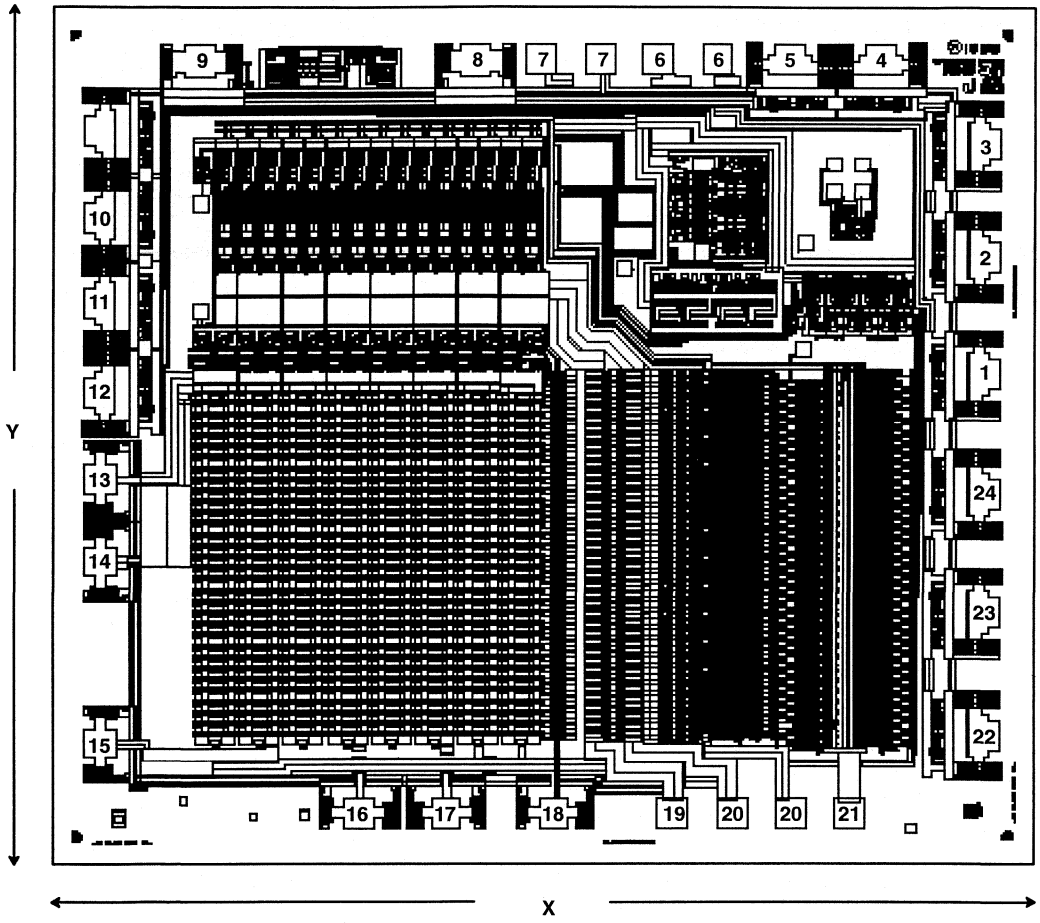
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP7695J-DIE	2.0	2.0

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 4.6 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	10		Bits	
INL	Relative Accuracy		2.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		2.0	LSB	
I_{O2}	Output Leakage Current	–10.0	10.0	µA	
R_{IN}	Ref. Resistance	420	980	KΩ	
V_{IN}	Logic "1"	2.0		V	
V_{IL}	Logic "0"		0.8	V	
V_{OH}	Digital o/p, Logic "1"	V_{DD}-.5		V	I_L = 2.0 mA
V_{IL}	Digital o/p, Logic "0"		0.4	V	I_L = 4.0 mA
I_{DD}	Supply Current		20.0	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 130 mils, Y = 148 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. DB3	9. $\overline{OE}$	17. R3
2. DB4	10. DB8	18. V_{IN}
3. DB5	11. DB9	19. AGND
4. DB6	12. OFW	20. AV_{DD}*
5. DB7	13. $V_{REF(+)}$	21. AGND
6. DGND	14. $V_{REF(-)}$	22. DB0
7. DV_{DD}	15. R1	23. DB1
8. CLK	16. R2	24. DB2

*Connect pin 20 first

MP8782 DIE

Monolithic 10-Bit High Speed
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... +7 V
V_{TOP} and V_{BOT} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
T_J (maximum) ..... 150°C

Ordering Information

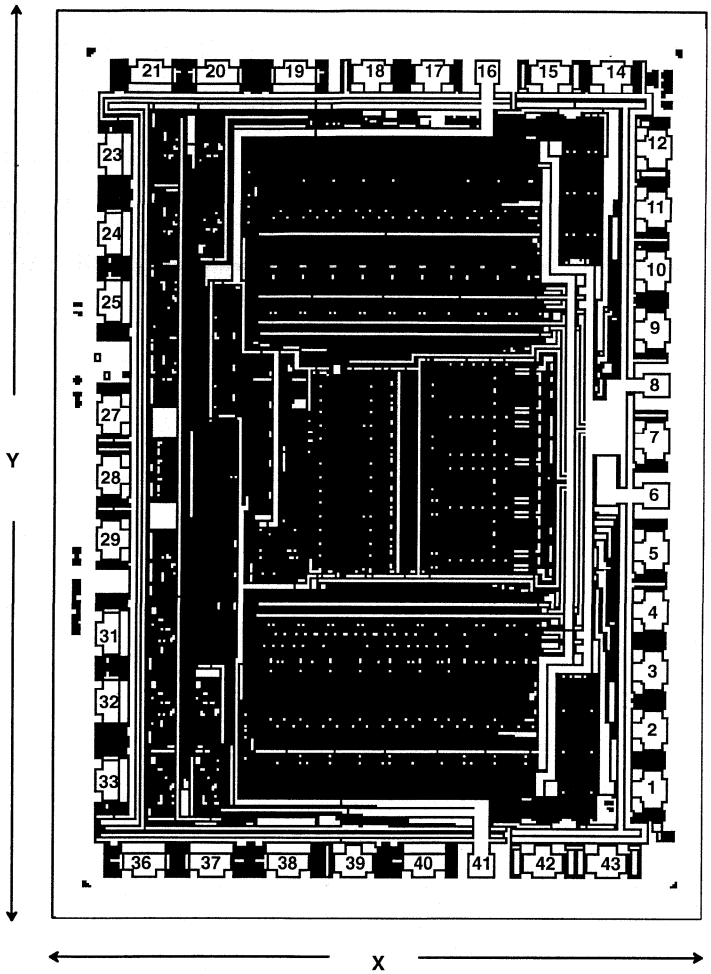
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP8782A-DIE	2	1

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{TOP} = 4 V, V_{BOT} = 1 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	10		Bits	
INL	Relative Accuracy		2	LSB	Best Fit Line
DNL	Differential Non-Linearity		1	LSB	
I_{LKG}	Tristate Leakage Current		5	µA	
R_{IN}	Input Resistance	0.2	0.8	KΩ	
V_{IH}	Logic "1"	4.1	5.0	V	
V_{IL}	Logic "0"	–0.10	0.75	V	
V_{OH}	Logical "1" Voltage	4.5		V	I_{SOURCE} = 1 mA
V_{OL}	Logical "0" Voltage		0.4	V	I_{SINK} = 1 mA
I_{LKG}	Input Leakage Current		20	µA	
I_{DD}	Supply Current		45	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 127 mils, Y = 184 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{SS} (DGND, AGND)

Pad Designations

1. V_{RT}	12. V_{RBS}	23. DB2	34. N/C
2. R7	13. N/C	24. DB3	35. N/C
3. R6	14. V_{RB}	25. DB4	36. DB8
4. R5	15. BRES1	26. N/C	37. DB9
5. R4	16. DGND*	27. PHASE	38. OFW
6. AV_{DD}	17. OE2	28. LINV	39. CLK
7. A_{IN}	18. $\overline{OE1}$	29. MINV	40. APERTURE
8. AGND*	19. UFW	30. N/C	41. DV_{DD}
9. R3	20. DB0	31. DB5	42. TRES1
10. R2	21. DB1	32. DB6	43. VRTS
11. R1	22. N/C	33. DB7	

*Bond pins 8 and 16 first

MP8785 DIE

Monolithic 8-Bit Flash
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... +7 V
V_{REF} to GND ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
T_J (maximum) ..... 150°C

Ordering Information

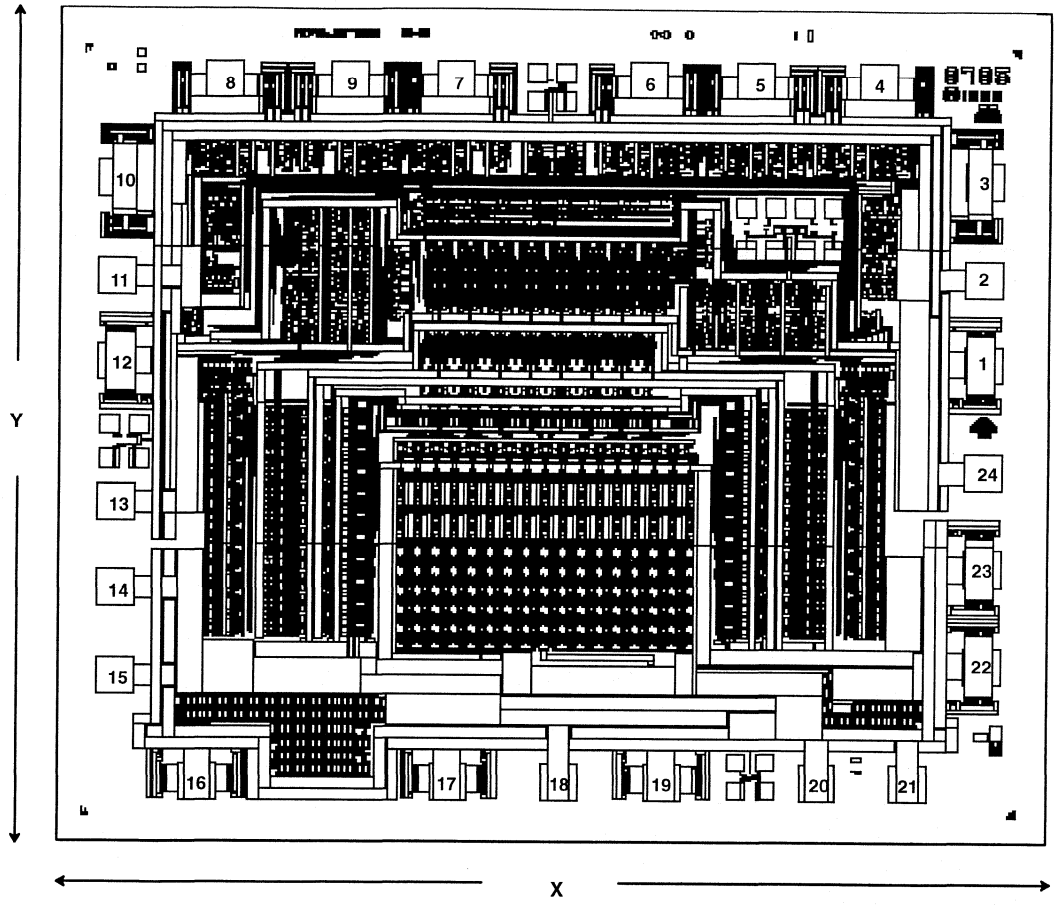
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP8785A-DIE	1.5	1

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, $V_{REF(+)}$ = 2.6 V, $V_{REF(-)}$ = 0.6 V, F_S = 2 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	8		Bits	
INL	Relative Accuracy		1.5	LSB	Best Straight Line
DNL	Differential Non-Linearity		1.0	LSB	
I_{LKG}	Output Leakage Current		20	µA	
R_{IN}	Input Resistance	200	800	KΩ	
V_{IN}	Logic "1"	V_{DD} –0.5		V	
V_{IL}	Logic "0"		0.8	V	
V_{OH}	Logical "1" Voltage	4.5		V	
V_{OL}	Logical "0" Voltage		0.4	V	
I_{LKG}	Input Leakage Current	–4.5	4.5	µA	
I_{DD}	Supply Current		20	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 133 mils, Y = 109 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{SS} (DGND, AGND)

Pad Designations

1.	$\overline{OE}$	8.	DB5	15.	V_{DD}	22.	VRBS
2.	DGND*	9.	DB6	16.	VRTS	23.	VRB
3.	DB0	10.	DB7	17.	VRT	24.	DGND*
4.	DB1	11.	V_{DD}	18.	V_{DD}		
5.	DB2	12.	CLK	19.	V_{IN}		
6.	DB3	13.	V_{DD}	20.	AGND*		
7.	DB4	14.	V_{DD}	21.	AGND*		

*Bond pins 2, 20, 21 and 24 first

MP8790 DIE

Monolithic 12-Bit
Flash Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 7 V
VRT and VRB ..... V_{DD} +0.5 V to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 V to GND –0.5 V
All Inputs ..... V_{DD} +0.5 V to GND –0.5 V
All Outputs ..... V_{DD} +0.5 V to GND –0.5 V
T_J (maximum) ..... 150°C

Ordering Information

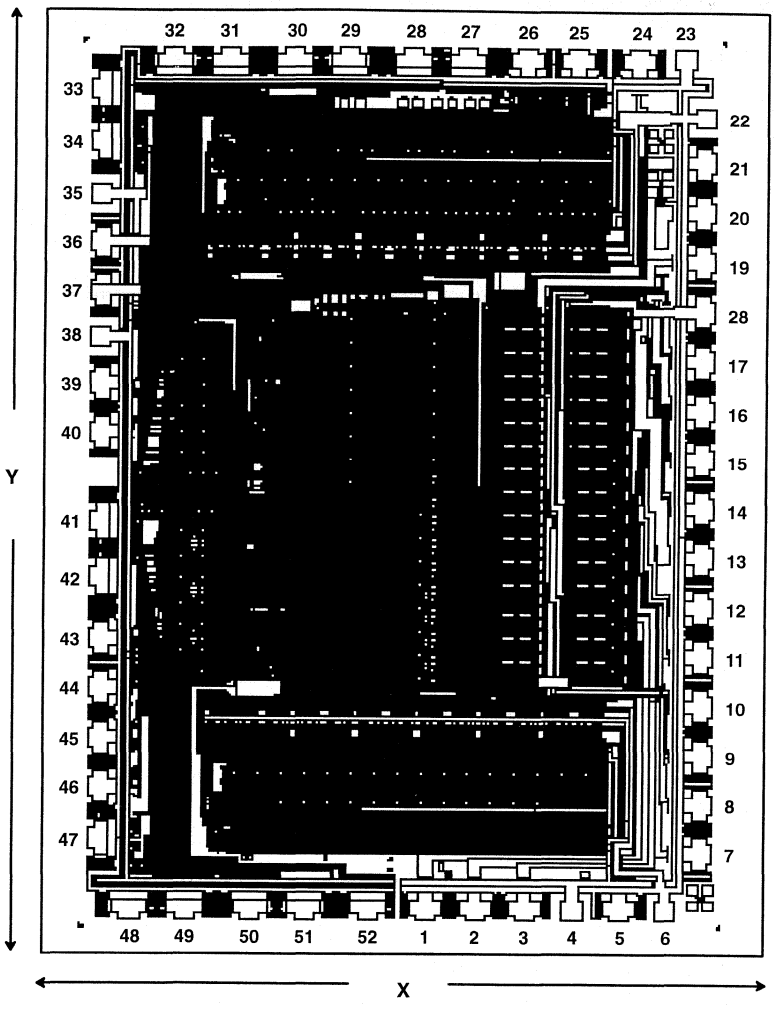
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP8790A-DIE	4	4

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{RT} = 5 V, V_{RB} = 0 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	12		Bits	
INL	Relative Accuracy		4	LSB	
DNL	Differential Non-Linearity		4	LSB	
I_{LKG}	Output Leakage Current		25	nA	
R_{IN}	Input Resistance	200	800	KΩ	
V_{IN}	Logic "1"	4.35	5.1	V	I_{SOURCE} = 1.5mA
V_{IL}	Logic "0"	–0.10	0.80	V	I_{SINK} = 4 mA
V_{OH}	Logical "1" Voltage	–0.5		V	
V_{OL}	Logical "0" Voltage		0.5	V	
I_{LKG}	Input Leakage Current		25	µA	
I_{DD}	Supply Current		45	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 168.9 mils, Y = 229.5 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{SS}

*Bond pins 23, 37 and 38 first

Pad Designations

1. R7
2. R9
3. R5
4. $V_{SS}3$
5. V_{IN}
6. $V_{DD}3$
7. R8
8. R10
9. R12
10. R11
11. R3
12. R13
13. R14
14. R1
15. R15
16. R2
17. R6
18. VRB
19. VRT
20. R16
21. $V_{DD}4$
22. $V_{DD}2$
23. $V_{SS}2$*
24. $V_{SS}4$
25. MINV
26. LINV
27. UFW
28. D0
29. D1
30. D2
31. D3
32. D4
33. D5
34. SDO
35. $V_{DD}1$
36. $V_{DD}5$
37. $V_{SS}5$*
38. $V_{SS}1$*
39. PHASE
40. SCK
41. APERTURE
42. OFW
43. OE2
44. $\overline{OE}$
45. CLK
46. $\overline{PLOAD}$
47. D6
48. D7
49. D8
50. D9
51. D10
52. D11

MP8799 DIE

Monolithic Very Low Power 10-Bit
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} to GND ..... 7 V
V_{REF} to GND ..... 7 V
V_{IN} ..... 7 V
All Inputs ..... V_{DD} –0.5 to V_{DD} +0.5 V
All Outputs ..... V_{DD} –0.5 to V_{DD} +0.5 V
Digital Input Voltage (V_{IN}) to GND
..... V_{DD} –0.5 to V_{DD} +0.5 V
T_J (maximum) ..... 150°C

Ordering Information

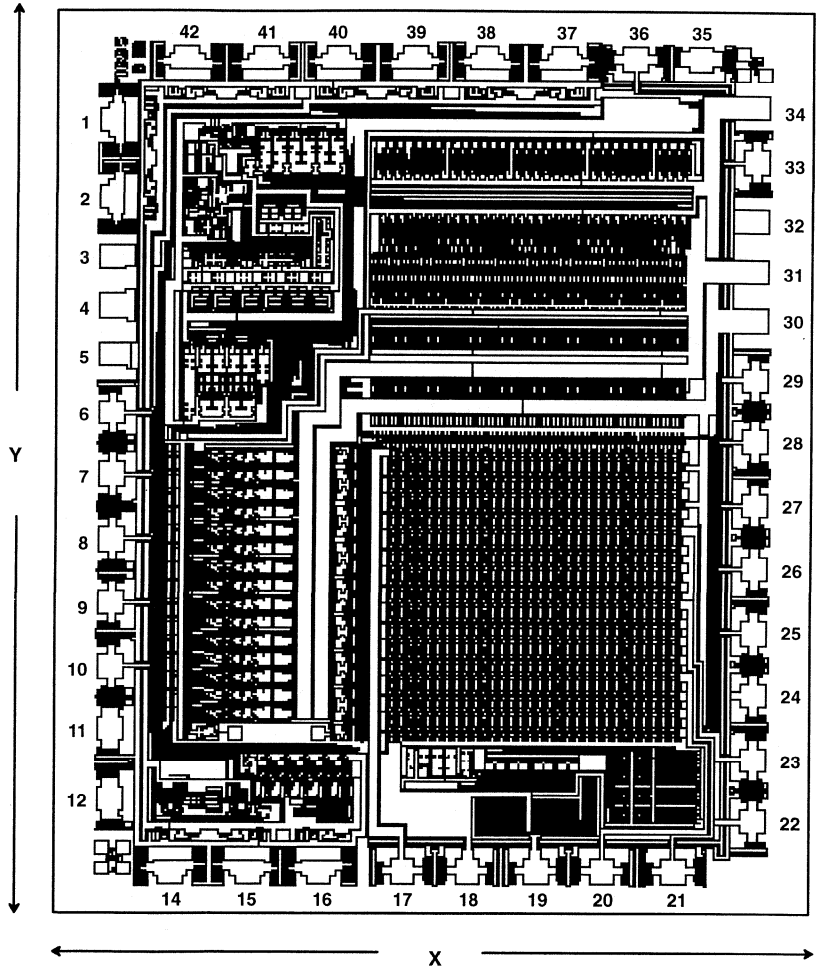
Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP8799A-DIE	2.0	1.5

Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 4.6 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	10		Bits	
INL	Relative Accuracy		2.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		1.5	LSB	
I_{LKG}	Output Leakage Current	–30.0	30.0	µA	
R_{IN}	Input Resistance	0.6	1.4	KΩ	
V_{IH}	Logic "1"	4.0		V	
V_{IL}	Logic "0"		0.8	V	
V_{OH}	Logical "1" Voltage	V_{DD}–0.5		V	
V_{OL}	Logical "0" Voltage		0.4	V	
I_{LKG}	Input Leakage Current	–20.0	20.0	µA	
I_{DD}	Supply Current		10	mA	

NOTES:
1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 130 mils, Y = 163 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. DB6	9. A1	18. $V_{REF(-)}$	26. $A_{IN}2$	34. AGND
2. DB7	10. A0	19. $V_{REF1(-)}$	27. $A_{IN}3$	35. PD
3. DGND	11. CLK	20. R1	28. $A_{IN}4$	36. $A_{IN}7$
4. DGND	12. $\overline{OE}$	21. R2	29. $A_{IN}5$	37. DB0
5. DV_{DD}*	14. DB8	22. $A_{IN}8$	30. AGND	38. DB1
6. $\overline{CLR}$	15. DB9	23. R3	31. AV_{DD}*	39. DB2
7. $\overline{WR}$	16. OFW	24. A_{IN}	32. AV_{DD}*	40. DB3
8. A2	17. $V_{REF(+)}$	25. $A_{IN}1$	33. $A_{IN}6$	41. DB4
				42. DB5

*Bond pins 5, 31 & 32 first

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Section 8

Application & Design Notes

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INTRODUCTION

A Digital-to-Analog Converter (DAC) is a circuit which changes a finite number of diverse digital codes into the same number of related analog levels. A DAC's resolution determines the number of digital codes which the device can convert into discrete analog values. An N-bit binary coded DAC converts 2^N digital codes into the same number of corresponding analog outputs.

CMOS DACs use MOSFET analog switches to connect binary weighted current sources to one of two outputs. These bidirectional switches enable the user to apply a positive or negative reference voltage for 2-quadrant multiplication. The addition of an output operational amplifier converts the output current into voltage. Also, full 4-quadrant multiplication may be achieved by using another op amp and 3 resistors.

Circuit Description

EXAR's monolithic CMOS 12-bit DAC uses a decoded 2 most significant bits to 3 segments network, plus an inverted R-2R resistor ladder network for the 10 least significant bits (LSBs), and 13 N-channel current switches. Other resolutions are similar. Switch driving circuits, decoding and interface logic complete the circuit. When a reference voltage is applied, the low tempco, matched thin-film resistors and switches deliver the resulting binary weighted, code dependent current to either the I_{OUT1} port or the I_{OUT2} port. The addition of an external op amp converts the output current to voltage. *Figure 1.* shows a simplified schematic of a typical 12-bit circuit.

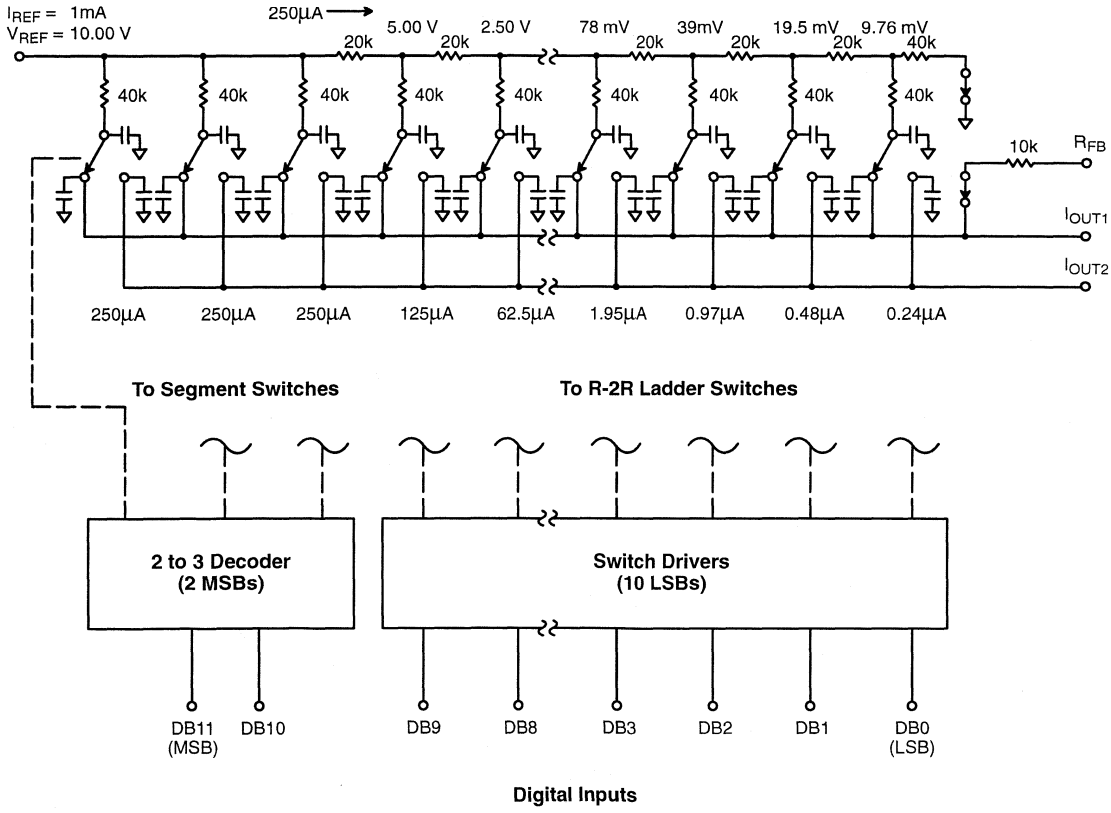

Figure 1. Typical CMOS 12-Bit, 3 Segment D/A Converter

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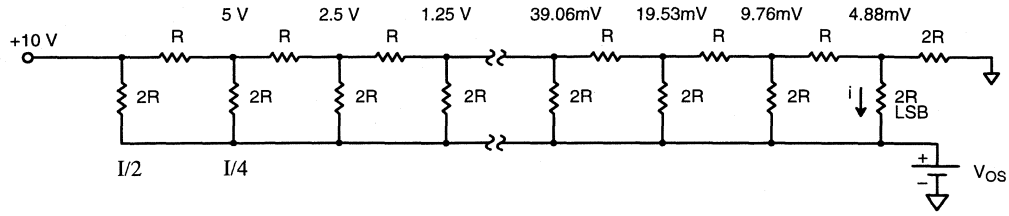
Decoding Advantages

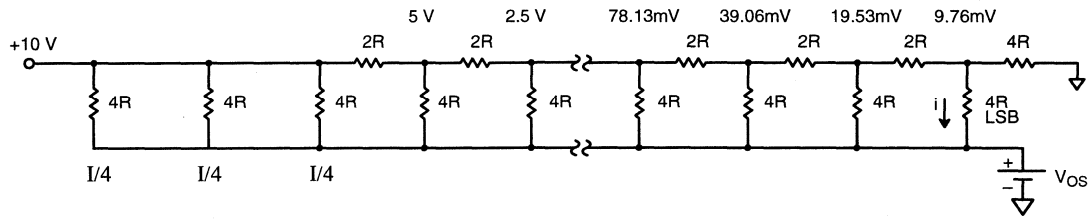
EXAR's 12-bit DACs decode the MSBs into 3, 7, or 15 equal current sources. This provides an improvement over conventional R-2R design in tolerance to resistor and switch matching errors, temperature drift and long term stability, plus a similar improvement in immunity to DNL errors due to output amplifier input offset voltage (*Figure 2.*). Furthermore, EXAR's decoding scheme reduces glitch energy during code switching. This is due to less MSB transient current, symmetrical switching of the three segment currents, and smaller switch geometries (*Figure 3.*). The smaller switch geometries also decrease the output capacitance and switching speed.



(a) Conventional R-2R Ladder (simplified)
Note that voltage across LSB resistor is half that in Figure (2b)

For R = 10k
when V_{OS} = 0
i = 4.88 mV/20k = 244 nA
when V_{OS} = 1 mV
i = 3.88 mV/20k = 194 nA
Error = (244 – 194) / 244 = 0.2 LSB

LSB DNL Error

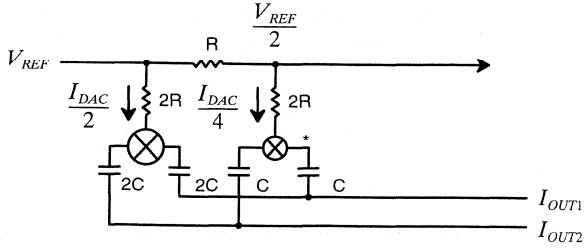


(b) Decoded Ladder Network (simplified)
Note that voltage across LSB resistor is double that in Figure (2a)

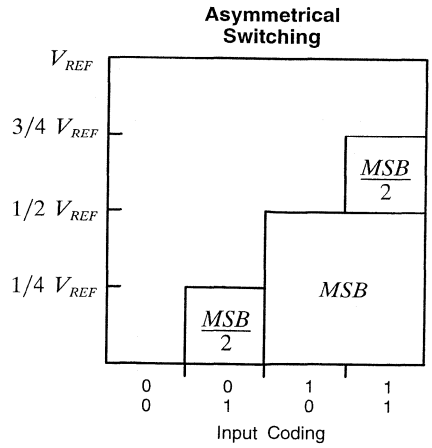
For R = 10k
when V_{OS} = 0
i = 9.76 mV/40k = 244 nA
when V_{OS} = 1 mV
i = 8.76 mV/40k = 219 nA
Error = (244 – 219) / 244 = 0.1 LSB

LSB DNL Error

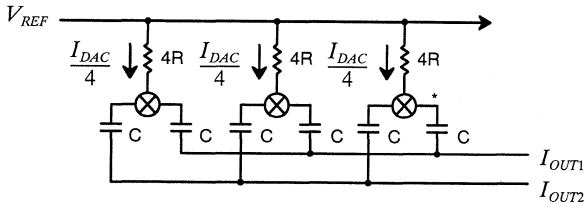
Figure 2. DAC Architecture Comparison for V_{OS} Contribution to Error



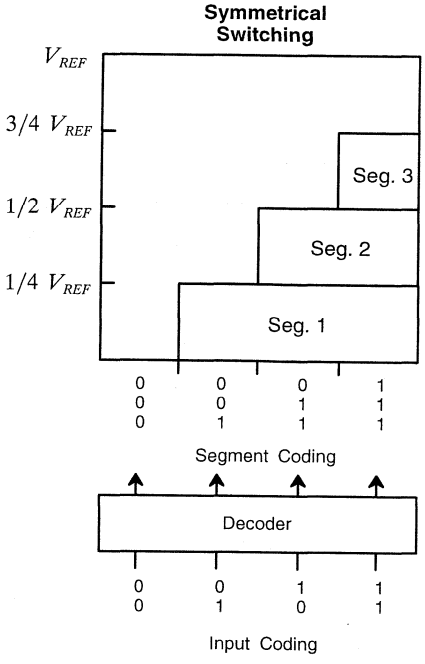
*During major carry transition to MSB this switch turns off and injects charge into output. Additional charge is also injected from MSB as it is switched on.



(a) 2 MSBs R-2R Ladder



*During major carry transition to MSB this switch remains on and adjacent switch turns on. Smaller geometry in adjacent switch (compared with 3a) injects less glitch energy into output as it turns on.



(b) 2 MSBs Decoded

Figure 3. Switching & Glitch Energy

8

STANDARD CONFIGURATIONS

Unipolar Configuration

Figure 4. shows a CMOS DAC in its basic form. The circuit can be used either as a fixed reference DAC to provide an output ranging from 0 to $-V_{IN}$ or as a 2-quadrant multiplier where V_{IN} is an AC signal. A voltage (V_{IN}) is applied to V_{REF} and converted into a code dependent current by the DAC's resistors and switches. The output op amp changes this current into voltage represented by the equation $V_{OUT} = -V_{REF} * m/2^N$ where m is the decimal value of the input code (*Table 1.*). Positive or negative voltages can be applied to V_{REF} allowing 2-quadrant multiplication operation (*Graph 1.*). V_{REF} can be an AC signal and V_{OUT} yields the V_{REF} waveform attenuated by the input code. The 10pF capacitor across R_{FB} compensates for the DAC's output capacitance which otherwise might cause ringing or oscillation when using higher speed op amps.

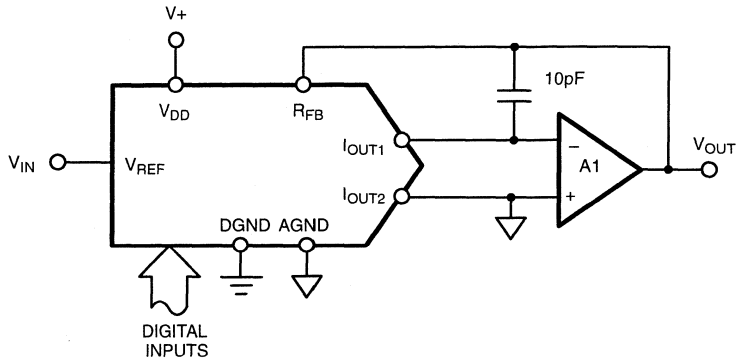
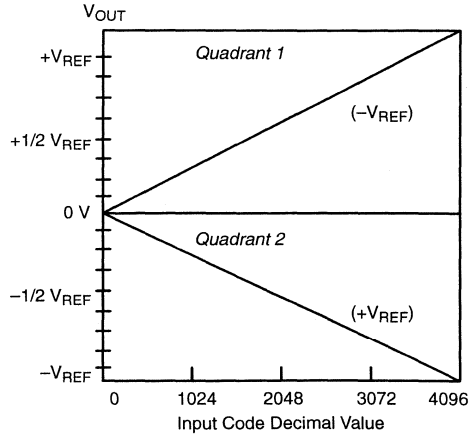


Figure 4. Unipolar Binary Operation (N = 12)
(2-Quadrant Multiplication)

Digital Input	Analog Output
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right) = -V_{REF} + 1\ LSB$
1 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{2049}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{2047}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\frac{1}{4096}$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{4096}\right) = 0\ V_{REF}$

Note : $1\ LSB = (2^{-12})\ (V_{REF}) = \frac{1}{4096}\ (V_{REF})$

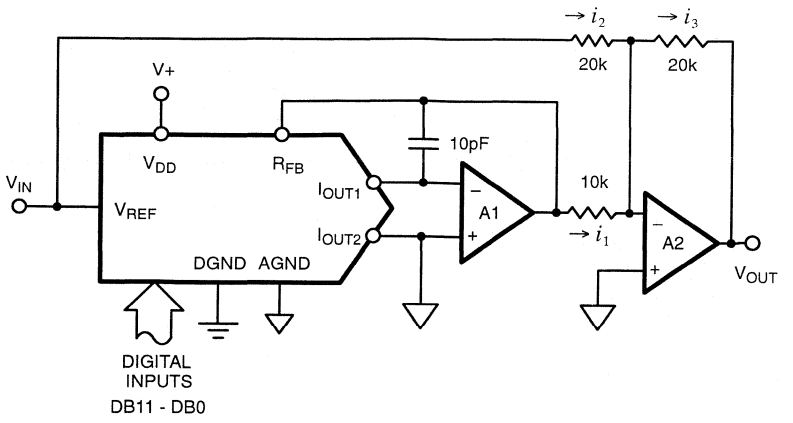
Table 1. Unipolar Code Table (for N = 12)



Graph 1. 2-Quadrant Multiplication

Bipolar Configuration

Figure 5. shows a CMOS DAC in its bipolar voltage output mode. The output amplifier (A2) inverts and doubles the DAC's op amp (A1) output voltage with an input resistor of 10k ohms and a feedback resistor of 20kΩ. Another input resistor of 20 kΩ is connected to V_{REF} which is the opposite polarity of the DAC's output voltage. The V_{REF} voltage is inverted at a gain of 1 by the output amplifier which offsets the output by 1/2 scale. This output voltage is represented by the equation $V_{OUT} = 2 * (-V_{REF} * m/2^N) + V_{REF}$ where m is the decimal value of the input code (*Table 2.*). Since the reference may be of either polarity, 4-quadrant multiplication is performed in this configuration (*Graph 2.*).



$$i_1 = \frac{-V_{IN}\,\frac{n}{4096}}{10k}$$

$$i_2 = \frac{V_{IN}}{20k}$$

$$i_3 = \frac{-V_{OUT}}{20k}$$

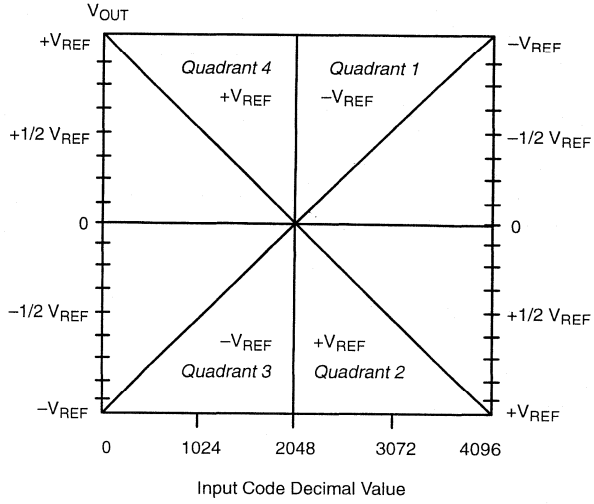
$$V_{OUT} = -V_{IN} + V_{IN}\left(\frac{n}{2048}\right)$$

Figure 5. Bipolar Binary Operation (N = 12)
(4-Quadrant Multiplication)

Digital Input	Analog Output
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

Note : $1\ LSB = (2^{-11})\ (V_{REF}) = \frac{1}{2048}\ (V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table
(N = 12)



Graph 2. 4-Quadrant Multiplication
(N = 12)

8

OFFSET AND SPAN ADJUSTMENT FOR STANDARD CONFIGURATIONS

Offset Adjust

For many DAC applications offset errors due to DAC output leakage current and output op amp bias current are significant enough to warrant offset adjustment. At the 12-bit level, an LSB is 2.4 mV (10 V reference), and is easily adjusted by using the particular circuit recommended by the manufacturer for the V_{OS} adjust of the op amp that the user chooses.

Span (Full Scale Gain) Adjust

Span is the difference between the output voltage with all lows on the digital bus (offset) and the output voltage with all highs on the digital bus (full scale). Ideally, a DAC's span is equal to the magnitude of the reference voltage minus one LSB. In the case of a 12-bit DAC this is shown by the equation $V_{OUT} = -V_{REF} + (V_{REF}/4096)$. When V_{OUT} does not equal the expression given, a mismatch in the reference impedance path and the feedback resistor path is present. Equal amounts of current must always flow through these two paths. The easiest way to adjust for perfect span is to monitor the output voltage and change the reference voltage until the desired potential is achieved. If the reference voltage cannot be changed, the resistance in the paths must be adjusted. If the output voltage is too high, resistance must be added to the reference current path and if the voltage is too low, resistance must be added to the feedback path. This is done by adding a fixed resistor to the feedback path and a potentiometer to the reference path as shown in *Figure 6.* The value of the added fixed resistor (R1) is calculated from the gain error specification and the maximum reference input impedance. Calculate the gain error of the reference input resistance (also R_{FB} value) and add 25% to compensate for tolerances. For example, if the gain error specification is 0.4% and the maximum DAC impedance value can be 20kΩ then:

$$.004 \times 20000\Omega = 80\Omega$$
$$.25 \times 80\Omega = 20\Omega$$

Therefore the added resistor, R1, is 80Ω plus 20Ω or 100Ω. The potentiometer (R2) value is double R1 or 200Ω. The addition of these resistors allows the user to set span to its ideal value without excessive trimming range.

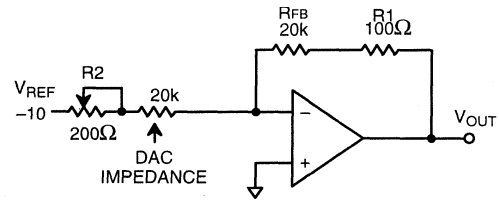


Figure 6. Span Adjust Circuit

SINGLE SUPPLY OPERATION

Most of EXAR's CMOS DACs can be configured to operate with a single power supply for both the DAC and output amplifier. Two modes are described here.

Voltage (Back DAC) Mode

In the voltage (Back DAC) mode (*Figure 7.*), the voltage reference input is applied to the I_{OUT1} port causing a code dependent output voltage at the V_{REF} pin.

The voltage reference input must be limited to 2.5 V or less. This limitation is necessary because the voltage reference input is fed directly to the FET switches whose ON resistance is a function of the voltage applied. Therefore, large values of input voltage could produce significant non-linearities. Also note only a positive reference voltage input is allowed. Furthermore, the voltage source should have low impedance to minimize voltage drops by the current flowing through it and the switch.

The complete configuration is shown in *Figure 8.* The output resistance at V_{REF} (amplifier input) may have a unit-to-unit variation of 5kΩ to 20kΩ, and requires a buffer amp to source current to a load. Note, however the output resistance is not code dependent and does not contribute to linearity errors due to amplifier offset voltage. A variety of high impedance single power supply op amps are available to comply with the required zero volt output with an all zero digital code input.

Finally, the DAC configuration significantly decreases glitch energy because the charge in the switches is directed to ground, either directly or through the low impedance voltage source, rather than to the summing point at the amplifier input.

Using the Back DAC configuration results in a fast, low noise, low glitch, data conversion scheme and is recommended where fixed positive reference, non inverted output, single supply is required.

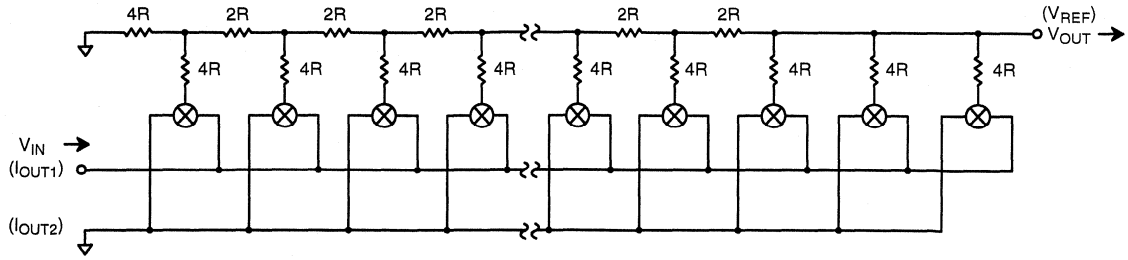
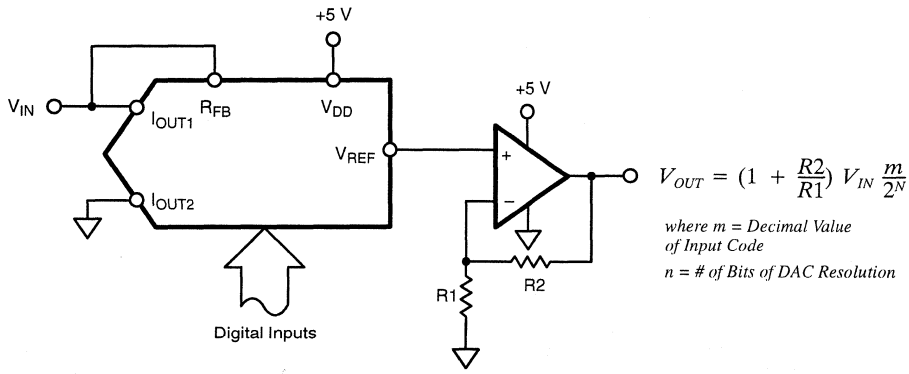


Figure 7. Back DAC Configuration



$$V_{OUT} = (1 + \frac{R2}{R1}) V_{IN} \frac{m}{2^N}$$

where m = Decimal Value of Input Code

n = # of Bits of DAC Resolution

Figure 8. Voltage Back DAC Mode

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Current Steering Mode

Another means of achieving single positive supply operation is to apply the reference voltage to the Analog Ground and I_{OUT2} pins and to use a buffer amplifier as shown in *Figure 9.* The amplifier's non-inverting input is, likewise, connected to the reference causing it (the amplifier) to act as a level shifter so that the output voltage does not approach zero volts. If a 2.5 volt reference is used, the amplifier output will swing between 2.5 V at 0 scale and 5 V at full scale. This mode, however, does not offer the speed advantage of the mode previously described.

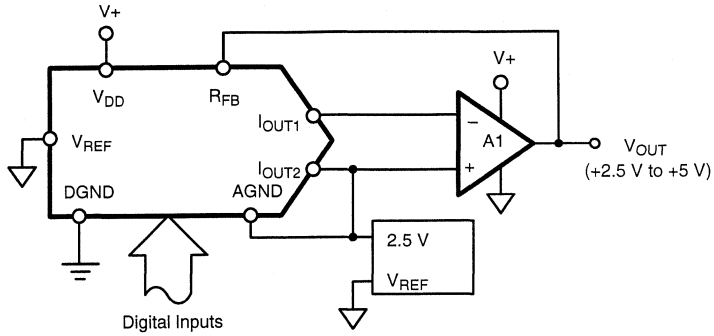


Figure 9. Current Steering Mode

APPLICATION CONSIDERATIONS

Grounding and Power Supply Decoupling

A digital-to-analog converter should be treated strictly as an analog component. Performance is much more dependent upon its relationship to the associated analog circuitry than the peripheral digital parts. Many DACs have only one ground pin and this must be tied to the system analog common ground, often a ground plane. This ground must be as noise free as the system performance specification warrants. In a 12-bit system with a 10 volt full scale, for example, the noise difference between any two analog ground pins should be kept below one tenth of an LSB ideally and one quarter of an LSB maximum. Common mode noise can be much higher, but it must be recognized as such.

DACs offering separate analog and digital grounds ideally should have these two pins connected at the devices and tied to the analog common. However, in systems having to separate the analog and digital grounds due to excessive digital noise, the grounds on the DAC should be tied to their respective planes. Inverse parallel diode clamps must be placed between the two ground pins at the device to ensure a limited potential between them. Some digital noise may be seen at the DAC's circuit output due to feedthrough inside the device. This noise should not exceed system performance specifications or output filtering must be employed.

V_{DD} on the DAC must be decoupled to ground with a .1µF capacitor. If low frequency noise is prevalent, a 10µF capacitor must also be added.

Output Operational Amplifiers

Input Offset Voltage (V_{OS})

CMOS D/A Converters exhibit a code dependent output resistance which will cause differential non–linearity if the DAC output is not held at zero volts. Therefore, the amplifiers input offset voltage (V_{OS}) should be less than a tenth of an LSB to ensure monotonicity. With a 10 volt reference the LSB weight is $10/2^N$ mV, therefore an amplifier should be selected which has less than $1/2^N$ µV of input offset voltage (V_{OS}) over the entire operating temperature range.

Input Bias Current (I_B)

The op amp's input bias current should be considered. A stable bias current simply creates a stable output offset voltage. A bias current that changes with time and/or temperature will produce a varying offset and even non-linearity if the current changes as the input code changes. With a worst case DAC impedance (also $R_{FEEDBACk}$ value) of 20 kΩ and a reference voltage of 10 volts, the full scale DAC current would be 500 µA, while an LSB's current value for a 12-bit converter would be 500uA/4096 or 122 nA. If the designer determines that bias current contribution to offset and/or linearity error should be kept below 1/10 LSB, for example, then the bias current may not vary more than 122nA/ 10 or 12.2 nA over the entire operating temperature range.

Video Digitizer and Variable Range A/D Converter

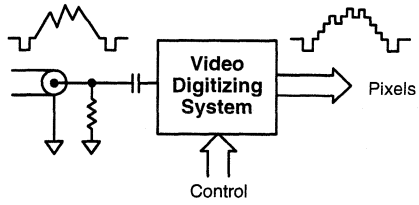
Simple and reliable video digitizer design using ADC with "variable input range"

FEATURES

- **Simple Fixed-Gain Analog Front End**
- **Digital Control of Gain, Clamping and Clipping**
- **Imaging Functions Available in Hardware:**
  - **Contrast Control**
  - **Brightness Control**
  - **Histogram Stretching**

BENEFITS

- **Reduction of Analog Circuitry**
- **Reduction of System Cost**
- **Increased Reliability and Testability**



Conventional Fixed Analog Range ADCs force designers to adjust signal range to the ADC's range with analog circuitry. "Variable Range" ADCs can be adjusted to match the input range. Design is simplified. The programmability of the conversion range adds some imaging features.

Video Digitizing is one of the fastest growing applications of ADCs. The time is not too far away when all computer users will add image data bases to their mass storage - images to be inserted in letters, documentation, database files etc. The technology is already available. The usual impediment is that the cost is still too high.

The conversion of a video image (or frame) into a computer image is still a costly affair because it involves the very delicate boundary where "always different" analog waveforms are reduced to "never changing" digital stairsteps.

It is an accepted notion that the total system cost is reduced when the introduction of a new component increases the percentage of digital hardware and reduces the percentage of analog hardware. All other parameters remaining the same, this change will reduce the design time, the debugging time and the cost of the system.

In the case of Video Digitizing Systems the "Variable Input Range A/D Converter" can provide all these benefits.

Video Design using "Fixed Range" ADC

Figure 1. shows the block diagram of a Video Digitizer which uses a fixed input range A/D (fixed reference A/D). The cable terminates on a 75Ω resistor and it is AC coupled to the first stage. DC levels have to be restored for the proper operation of this first stage. One often used solution is to force a DC voltage when the video input is not "active" (i.e. back porch of horizontal blanking). Then one or two stages are used to set the proper gain and the proper DC levels to the signal going to the A/D converter. Design efficiency requires that the A/D input range (or reference range) matches the part of the video signal range which contains the image.

Changes in component values (R, C, or amplifier gain, etc.) and in operating conditions (supply voltages, temperature, etc.) add up to cause a mismatch of ranges. These factors force video designers either to insert feedback loops which increase system cost or to use only a percentage (85 to 95%) of the ADC range.

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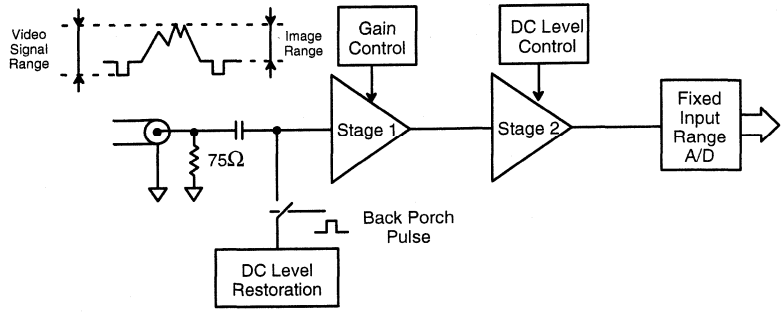


Figure 1. Video Input Signal has to be carefully gained and DC-biased to fit the A/D input range

A better approach would be:

1) to design an analog front end as simple as possible (which in most cases yields the best performance/cost ratio), and to let the components' real parameters and the operating conditions add the second order variation to the first order design goal.

2) match the ADC's reference range to the resulting input range.

Video Design using "Variable Range" ADC

EXAR's line of Flash Converters (MP7682, MP7686, MP7684, MP7684A, MP8780, MP8785, MP8775, MP8784, MP7695, MP8791) gives to video designers the flexibility of a user programmable input range. The user simply biases the two reference inputs to encompass the desired input range.

Figure 2. shows a video digitizer built with a variable range ADC. The video termination is the same 75Ω resistor. The DC restoration can be the same as that of the system in *Figure 1.*, or it can be simplified when it is not necessary to remove the sync before the ADC. The ADC can ignore the sync (if so desired) by simply "ranging it out".

One amplification stage accomplishes the double task of driving the ADC and of amplifying the video input signal. The ADC can convert a 0.7 V p-p signal but it delivers the best accuracy at 1.5 to 3.0 V p-p. A suggested range for the MP8780 is 2.0 to 2.5 V p-p anywhere in the GND to V_{DD} range.

The design of the circuitry which sets the conversion range (or reference range) for the ADC is even simpler. A dual DAC gives to the digitizing system the flexibility to adjust top and bottom limits under software control. A series of variable resistors can provide a cost effective solution when cost (and flexibility) are to be reduced. *Schematic 1* gives an example of D/A control while *Schematic 2* shows a simpler circuit. *Figure 3.* illustrates how to adjust $V_{REF(+)}$ and $V_{REF(-)}$ to:

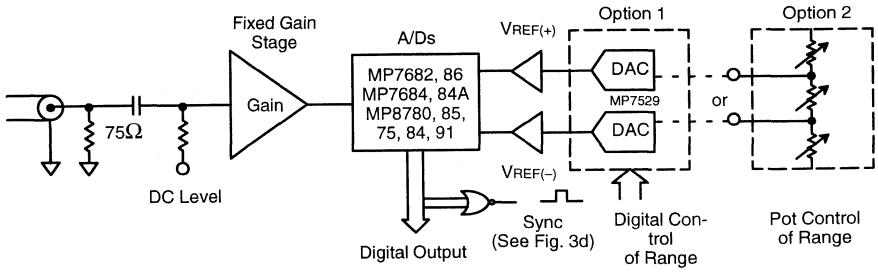


Figure 2. Video Input Signal is biased and gained to any range between GND and V_{DD}. The two DACs fit the A/D range to the signal.

a) include the entire video signal
b) extract the sync
c) digitize the video image
d) digitize the video image and extract sync
e) increase contrast
f) decrease contrast
g) make picture darker
h) make picture lighter

If an image is too dark, the reduction of $V_{REF(+)}$ will provide a lighter image. Similarly an increase of $V_{REF(-)}$ will darken a very light image. Software manipulation of the code distribution of the image (histogram stretching) provides similar but less accurate results. A/D non linearities are proportionally stretched as well!

The ADC outputs all 0's when the input voltage is below $V_{REF(-)}$ and all 1's when is it above $V_{REF(+)}$. A choice of input range like the one shown in *Figure 3d* would yield an ADC output that is equal to 0 only during the sync pulse. In this case, a system can generate the sync pulse by simply using an 8 input NOR, as seen in *Figure 2*.

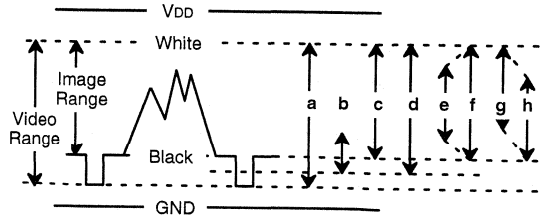
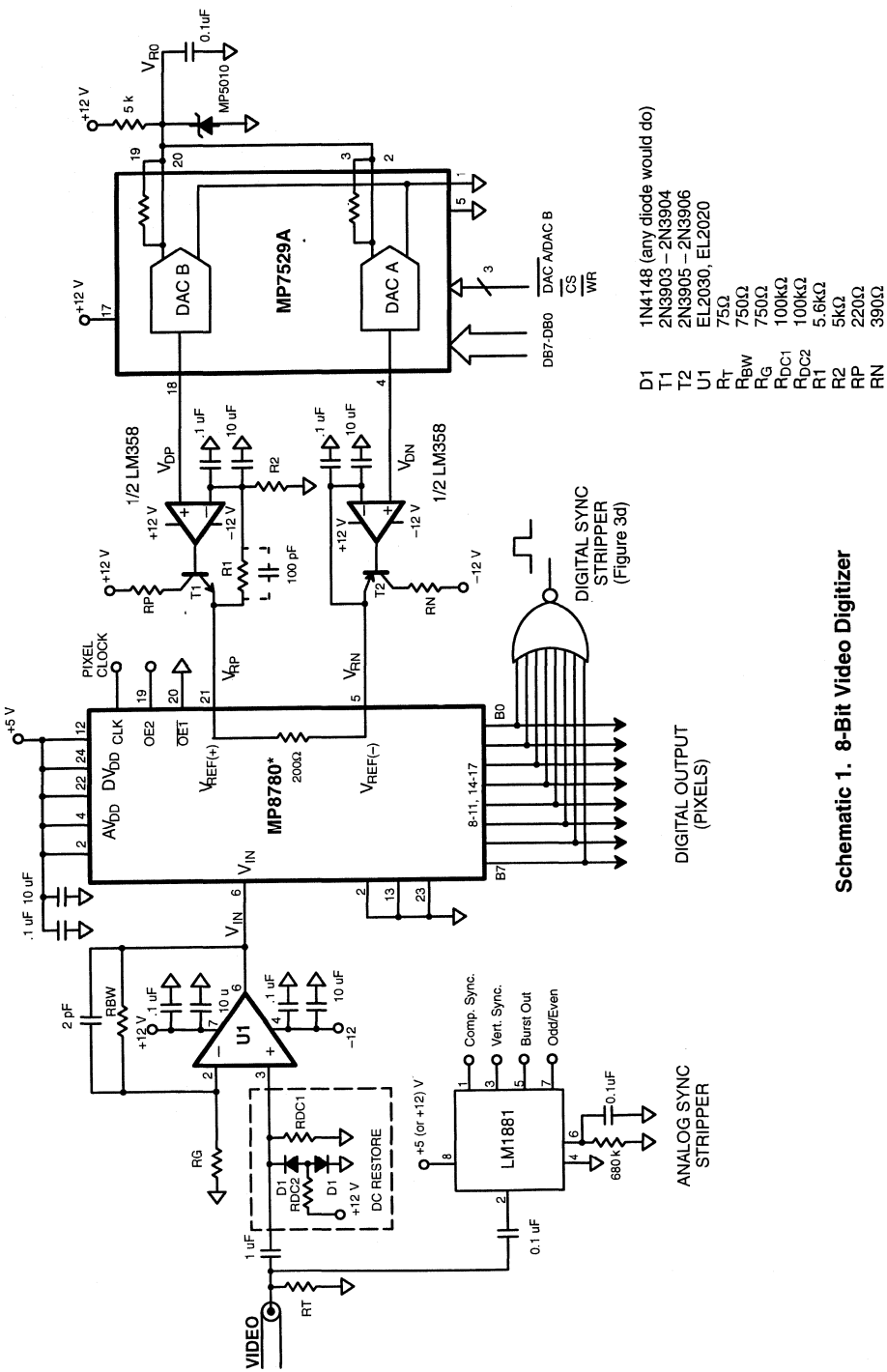


Figure 3. Selecting the ADC Input Range

a) full video signal
b) sync only
c) video image only
d) video image and sync
e) increase contrast
f) decrease contrast
g) darker image
h) lighter image

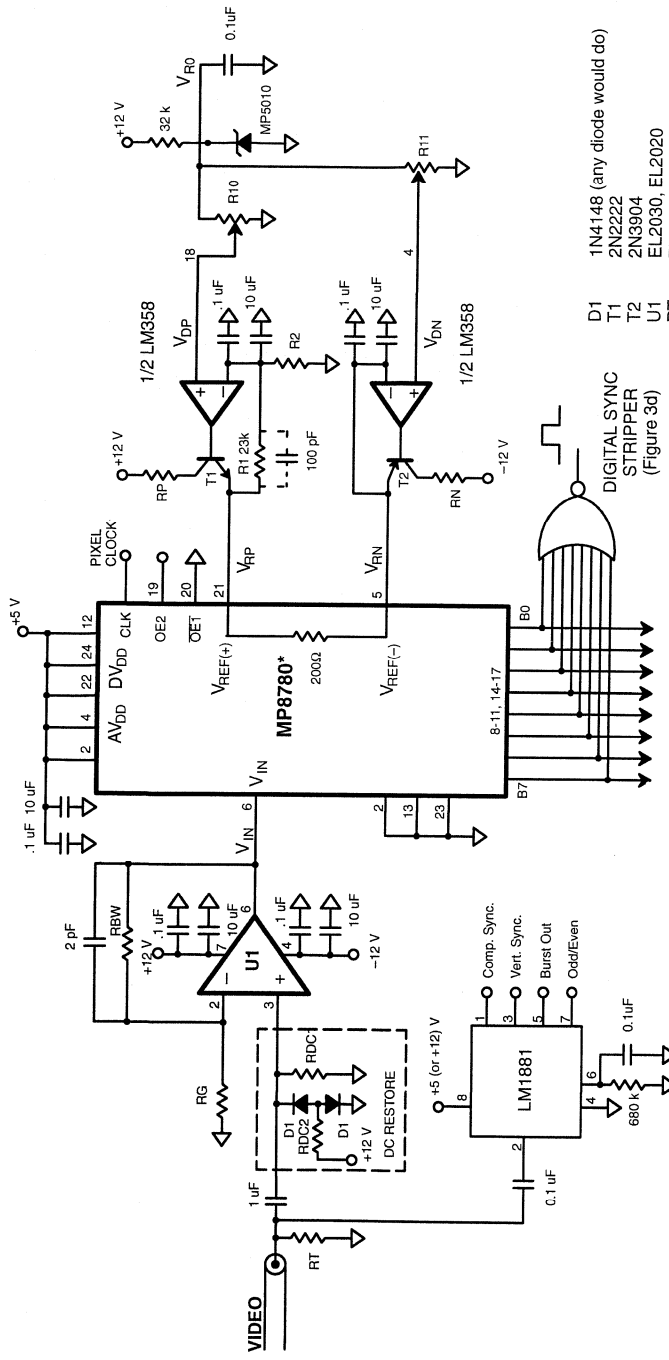
8



D1 1N4148 (any diode would do)
T1 2N3903 – 2N3904
T2 2N3905 – 2N3906
U1 EL2030, EL2020
R_T 75Ω
R_{BW} 750Ω
R_G 750Ω
R_{DC1} 100kΩ
R_{DC2} 100kΩ
R1 5.6kΩ
R2 5kΩ
RP 220Ω
RN 390Ω

Schematic 1. 8-Bit Video Digitizer

*Same circuit can be used for MP7682, 7686, 7684, 7684A, 8780, 8775, 8785, 7695, 8784, 8791



D1	1N4148 (any diode would do)
T1	2N2222
T2	2N3904
U1	EL2030, EL2020
RT	75Ω
RBW	750Ω
RG	750Ω
RDC1	100kΩ
RDC2	100kΩ
R1	5.6k
R2	5k
RP	220Ω
RN	390Ω
R10	10k Pot
R11	10k Pot

Schematic 2. Video Digitizer

*Same circuit can be used for MP7682, 7686, 7684, 7684A, 8780, 8775, 8785, 7695, 8784, 8791

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USING THE MP7641 (& MP7651) IN TWO AND FOUR QUADRANT MULTIPLIER CONFIGURATIONS

Introduction

The MP7641 contains eight 8-bit two-quadrant multiplying digital-to-analog converters (MDACs). The MDACs are individually addressed and the digital input codes are programmed serially. Each channel's output is the instantaneous algebraic product of an attenuation ratio ,"a", and the analog reference input. The variable "a" is proportional to the 8-bit digital input code which is stored for each channel. This multiplication is accurate to frequencies above 10 MHz. The analog input (V_{REF}) can be either positive or negative. The digital input ranges from a code of all zeroes to all ones. The variable "a" ranges from 0 to 1 and is never negative, therefore the standard MP7641 channel is defined as a two quadrant multiplier.

Sometimes, applications require four-quadrant multiplication. External circuitry can convert an MP7641 channel to a four-quadrant MDAC. The digital input code now behaves as an offset binary representation of the digital variable. The most significant bit of the input code becomes a sign bit. All four quadrants can be used.

Three topologies usable for four quadrant multiplication are discussed below. Different levels of external circuit complexity were evaluated and the data is presented. The results indicate that frequency and transient response characteristics are improved by using the phase equalizing techniques of the more complex circuits.

Two Quadrant Operation

The MP7641 integrated circuit contains eight, two-quadrant, wide bandwidth, multiplying 8-bit digital-to-analog converters. The MP7641 data sheet lists the guaranteed and typical specifications. Each channel can be viewed as a potentiometer where the wiper can be serially set digitally. The analog (V_{REF}) is connected to the top of the potentiometer and the bottom is connected to AGND which can be set externally (within limits.) An active buffer amplifier isolates the wiper from the output and provides a low output impedance. The input/output relationship is:

$$V_{OUT} = \frac{a \cdot V_{VREF}}{1 + s\,T}$$

where,

$$a = \frac{Input\ Code\ (Decimal\ Equivalent)}{256}$$

and,

$$0 \leq a < 1$$

and,

$$s\ is\ the\ Laplace\ variable$$

Note that the finite bandwidth is modeled by the single pole having a time constant, "T". This time constant of 18 nsec, which was determined empirically, is consistent with the 10 MHz bandwidth specification.

The digital signal path frequency response is limited to a few kilohertz by the serial input data update rate. Updating a DAC input register takes approximately one microsecond. All eight MDACs can be changed in ten microseconds. Fast sweeping of the variable "a" provides the equivalent of eight high speed ganged potentiometers.

Four Quadrant Operation

When four quadrant operation is needed, external circuitry is required. *Figure 1.* shows a channel of an MP7641 connected to an external high speed op amp with precision resistors to implement this. The external amplifier's output is the output of the four quadrant multiplier and is represented by the following relationships:

$$V_{OUT} = \frac{b \cdot V_{REF}}{1 + s\,T}$$

where,

$$b = 2 \cdot a - 1$$

and,

$$a = \frac{Input\ Code\ (Decimal\ Equivalent)}{256}$$

and,

$$0 \leq a < 1$$
$$-1 \leq b < 1$$

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Since "b" can be either positive or negative, all four quadrants are now usable and the digital code can be used to invert the analog input. The op amp and resistors are assumed to be ideal in these formulas.

Parallel summation paths are required to convert a two quadrant circuit to four. In *Figure 1.*, the bandwidth through the MDAC path is lower than through the resistor path. This causes errors at higher frequencies and the above equations no longer apply. By adding delays in the resistive path, the errors can be significantly reduced. The next section explores this.

Code tables for the configuration of *Figure 1.* are the same as those given in the EXAR 1995 databook Section 4.

MP7641 Evaluation – Four Quadrant Operation

Three four-quadrant MDAC circuits were tested and the results are presented here. The circuits are shown in *Figure 1.*, *Figure 4.*, and *Figure 7.* The primary features of each circuit are:

Figure 1. – Simplest, Worst Frequency Characteristics
Figure 4. – Most Complex, Best Frequency Traits
Figure 7. – A compromise between the above

In all configurations, the R_L and C_L are added to simulate worst case application loads. They are not required for circuit operation. Replacing R_L to GND with a 5k to V_{EE} further improves the large signal response at the expense of increased power.

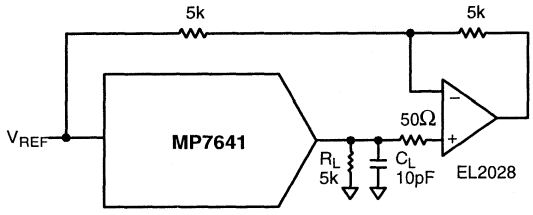

Figure 1. – Circuit 1.

Basic operation of the four quadrant multiplier of *Figure 1.*, with square wave input of 0 to 3 V is shown in the following two figures. *Figure 2.* shows the output of the op amp when the MP7641 is set to zero scale. In this condition the input signal from V_{REF} is simply inverted at the output of the op amp (*Figure 2.*)

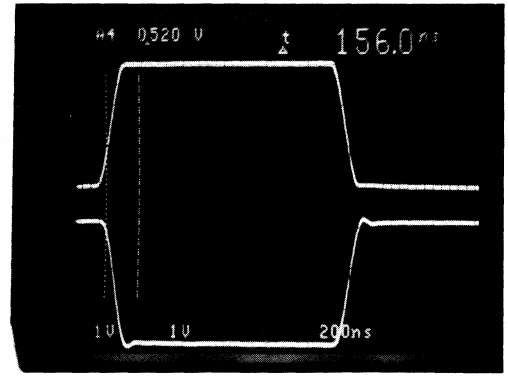

Figure 2.

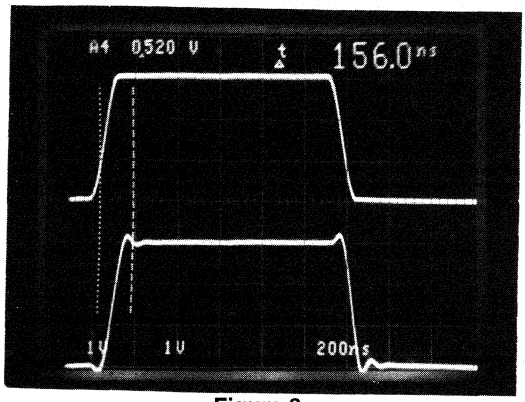

Figure 3.

When a MP7641 DAC is set to full scale, the result is shown in *Figure 3.* This results in a positive output in accordance with the equations above. *Figure 2.* and *Figure 3.* clearly show the MP7641 and the op amp operating as a four-quadrant multiplier.

For most applications, this simple configuration is all that is needed to achieve the desired results. If however, your system requires better response at higher frequencies, there are two additional configurations that can be used to enhance the performance of the basic four-quadrant multiplier. The second configuration is shown in *Figure 4.*

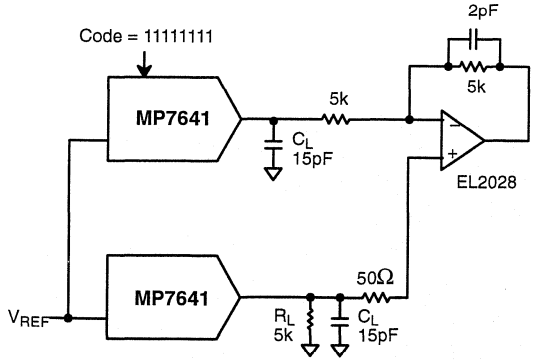

Figure 4. – Circuit 2.

Note that a second MDAC, whose digital input is fixed at all ones, is used in the inverting path to provide a delay equal to the positive path delay. Since the MP7641 DACs are matched, this topology reduces the errors due to delay effect by at least an order of magnitude (the measured performance will demonstrate this).

Figure 5. and *Figure 6.* demonstrate four-quadrant operation of this circuit (*Figure 4.*) with the sawtooth (for variety only) as the input signal.

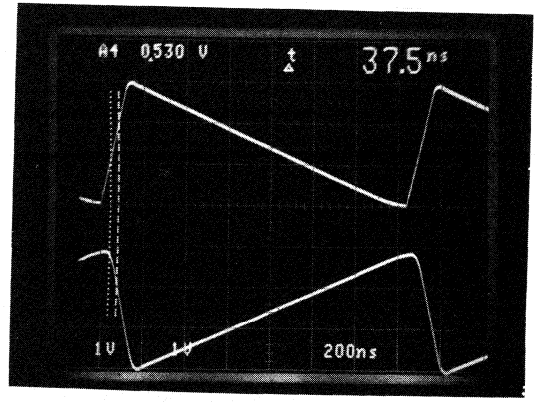

Figure 5.

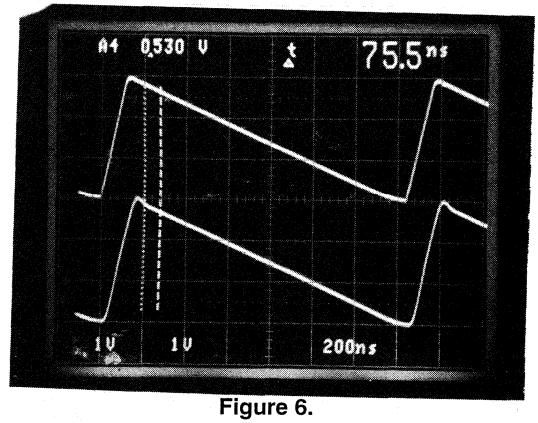

Figure 6.

The third and final circuit that we evaluated is similar to the second. In the place of the second MDAC, an analog delay generated by an RC time constant is used for phase equalization. The schematic for this configuration is shown in *Figure 7.*

Figure 8. and *Figure 9.* show the basic full scale response of the four-quadrant MDAC with an analog delay line generated by the RC time constant. To introduce a delay of 18 ns we used an 180pF capacitor and 100 ohm resistor to generate the required delay time. A compen-

sating 100 ohm was added to the feedback resistor to preserve the correct gain ratios.

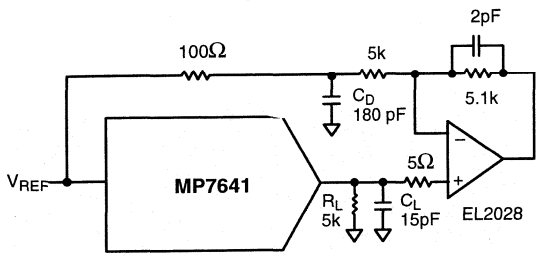

Figure 7. – Circuit 3.

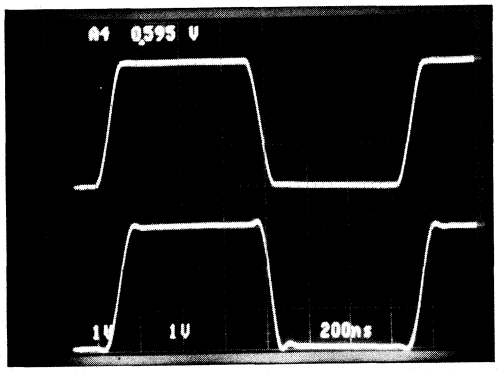

Figure 8.

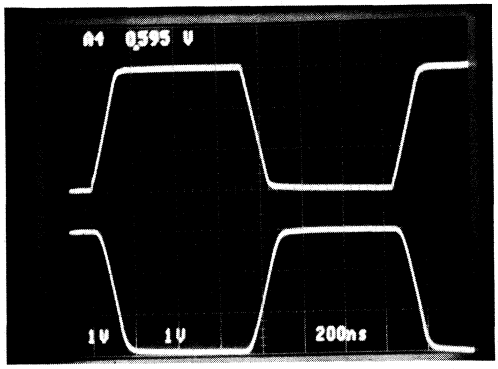

Figure 9.

Feedthrough Evaluation – Square Wave

For all of these circuits, the rise time of the input signal was kept to 100 ns. From design considerations, this is the fastest signal that should be placed into the device in order to achieve true linear response and prevent slew rate limiting.

The more complex circuit configurations as shown in *Figure 4.* and *Figure 7.* improve the performance over the basic configuration of *Figure 1.* This is demonstrated at half scale. With just the MSB of the MP7641 high, the output should stay at zero ("b" = 0 from above) for any analog input. Delay mismatches between the two paths permit unwanted transient signals to reach the output.

Figure 10. shows the input and output for "b"=0 for the circuit of *Figure 1.* Because we have a finite delay through the MP7641 and a direct path to the inverting 5 k ohm resistor, we see a band pass "feedthrough" at the output of the op amp. We get approximately a 1.6 V pulse that is about 180 ns wide at the base. The op amp that is in use for this evaluation is an Elantec (EL2028) device. By choosing a slower op amp, the magnitude of this spike can be reduced (at the expense of reduced bandwidth). If the magnitude of this spike can be tolerated, then going to any of the other circuit configurations is not necessary.

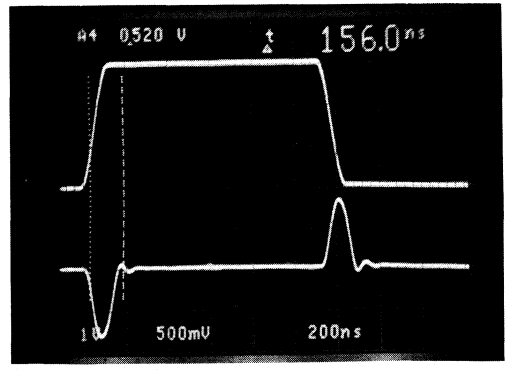

Figure 10.

Figure 11. shows the results of performing the same test on the circuit of *Figure 4.* The bottom trace is the output of the op amp. As a result of matching the delay, the magnitude of the spike is reduced by approximately 30 times. The error amplitude is reduced from 1.6 volts to .05 volts.

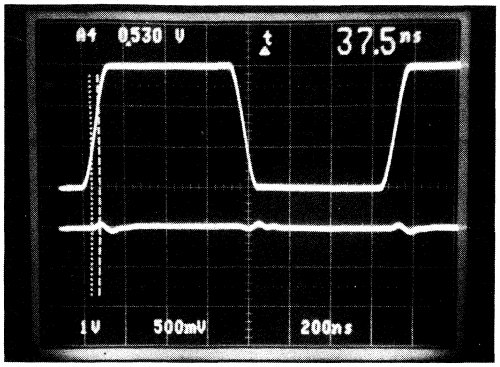

Figure 11.

Figure 12. shows the results of performing the same test on the circuit of *Figure 7.* The RC time constant was chosen as 18 nsec. This was based on the known bandwidth of the MDAC (10 MHz). To compare the magnitude of the spike, please observe *Figure 11.* and *Figure 12.* Peak feedthrough is now 120 mV. Thus the dual DAC configuration of *Figure 4.* results in the lowest amplitude feedthrough.

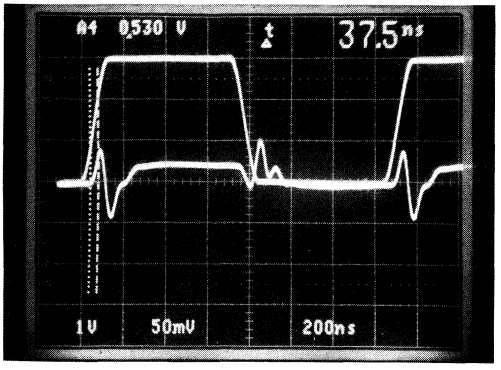

Figure 12.

Feedthrough Evaluation – Sawtooth

Figure 13. and *Figure 14.*, which apply to the circuits of *Figure 1.*, and *Figure 4.*, respectively, show the performance using a sawtooth with 100ns rise time as the input instead of a square wave. As can be seen from these figures, the performance for the circuit shown in *Figure 4.* is clearly the best whether driven by a square wave or a sawtooth. The magnitudes of the 1/2 scale spike errors for square wave and sawtooth waveforms are summarized in *Table 2.*

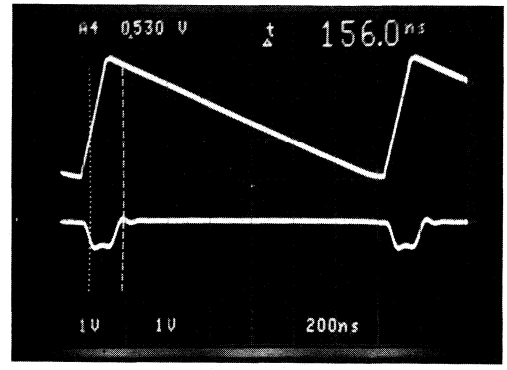

Figure 13.

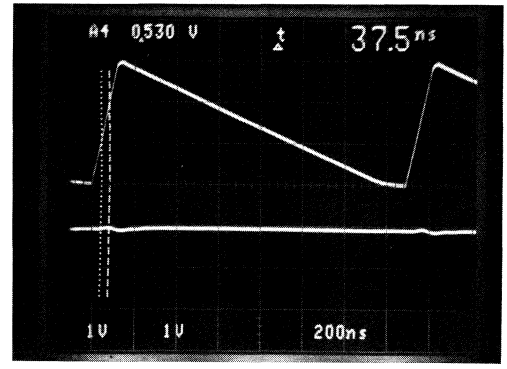

Figure 14.

Ramp Linearity

Transient feedthrough errors affect the linearity of the ramp. The circuit of *Figure 4.* significantly improves the linearity of the ramp over the other figures. This improvement can be seen in *Figures 5, 6, 16 and 17.* The input is shown by the upper trace in these figures, and the bottom

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trace is the output of the op-amp. As can be seen in these figures, the bottom trace is more linear if we can reduce the magnitude of the spike, and the circuit without the delay line matching performs worse as shown in *Figure 15.* and *Figure 16.*

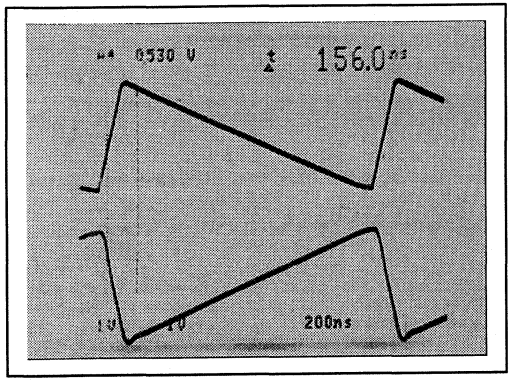

Figure 15.

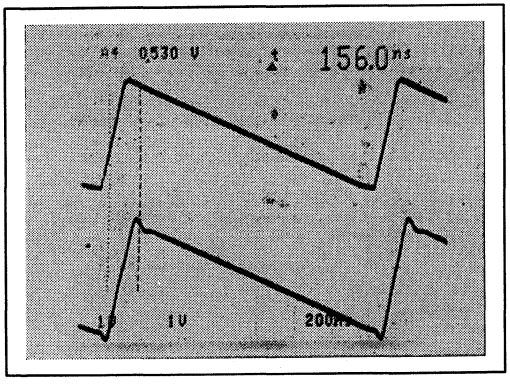

Figure 16.

Conclusion

The results of this evaluation suggest that the circuit of *Figure 1.* can be used for four quadrant multiplying applications where high speed performance is not critical. The best high speed, high performance choice is the two MDAC arrangement of *Figure 4.* A compromise solution is given in *Figure 7.*

Data Tables

For all the circuit configurations the following information was measured and is summarized in the following tables.

There are six areas that the performance was measured. These are:

Square Wave operation 0 to 3 Volts
into rated load resistance and capacitance
- @ Digital Code 00000000
- @ Digital Code 11111111
- @ Digital Code 10000000

Sawtooth Wave operation 0 to 3 Volts
into rated load resistance and capacitance
- @ Digital Code 00000000
- @ Digital Code 11111111
- @ Digital Code 10000000

Small signal mode Plot 800mV
into rated load resistance and capacitance
- @ Digital Code 00000000
- @ Digital Code 11111111
- @ Digital Code 10000000

Settling time 0 to 3 Volts
into rated load resistance and capacitance
- @ Digital Code 00000000
- @ Digital Code 11111111

Settling time 0 to 3 Volts
into rated load resistance and 10pF + parasitic
- @ Digital Code 00000000
- @ Digital Code 11111111

Settling time 0 to 3 Volts
into rated load resistance and parasitic capacitance
- @ Digital Code 00000000
- @ Digital Code 11111111

THD 0 to 3 Volts
into rated load resistance and capacitance
- @ Digital Code 00000000
- @ Digital Code 11111111

ZERO SCALE SPIKE		
	V_{IN} = 0 to +3 V (pulse)	V_{IN} = 0 to +3 V (ramp)
Circuit #	V_{SPIKE} (± V)	V_{SPIKE} (± V)
1	1.6	.8
2	.05	.02
3	.12	

Table 1.

SETTLING TIME +FS TO 1 LSB (12 mV)				
	V_{IN} = 0 to +3 V		V_{IN} = –3 to 0 V	
Circuit # and Load Cap	t_{S-} (ns)	t_{S+} (ns)	t_{S-} (ns)	t_{S+} (ns)
1, C_L = 0 pF	105.2	107.0	122.8	108.2
1, C_L = 20 pF	155.8	100.8	361.6	150.6
2, C_L = 0 pF	146.2	89.0	148.4	116.2
3, C_L = 20 pF	128.8	138.8	351.8	128.6

Note: Only +FS was measured, since –FS will measure the performance of the op amp.

Table 2.

BANDWIDTH			
Circuit #	Zero Scale bw (–3 dB)	Full Scale bw (–3 dB)	Half Scale dB down @ 3 MHz
1	14.1 MHz	15 MHz	–7.45
1, with 1kΩ to V_{EE}	14.1 MHz with 5 dB less peaking than w/o1KΩ	15 MHz	
2	12 MHz	14 MHz	–39.82
2, C_L = 0 pF	10 MHz	12 MHz	–37.11
3	12 MHz	15 MHz	–24.47
2, with 1kΩ to V_{EE}	9.5 MHz	14 MHz	

Note: Zero scale measures the performance of the op amp. 1kΩ to V_{EE} increases the current in the output stage. The net effect of this is to improve the frequency performance but also reduces the output swing to approximately 2 V.

Table 3.

THD (100 kHz)				
	V_{IN} = 0 to +3 V p-p		V_{IN} = –3 to 0 V p-p	
Circuit # and Load Cap	–FS (b = –1) (%, dB)	+FS (b = +1) (%, dB)	–FS(b = –1) (%, dB)	+FS(b = +1) (%, dB)
3, C_L = 15 pF	.017, –75.2	.147, –56.6	.022, –72.9	.051, –65.8
2, C_L = 0 pF	.069, –63.1	.120, –58.4	.017, –75.2	.019, –74.0
1, C_L = 15 pF	.026, –71.5	.150, –56.5	.027, –71.3	.058, –64.7

THD (1 MHz)				
	V_{IN} = 0 to +3 V p-p		V_{IN} = –3 to 0 V p-p	
Circuit # and Load Cap	–FS(b = –1) (%, dB)	+FS(b = +1) (%, dB)	–FS(b = –1) (%, dB)	+FS (b = +1) (%, dB)
3, C_L = 15 pF	.090, –60.9	.943, –40.5	.107, –59.4	.051, –65.8
2, C_L = 0 pF	.454, –46.8	.589, –44.6	.164, –55.7	.225, –53.0
1, C_L = 15 pF	.084, –61.9	.963, –40.3	.027, –71.3	.535, –45.3

THD – 2 QUADRANT OPERATION		
	V_{IN} = 0 to +3 V p-p	
	100 kHz (%, dB)	1 MHz (%, dB)
Full Scale	.074, –62.6	.484, –46.4
Half Scale	.039, –68.1	.139, –57.1

Settling Time Plots

When measuring settling time it is important to realize that if measuring with a DAC set at zero scale, you are ONLY measuring the performance of the external op amp. The figures below are indicative of the kind of settling time performance that can be expected from the MP7641. We have included settling time figures from all three circuit configurations. Of course all of this data has been summarized in the settling time results table. The figures are included to give an idea what the dynamic performance looks like.

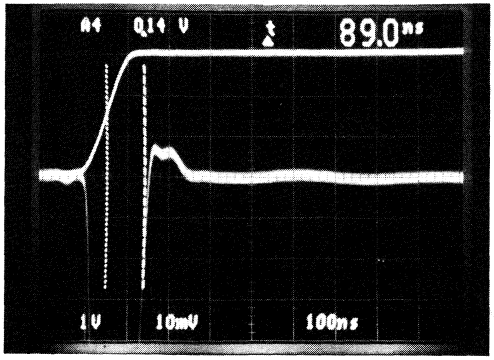

Figure 17.
Circuit #2
C_L = 0 pF

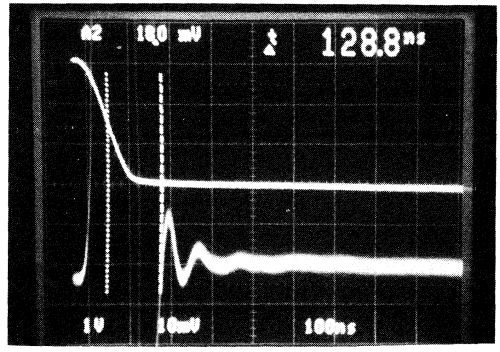

Figure 20.
Circuit #3

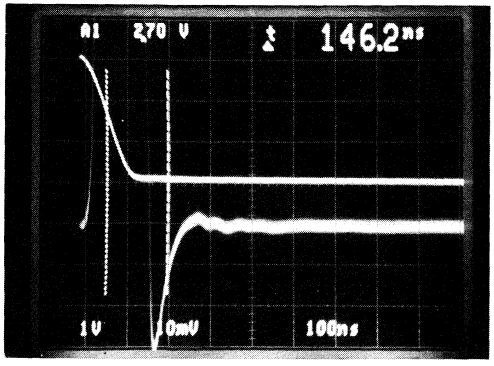

Figure 18.
Circuit #2
C_L = 0 pF

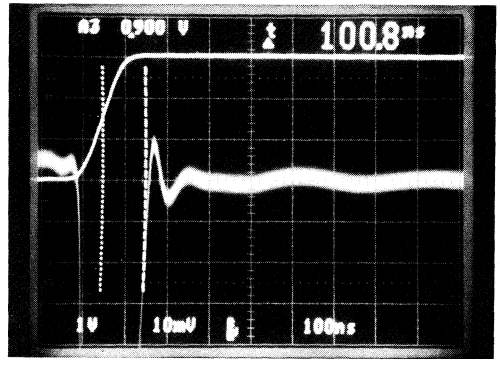

Figure 21.
Circuit #1

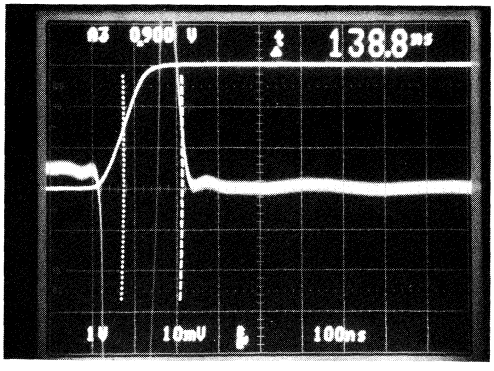

Figure 19.
Circuit #3

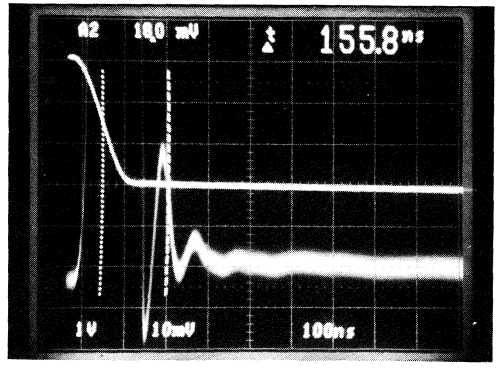

Figure 22.
Circuit #1

All measurements are settling time to +FS with an input pulse from 0 to 3 V

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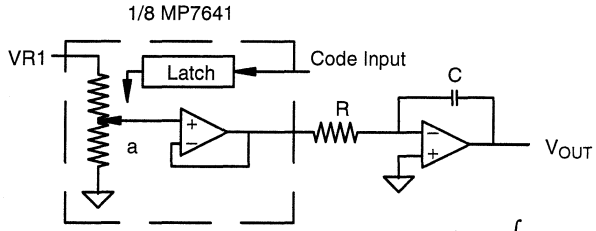
SOFTWARE CONTROLLABLE FILTERS USING THE MP7641

Introduction

The MP7641, octal eight bit multiplying DAC, has such outstanding electrical characteristics that software tuning of active filters to frequencies of one megahertz and higher is now practical and economical. Each of the eight DACs can be programmed serially and independently to a desired attenuation ratio with eight bits of resolution. The part is equivalent to eight digitally controlled precision wide bandwidth potentiometers with zero output impedance.

Active filters have frequency behavior that is typically determined by circuit topology, gain ratios, resistor values, capacitor values, and clock frequencies. The MP7641 can be substituted for ganged potentiometers in these systems and provide digital control of their frequency response as demonstrated in the following examples.

Two types of filters are discussed. The first is a state variable continuous time circuit using discrete op amps and passive components. The second is a switched capacitor biquad application where only external resistors are required.



a = *attenuation ratio*

$$a = \frac{code\ (decimal\ equivalent)}{256}$$

$$0 \leq a \leq \frac{255}{256}$$

$$V_{OUT} = -\frac{1}{Req \cdot C} \int VR1 * dt + V_{OUT}(0)$$

where :

$$Req = \frac{R}{a}$$

Figure 1. Multiplying DAC Time Constant Control of Integrator

8

Sweepable Continuous Time Discrete Filters

Adaptive continuous time filters are frequently required for high resolution applications because the more economical and easily tuned switched capacitor circuits introduce higher distortion and clock noise than is acceptable. The low harmonic distortion and wide bandwidth of the MP7641 permits its use in high resolution continuous time filters where frequency sweeping is needed.

Tuning continuous time filter circuits requires analog multipliers, ganged potentiometers, multiple MDACs or their equivalent. To keep the shape of the frequency response undisturbed while shifting frequency, each of the "RC" time constants in a system must be ratioed by the same factor. Multiplying DACs are a convenient method of introducing these controlled ratios. In an "nth" order filter, "n" multiplying DACs can be used to simultaneously change these time constants. The serial loading of the octal MP7641, though not simultaneous, can be implemented at speeds much higher than is normally required for frequency sweeping applications.

Figure 1. shows one conventional inverting analog integrator being driven by one eighth of an MP7641. The input resistance to the integrator is "R". Inserting the MDAC as shown provides an attenuation "a". An equivalent resistance, "Req", is defined equal to "R/a". This "Req" can range from "R" to infinity as the DAC attenuation is changed from one to zero. The effective integration rate or "RC" time constant of eight individual integrators can therefore be digitally set by one MP7641.

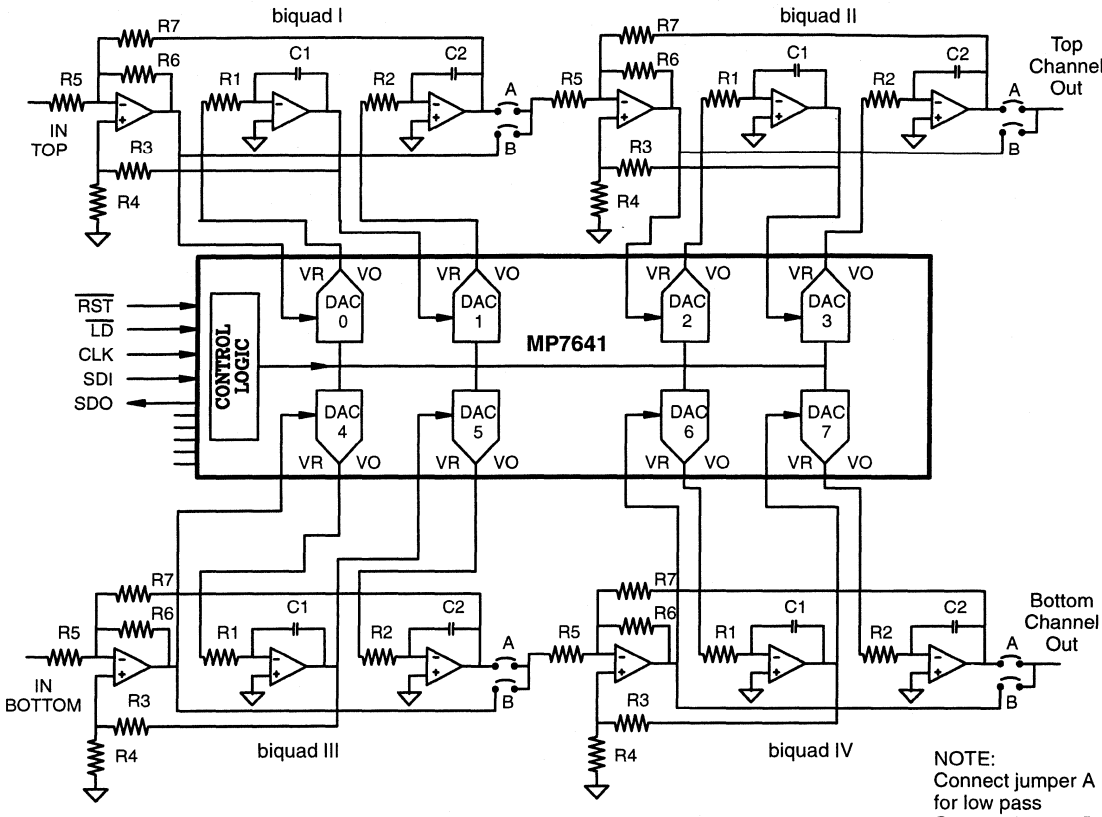


Figure 2. Two Channel Sweepable Butterworth High/Low Pass

Figure 2. shows a two channel continuous time, low pass or high pass, state variable filter circuit. Each channel has four poles generated by two cascaded second order state variable sections. Each of the integrators contains one eighth of a MP7641 to adjust it's "RC" time constant. The circuit shown is designed to produce a maximally flat (Butterworth) response in both channels. The highest frequency response is realized when each of the MDACs offers essentially no attenuation (255/256). Increasing the attenuation lowers the frequency while preserving the Butterworth response, if and only if we keep the attenuation ratio the same for each integrator. The frequency response in either channel is lowered from it's highest value by an amount proportional to the attenuation ratio used for that channel.

Design information for the filter circuit of *Figure 2.* is given in *Table 1.* The initial frequency and type of filter (i.e. Butterworth, Chebyshev, etc.) is determined by the values of the passive components. Low distortion (80 dB) filter circuits ranging from DC to one megahertz are practical using this topology and EXAR's MP7641.

Note that Chebyshev, Bessel, Elliptical or other realizations can be implemented. Band-pass, high-pass, notches, phase equalization, and combinations of these circuits can be developed using normal filter synthesis procedures. The digital control feature is implemented as in *Figure 1.* The calculated integration resistor "R" for the highest frequency is then replaced by "Req". Sweeping to lower frequencies is now realized by reducing the gain of all MDACs proportionally and simultaneously.

Changing the pin strapping from position "A" to position "B" in *Figure 2.* produces a high pass configuration instead of a low pass. The "Butterworth" response and digitally controlled sweepability is preserved. Now by cascad-

ing the two channels and programming the low-pass and high-pass break frequencies independently, a variety of frequency and band-pass options become available.

The resolution of the MP7641 DAC is eight bits which allows 256 discrete settings for the frequency. Attenuations of less than 5% are impractical due to linearity errors. A tuning range of 20 to 1 in increments of .4% is a realistic design goal for circuits of this type.

	I	II	III	IV
R1	1.0k	1.0k	1.0k	1.0k
R2	1.0k	1.0k	1.0k	1.0k
R3	1.46k	0.31k	1.46k	0.31k
R4	0.5k	0.5k	0.5k	0.5k
R5	2.0k	2.0k	2.0k	2.0k
R6	2.0k	2.0k	2.0k	2.0k
R7	2.0k	2.0k	2.0k	2.0k
C1	160pF	160pF	160pF	160pF
C2	160pF	160pF	160pF	160pF

*Note – values are for 1 MHz bandwidth

Table 1. Biquad from Figure 2.

$$w_o = \sqrt{\frac{R6\ a2\ a1}{R7\ R1\ R2\ C1\ C2}}$$

$$Q = \frac{R5(R3 + R4)}{R4(R5 + R6 + R7)}\sqrt{\frac{R1\ R6\ C1\ a2}{R2\ R7\ C2\ a1}}$$

$$Hlp = -\frac{R7}{R5}$$

$$Hbp = -\frac{R6}{R5}$$

$$Hhp = \frac{R6(R3 + R4)}{R4(R5 + R6 + R7)}$$

Design Formulas – State Variable Filter

8

Software Controlled Switched Cap Filters

Switched capacitor filters are often selected as a solution to filtering problems in the frequency ranges from DC to 150 kHz because of cost and size. They require no external op amps or capacitors and as many as four biquads come in one package. New generation designs offer significantly improved noise and distortion performance making their use practical in many more situations. An advantage switched capacitor filters have over continuous time filters is that they can be tuned by changing the clock frequency. This is because the switched integrators are incremented only at each clock period. A slower clock means a slower integration time constant. Frequency domain characteristics are scaled in proportion to the clock frequency.

Changing the clock frequency can cause problems if two circuits in the same system must be tuned separately. Beat frequencies between two clocks causes serious noise disturbances. The MP7641 can be used to provide tuning of multiple switched capacitor filter circuits in the same system without introducing two or more clocks. Size advantages gained by choosing the switched cap circuit are not lost since one MP7641 can be used to "tune" one quad biquad yielding an eight pole adaptive filter with only two "IC's".

Figure 3. shows some common switched capacitor biquads modified to include two multiplying DACs from an

MP7641. These biquads are available from several suppliers as singles, duals, triples, and quads in a single package. Note that each of the three biquads shown has four external resistors and two MDACs. The resistor ratios configure the biquad frequency and gain characteristics according to the manufacturers design equations. Generic sets of these equations are given for each of the three configurations but with the gain ratios of the two MDACs included in each case. The resonant frequency, gain and "Q" of each second order system is settable by specifying the resistor ratios. The gain ratios of the MDACs can be used to change the frequency and "Q" in accordance with the formulas. These relationships are not linear and must be computed. Very complex filter circuits can be implemented with minimal hardware using these circuits.

Three configurations are shown in *Figure 3.* They include biquad I, for high pass, biquad II, for band pass, and biquad III, for low pass. Three configurations are required in order to conveniently alter the "Q" and resonant frequency of the biquad while leaving the gain unaltered without having to resort to three MDACs per stage. The added attenuation ratio of the two MDACs is included as the variables "a2","a3", and "a4" in these equations corresponding to the resistor that particular MDAC is associated with. The frequency response of a biquad can now be software specified by loading the appropriate eight bit word into the two MDACs. The clock frequency is usable as an additional variable.

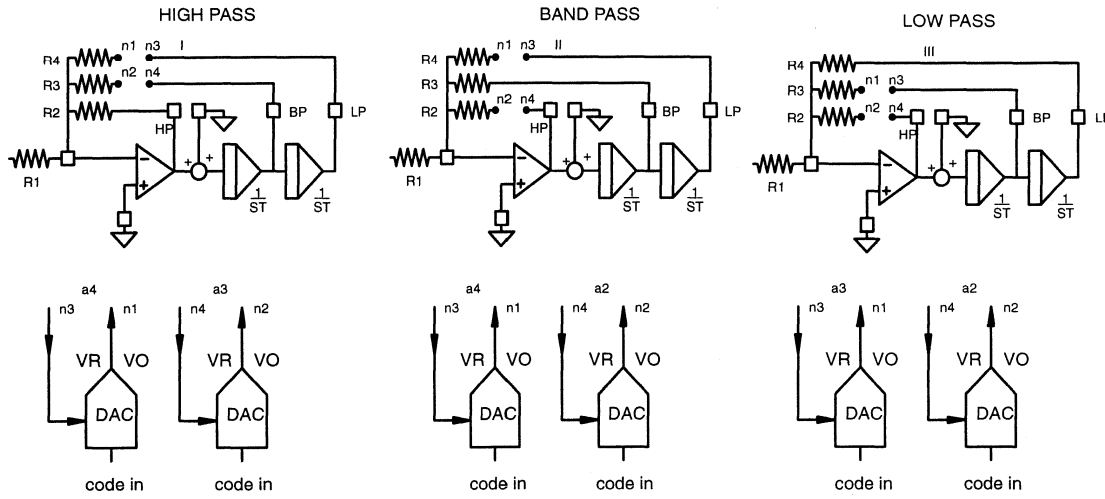


Figure 3. Adjustable Switched Cap Filter Configurations

$$fo = \frac{Fclk}{100}\sqrt{\frac{R2\ a4}{R4}} \qquad fo = \frac{Fclk}{100}\sqrt{\frac{R2\ a4}{R4\ a2}} \qquad fo = \frac{Fclk}{100}\sqrt{\frac{R2}{R4\ a2}}$$

$$Q = \frac{R3}{R2\ a3}\sqrt{\frac{R2\ a4}{R4}} \qquad Q = \frac{R3\ a2}{R2}\sqrt{\frac{R2\ a4}{R4\ a2}} \qquad Q = \frac{R3\ a2}{R2\ a3}\sqrt{\frac{R2}{R4\ a2}}$$

$$Hohp = -\frac{R2}{R1} \qquad Hobp = -\frac{R3}{R1} \qquad Holp = -\frac{R4}{R1}$$

Design Formulas

Figure 4. demonstrates the principle. Shown is an eight pole Butterworth filter configured to be an adjustable bandpass. The top channel uses two of the biquad I circuits from *Figure 3.* The bottom channel uses two of the biquad III's from *Figure 3.* Both channels together use all eight of the MP7641 DACs. The top channel is a four pole high pass and the bottom channel is a four pole low pass filter. The circuit is scaled so that each channel rolls off at 50 kHz when all MDACs have no attenuation (code=11111111, fclk=5 MHz). The "f_{3dB}" frequency of the top channel high pass is lowered as DAC attenuation is increased. The "f_{3dB}" frequency of the bottom low pass section is increased as DAC attenuation is added. The frequency of both channels is proportional to the clock frequency but can also be altered independently by setting the appropriate biquad's to the values given by the formulas in *Table 2.* and *Figure 3.* Note that a non-linear relationship is needed to specify these settings and that the relationship between the DAC coefficients must be maintained to preserve the "Butterworth" response.

Because the frequency "f_{3dB}", is proportional to the square root of DAC settings, the tuning range is limited to approximately four to one due to finite DAC resolution. A combination of clock and DAC tuning can produce a wide tuning range while minimizing noise problems since the clock can stay an integer sub-multiple of the master clock.

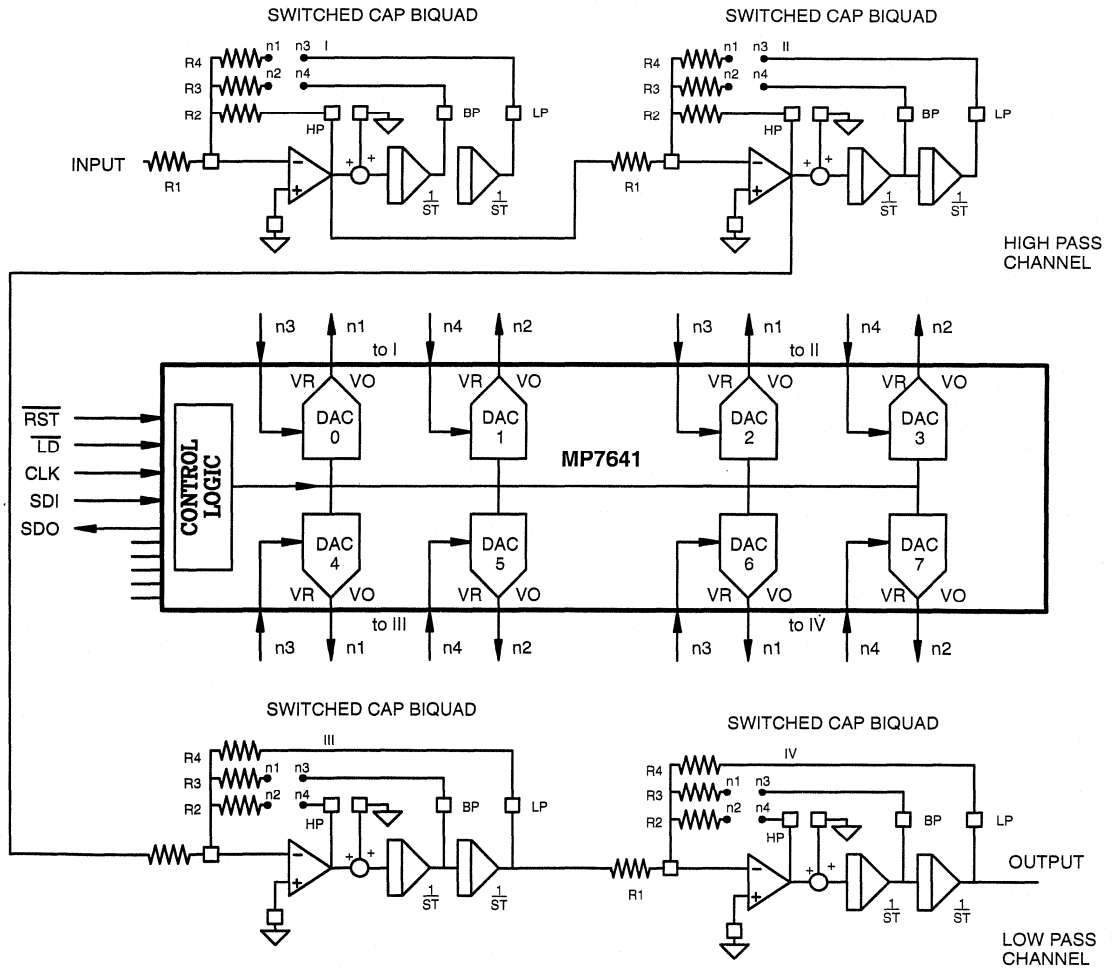


Figure 4. Switched Cap Adjustable Band Pass

	I	II	III	IV
R1	10k	10k	10k	10k
R2	10k	10k	10k	10k
R3	13k	5.4k	13k	5.4k
R4	10k	10k	10k	10k

Table 2. Resistor Values from Figure 4.

f_{3dB} *top (high pass)* $= 50kHz\sqrt{a4}$ if $a3 = \sqrt{a4}$

f_{3dB} *bottom (low pass)* $= 50kHz\frac{1}{\sqrt{a2}}$ if $a3 = \sqrt{a2}$

Conditions for Adjustment
Nominal Clock of 5 MHz, f_{3dB} top=f_{3dB} bottom=50kHz

BREADBOARD RESULTS

Continuous Time Circuit – Figure 2.

A breadboard of the filter circuit of *Figure 2.* was constructed and evaluated. *Figures 5, 6, 7, and 8* show the spectrum analyzer generated frequency responses of the circuit for various test conditions. High speed op amps (i.e., EL2424) were used with the resistor values given in *Table 1.* The capacitor values are specified for each figure.

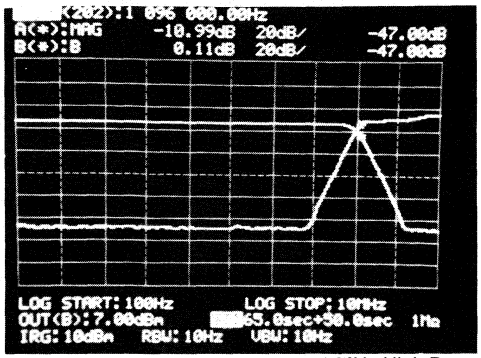
Figures 5 and 6 demonstrate the wide bandwidth capability of the MP7641. The top channel is configured as a high pass and the bottom channel is jumpered as a low pass filter. The MDAC is removed and replaced by a jumper for *Figure 5.* and is included at a gain of one for *Figure 6.* The two configurations should show the same frequency response, roll off's of 80 dB per decade with "f_{3dB}" points at 1 MHz for all channels. Note that a slight peaking difference can be seen in *Figure 7.*, the case where the MDACs are included. This peaking is due to the finite 12 MHz bandwidth of the MP7641. Few multiplying DACs have adequate bandwidth to perform as well at this frequency. The Q of second order systems is sensitive to the additional phase shift introduced by the MDAC. Compensation resistors in series with each integration capacitor can improve performance further by offering phase lead to offset the lag introduced by the MDAC and op amp.

Figures 7 and 8 demonstrate the flexibility of the cascaded system. At MDAC settings of one and an integrator capacitor of 1,160 pF, the "f_{3dB}" point for a channel calculates to be approximately 140 kHz. *Figure 7.* shows a band pass response where the low pass is set to 140 kHz. and the high pass response is at 17 kHz. The latter is accomplished by setting the MDACs in the top channel to 1/8 full scale. *Figure 8.* shows the low pass at 100 kHz and the high pass at 33 kHz. The top and bottom channel MDACs attenuations are set to 3/4 and 1/4, respectively. Note the smooth Butterworth response in both these examples.

Switched Capacitor Circuit – Figure 4.

A breadboard of the switched capacitor band pass filter circuit of *Figure 4.* was constructed and evaluated. *Figures 9, 10, 11, and 12* show the spectrum analyzer generated frequency responses of the circuit for various test conditions. An LTC1064 switched capacitor circuit was used with the resistor values given in *Table 2.* The design equations of *Figure 3.* were used to establish a Butterworth response. They also must be used to calculate the MDAC attenuation for different frequency responses while maintaining the proper shape in the frequency domain. Each time the ratio's a4 or a2 is changed, a3 must be changed by an amount equal to the square root of that change. This keeps the "Q" of each biquad constant while allowing a frequency shift.

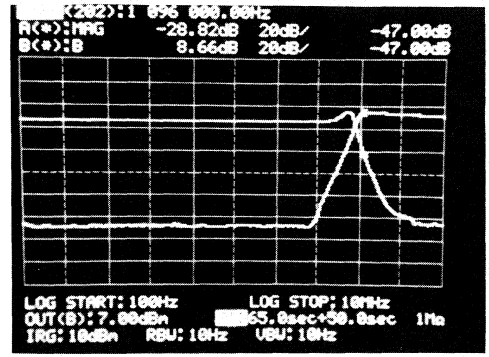
Figure 9. shows the response with the MDACs ratios set at unity and the clock at 4 MHz. The "f_{3dB}" frequency for both the low pass and high pass is 40 kHz, thus the sharp corner at the peak. In *Figure 10.*, the MDACs ratios a4, a2, and a3 are set to 1/4, 1/4, and 1/2, respectively. This lowers the high pass frequency to 20 kHz and raises the low pass frequency to 80 kHz. The flat top is 60 kHz wide. *Figure 11.* and *Figure 12.* show the same banc pass after the clock frequency has been reduced 2 to 1 and 4 to 1. The "f_{3dB}" points shift proportional to the clock frequency.



C = 160 pF
R's = (see table)

1 MHz High Pass
1 MHz Low Pass

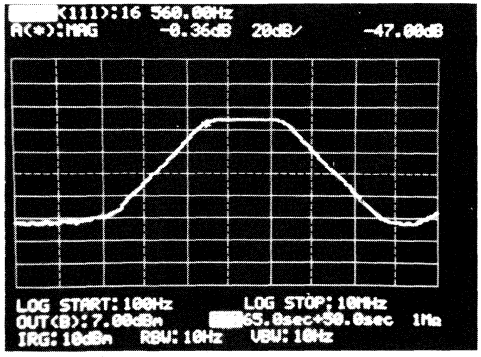
Figure 5.
Continuous Time Filter
with No DACs



C = 160 pF
R's = (see table)

1 MHz High Pass
1 MHz Low Pass

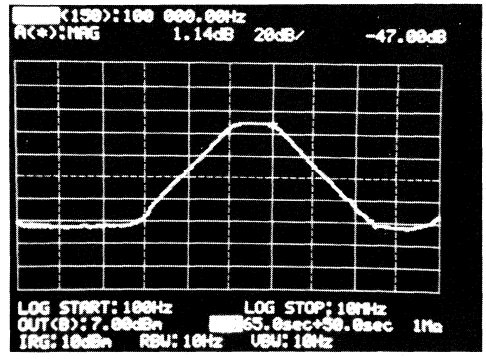
Figure 6.
Continuous Time Filter
with MDACs set to 1



C = 1, 160 pF
R's = (see table)

Top Channel Attentuation = 1/8 (17 kHz)
Bottom Channel Attentuation = 1 (140 kHz)

Figure 7.
Continuous Time Filter
Band Pass

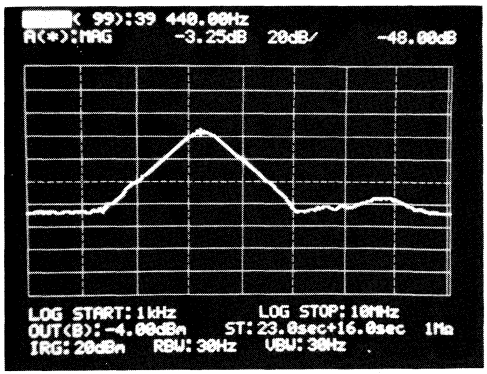


C = 1, 160 pF
R's = (see table)

Top Channel Attentuation = 1/4 (33 kHz)
Bottom Channel Attentuation = 3/4 (100 kHz)

Figure 8.
Continuous Time Filter
Band Pass

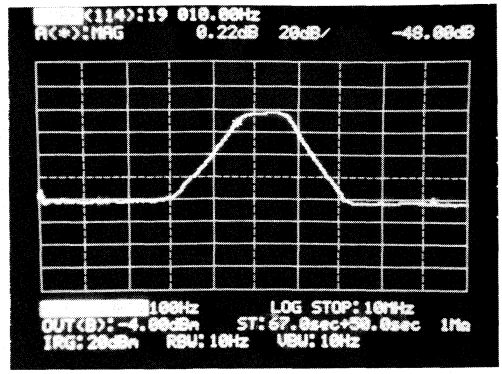
8



F_{CLK} = 4 MHz

High Pass – $a_4 = 1$, $a_3 = 1$ (40 kHz)
Low Pass – $a_2 = 1$, $a_3 = 1$ (40 kHz)

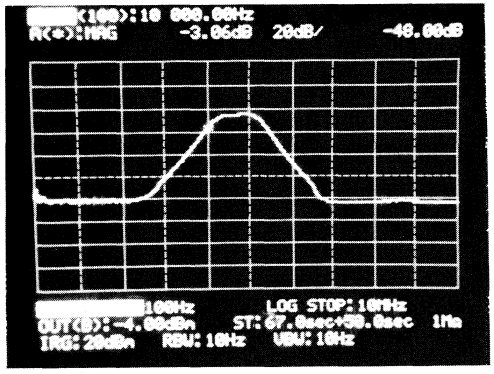
Figure 9.
Switched Cap Filter
with MDACs set to 1



F_{CLK} = 4 MHz

High Pass – $a_4 = 1/4$, $a_3 = 1/2$ (20 kHz)
Low Pass – $a_2 = 1/4$, $a_3 = 1/2$ (80 kHz)

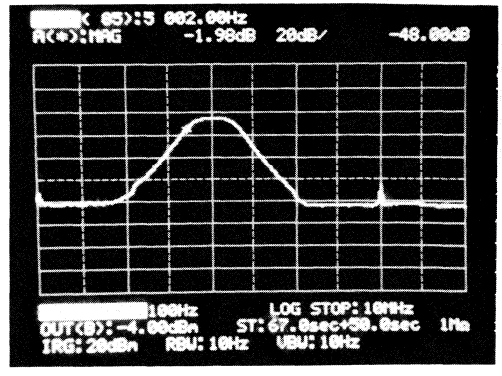
Figure 10.
Switched Cap Filter
20 kHz to 80 kHz



F_{CLK} = 2 MHz

High Pass – $a_4 = 1/4$, $a_3 = 1/2$ (10 kHz)
Low Pass – $a_2 = 1/4$, $a_3 = 1/2$ (40 kHz)

Figure 11.
Switched Cap Filter
10 kHz to 40 kHz



F_{CLK} = 1 MHz

High Pass – $a_4 = 1/4$, $a_3 = 1/2$ (5 kHz)
Low Pass – $a_2 = 1/4$, $a_3 = 1/2$ (20 kHz)

Figure 12.
Switched Cap Filter
5 kHz to 20 kHz

Conclusion

Flexible software control of frequency shaping circuits including adaptive filter networks, adaptive control system compensation, adaptive equalization circuits, etc. can conveniently be implemented using the MP7641. It's patented features open new avenues including:

- Eight voltage output 8-bit MDACs
- Low cost
- Low distortion
- Wide bandwidth – 10 MHz
- Excellent applications support

NEW PRODUCT NOTE

EXAR also offers an 8 bit, 16 channel multiplying DAC, the MP7642. This part will double the order of a filter controllable by one MDAC package. Most of the techniques proposed in this design note are applicable.

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SPICE MACROMODEL FOR THE MP7641

Introduction

The MP7641 eight channel video multiplying digital-to-analog converter can be used in applications where digitally controlled gain with wide bandwidth buffering is required. Video channel gain control, communications channel equilization, active tunable filters, and adaptive feedback systems are examples. Behavioral system simulation is often useful in evaluating topologies under consideration. The SPICE subcircuits offered here approximate the linear behavior of a MP7641 channel and can be used with PSPICE (*copyright Microsim Corporation*) to gain insight into the linear behavior of MP7641 based circuits. Small nomenclature changes permit its use with most versions of SPICE.

Performance

Graph 3. demonstrates the accuracy of the Macro. Amplitude, phase, and group delay are plotted versus frequency. The plot includes the same information for a full I.C. simulation that includes all devices and parasitics. The digital code was set for a gain of 0.5 (half scale).

Graph 4. shows the Macro's gain, phase, and group delay for input code values ranging from 1/8 full scale to full scale. The actual circuit and the Macro have frequency characteristics that vary slightly with code input values. The Macro uses a voltage controlled resistor to model this trait. Note that input code is represented by an analog voltage that must be set between 0 and .996, corresponding to 0 to full scale digital input (0 to 255 decimal code).

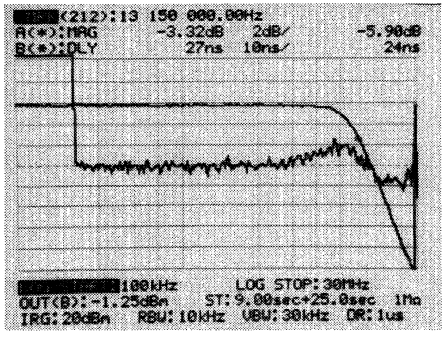
Graph 1. shows the amplitude and group delay of a typical device versus frequency. *Graph 2.* is an oscillograph of amplitude and phase for a typical device. Comparing this data to *Graph 3.* further demonstrates the accuracy of the Macro.

The Test Circuit

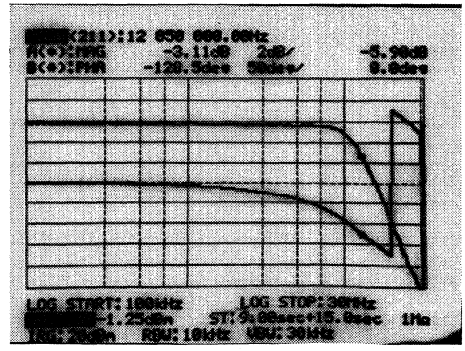
Figure 1. shows a test circuit diagram that uses the MP7641 Macro. The two subcircuits shown must be included together in a SPICE file. The 7641 subcircuit calls the voltage controlled resistor subcircuit. The file listings are given below.

Cautions

This Macro accurately predicts the typical linear behavior only. Nonlinear effects such as clipping, output current limiting, etc. will not be reproduced. Temperature and noise effects are not included. The macro is primarily useful in determining small signal frequency and phase response characteristics, and consequently EXAR does not warrant designs based on its use. The model is copyrighted and is a member of the EXAR macro library.



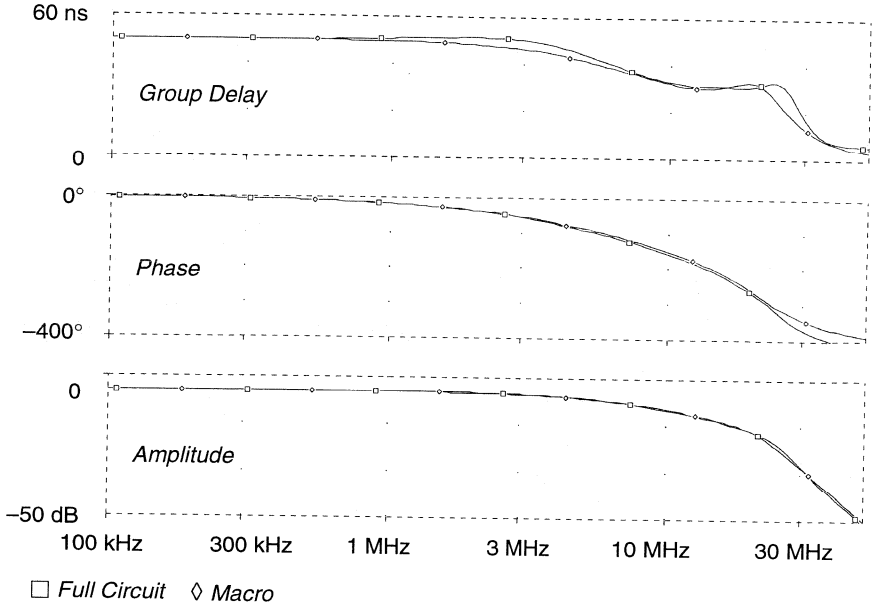
Graph 1. (Oscillo) Amplitude and Group Delay vs. Frequency



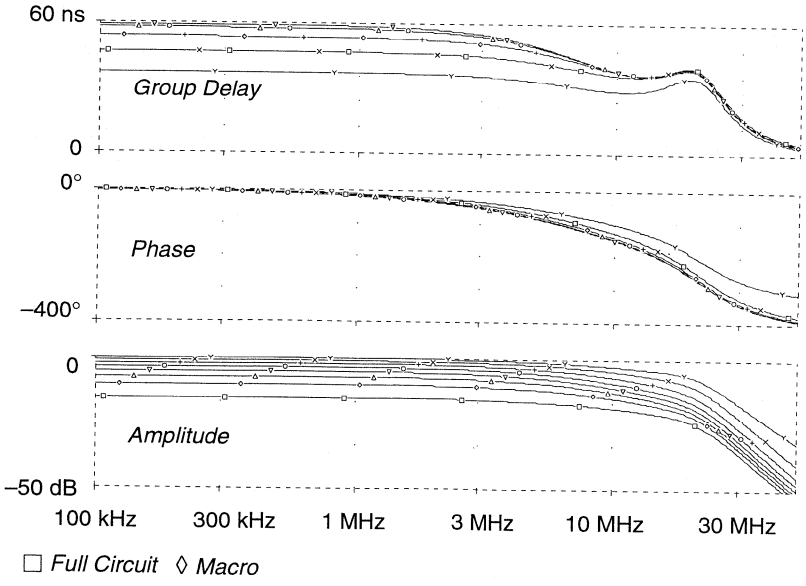
Graph 2. (Oscillo) Amplitude and Phase vs. Frequency

SAMPLE SPICE FILE

```
7641 macro test file
*Runs AC response for 8 input codes (.125 Full scale to Full
*scale in .125 increments
**************************************************
.param   test=1                ;parameter used in step
.step param test .125 1 .125   ;steps code
.OP
.ac oct 40 10k 100meg
*.TRAN .1U 1u 00u 20n ;(UIC)
**************************************************
vin 1 0 ac 1          ;analog input source
vcode 2 0 {TEST}      ;variable defining code input
x7641 1 3 2 7641      ;MP7641 macro
*=============== Beginning of Macro ========================©1993 Micro Power Systems
*Note the code input is represented by an analog voltage
*between 0 and 1 which scales the gain from 0 to 1.
          .subckt 7641 in out code
          einiso in1 0 in 0 1
          empot 9 0 poly(2) (code,0) (8,0) 0 0 0 0 -1
          vunit code 8 1
          x1 9 0 10 in1 7 vr  ;voltage controlled resister
          clad 7 0 6p
          emout in2 0 poly(2) (7,0)(code,0) 0 0 0 0 1
          r1 in2 1 1k
          r2 2 3 1k
          r3 5 0 1.429
          c1 1 0 16p
          c2 3 0 10p
          c3 5 0 .00753u
          l1 4 5 .00753u
          e1 2 0 1 0 1
          e2 4 0 3 0 1
          e3 out 0 5 0 1
          rref 10 0 12k
          rn8 8 0 1t
          rout out 0 1t
          rin1 in1 0 1t
          rin in 0 1t
          .ends
          * Voltage Controlled Resister Subcircuit *
          .subckt vr 1 2 3 4 5
          eout 4 6 poly(2) (1,2) (3,0) 0 0 0 0 1
          fcopy 0 3 vsense 1
          rin 1 2 1t
          vsense 6 5 0
          .ends
*================= End of Macro ==================
.OPTIONS   ITL5=0 ITL4=140 itl1=150 itl2=150 RELTOL=.001
NOPAGE NUMDGT=6 abstol=1e-15
.probe
.END
```



Graph 3. Macro/Full Circuit Comparison



Graph 4. Macro Response

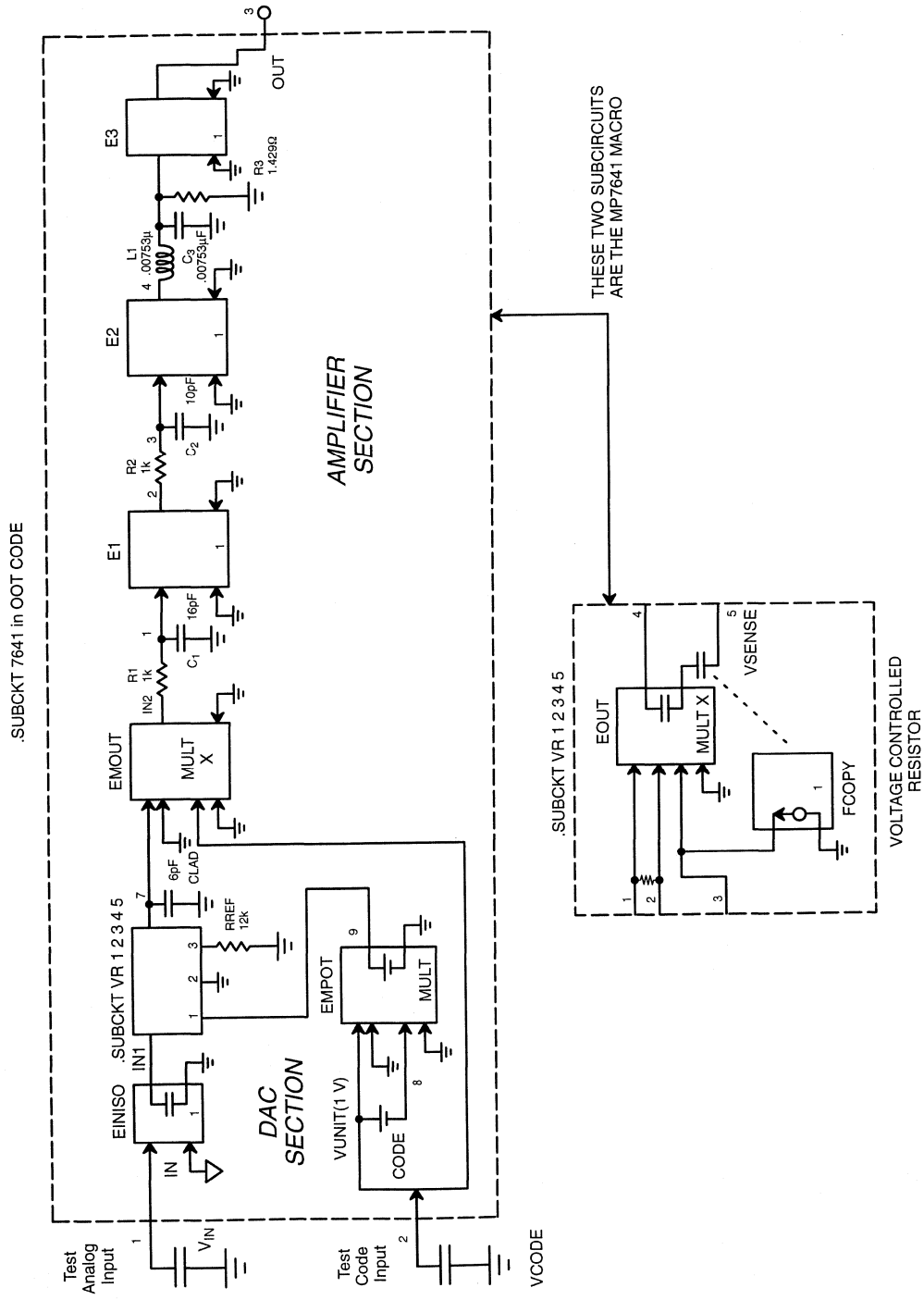


Figure 1. MP7641 Spice Macromodel Test Circuit

MP7610/11/12/13 APPLICATION HINTS

ANALOG GROUND CURRENT

The MP7610 family of Octal DACs has extremely small analog ground current, which significantly reduces channel-to-channel intermodulation and board layout complexity. Unlike a standard R-2R DAC architecture, the MP7610 family uses a voltage mode operation which eliminates both large, code dependent analog ground currents and reference voltage kickback. *Figure 1.* shows a simplified diagram of one DAC channel. The analog ground current, IGND, per channel is determined by the following expression:

$$IGND = \left(\frac{MSB\ CODE}{8} - 1\right) * \frac{V_{REF}}{R}.$$

For values of V_{REF} = 5 V and R = 75kΩ,

$$IGND = \pm 60\mu A$$

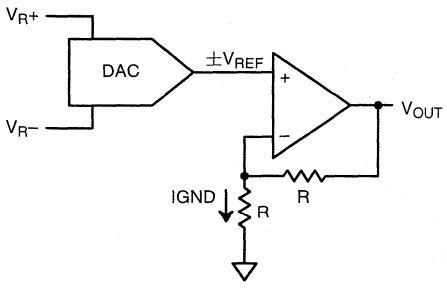
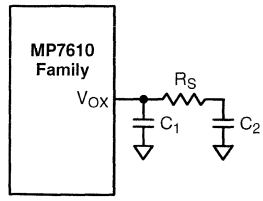


Figure 1. Simplified Block Diagram of One DAC Channel from the MP7610 Family.

CAPACITIVE DRIVE CAPABILITY

The MP7610 Family settling time is specified for a 50pF load. Each channel is capable of driving up to a 500pF capacitive load without any impact on stability and with minor degradation in settling time. For capacitive loads above 500pF, isolate the capacitive load from the DAC output with a 50Ω resistor. With the isolation resistor, the DAC output can drive up to 1μF of capacitance without any impact on stability (*Figure 2.*)



Conditions for Stability

For $C_2 = 0$	$C_1 \leq 500pF$ $R_S = 0$
For $(C_1 + C_2) > 500pF$	$C_1 < 500pF$ $C_2 < 1\mu F$ $R_S = 50\Omega$

Figure 2. Capacitive Drive Capability. Recommended configuration to maintain stability.

ANALOG APPLICATION HINTS

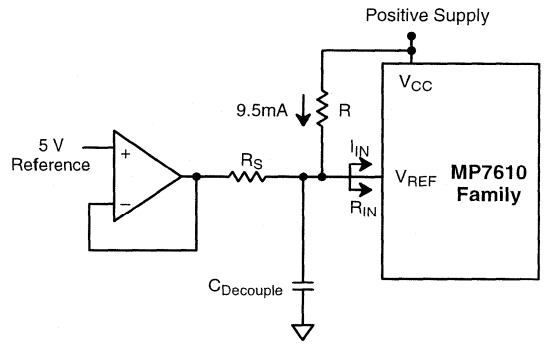


Figure 3. Driving the Reference Pin

Since R_{IN} of the V_{REF} pin can vary from 350Ω to 1.05kΩ, I_{IN} will vary from 14.3mA to 4.8mA for a 5 V reference. By connecting a resistor from the positive supply to the reference pin and appropriately decoupling it, the resistor can provide a current of 9.5mA to the reference pin and the op amp only needs to drive at most ±4.8mA. R_S may be required to stabilize the reference driving amplifier due to the decoupling capacitor (*Figure 3.*)

8

LINEARITY SPECIFICATIONS

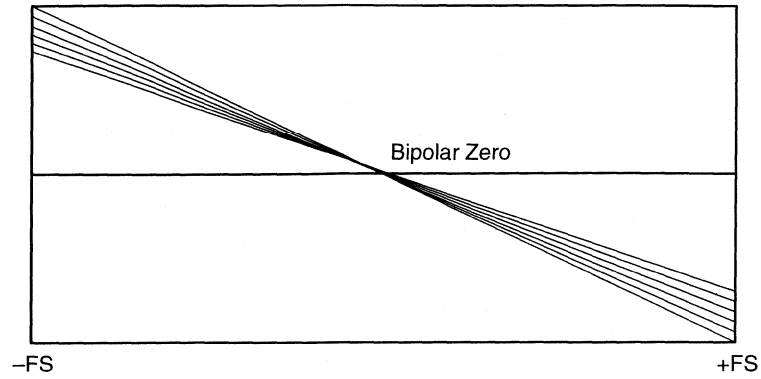


Chart 1. Total Unadjusted Error

This section will explain how the linearity specifications are defined, measured and used. First, all channels are measured at all codes with the voltage reference equal to 5.000V. *Chart 1.* represents a typical error plot of all channels over all codes. From this data INL, DNL, positive and negative full scale errors, and bipolar zero error for each channel are obtained.

Then, the reference voltage at the V_{REF} terminal is adjusted such that the positive and negative full scale errors for DAC0 are equal. This allows us to provide three parameters that are not normally specified. These are, Channel to Channel Maximum Error (ΔE), All Channels Maximum Error (ME), and All Channels Maximum Error Span (MES). The Channel to Channel Maximum Error (ΔE) is effectively the worst case matching between any two channels at any code. The All Channels maximum Error (ME) is the total error bound for all channels when the voltage reference, V_{REF}, has been adjusted to give DAC0 minimum total error. Since the ME specification includes offset, the total error span will be smaller than the ± ME bound, therefore a Maximum error span is specified, MES. *Chart 2.* shows an example error plot for all channels at all codes after V_{REF} has been adjusted. In this example, the Channel to Channel Maximum Error, ΔE = 1 LSB, the All Channels Maximum Error, ME = ±2 and the All Channels Maximum Error Span, MES = +2 – (–0.5) = 2.5 LSB.

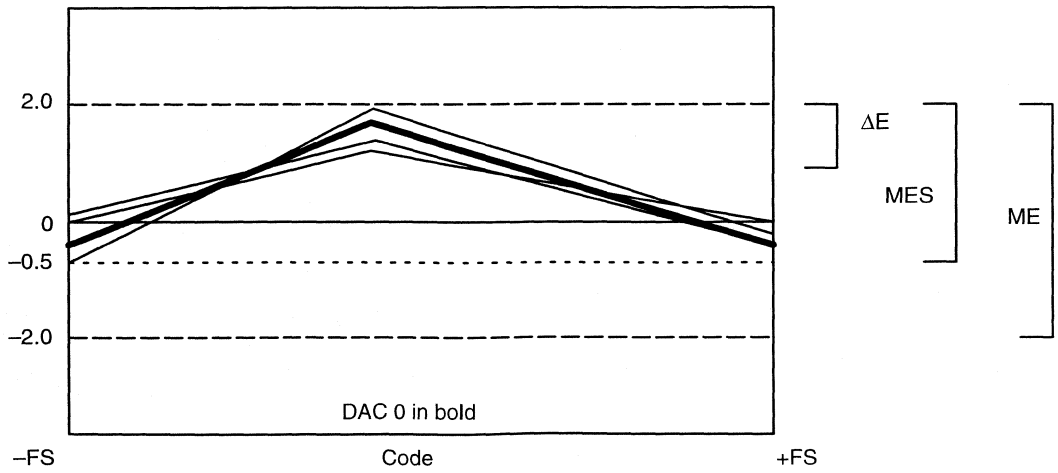


Chart 2. Total Remaining Error after DAC 0 Adjusted

SYSTEM CALIBRATION

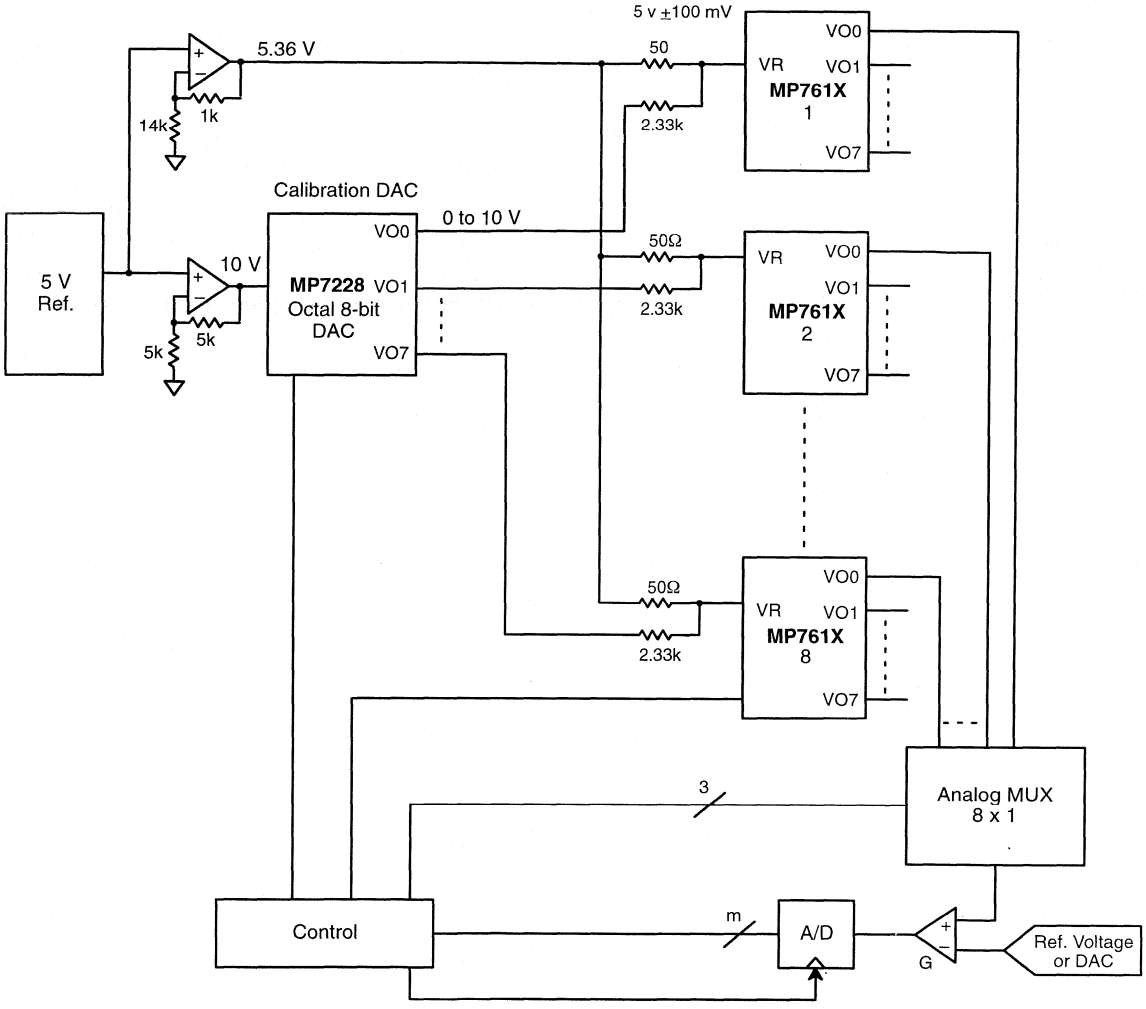


Figure 4. Calibration Block Diagram

One of the advantages of the 761X series of octal DACs lies in the inherent matching between all eight channels which greatly simplifies system calibration. *Figure 4.* shows a block diagram of a calibration scheme which illustrates how to calibrate 64 DAC channels using one 8 channel data acquisition circuit, a controller and an octal calibration DAC. Since the input resistance at the VR pin is 700Ω, the reference voltage applied to each octal DAC can be set to 5 V ±100mV in 780µV steps.

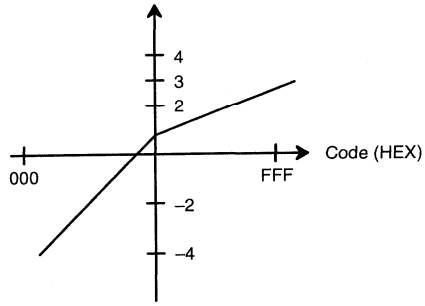
Because of the unique method used to specify the accuracy of the 761X family of octal DACs, one need only calibrate DAC0 and all of the channels are fully specified. By calibrating the +FS and –FS values of DAC0 to have the SAME error, the total error of all of the channels is minimized and is specified by ME. Therefore, as shown in *Figure 4.*, only the output of DAC0 for each IC is connected to the data acquisition circuitry.

The calibration system functions as follows. The controller selects which IC to calibrate by addressing the analog MUX appropriately. Then DAC0 is loaded with all zeros to set the output to minus full scale. The difference between the output and an ideal (reference point) output is gained by the difference amp and the resulting error is digitized by the A/D. The same operation is repeated to measure the +FS error. Once the +FS and –FS errors are known, the reference voltage supplied to the DAC is adjusted with the calibration DAC to set the +FS error EQUAL to the –FS error. This process is then repeated for all of the ICs.

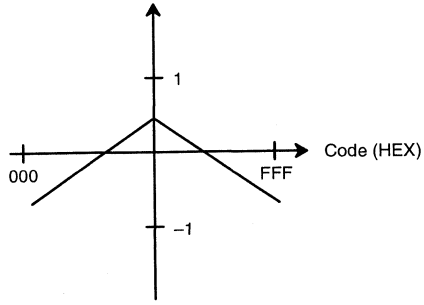
Figure 5. shows a graphical example of the calibration process. *Figure 5A* shows the transfer curve of DAC0 before calibration (i.e. V_{REF}=5.000V). The –FS error is measured to be –4 LSBs (–19.5mV) and the +FS error is measured to be +3 LSBs (+14.65mV). In order to make the +FS error equal the –FS error = –0.5, the calibration DAC would be incremented to make

$$V_{REF} = 5.0\ V - (3.5\ LSBs/2) = 4.9915\ V$$

Therefore, the output of the calibration DAC would be set to 5 – [(5.0 – 4.9915) X 50] = 4.575 V. The input code to the calibration DAC would be HEX (75). *Figure 5B* shows the resulting error curve for DAC0 after calibration.



A. DAC0 Error Curve before Calibration



B. DAC0 Error Curve after +FS Error = –FS Error

Figure 5.

MP8795 / GENERAL HIGH SPEED ADC EVALUATION CIRCUIT

This note provides suggestions for building a test circuit and evaluating the MP8795. Assembly of high speed data conversion circuits require special layout and construction techniques. Improper circuit board design will seriously degrade performance.

Construction

The circuit shown in *Figure 1.*, when properly assembled, can be used for evaluating the performance of the MP8795. The following construction "hints" may be used as a guide.

1. Avoid using wire wrap and sockets. These add parasitic capacitance and inductance that will seriously degrade performance. The use of surface mounted components is recommended where possible.

2. Use separate analog and digital ground planes for shielding only. Use separate analog and digital ground paths. Use large traces or wire, and connect analog and digital grounds and ground planes together at one point only. This common connection should be as close to the analog ground pin of the package as possible.

3. Use a solid tantalum capacitor (4.7 µF) in parallel with a small ceramic capacitor (.1 µF) for all decoupling. Place all ceramic decoupling capacitors as close to the package as possible (less than 1/4 in.). Chip capacitors have the lowest lead inductance and are preferable. The optional inductors shown add further isolation from noise on the 5 volt supply lines. The 5 V power for AV_{DD} and DV_{DD} should be derived from the same source since they are connected to the substrate internally.

4. Use digital latches as buffers at the output to minimize output capacitance which increases internal transient currents in the digital circuitry. High speed, low power logic is preferred. An output enable should be used to tristate these latches during the A_{IN} sample time.

5. The analog input must be a low impedance source or the optional analog buffer amplifier should be used. Ground plane voids should be put in the vicinity of the input terminals to the amplifier and the feedback resistor to reduce stray capacitance to ground. This buffer will also require decoupling capacitors, short input leads, shielding from logic signals, wide bandwidth, stable performance, and a 50Ω isolation resistor from its output to the input to the MP8795. Signal transmission to the amplifier should be from a 50Ω source through a terminated coax (50Ω to ground at the receiving end), to minimize reflections. The amplifier shown produces satisfactory performance.

6. The clock input should be shielded, properly terminated, and dressed so that coupling from the digital output to the analog input and other analog terminals is minimized. The termination current should be through the shield back to the source.

7. The reference voltage source should be low impedance and decoupled as indicated. Adding the decoupling capacitors to the resistor divider string taps improves high frequency performance.

8. Avoid any inputs on any pin exceeding AV_{DD} +0.5 V or AGND– 0.5 V. Observe the absolute maximum electrical ratings listed on the data sheet.

8

Dynamic Performance Evaluation

Dynamic testing of high resolution, high speed "flash" analog to digital converters is commonly done by inputting low distortion sinusoidal waveforms, digitizing this input with the A/D under test, then calculating the effective resolution, linearity error and distortion using DSP and FFT software packages.

No matter what data gathering system or what level of software sophistication is used to perform dynamic testing, meaningful results will only be attained with a good clean hardware setup. It is absolutely necessary that the input source have lower distortion than is expected from the circuit being tested.

Cross Plot Performance Evaluation

An evaluation of integral and differential linearity can be done by using a simple "bench" approach which displays a "cross plot" of code widths on an oscilloscope. In addition to the circuit being evaluated, the test setup requires an oscilloscope, a low noise D.C. voltage source, and a triangle wave generator. This "cross plot" technique is implemented as is shown in *Figure 1.* and used as follows.

The precision voltage source is used to manually set any D.C. input level. A small portion of the 1 kHz triangle wave generator output is added to the D.C. input signal and the sum is applied to the A/D under test. The amplitude of this "dither" signal is nominally eight LSBs, peak to peak, referred to input. The full output of the triangle wave source also drives the horizontal input (x axis) of the oscilloscope and the gain control is set so that each division is one LSB referred to the D.C. input. The two weighted resistors, connected between the least significant two output bits, are used to detect code changes and generate four output levels at node "C". This node drives the vertical scope input (set at 1 volt per division).

The small added "dither" signal will sweep through several LSBs about the D.C. input level causing the A/D output to change accordingly. These code changes are displayed on the oscilloscope as a staircase and where each horizontal division represents one LSB. Note that it is the horizontal stair step width that is a measure of input code width. The vertical height of each step is not meaningful.

The input can be manually swept over the input range and all code widths observed. Missing codes will cause one or more of the staircase steps to be skipped. Wide codes will cause the steps to be greater than one division wide. If the endpoint thresholds (zero and full scale) are set to coincide with the oscilloscope vertical grid lines, integral linearity errors are displayed as code changes which are off centered from these grid lines. The slow "dither" at the input allows several conversions to be made at each threshold. The dispersal of the vertical step is a qualitative measure of noise at that threshold.

These observations can be made at various conversion rates, power supply levels, and over temperature so that significant performance data can be attained without sophisticated acquisition hardware and software packages.

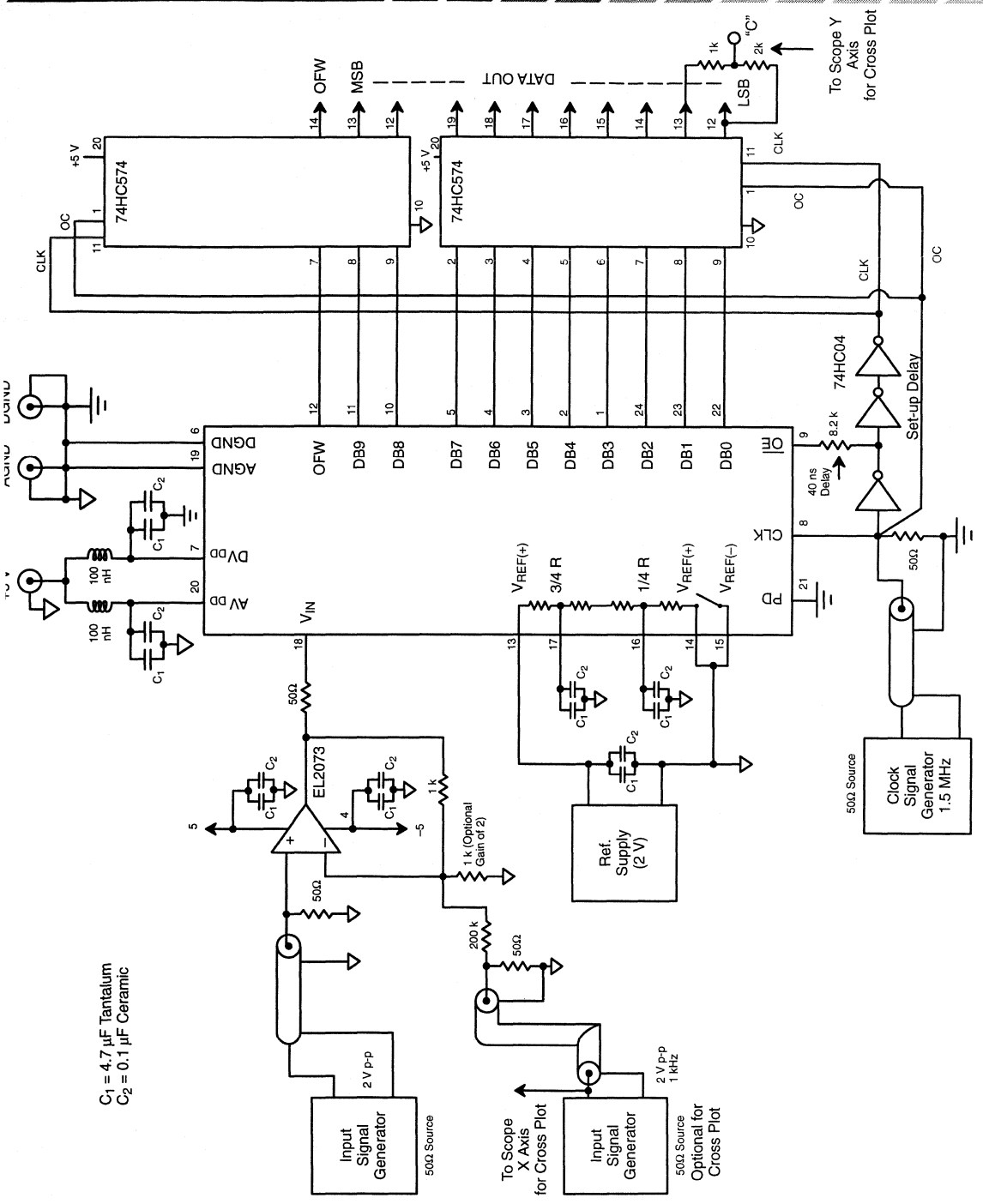


Figure 1. MP8795 Evaluation Circuit

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COMPENSATING FOR ZERO ORDER HOLD EFFECTS

Introduction

EXAR's family of high resolution and high speed analog-to-digital and digital-to-analog converters are often used in digital video, digital graphics and other mixed signal systems where sampled data phenomenon must be accounted for in optimizing performance. The amplitude attenuation introduced by the "hold" function when recreating analog signals from sampled data is an example. A simple, one amplifier circuit to compensate for this unwanted frequency response loss, while preserving constant group delay, is introduced.

Circuit Description and Results

A diagram of a sample-hold and the proposed compensation circuit is shown in *Figure 1.* When data is taken directly from the output of the sample–hold (OUT1), the magnitude of the frequency response follows a SIN(X)/X curve. Adding the compensation circuit produces a modified and significantly improved frequency response (OUT2). The value of the RC product in the compensation circuit is determined by the sampling frequency (1/4 of sampling period) as shown.

Plots of these effects are shown in *Figure 2.* and *Figure 3.* The frequency responses shown were generated by a SPICE simulation of the circuit shown in *Figure 1.* The sampling frequency (F_S) used was 15 MHz. The RC product for the compensation circuit was 16.6 ns. An ideal op amp was used for the simulation.

The amplitude plot in *Figure 2.* displays three curves. Curve "A" represents the hold transfer function alone. Curve "B" shows the improved transfer characteristics after compensation. Curve "C" shows the amplitude of the first order lead response supplied by the compensation circuit to hold the overall response flat to higher frequencies. If the compensation circuit was only a simple first order lead, it would introduce phase distortion into the modified frequency response. To prevent this, a portion of the compensation section is an all pass, phase equalization circuit to keep the phase shift linear. The group delay plot in *Figure 2.* presents the results. Curve "D" shows the ideally constant group delay of the hold circuit. Curve "E" shows group delay after amplitude compensation and phase linearization. Note that only a few nanoseconds deviation from constant group delay exist for frequencies lower than half the sampling rate (7.5 MHz).

Figure 3. repeats the information of *Figure 2.* but uses an expanded scale so more detail is visible in the signal band. It can be seen that the amplitude error at half sampling frequency (7.5 MHz) can be lowered from almost 4 dB to less than 0.25 dB. Curve "F" was added to the group delay plot, This shows the group delay response to be expected with lead compensation alone. This demonstrates that the phase equalization is desirable since considerable phase distortion would be present otherwise.

Conclusion

The circuit to compensate for the effects of the sample/hold operation can also be placed in the analog path prior to the A/D converter when linear operations are being performed on the signals. Antialiasing and smoothing filters sometimes have the SIN(X)/X compensation function built in.

The single amplifier circuit proposed in *Figure 1.* approximately implements the transfer function:

$$\frac{OUT2(s)}{OUT1(s)} = \frac{(1 - s \cdot RC)\ (1 + 1.4 \cdot RC \cdot s)}{(1 + s \cdot RC)\ (1 + 0.25 \cdot RC \cdot s)}$$

Any alternate circuit having this transfer function will produce the same results. The resistors, capacitors, and op amps used must be selected carefully to be compatible with the frequency requirements. The SPICE file used to generate the frequency response plots is listed below.

8

PSPICE CIRCUIT FILE

```
hold compensation test
*****************************************************
.ac oct 200 1k 100meg
*****************************************************
vin 1 0 ac 1
ehold 2 0 LAPLACE {v(1)}={(1-exp(-s/15e6))/(s/15e6)}   ;hold

e1 14 0 11 10 1000
r1 2 10 1.0k
r2 2 11 1.0k
r3 10 12 1.0k
r4 14 12 .1k
r5 13 0 .02k
c1 11 0 16.5p
c2 12 13 200p

rn1 1 0 1t
rn2 2 0 1t
*********************************************************
.OPTIONS    ITL5=0 ITL4=140 itl1=150 itl2=150 RELTOL=.001
NOPAGE NUMDGT=6 abstol=1e-15
*********************************************************
.probe
.END
```

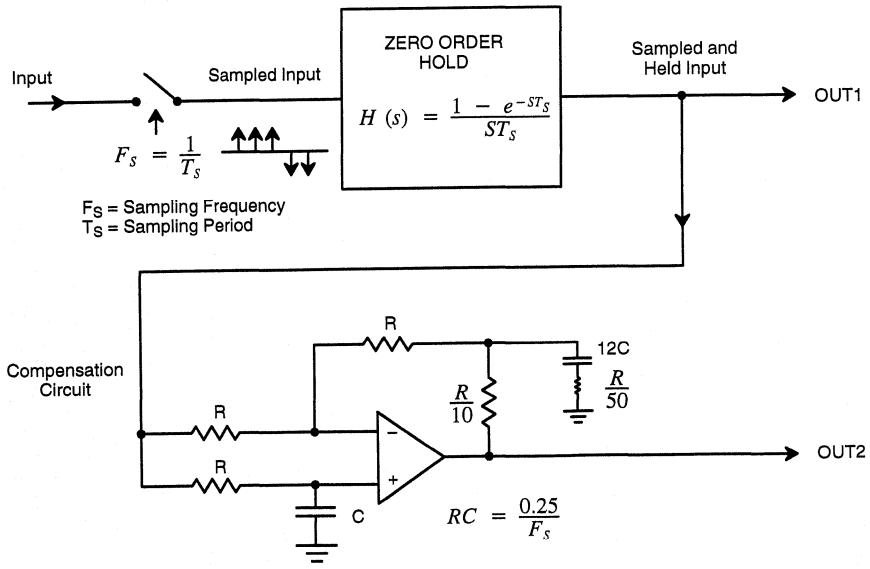

Figure 1. Compensating for Zero Order Hold Amplitude Attenuation

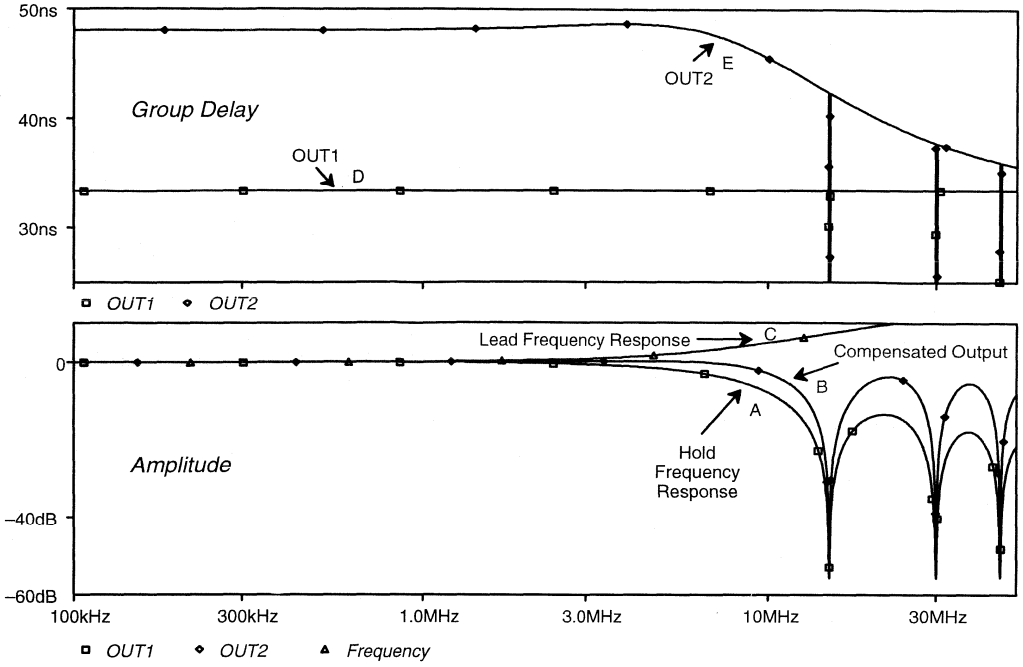

Figure 2. Comparison of Hold Response before and after Compensation

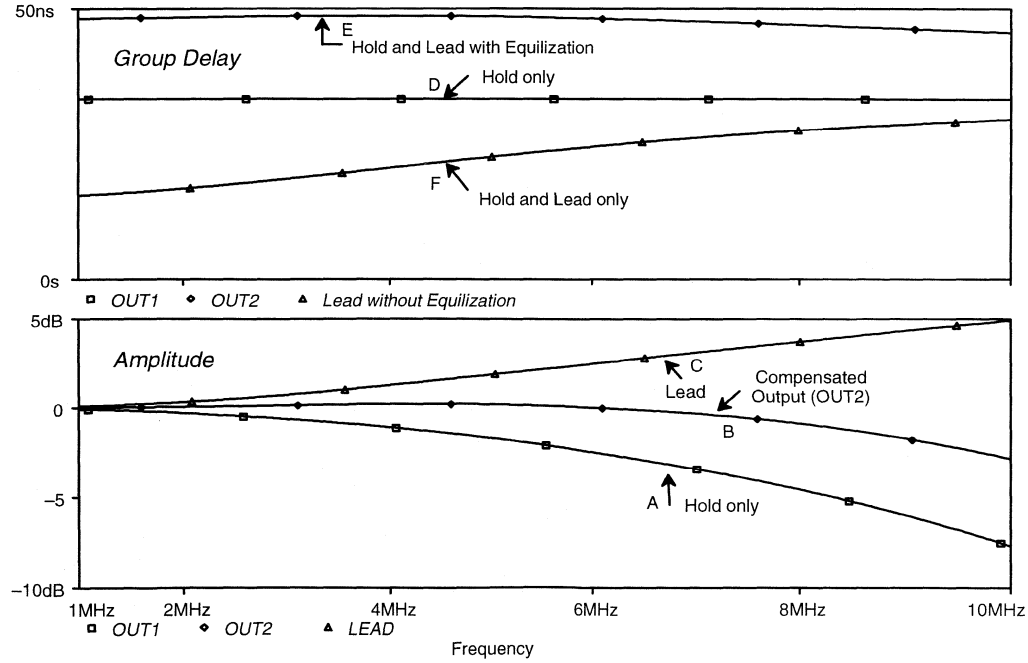

Figure 3. Comparison of Hold Response before and after Compensation

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FREQUENCY RESPONSE EFFECTS OF OVERSAMPLING AND AVERAGING ON A/D OUTPUT DATA

Introduction

EXAR's family of high resolution and high speed analog to digital converters are often used in digital video, digital graphics and other mixed signal sampled data systems where Digital Signal Processing is used to relax analog antialiasing filter requirements. Reducing the effects of aliasing (which is the translation of unwanted out of band noise and signals into the signal band) can require high order lowpass filtering prior to A/D conversion.

The analog filter complexity can be significantly reduced if the data is oversampled, that is, sampled at a higher rate. This raises the Nyquist rate (half sampling frequency) thereby reducing the attenuation required of the analog filter. Typically, doubling the sampling rate cuts the filter order (therefore size) in half. The higher digital output data rate can be reduced by averaging several samples then outputting these computed values at the original lower data rate. This process, called "decimation", provides additional filtering but is also a sampling operation at the decimation frequency. The exact frequency characteristics of the averaging operation (digital filter) is important since it impacts the overall effects of aliasing and modifies the in band response of the system. The transfer function of two commonly occurring cases is presented below.

Example I (*See Figure 1.*)

The input signal for this example is initially sampled at 30 MHz. After conversion, two data words are averaged and the calculated data is output at a rate of 15 MHz. The input pass band is 5 MHz.

An equivalent block diagram of this system is shown in *Figure 1.* The transfer function is also given. Note that in the equivalent circuit, the input signal is delayed by 1/(30 MHz), added to itself, divided by two, then sampled at 15 MHz. The operation and transfer function are typical of finite impulse response discrete filters.

Example II (see Figure 2)

The input signal for this example is initially sampled at 30 MHz. After conversion, four data words are averaged and the calculated data is output at a rate of 7.5 MHz. The input pass band is 2.5 MHz.

A equivalent block diagram of this system is shown in *Figure 2.* The transfer function is also given. Note that in this equivalent circuit, the input signal is delayed down three paths by integer multiples of 1/(30 MHz), these delayed signals are added to the undelayed input, divided by four, then sampled at 7.5 MHz. The operation and transfer function are typical of a higher order (than above) finite impulse response discrete filter.

Results

Frequency response plots for both examples are given in *Graph 1.* Both amplitude responses have zero output at their respective output frequency, which is often called the decimation frequency. Both are periodic about the input sampling frequency. The pass band attenuation for both examples is not insignificant and might require compensation at some point in the signal channel. This can be done as part of other analog or digital signal conditioning functions.

Conclusion

The frequency responses for these discrete filter examples can be considered to be cascaded with the input antialiasing filter. It adds to the low pass attenuation and helps reduce the order of the analog filter. It does not totally eliminate input filtering since it provides little attenuation at half the output sampling frequency. The benefits are realized at the expense of higher conversion speed requirements in the A/D and a small amount of digital signal conditioning.

The transfer function can be generalized for other sampling and decimation frequencies as follows:

$$D_{OUT}(s)/D_{IN}(s)=(1-\exp(-N*s/F_S))/(N(1-\exp(-s/F_S)))$$

where, F_S= sampling frequency (input sampler)

F_d= decimation frequency (output rate)
and, $N= F_S/F_d$

This equation can be used to plot amplitude and phase response for any combination of input and output frequencies. This decimation circuit is common in Delta-Sigma converters.

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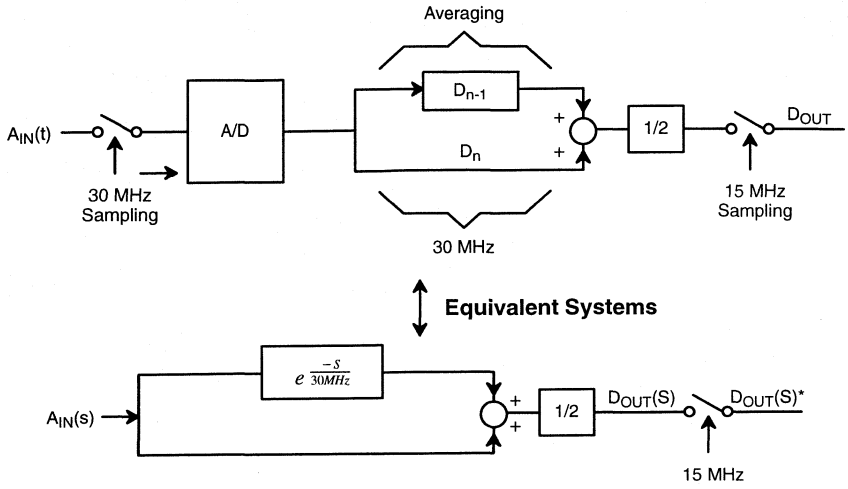
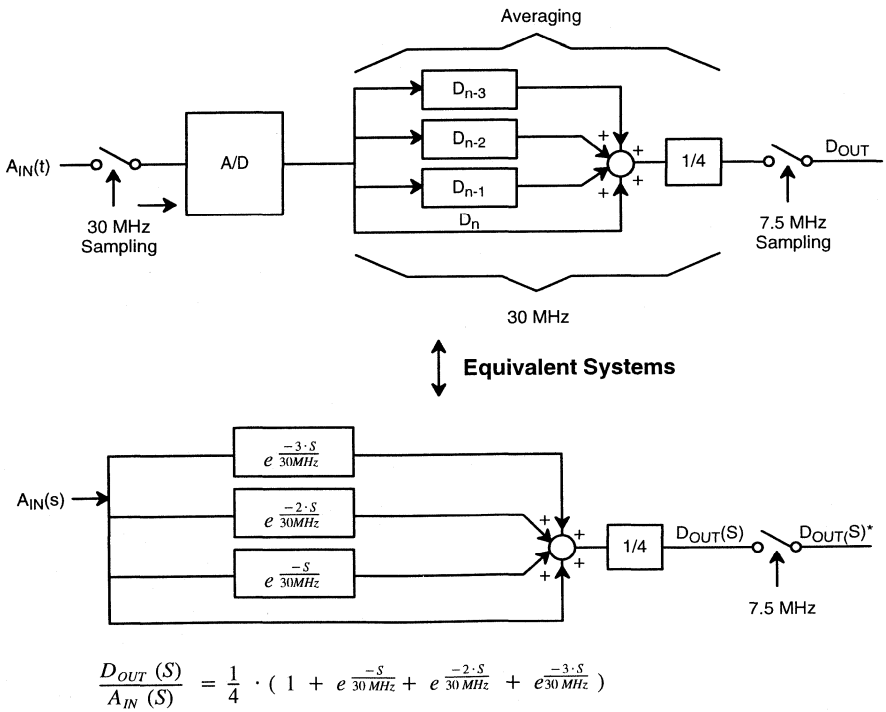


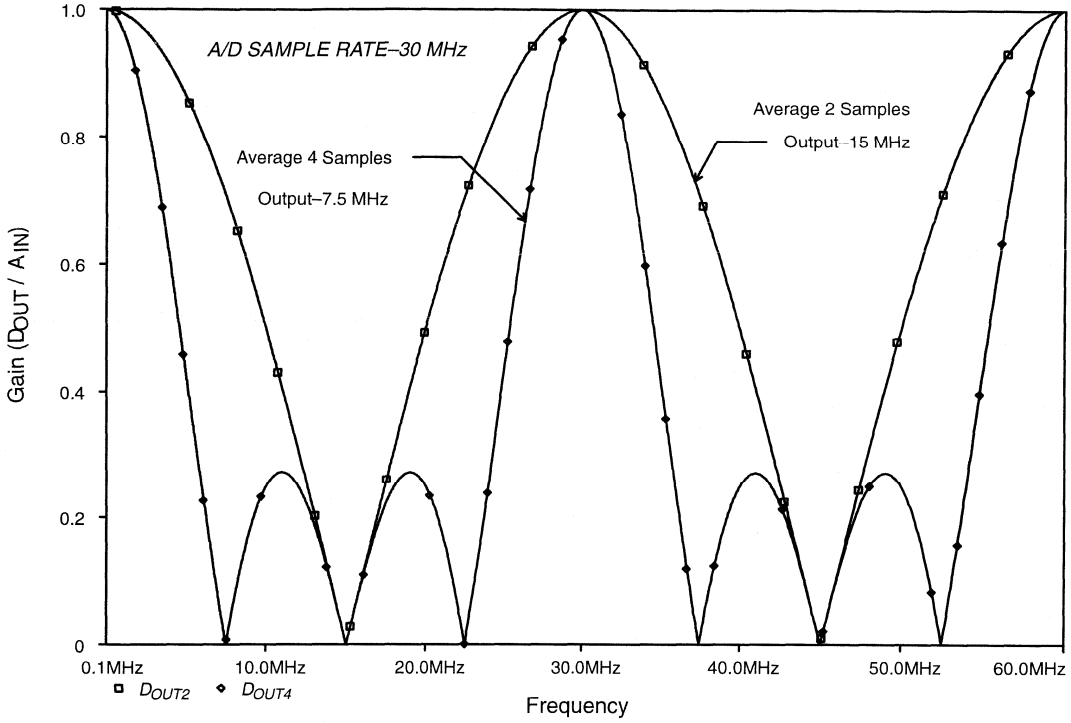
$$\frac{D_{OUT}(S)}{A_{IN}(S)} = \frac{1}{2} \cdot (1 + e^{\frac{-S}{30\,MHz}})$$

Figure 1. Two Samples Averaged



$$\frac{D_{OUT}(S)}{A_{IN}(S)} = \frac{1}{4} \cdot (1 + e^{\frac{-S}{30\,MHz}} + e^{\frac{-2\cdot S}{30\,MHz}} + e^{\frac{-3\cdot S}{30\,MHz}})$$

Figure 2. Four Samples Averaged



Graph 1. Decimation Filter Frequency Response

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CRITERIA FOR ACCURATE SAMPLING OF ANALOG SIGNALS

Introduction

EXAR's family of high resolution, high speed analog-to-digital converters sample the input signals then convert these samples to a digital format for processing. The sampling of analog signals is subject to restrictions and limitations. The choice of sampling frequency and the effect of aperture uncertainty are two important considerations in sampled data systems. These are discussed below.

Choosing a Sampling Frequency

The Nyquist sampling theorem defines the limitation on sampling frequency of an analog signal: In order to sample an analog signal for future reconstruction, the sampling frequency, fs, must be greater than twice the maximum frequency component of the analog signal being sampled.

An anti-aliassing filter must be placed in front of the sampler if the the signal bandwidth is greater than half the sampling rate. The tradeoffs to be considered in selecting the filter and sampling frequency are:

a) A steep cutoff filter permits the use of a lower sampling frequency but requires a high order filter.

b) Gradual filter rolloff (lower order filter) implies a higher sample rate (faster A/D).

c) Phase linearity of the filter must sometimes be considered which increases filter complexity.

Undersampling (sampling at a rate lower than double the maximum frequency) is a technique that can be usefully applied in particular applications. It can for example be employed for down conversion of band limited signals.

Aperture Uncertainty

Consider a continuous analog signal, v(t), having a maximum bandwidth of f_{MAX}. When converting this signal, a periodic sampler, such as a high speed A/D converter can introduce errors due to sampling time uncertainty. The clock signal, which dictates when samples are taken, deviates from a perfectly timed periodic signal by some amount and the actual system sample time is characterized by a mean and standard deviation called aperture delay, t_d, and aperture uncertainty, t_a.

When sampling an analog signal, the maximum allowable signal bandwidth can be related to the aperture uncertainty of the sampler & clock.

Consider a sinusoidal signal of maximum amplitude V:

$$v(t) = V \cdot sin(2\pi ft)$$

its maximum slope, occurs at V(t)=0 and is:

$$\frac{dv}{dt} = 2\pi fV$$

An analog signal which has a upper spectral component of f_{MAX} will thus have a maximum voltage slope:

$$\frac{\Delta v}{\Delta t} = 2\,\pi\, f_{MAX}\, V$$

Sampling this slope with an rms time uncertainty of t_a will generate an rms amplitude uncertainty of:

$$V_{ERR} = 2\pi \cdot V \cdot t_a \cdot f_{MAX}$$

Amplitude quantization by an n-bit A/D converter typically yields a 1/2 LSB to 1LSB integral nonlinearity. If one allows the sampler to add an 1/2LSB rms error due to the sampling inaccuracy:

$$\frac{V_{ERR}}{2V} = \frac{1}{2^{n+1}}$$

then by substitution:

$$f_{MAX} = \frac{1}{\pi \cdot t_a \cdot 2^{n+1}}$$

As an example, an n = 8-bit high speed A/D converter with t_a = 40ps can convert an analog input signal with a highest full-amplitude spectral component of f_{MAX} =15.5 MHz, assuming a 1/2 LSB rms amplitude error is allowable.

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CMOS CURRENT OUTPUT D/A CONVERTER DESIGN CONCEPTS FOR WIDE BANDWIDTH APPLICATIONS

Introduction

EXAR's family of high resolution, high speed current output digital-to-analog converters are often used in applications where speed is critical. Since applying these devices requires interfacing with an op amp, the DACs code dependent output capacitance becomes important. Capacitance from the input of the op amp to ground adversely affects transient and overshoot characteristics. Solutions to this problem are addressed below.

Capacitive loading of the output amplifier can also cause a ringing problem and circuit considerations to minimize these effects are discussed.

The Effect of DAC Output Capacitance

Below (*Figure 1.)* is the classical connection for creating a voltage output from a CMOS current output D/A converter. *Figure 2.* shows the equivalent AC circuit at Full Scale output.

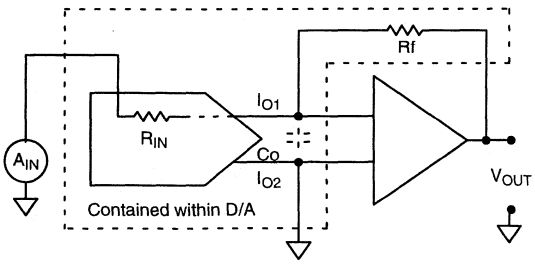

Figure 1. Typical Configuration CMOS I_{OUT} DAC with External Op Amp forming Voltage Output Configuration

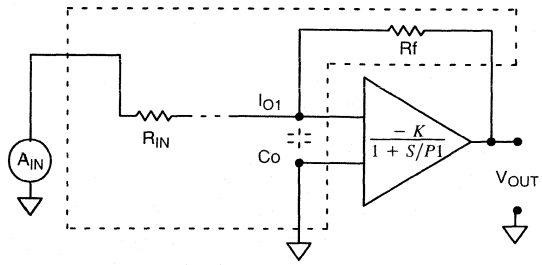

Figure 2. Equivalent Circuit at Full Scale for AC Analysis

By inspecting the linear systems characteristics of this circuit (in the form of the classical Bode plots and root locus plot, *Figures 3, 4 and 5.*), it is evident that this circuit will exhibit an under damped response, which could be unacceptable in some wide bandwidth applications. This non ideal response is due to the Co parasitic of the D/A.

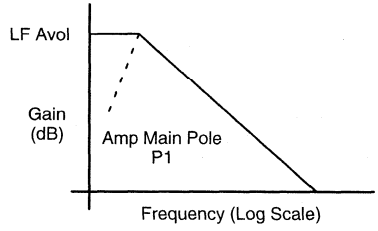

Figure 3. Op Amp Open Loop Characteristics

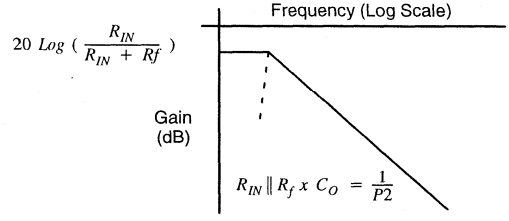

Figure 4. Feedback Signal Path Transfer Characteristics

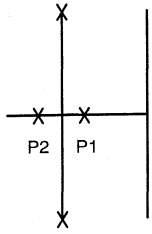

Figure 5. Root Locus

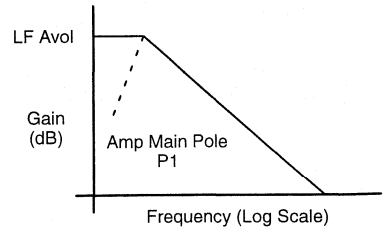

Figure 8. Op Amp Open Loop Characteristics

Most manufacturers propose the solution of inserting a Zero (a capacitor) in the feedback loop to compensate for this Co generated pole *(Figure 6. and Figure 7.)* The resulting linear systems plots (Figures 8, 9, and 10*)* show what is expected.

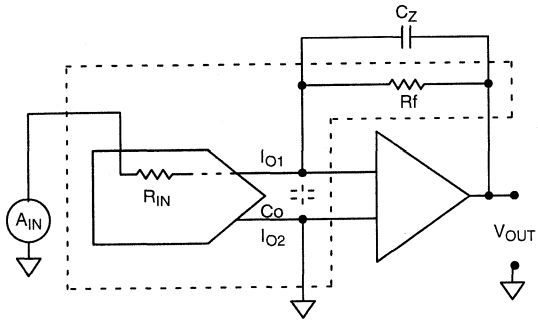

Figure 6. Typical Zero Compensation of Co General Pole

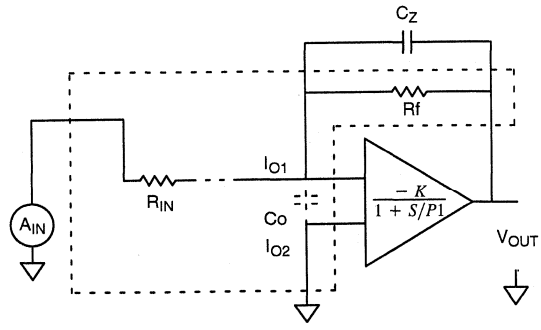

Figure 7. Equivalent Circuit at Full Scale for AC Analysis

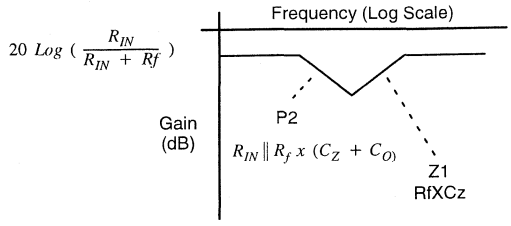

Figure 9. Feedback Signal Path Transfer Characteristics

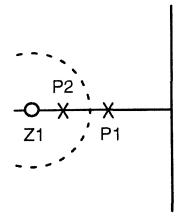

Figure 10. Root Locus

By adding Ra across Co *(Figure 11. and Figure 12.)*, 4 improvements are obtained :

1) The loop gain of the circuit is lowered, making the response more damped *(Figures 13, 14, and 15).*
2) The Co X R is decreased, separating the Amp pole from the parasitic Co pole.
3) The Resistance at the Co node is made more constant versus DAC code, minimizing variations due to code changes. (The Co still will change versus code, so this circuit is still not perfect.)
4) Cz can be made smaller, which increases the DAC frequency response.

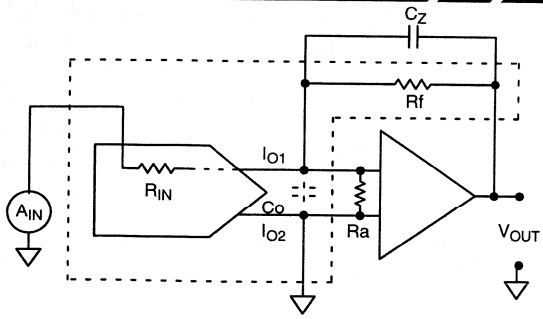

Figure 11. Typical Zero Compensation of Co General Pole

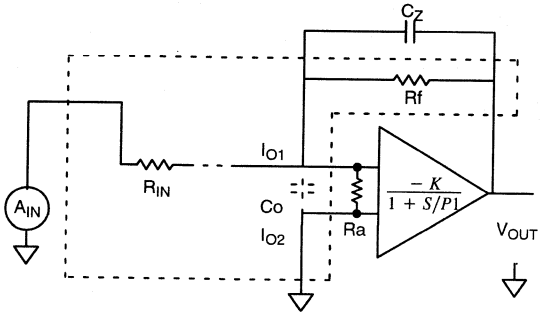

Figure 12. Equivalent Circuit at Full Scale for AC Analysis

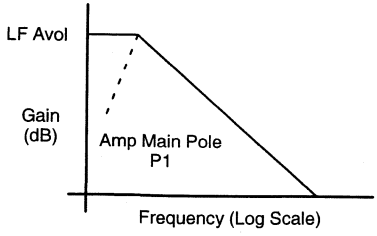

Figure 13. Op Amp Open Loop Characteristics

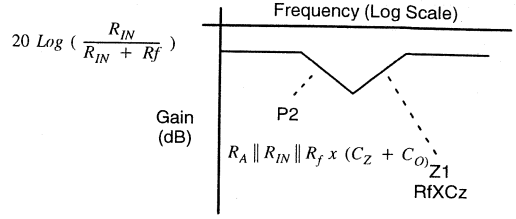

Figure 14. Feedback Signal Path Transfer Characteristics

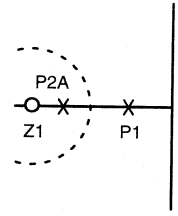

Figure 15. Root Locus

The best way to characterize the various alternatives is to do both a step or impulse response and a frequency / phase plot for the A_{IN} to V_{OUT} transfer function.

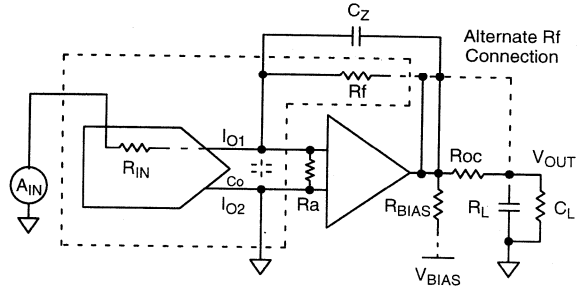

Figure 16. Typical Zero Compensation of Co General Pole

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Output Loading Effects

Finally, the last area to be addressed is the characteristic of the op amp output stage itself *(Figure 16.)*

Where high frequency impulse current loads are experienced, like at the input of most modern high speed A/D converters, the output stage itself will overshoot. Even if this seems to be at very high frequencies and very short duration, this overshoot will degrade the A/D linearity in most cases. The overshoot is due to the Inductive tendency of the output emitter followers at very high frequencies.

Most manufacturers recommend 25 to 50Ω in series with their op amp output when driving capacitive loads to alleviate this problem. The only drawback of this configuration is the DC error generated by the insertion of Roc. The addition of R_{BIAS} – from the amp output to a minus supply in some cases provides enough additional current in the output NPN to give adequate response without this series Roc.

Finally, the alternate connection shown for Rf may in some cases give satisfactory AC results while compensating the loop for the DC error generated by the Roc – R_L voltage divider. This connection is possible only because Cz provides feedback for high frequencies. The best configuration is determined by experimentation and depends upon the op amp being used.

One last trick for applications which can tolerate a shifted Ground: By connecting the Op Amp and I_{O2} to a voltage of 0.3 to 0.6 volts above the CMOS D/A ground, The Co will be reduced by over 30 % due to the "Body Back Bias" effect on the D/A switches.

A Practical Example

Now, specifically for the MP7529A or B versus the PM7628: The MP7529A or B Co is 120 pF. The PM7628 Co is 60 pF. By adding the Ra = 2kΩ, to the application, the MP7529A or B will actually settle faster since the data path to the analog current steering switches is about 30 to 60 nS faster than the PM7628. Without the Ra, the MP7529A or B will have overshoot when in a circuit "tuned for the PM7628".

ADDING EXTERNAL INPUT RESISTANCE TO THE MP3274/3276 PROVIDES FLEXIBLE FAULT CONTROL, GAIN CONTROL AND ANTIALIASING

Voltage Fault Protection Beyond ±150 Volts For Transient Conditions

The input pins of the MP3274/MP3276 are fault protected to ±50 volts. Higher voltage fault protection can be achieved by adding external resisters in series with each input. The gain of each channel will be reduced by this addition (the input range is increased) and can be restored to the original by adding a resister from the reference output terminal to the reference input terminal, since lowering the reference voltage to the ladder network raises the gain of the A/D. A formula describing the input range as a function of these added resisters *(Figure 1.)* can be written as follows:

$$V_{INPUTRANGE} = \pm 2 \cdot \frac{R_{IN}}{R_{FN}} \cdot \left(\frac{1 + \frac{R_{XN}}{R_{IN}}}{1 + \frac{R_{REFX}}{R_{LAD}}} \right)$$

Eqn 1.

By choosing the external resisters so that:

$$\frac{R_{XN}}{R_{IN}} = \frac{R_{REFX}}{R_{LAD}}$$

Eqn 2.

The input range is maintained at ±10 volts, the standard input range for these parts, while increasing the voltage fault protection.

The reference voltage reduction should be kept to less than 10% so that other specifications are not adversely affected. *Figure 1.* shows the recommended configuration for increasing the fault protection to ±150 V. Note that the common mode input requires a matching external series resister to maintain high common mode rejection.

The tolerance of the 13KΩ external resisters, R_{XN}, needs only be 1% to maintain 0.1% gain accuracy (R_{IN} = 130KΩ) and 60 dB common mode rejection ratio. Mismatches between internal and external absolute values completely cancel out so long as the external resisters track each other.

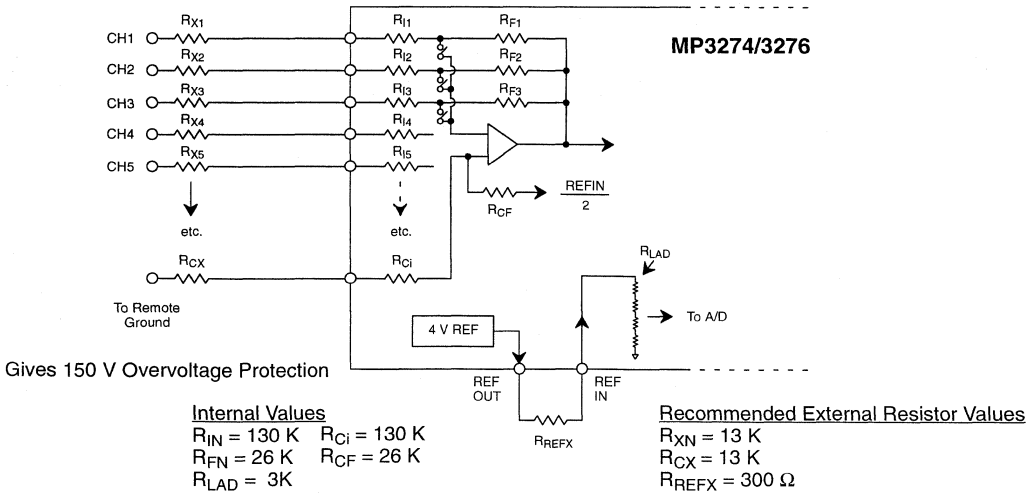

Figure 1. Increase Fault Protection to ±150 V with External Resistors

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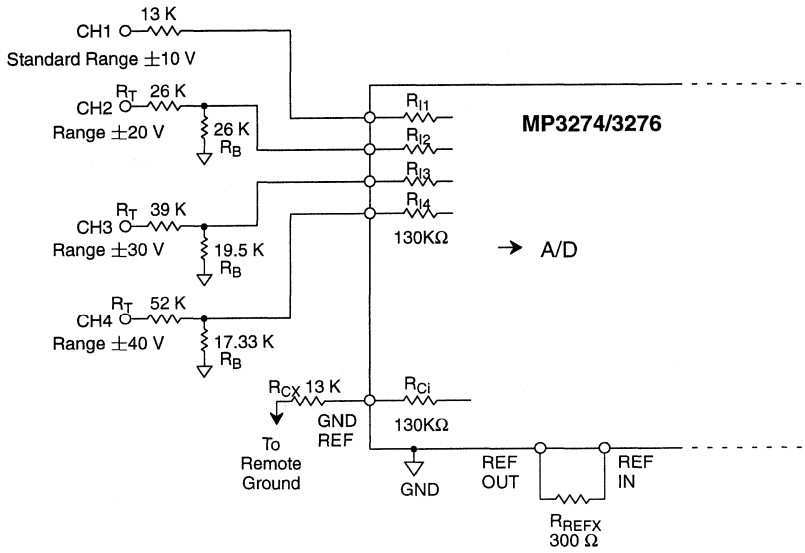
Gain Control

The design formula above (*Eqn 1.*) can be applied to more universal requirements where gain calibration as well as fault protection is an issue. Varying R_{REFX} about its nominal value will raise or lower the gain simultaneously for all channels. Individual channel gain adjustment is done with the input series resisters, R_{IN}. CMRR can be adversely affected if the mismatch between the input resistance and the common mode resister, R_{CI}, is large.

Using this method to calibrate the gain will introduce a small scale factor error due to the absolute tolerance of the internal resistors. If the gain is adjusted by 10% using R_{XN} = 13K, the deviation from the calculated input range can be as much as 3% for IC resister absolute tolerances of 30%. Temperature and time stability after calibration will be satisfactory if medium quality thin film external resisters are used.

Because a maximum deviation around 4 volts of 10% is all that is allowed at the reference input, the input range cannot be lowered below ±9 volts. It can be raised to any desired range above 10 volts by using resister dividers as inputs to each channel and using the equivalent output resistance of the divider as the channel input resistance term in the above formula and meeting the constraint of *Eqn 2. Figure 2.* shows an example of this for several input ranges. No gain or CMRR error is introduced by absolute tolerance mismatches in these configurations.

The internal reference supply can be replaced by a software controlled digital-to-analog converter as shown in *Figure 3.* Control of gain error on a per channel basis is achieved. No resister induced range errors are introduced since the condition of *Eqn 2.* can be met.



General Case

$$\text{Let } N = \frac{\text{(Peak to Peak) Input Voltage Range}}{20} \quad \text{where } N > 1$$

then

$$RT = N \cdot 13K$$

$$RB = \frac{N}{N-1} \cdot 13K$$

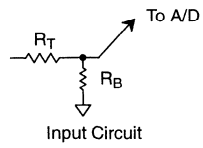


Figure 2. Using Input Resistor Dividers to Set Input Range and Increase Input Fault Protection

Increased Fault Protection

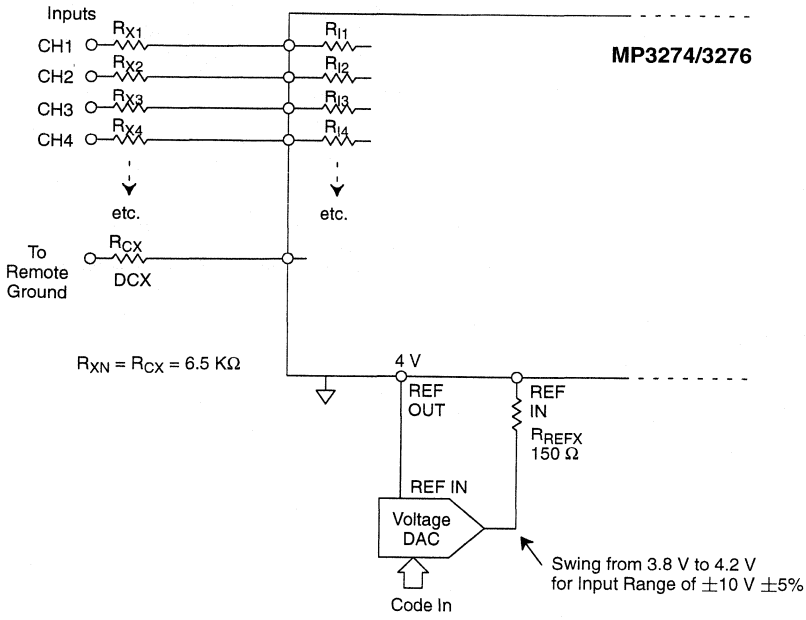


Figure 3. Software Gain Control – Individual Gain Control

Antialiasing Filter

A single pole, passive, antialias filter can be implemented if an input resister is added as described above. The common mode rejection for remote grounding can also be preserved by balancing the time constants on the channel inputs and common mode input as shown in *Figure 4.*

The resisters are chosen as described above then a capacitor is selected using the formulas given below for the 3 dB down point and CAPSIZE. Each channel is required to have the same frequency response if common mode matching is needed for every channel otherwise each channel can be set to a different frequency. The 3 dB down frequency is selected by considering the sampling rate, the attenuation required at half sampling frequency, and applying the following formula:

$$f_{3dB} = \frac{1/2\ fs}{10^{(att/20)}}$$

Eqn 3.

where,
fs = sampling frequency
att = desired attenuation in dB

$$CAPSIZE = \frac{1}{(2\ \pi\ f_{3dB} \cdot Req)}$$

Eqn 4.

Obviously a single pole filter does not permit input bandwidths approaching half sampling frequency but in many situations wide bandwidth is unnecessary and the simplicity of a one pole passive filter is attractive.

Higher order filtering is possible using the active circuit shown in *Figure 5.* A single inexpensive opamp per channel is needed and a second order Butterworth can be implemented. The circuit shown introduces no offset voltage since it is AC coupled. The 3 dB down formula for this circuit is:

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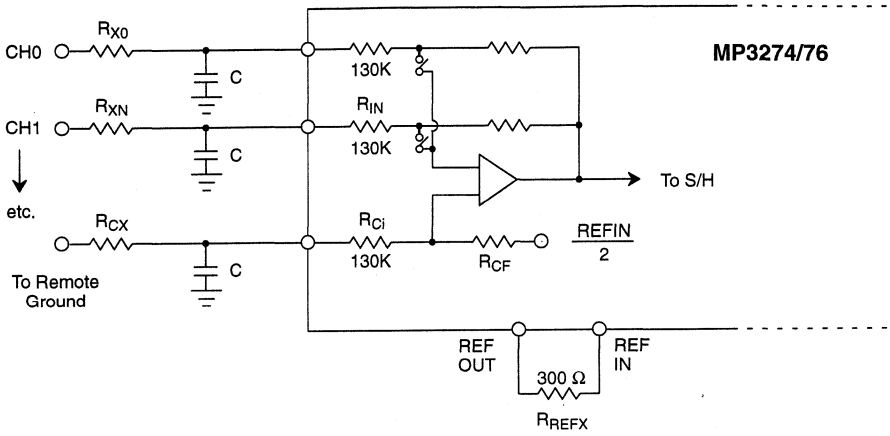
$$f_{3dB} = \frac{1/2\ fs}{10^{(att/40)}}$$

Eqn 5.

where,
fs = sampling frequency
att = desired attenuation in dB

The formulas given in *Figure 5.* can be used to select component values based on f3db. The allowable input bandwidth is improved over the single pole filter by the factor $10^{(att/40)}$, which is normally an order of magnitude or better. Identical circuitry on the common mode input preserves the CMRR for those channels that are matched.



$$Req = R_{XN} \,//\, 130K$$

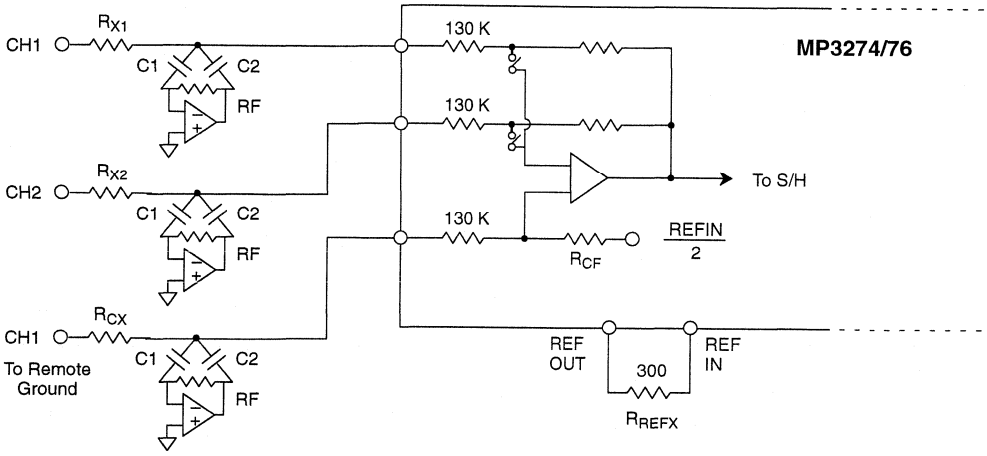
$$R_{XN} = R_{REFX} \cdot \frac{130K}{3K} = R_{REFX} \cdot \frac{R_{IN}}{R_{AD}}$$

$$CAPSIZE = \frac{1}{2\ \pi\ f_{3db} \cdot Req}$$

$$R_{LAD} = 3\ K\Omega$$

$$R_{IN} = 130\ K\Omega$$

Figure 4. Passive First Order Antialiasing Filter



Butterworth Design Equations

$$R_{XN} = R_{CX} = R_{REFX} \cdot \frac{130K}{3K} \qquad C = \frac{\sqrt{2}}{2\pi / f_{3db}\ RF}$$

$$Req = R_{XN} \,//\, 130K$$

$$C_1 = C_2 = C$$

Figure 5. Second Order, One Amplifier, No Offset Antialiasing Filter

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MP8784AB APPLICATION BOARD DOCUMENTATION

Evaluation Kit Parts List

This kit contains the following:

- One MP8784AB Applications Board with sample MP8784
- MP8784AB Documentation
- Circuit Diagram
- Layout Diagrams

Features include:

- Easy Evaluation of MP8784
- Optimized Printed Circuit Board Design
- Optimized Support Circuits
- User Friendly Interface
- Layout Applicable to Final Design

Introduction

The MP8784AB is a complete printed circuit test board designed to permit quick and accurate evaluation of EXAR's MP8784, 10-bit 5 MSPS analog-to-digital converter. This applications board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested (MP8784), operational amplifiers for input buffers, control logic and latches, and numerous connectors and jumper options.

With external laboratory equipment, complete DC and AC performance of the part can be evaluated.

Flexible user interface is provided by selectable jumper options and convenient connectors. Observation test points are available at commonly used locations.

A Preview of a Common Test Configuration

The board is set up as a general A/D test circuit where the references are fixed. *Figure 2.* shows the overall circuit, *Figure 5.* shows the PC board layout and jumper locations, also listed in Table 1. There are many other circuit possibilities built into the universal test board; however, starting with the default circuit is recommended.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.

System Configuration

Two complete evaluation circuit block diagrams showing the MP8784AB with typical external test equipment are shown in *Figure 2. and Figure 3.* The following is a more detailed description of the major on-board and external components used in these systems as seen in *Figure 2., Figure 3., and Figure 6.*

Application Board Circuitry

The application board support circuitry is shown in *Figure 6.* The major components supporting the A/D under test are:

1. V_{REF} BUFFER – A dual op amp (EL2224C) can be used to isolate the externally supplied $V_{REF(+)}$ and $V_{REF(-)}$ from the device under test and provides a low source impedance. These buffers can be bypassed with onboard jumpers (J6 and J13). If voltage feedback op amps are used, holes for optional compensation caps are provided.
2. ANALOG INPUT AMPLIFIER – An operational amplifier (AD847) is used in an instrumentation amp configuration (gain –5) to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input. Holes for optional compensation caps are provided on-board.
3. DATA LATCHES – The digital output of the A/D drive on-board latches which buffer the device under test from the external test equipment.
4. CONTROL LOGIC – Allows control of the data latch clocks as well as the $\overline{OE}$ pin of the DUT.

External Equipment Required

The system block diagrams (*Figure 2. and Figure 3.*) show the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES – ±15 volt and one (or two) +5 volt external power supplies are needed. Decoupling circuits are provided on the applications board, however, low noise, low output impedance supplies are necessary for best performance. A connector (CON3) is used for all power and ground connections. This connector is the 10 pin connector located next to the $V_{REF(-)}$ input. For best results, twist the power supply cable pairs. This minimizes coupling to and from these to unrelated sections of the setup.
2. CLOCK GENERATOR – A 1 KHz to 5 MHz symmetrical clock signal must be applied to the SMB coax connector labeled CLOCK. Note the 50Ω input impedance.
3. INPUT SIGNAL GENERATOR – A clean, low distortion sine wave generator is used as a signal source. A band pass filter is sometimes required to further reduce harmonics and bandlimit noise as shown. The SMB coax connector labeled V_{IN} accepts the analog input. An on board op amp (AD847) is used to amplify this input (gain of –5) and provide low source impedance to drive the A/D under test. The socket has a standard 741 type pinout which allows experimentation with alternative amplifiers.
4. DITHER INPUT – The cross plot test configuration (later described) requires a triangle wave signal source. This signal is added to a DC input signal through the SMB connector labeled DITHER (an inverting input with gain of 1/50). J7 connects this point to ground via a 50Ω resistor.
5. V_{IN} COMMON – An alternate, non inverting input (gain of five when dither is disconnected). Connect to ground when not used. J11 connects V_{IN} COMMON to ground via a 50 Ω resistor. This input allows use of differential inputs or used for applying a DC offset for level shifting the V_{IN}.
6. OSCILLOSCOPE – The output of a dither DAC, TP3, is used to drive the vertical input of the oscilloscope for manual linearity testing using the "cross plot" method described on the following page.
7. DSP – Evaluation of dynamic and static performance is done by external processing devices that perform histogram and harmonic analysis to determine characteristics like linearity, noise, distortion, intermodulation effects, etc. The data is available at the CON1 connector, which is the inside column of jumper connectors labelled D0 through D9.

Optional Equipment

1. REFERENCE SUPPLIES – Internal reference voltages can be used by shorting J11B and J12B. This generates voltages of nominally V_{RT} = 4 V and V_{RB} = 1 V. Alternatively, external references may be applied through the SMB coax connectors labeled $V_{REF(+)}$ and $V_{REF(-)}$ (typically +5 and 0 volts respectively). The external reference voltages can be configured to go through op amp buffers or go directly to the A/D by using jumpers J6 and J13. Note that $V_{REF(+)}$ must be more positive than $V_{REF(-)}$, since V_{RT} must be >V_{RB} on chip.
2. PRECISION EXTERNAL OUTPUT DAC – As an alternative to DSP, a high speed precision digital to analog converter can reconstruct the output in analog form. The analog measurements can be used to evaluate the A/D's performance using conventional analog instrumentation. Use the DACEN output at CON1 to load the reconstruction DAC.
3. REFERENCE CONTROL DACS – The reference voltage at the top (V_{RT}) and bottom (V_{RB}) of the A/D can be changed by external DACs on alternate CLOCK cycles to change offset and scale factor. Data can be loaded into the DACs by using the logic signal DACEN on the output connector. The two DACs must have resolution and settling time characteristics consistent with the application. Note that C14, C13, C21, and C22 are decoupling capacitors at the reference pins. These have to be removed when V_{RT} and V_{RB} are driven dynamically.

SYSTEM OPERATION

Reference Inputs

With the reference op amps in circuit, the ADC's reference pins (V_{RB} and V_{RT}) are driven in an offset and range mode:

$V_{RB} = V_{REF(-)}$
$V_{RT} = V_{REF(-)} + V_{REF(+)}$

Hence $V_{REF(-)}$ defines the offset and $V_{REF(+)}$ defines the span.

Analog Inputs

V_{IN} and V_{IN} COMMON Input Only

Differential input can be achieved by using V_{IN} and (V_{IN} COMMON). If the dither input is left floating, then the differential input to the ADC is given by:

ADCIN – $V_{REF(-)}$ = 5 (V_{IN} COMMON) – 5 V_{IN}
where ADCIN = V_{IN} (MP8784 pin 19)

under the assumption of ideal components. This allows reduction of common mode signals between V_{IN} and (V_{IN} COMMON).

Dither and V_{IN} COMMON Input Only

With V_{IN} floating and a signal applied to dither:

ADCIN = 0.875 • V_{IN} COMMON – 0.05 • dither +
0.175 • $V_{REF(-)}$
where ADCIN = V_{IN} (MP8784 pin 19).

Outputs

The parallel digital output of the A/D can be accessed on connector "CON1". A system clock (PTSCLK) and an external DAC enable (DACEN) are also available on that connector. This output data, in conjunction with various input stimuli, is used to evaluate the A/D and timing performance. The three common methods are described below.

Digital Signal Processing

A comprehensive dynamic performance evaluation is most often done by using external hardware capable of fast data acquisition and storage. The computation of integral linearity, differential linearity, signal to noise and distortion ratios, the effective number of bits, and other useful figures of merit is done using software having histogram and FFT capability. The accuracy of the test results depends upon the quality of the input sine wave. A low distortion sine wave generator with a band pass filter will be necessary.

Commercial software packages with the needed computational features are available. The Tektronix PTS101 is used by EXAR to acquire and analyze the ADC data.

Analog Testing with External DAC

The logic output of the system can be converted back to analog by using a high performance digital to analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D's dynamically. In addition to a high quality sine wave input, the output D/A converter must be significantly more accurate than the A/D under test. The filtering effects of adding a zero order "hold" in the signal path are described in EXAR Application Note MPSAN27 which can be found in the 1995 data book.

Cross Plot

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave generator and a low noise DC signal source. Input jacks are provided on the board so this "cross plot" method can be conveniently implemented (See *Figure 3.*). The oscilloscope must be set in the X-Y display mode.

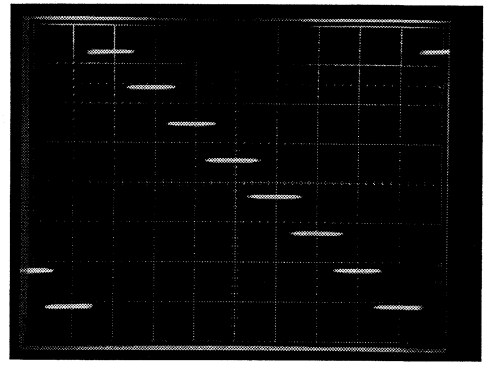

Figure 1. Cross Plot

A triangle wave (100 Hz) with a peak-to-peak amplitude of approximately 160 LSBs peak is supplied to the "dither" input. This is attenuated to 8 LSB's by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that ±4 divisions are swept. Look at Test Point 3 (TP3) with the vertical input. Set the horizontal gain for 1 LSB per division.

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A stair step waveform will result (See *Figure 1.*). By changing the DC input, eight code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the endpoint thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are off-centered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

Since the conversion speed is much faster than the dither frequency, multiple readings are taken at each threshold. The horizontal variation of each threshold gives a qualitative measure of noise (in LSB's).

Using this "cross plot" method is a good way to prove out the lab setup prior to more sophisticated DSP test.

Jumper Options

The MP8784AB offers flexibility through configuration determining jumpers. These optional jumpers furnish choices for (1) input termination resistors, (2) bypassing of the reference input buffers, and (3) the selection of several logic and clock options. *Table I., Figure 4., and Figure 5.* show the jumper functions along with the default configuration set up prior to shipment.

Termination Options

Termination resistors (50 Ω) can be added to the five analog input coax SMB connectors as indicated in *Table I.* (J11, J4, J7, J9, and J12). Note that the CLOCK input is not optional. A permanent 50 Ω termination is connected from its input to digital ground (DGND). The default configuration for the other five coax inputs is — no termination resistors are connected.

Bypass Options

The reference input buffers can be bypassed with J6 and J13 or the V_{RB} pin of the A/D grounded if J8 is inserted. Remove U4, the dual op amp (EL2224C) when using these unbuffered modes. The default mode is — buffers are out. J11B and J12B allow use of the internal references.

Logic Options

The logic options are selected using the five jumpers as listed in *Table I.* and shown in detail in *Figure 6.* Note that three of these jumpers have multiple combinations. Note also that the clock connected to the A/D being tested is always the same as the external clock after a two inverter delay. A simplified logic diagram is given in *Figure 4.* The logic control jumpers are primarily set for two basic test configurations. The standard evaluation mode is shown in *Figure 4.*

Final Design Considerations

After the MP8784AB has been used to demonstrate that the MP8784, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices. Where this is not possible, the following advice should be heeded:

1. Be generous with analog and digital ground planes. Repeat as closely as possible the ground plane system on the application board.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the MP8784AB.
3. Coupling between logic signals and analog circuitry can easily change a 10-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations for example.
4. Hi Z the output latches and the A/D outputs during the V_{IN} sample time.
5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front. Use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application.
7. For sampling of high frequency signals, a sample and hold amplifier like the AD783 is recommended.
8. Decoupling capacitors on pins R1, R2 and R3 do not improve the ADC's performance.

Additional Documentation

A set of drawings showing the details of the electrical circuit and board layout are given in *Figure 7., Figure 10., Figure 8. and Figure 9. Figure 6.* is the complete electrical circuit. *Figure 5.* shows the jumper locations.

Technical Hotline

For any application hints, please call our hotline at (408) 562-3615.

Table I. Jumper Options

Termination of Input Coax Cables		
Jumper	**Description**	**Default**
J11	Connecting adds 50 Ω from V_{IN} COM to AGND	
J4	Connecting adds 50 Ω from V_{IN} to AGND	✔
J7	Connecting adds 50 Ω from DITHER to AGND	
J9	Connecting adds 50 Ω from $V_{REF(+)}$ to AGND	
J12	Connecting adds 50 Ω from $V_{REF(-)}$ to AGND	
Reference Amplifer/Buffer Bypass (See note 4)		
J6	Connecting shorts coax $V_{REF(+)}$ Jack to $V_{REF}T$ of ADC	✔
J13	Connecting shorts coax $V_{REF(-)}$ Jack to $V_{REF}B$ of ADC	
J8	Connecting shorts $V_{REF}B$ (on ADC) to AGND	✔
J11B	Connecting connects internal ADC V_{RTS} reference	
J12B	Connecting connects internal ADC V_{RBS} reference	
Logic and Clock Jumpers (See note 3)		
J2 (2, 3)	Connecting makes the latch clock the same or inverted as the ADC clock. Dependent on J12A.	
J2 (2, 1)	Connecting delays latch clock by 2 prop delays	✔
J3	Divides latch clock by 2 for dynamic V_{REF} testing	
J5	Usually connected – except for dynamic V_{REF} control	✔
J12A (2, 1)	Latch clock is inverted ADC clock	
J12A (2, 3)	Latch clock is same as ADC clock	✔
J12A (2, 4)	Used for dynamic V_{REF} control	
J13A (2, 1)	Connects clock to $\overline{OE}$ through 4.7kΩ (delays $\overline{OE}$)	✔
J13A (2, 4)	Connects Latch CLK to $\overline{OE}$	
J13A (2, 3)	Leaves $\overline{OE}$ open – thus pulled down internally	

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Notes:
1. J*x* (a, b) means short pin a and pin b of jumper *x*.
2. The ADC clock is not affected by the jumper combinations and is the same as the external clock – except for 2 inverter delay.
3. Connect either J3 or J5 but not both simultaneously.
4. When using the amplifier bypass jumpers or the internal reference select jumpers, remove the op amps from the sockets.

Table II. Test Points

TP1	CLK into MP8784
TP2	V_{REFT} via 100Ω resistor
TP3	Crossplot output
TP6	D0 output of MP8784 i.e. LSB
TP7	$\overline{OE}$ of MP8784
TP9	V_{REFB} via 100Ω resistor

Table III. List of Components

Qty	Value	Ref Designators
1	74HC02	U2
1	74HC04	U1
3	74HC174	U3,U5,U6
1	MP8784	U7
1	AD847	U8
1	EL22224C or equiv.	U4 (optional)
7	10µF	C13, C20, C21, C27, C4, C8, C9
13	0.1µF	C11, C14, C19, C2, C22, C23, C24, C25, C3, C5, C6, C7
6	1.5KΩ	R1, R10, R19, R2, R22, R8
1	20KΩ	R11
1	10KΩ	R12
1	5.1KΩ	R13
4	10Ω	R14, R18, R25, R3
1	150KΩ	R15
7	49.9Ω	R17, R20, R26, R29, R31, R4, R6
3	39Ω	R21, R28, R7
1	4.7KΩ	R24
2	1KΩ	R27, R9
2	100Ω	R30, R5
2	7.5KΩ	R16, R23
6	SMB CONNECTOR	V_{IN}, V_{IN} COM, CLOCK, DITHER, $V_{REF(+)}$, $V_{REF(-)}$
6	TESTPOINT	TP1, TP2, TP3, TP6, TP7, TP9
3	50 Ω Cables	BNC Male to SMB Jack. Can be purchased from Pasternack, Irvine, CA.
9	Jumpers	J4, J6, J5, J8, J2, J12A, J13A, J12B, J11B
2	8 Pin DIP Socket	SU4, SU8
24	IC Socket Pins	
1	10 Pin Header Connector	CON3
1	30 Pin Header Connector	CON1, CON2
1	PCB–Rev 1	MP8784AB PC Board

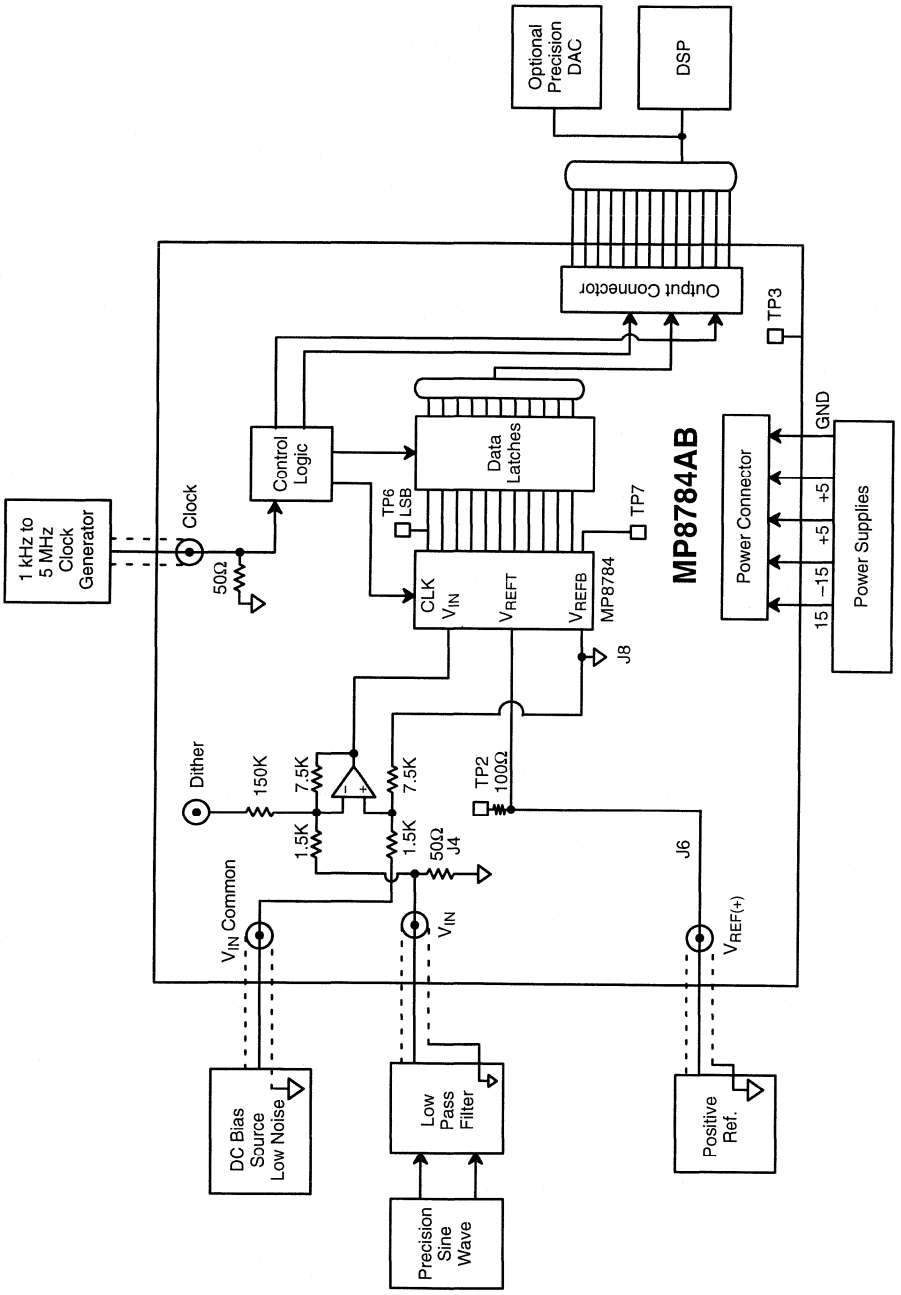

Figure 2. General A/D Test Circuit with Fixed Reference

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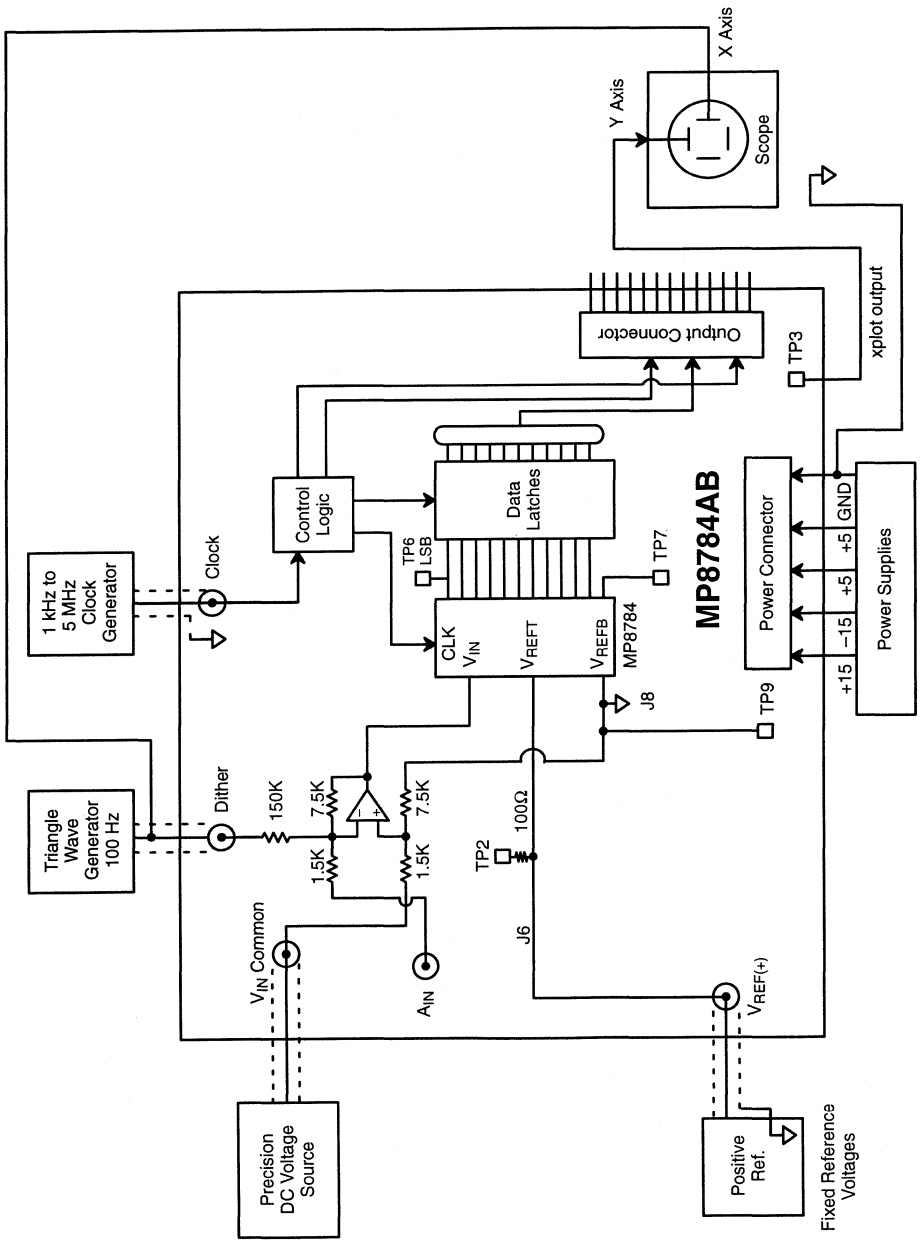


Figure 3. "Cross Plot" Set-Up

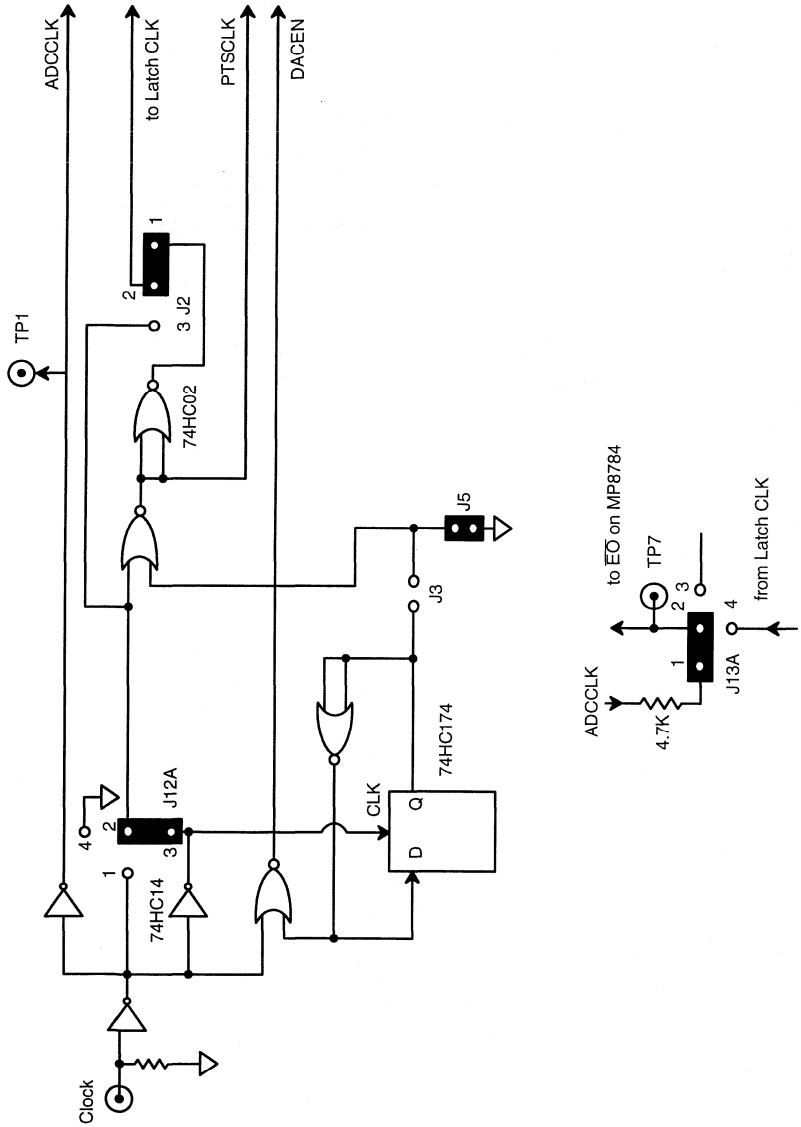
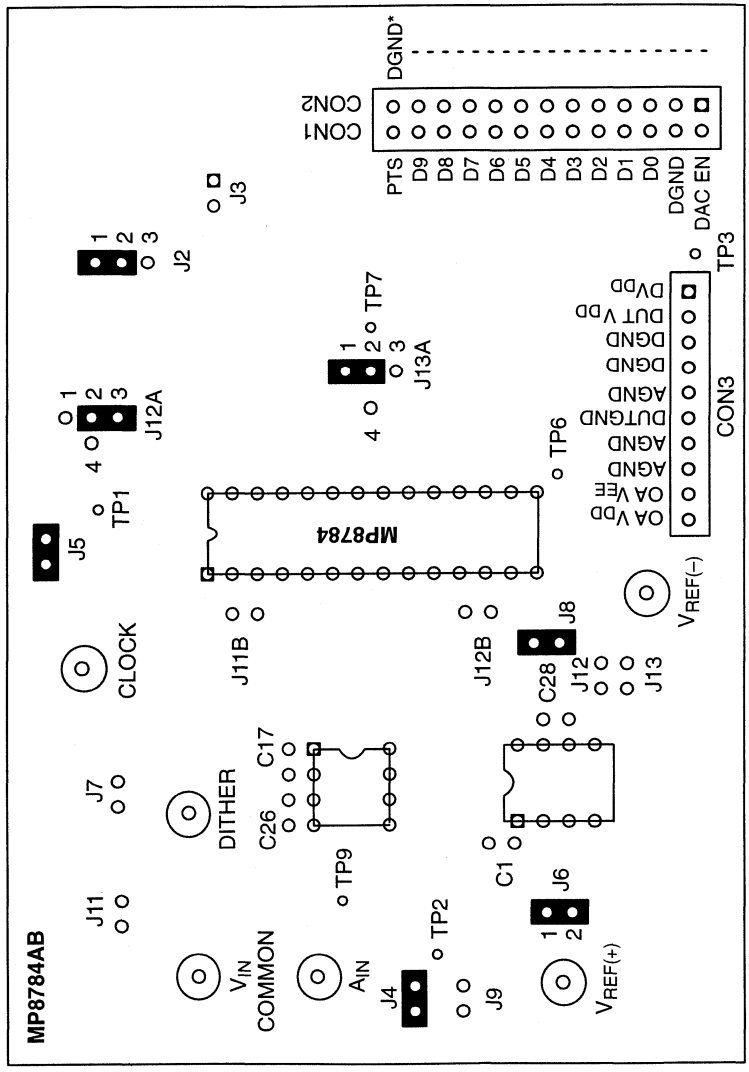


Figure 4. Default Jumper Configuration



*Note: All pins of CON2 are DGND.

Figure 5. MP8784AB Default Jumper Settings

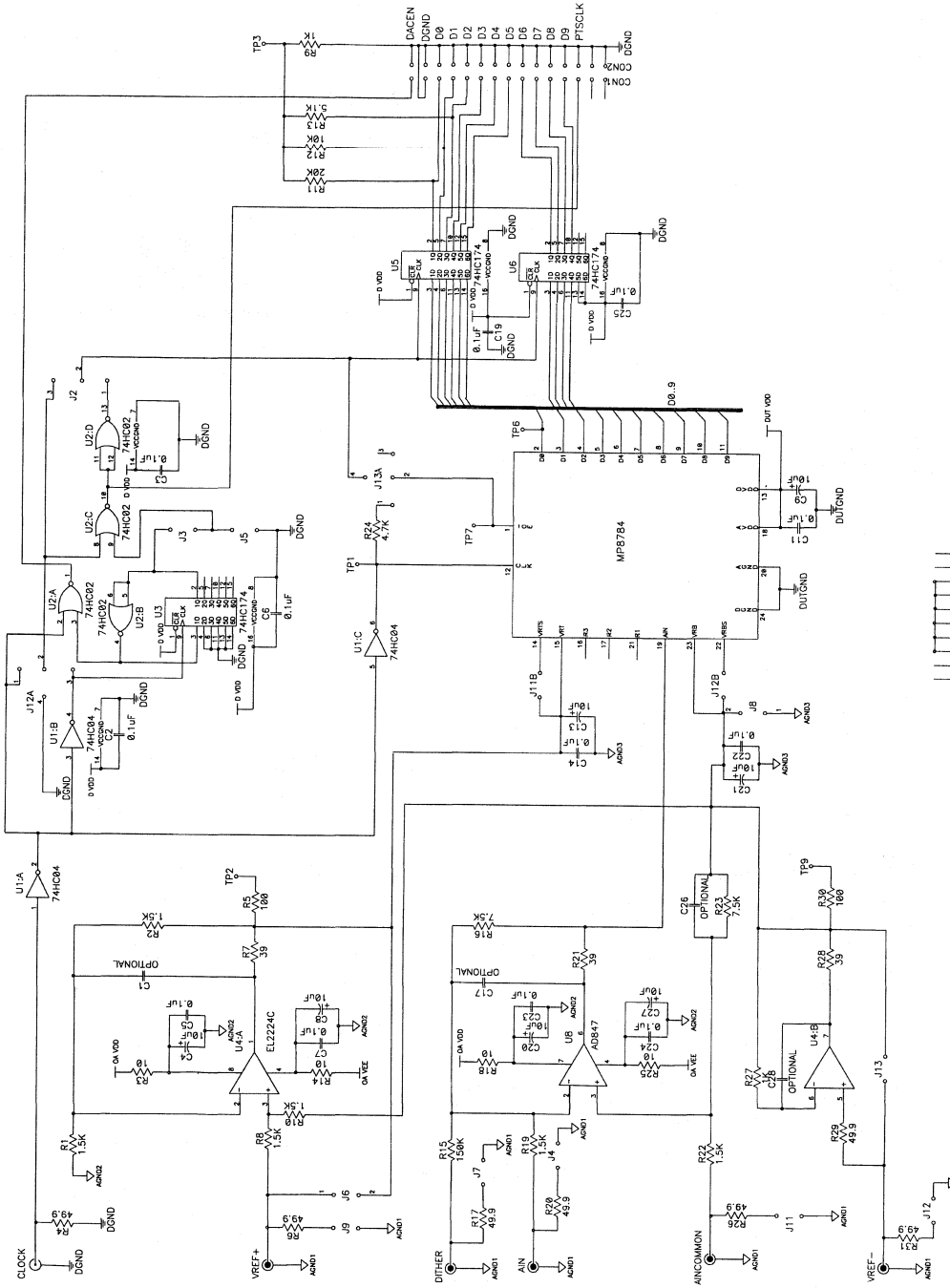


Figure 6. MP8791AB Schematic

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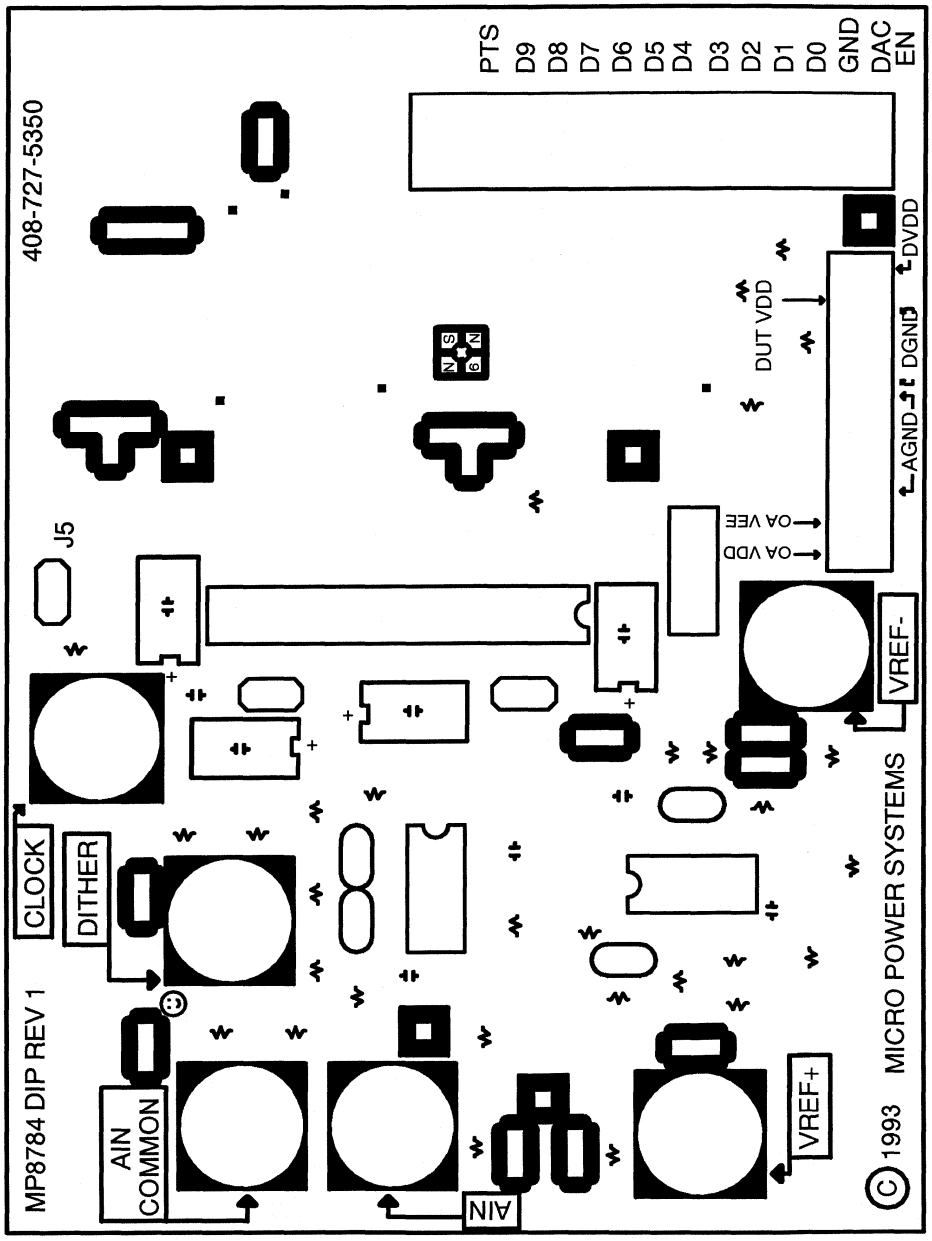
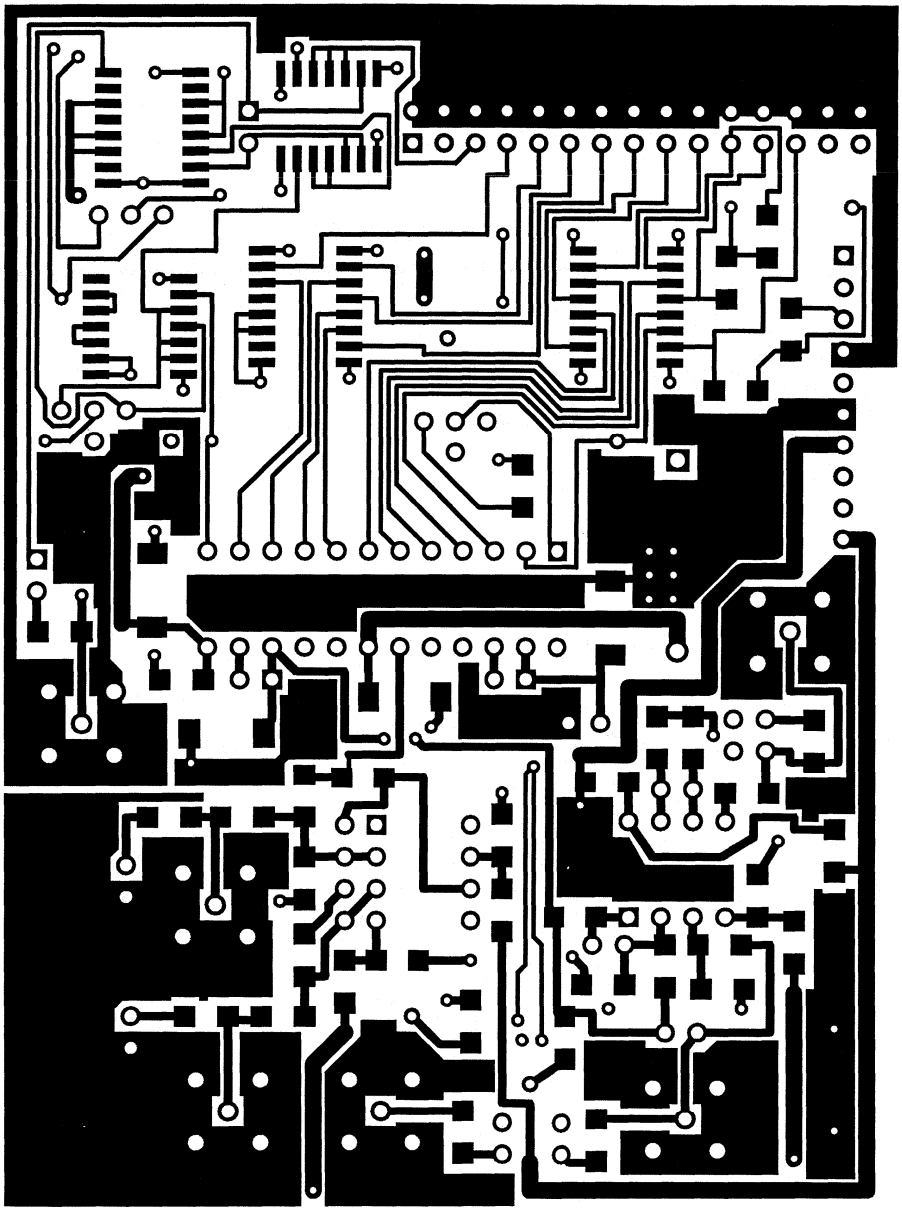


Figure 7. Top Silk



TOP TRACE

Figure 8. Top Trace

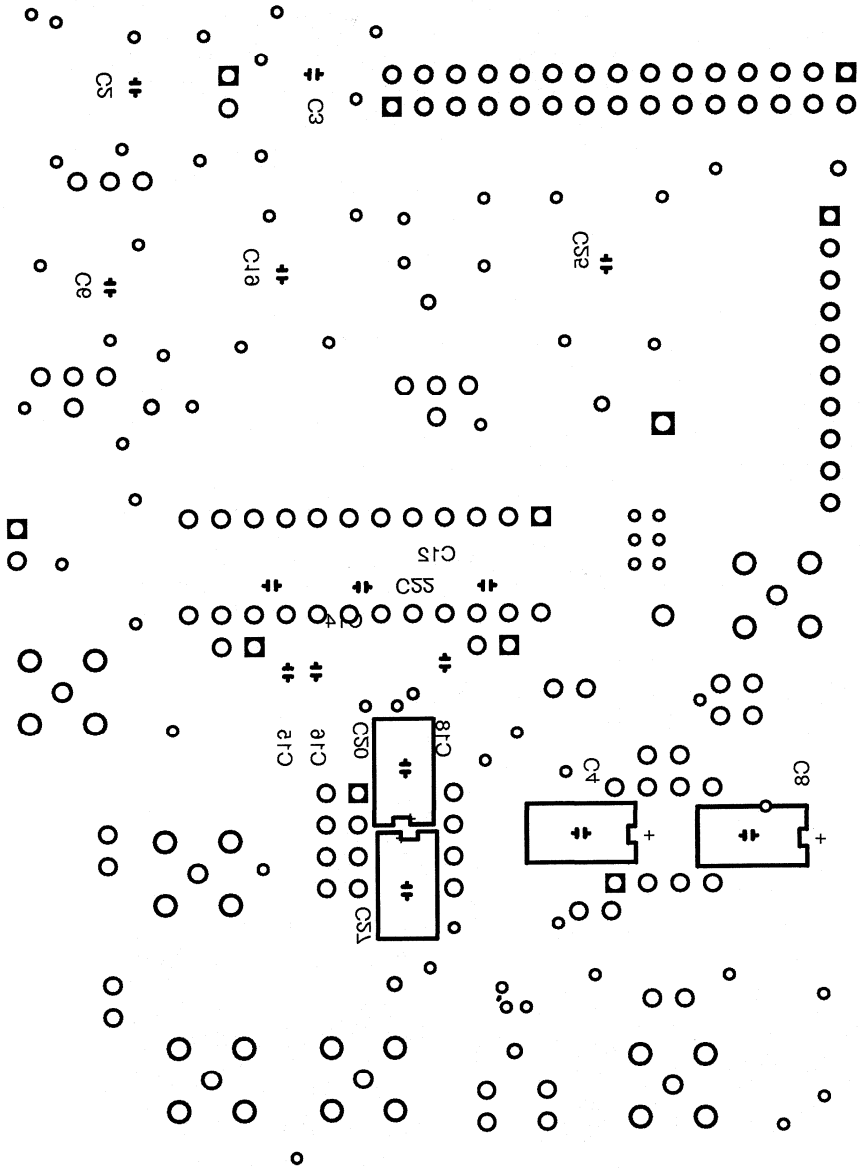
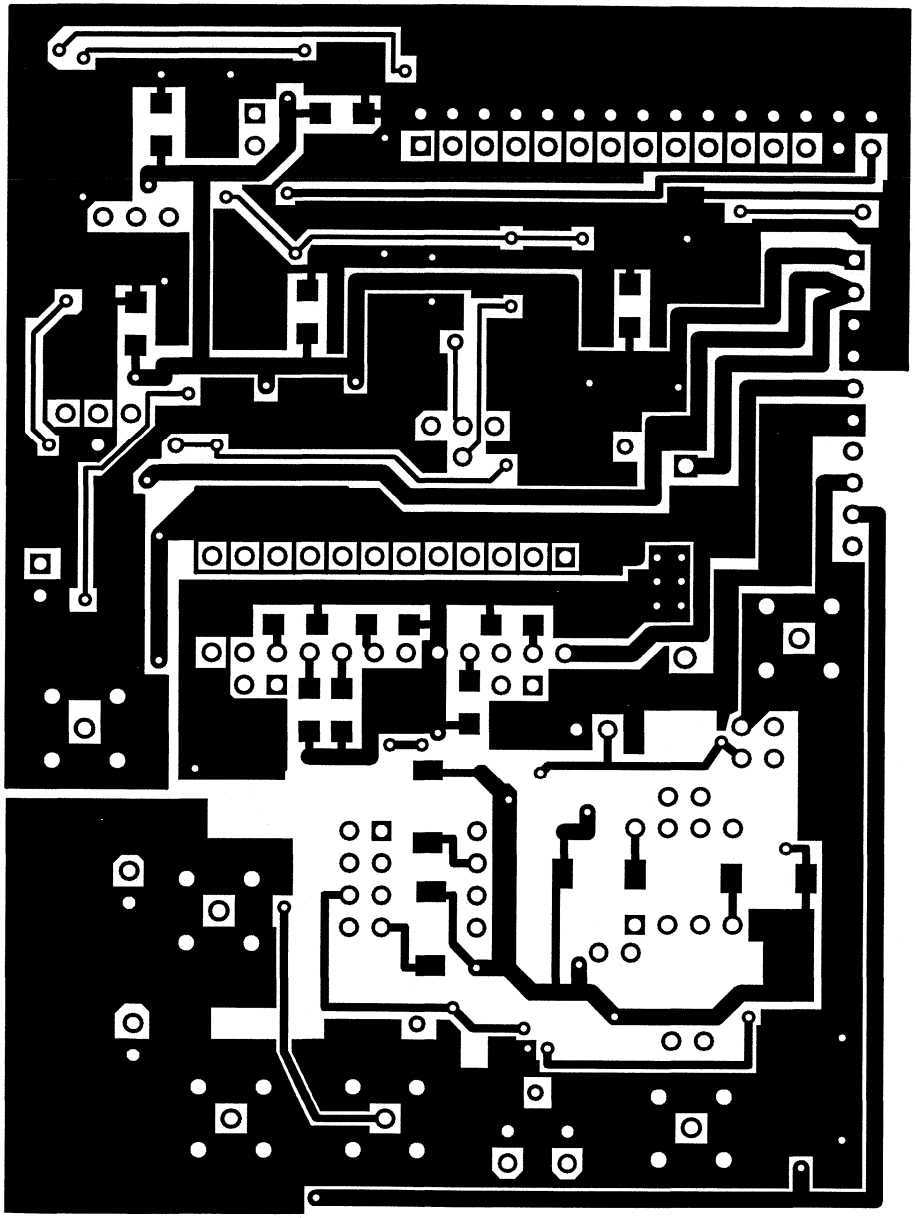


Figure 9. Bottom Silk – Top View



BOTTOM TRACE

Figure 10. Bottom Trace

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MP8785AB APPLICATION BOARD DOCUMENTATION

Evaluation Kit Parts List

This kit contains the following:

- One MP8785AB Applications Board with sample MP8785
- MP8785AB Documentation
- Circuit Diagram
- Layout Patterns

Features include:

- Easy Evaluation of the MP8785 8-bit ADC
- Optimized Printed Circuit Board Design
- Optimized Support Circuits
- User Friendly Interface
- Layout Applicable to Final Design

Introduction

The MP8785AB is a complete printed circuit test board designed to permit quick and accurate evaluation of the MP8785, 8-bit analog-to-digital converter. This application board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested (MP8785), an operational amplifier for input buffering, control logic and latches, and numerous connectors and jumper options.

With external laboratory equipment, complete DC and AC performance of the part can be evaluated.

Flexible user interface is provided by selectable jumper options and convenient connectors. Observation test points are available at commonly used locations.

A Preview of a Common Test Configuration

The board is set up as a general A/D test circuit where the references are fixed. *Figure 5.* shows the overall circuit, *Figure 4.* shows the defalt jumper settings, also listed in *Table I. Figures 6 through 9* show the PC board layout and component locations. There are many circuit possibilities built into the universal test board; however, starting with the default circuit is recommended.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.

System Configuration

Two complete evaluation circuit block diagrams showing the MP8785AB with typical external test equipment are shown in *Figure 2. and Figure 3.* The following is a more detailed description of the major on-board and external components used in these systems as seen in *Figure 2., and Figure 3.*

Application Board Circuitry

The application board support circuitry is shown in *Figure 5.* The major components supporting the A/D under test are:

1. ANALOG INPUT AMPLIFIER – An operational amplifier is used in an instrumentation amp configuration (gain –1) to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input. Holes for optional compensation caps are provided on-board.
2. DATA LATCH – The digital output of the A/D drive on-board latches which buffer the device under test from the external test equipment.
3. CONTROL LOGIC – Allows control of the data latch clocks as well as the $\overline{OE}$ pin of the DUT.

External Equipment Required

The system block diagrams (*Figure 2. and Figure 3.*) show the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES – ±15 volt and one (or two) +5 volt external power supplies are needed. Decoupling circuits are provided on the applications board, however, low noise, low output impedance supplies are necessary for best performance. A connector (CON3) is used for all power and ground connections. This connector is the 10 pin connector located along the top of the board. For best results, twist the power supply cable pairs. This minimizes coupling to and from these to unrelated sections of the setup.

2. CLOCK GENERATOR – A symmetrical clock signal must be applied to the SMB coax connector labeled CLOCK. Note the 50Ω input impedance. This drives the MP8785 via a two inverter delay.

3. INPUT SIGNAL GENERATOR – A clean, low distortion sine wave generator should be used as a signal source. A band pass or low pass filter is sometimes required to further reduce harmonics and bandlimit noise as shown in *Figure 2.* The SMB coax connector labeled A_{IN} accepts the analog input. An on board op amp is used to buffer this input (gain of –1) and provide low source impedance to drive the A/D under test. The socket has a standard 741 type pinout which allows experimentation with alternative amplifiers. J9 provides a 50Ω input termination impedance.

4. DITHER INPUT – The cross plot test configuration (described later) requires a triangle wave signal source. This input is attenuated by a factor of 10 and added to the A_{IN} signal. J6 connects this input to a 50Ω termination resistor.

5. COMMON – An alternate, non inverting input (gain of one when dither is disconnected). Connect to ground when not used. J12 connects COMMON to ground via a 50 Ω resistor. This input allows use of differential inputs or is used for applying a DC offset for level shifting the A_{IN}.

6. OSCILLOSCOPE – The output TP2 of a dither DAC, is used to drive the vertical input of the oscilloscope for manual linearity testing using the "cross plot" method described on the following page.

Optional Equipment

1. DSP – Evaluation of dynamic and static performance is done by external processing devices that perform histogram and harmonic analysis to determine characteristics like linearity, noise, distortion, intermodulation effects, etc. The data is available at the CON2 connector.

2. REFERENCE SUPPLIES – Internal reference voltages can be used by connecting V_{RT} to V_{RTS} through jumper J3 (top position) and connecting V_{RB} to V_{RBS} through jumper J7 (top position). This generates 2.6 V at V_{RT} and 0.6 V at V_{RB}. Alternatively, J3 and J7 can be placed in their bottom positions to connect V_{RT} to V_{DD} and V_{RB} to GND.

3. PRECISION EXTERNAL OUTPUT DAC – As an alternative to DSP, a high speed precision digital to analog converter can reconstruct the output in analog form. The analog measurements can be used to evaluate the A/D's performance using conventional analog instrumentation. Use the CLK pin of the output connector (CON2) to load the reconstruction DAC.

SYSTEM OPERATION

Analog Inputs

A_{IN} and COMMON Input Only

Differential input can be achieved by using A_{IN} and COMMON. If the dither input is left floating, then the differential input to the ADC is nominally given by:

$V_{IN} - V_{RB} = COMMON - A_{IN}$
where V_{IN} = MP8785 (pin 19)
V_{RB} = MP8785 (pin 23)

This allows reduction of common mode signals between A_{IN} and COMMON.

Dither and COMMON Input Only

With A_{IN} floating and a signal applied to DITHER:

$V_{IN} = 0.55 (COMMON + V_{RB}) - 0.1 (Dither)$
where V_{IN} = MP8785 (pin 19)
V_{RB} = MP8785 (pin 2)

Outputs

The parallel digital output of the A/D can be accessed on connector "CON1". A system clock (CLK) is available on that connector. This output data, in conjunction with various input stimuli, is used to evaluate the A/D and timing performance. The three common methods are described below.

Digital Signal Processing

A comprehensive dynamic performance evaluation is most often done by using external hardware capable of fast digital data acquisition, storage and analysis. The computation of integral linearity, differential linearity, signal to noise and distortion ratios, the effective number of bits, and other useful figures of merit is done using software having histogram and FFT capability. The accuracy of the test results depends upon the quality of the input sine wave. A low distortion sine wave generator with a low pass filter will be necessary.

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The logic output of the system can be converted back to analog by using a high performance digital to analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D's dynamically. In addition to a high quality sine wave input, the output D/A converter must be significantly more accurate than the A/D under test. The filtering effects of adding a zero order "hold" in the signal path are described in the Application Note MPSAN27 which can be found in the Micro Power Systems 1995 data book.

Cross Plot

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave generator and a low noise DC signal source. Input jacks are provided on the board so this "cross plot" method can be conveniently implemented (See *Figure 3.*) The oscilloscope must be set in the X-Y display mode.

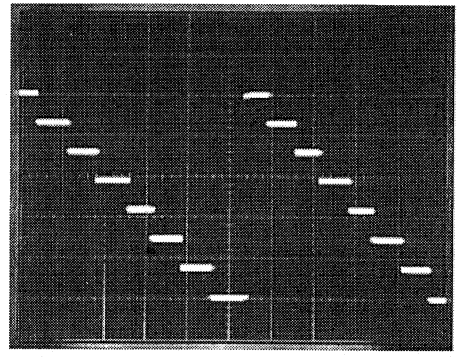

Figure 1. Cross Plot

A triangle wave (100 Hz) with a peak-to-peak amplitude of approximately 160 LSBs peak is supplied to the "dither" input. This is attenuated to 16 LSBs by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that ±8 divisions are swept. Look at Test Point 2 (TP2) with the vertical input. Set the horizontal gain for 1 LSB per division.

A stair step waveform will result (See *Figure 1.*). By changing the DC input, eight code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the endpoint thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are off-centered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

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Using this "cross plot" method is a good way to prove out the lab setup prior to more sophisticated DSP test.

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The MP8785AB offers flexibility through configuration determining jumpers. These optional jumpers furnish choices for (1) input termination resistors, and (2) the selection of several logic and clock options. *Table I.* and *Figure 4.* show the jumper functions along with the default configuration set up prior to shipment.

Termination Options

Termination resistors (50 Ω) are provided for all inputs. The CLOCK input has a permanent termination resistor to DGND. The Dither, A_{IN} & COMMON inputs have termination resistors which are selected by shorting jumpers J6, J9 or J12 as indicated in Table I. The default configuration terminates A_{IN} & COMMON, but not Dither: J9 & J12 shorted, J6 open.

Reference Options

Jumpers J3 and J7 are used to set the top and bottom reference voltages for the ADC. Both of these are two position jumpers that connect V_{RT} (top reference) and V_{RB} (bottom reference) to either the internal reference bias (V_{RTS} & V_{RBS}) or to the supply rails. See Table I for a complete description. The default connects V_{RT} to V_{DD} and V_{RB} to GND: J3(1,2) J7(1,2).

Logic Options

There are two logic option configured by jumpers. The ADC always receives a clock that is delayed by two inverters from the externally applied clock input. Jumper J1 (next to CLOCK SMB) configures the output register to either latch every output from the ADC or every other output. Jumper J11 is used to connect the $\overline{OE}$ input of the ADC to GND (ADC outputs always active) or to a delayed version of the ADC clock (disable ADC outputs on high phase of clock to reduce digital noise). The default positions will latch every ADC output, J1(1,2), and connect $\overline{OE}$ to the delayed clock signal, J11(1,2).

Final Design Considerations

After the MP8785AB has been used to demonstrate that the MP8785, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices. Where this is not possible, the following advice should be heeded:

1. Be generous with analog and digital ground planes. Repeat as closely as possible the ground plane system on the application board. A four layer board with the two internal layers dedicated to power and ground planes is ideal.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the MP8785AB.
3. Coupling between logic signals and analog circuitry can easily degrade an 8-bit system to a 6-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations for example.
4. Hi Z the A/D outputs during the V_{IN} sample time (when CLK is high).
5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front. Use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application.

Additional Documentation

A set of drawings showing the details of the printed circuit board layout are given in *Figure 6., Figure 7., Figure 8. and Figure 9. Figure 5.* is the complete electrical circuit. *Figure 4.* shows the jumper locations.

Technical Hotline

For any application hints, please call our USA hotline at (408) 562-3615.

Table I. Jumper Options

Jumper	Description	Default
J1 (2, 1)	Output data at same rate as ADC clock	✓
J1 (2, 3)	Divides output latch clock by 2 for dynamic V_{REF} testing	
J3 (2, 1)	V_{RT} tied to AV_{DD} of MP8785	✓
J3 (2, 3)	V_{RT} tied to V_{RTS}: 2.6 V at V_{RT}	
J6	Dither terminated to GND via 50 Ω	
J7 (2, 1)	V_{RB} tied to GND	✓
J7 (2, 3)	V_{RB} tied to V_{RBS}: V_{RB} at 0.6 V	
J9	A_{IN} terminated to GND via 50 Ω	✓
J11 (2, 1)	$\overline{OE}$ tied to CLK via 2K Ω : $\overline{OE}$ delayed	✓
J11 (2, 3)	$\overline{OE}$ tied to GND: The data is continuously available to the latches	
J12	COMMON terminated to GND via 50 Ω	✓

Notes:
1. J*x* (a, b) means short pins a and b of jumper *x*.
2. The ADC clock is not affected by the jumper combinations and is the same as the external clock – except for a 2 inverter delay.

Table II. Test Points

TP1	Output Data Latch Clock
TP2	Cross Plot Output

Table III. List of Components

Qty	Value	Ref Designators
1	74HC574	U3
1	74HC04	U1
1	74HC174	U2
1	MP8785	U4
1	Op Amp (AD811 AN)	U5
8	10µF	C5, C6, C8, C9, C12, C16, C18, C22
12	0.1µF	C1, C2, C3, C4, C7, C10, C11, C13, C15, C17, C19, C20
2	1 pF	C14, C21
1	2 KΩ	R15
4	1.5KΩ	R7, R10, R14, R17
1	10KΩ	R3
1	5KΩ	R4
1	2.5KΩ	R5
2	10Ω	R9, R16
1	15KΩ	R6
6	49.9Ω	R1, R11, R12, R13, R8, R18
1	1KΩ	R2
4	SMB CONNECTOR	A_{IN}, CLOCK, DITHER, COMMON
2	TESTPOINT	TP1, TP2
3	50 Ω Cables	BNC Male to SMB Jack. Can be purchased from Pasternack, Irvine, CA.
7	Jumpers	J1, J3, J7, J9, J11, J12, J7
18	IC Socket Pins	
3	10 Pin Header Connector	CON 1, CON2, CON3
1	PCB–Rev 0	MP8785AB PC Board

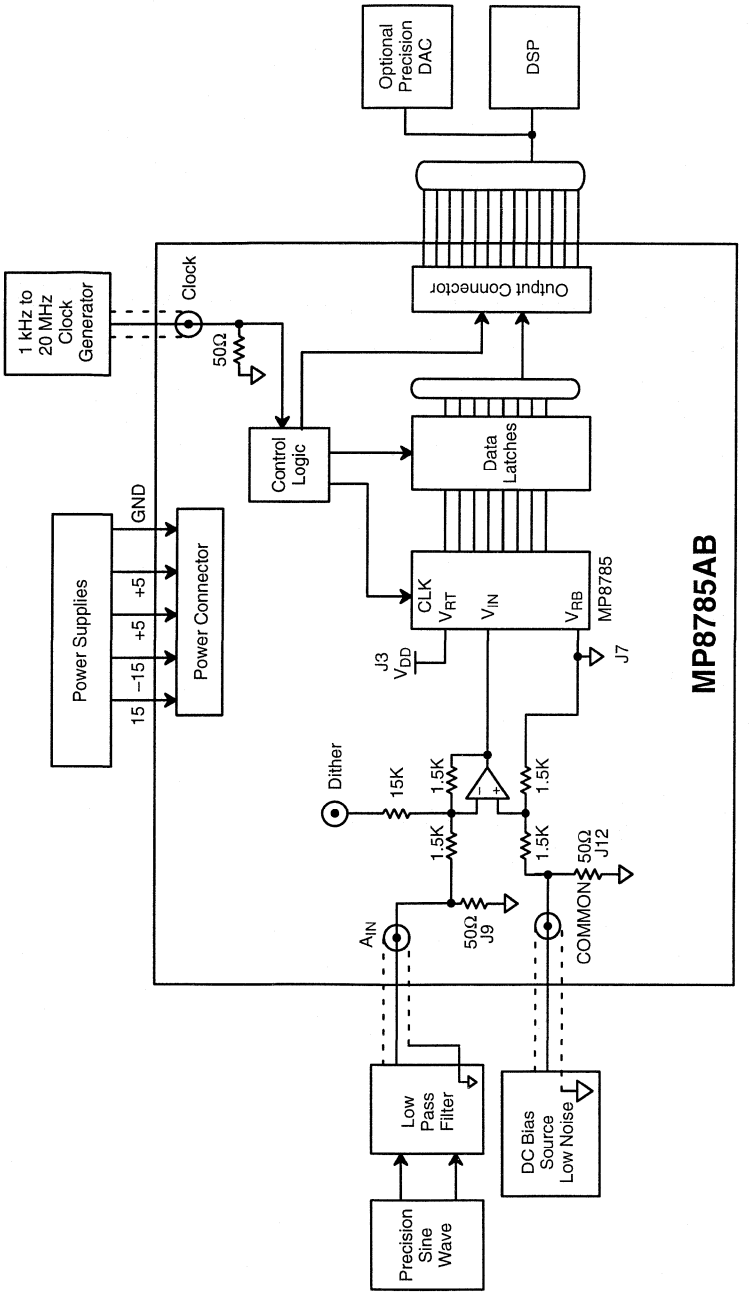

Figure 2. General A/D Test Circuit with Fixed Reference

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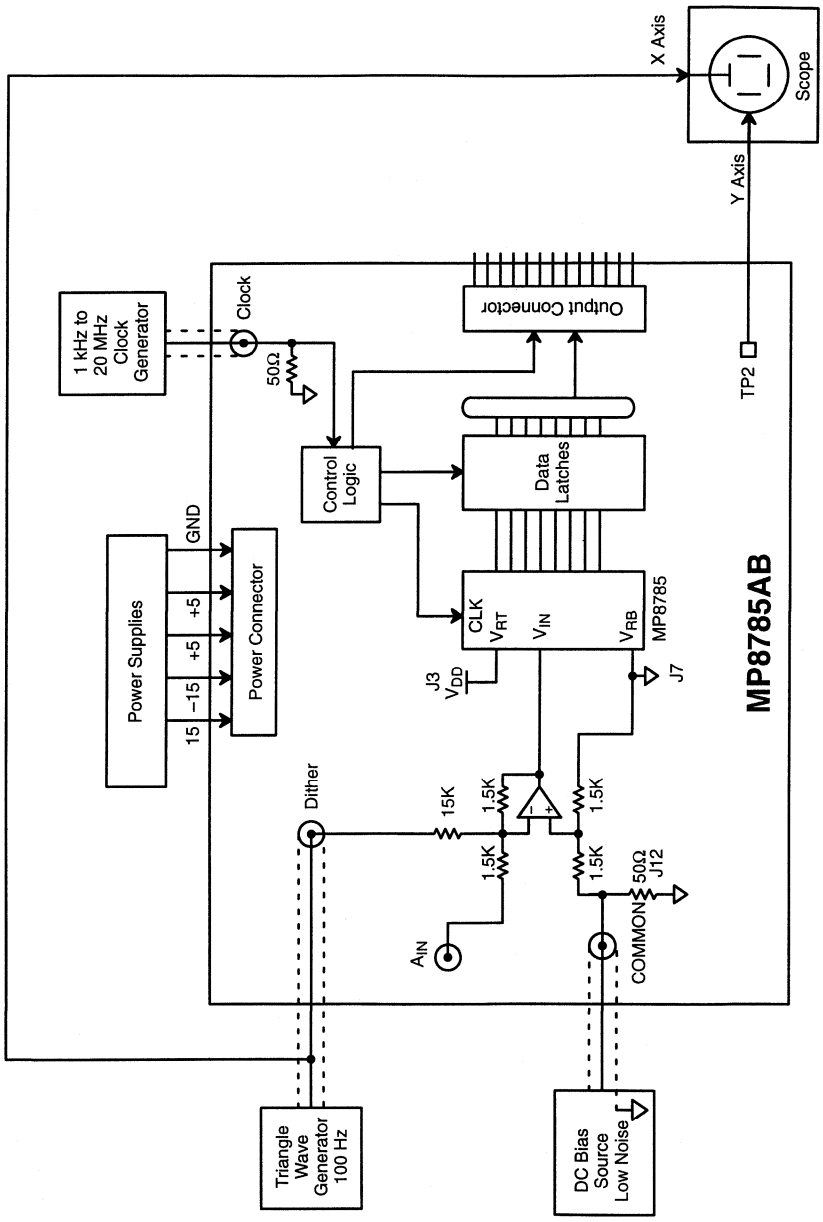

Figure 3. "Cross Plot" Set-Up

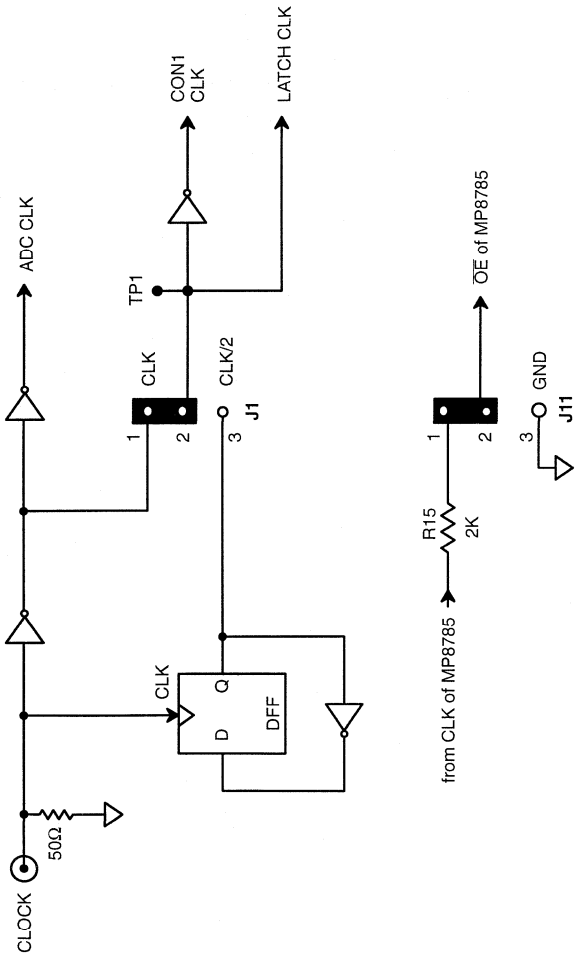

Figure 4. Default Jumper Configuration

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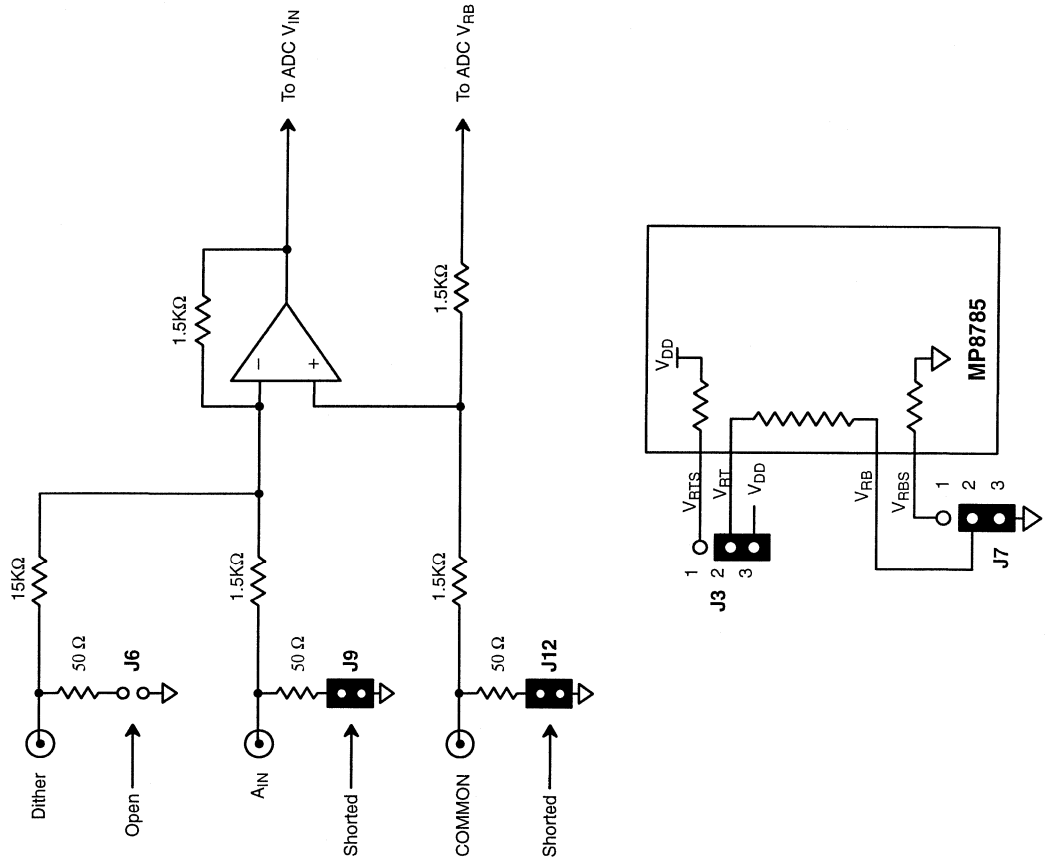

Figure 4. (Cont'd) Default Jumper Configurations

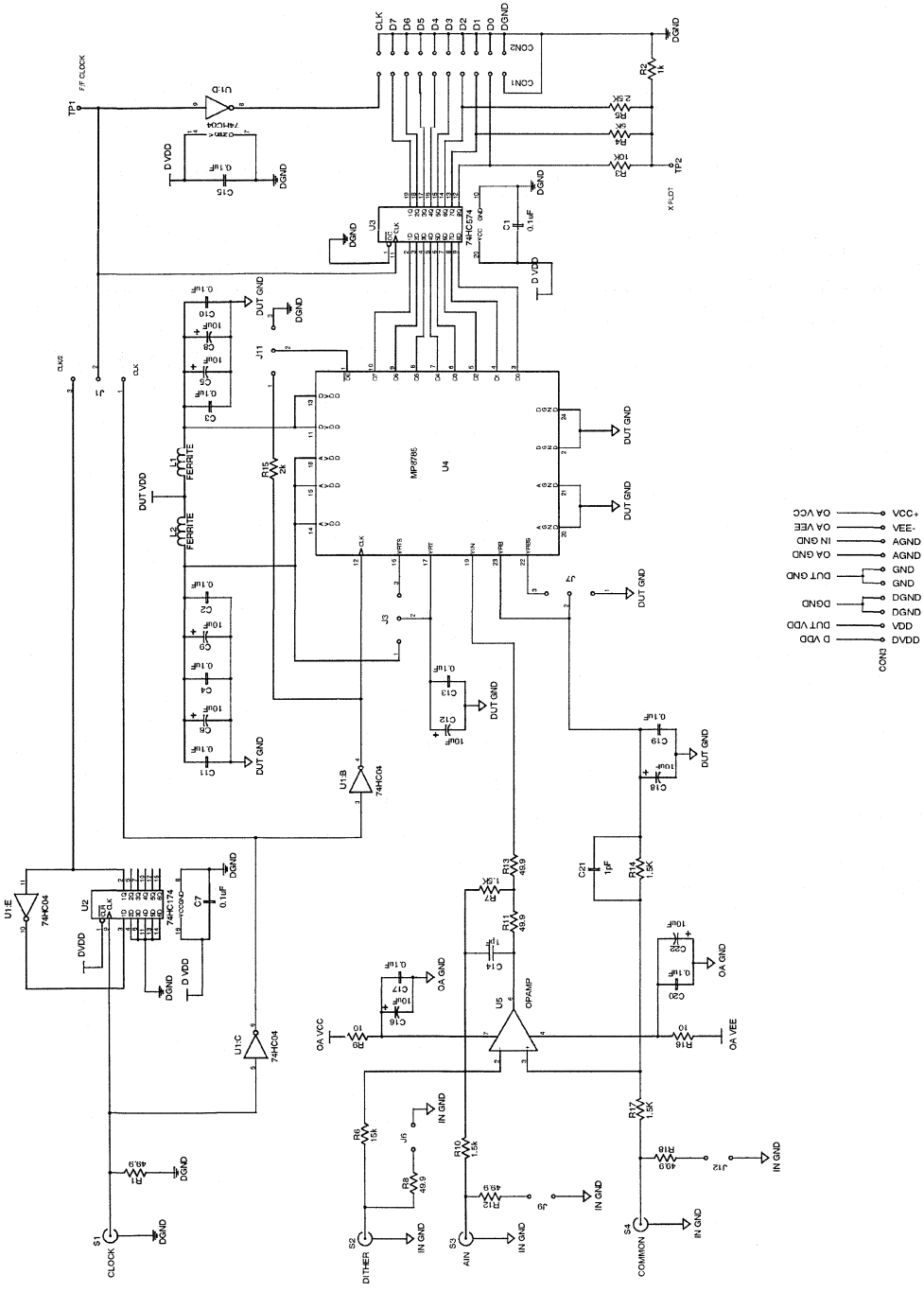

Figure 5. MP8785AB Schematic

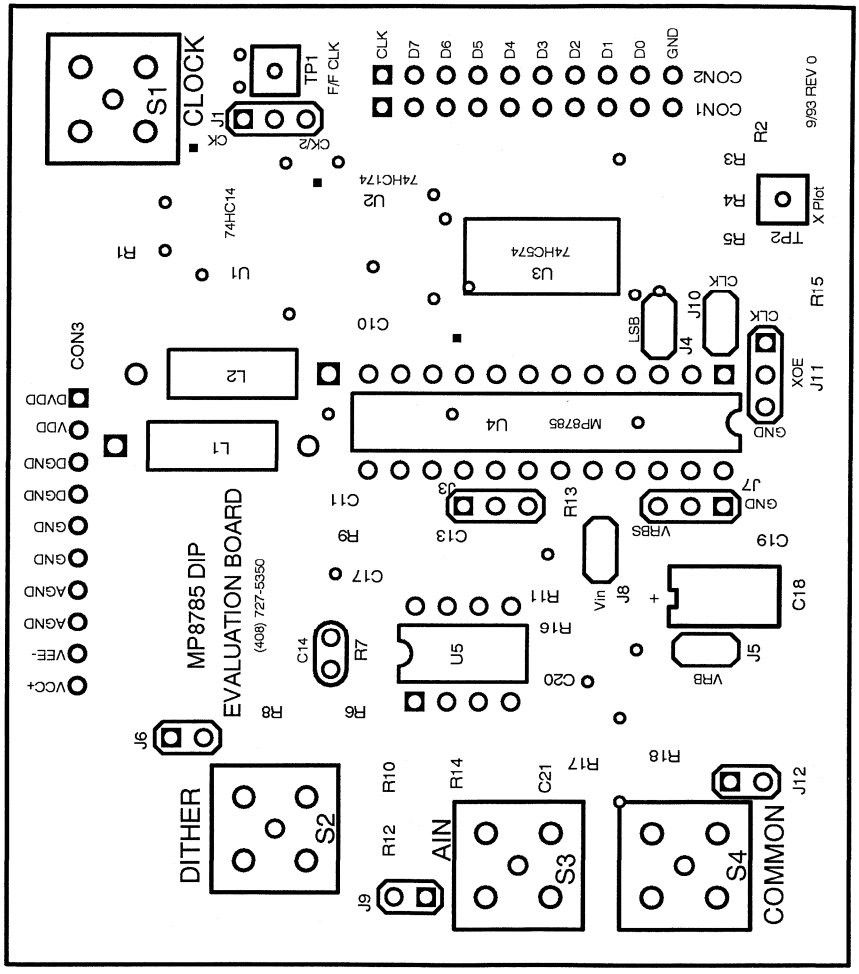

Figure 6. Top Silk

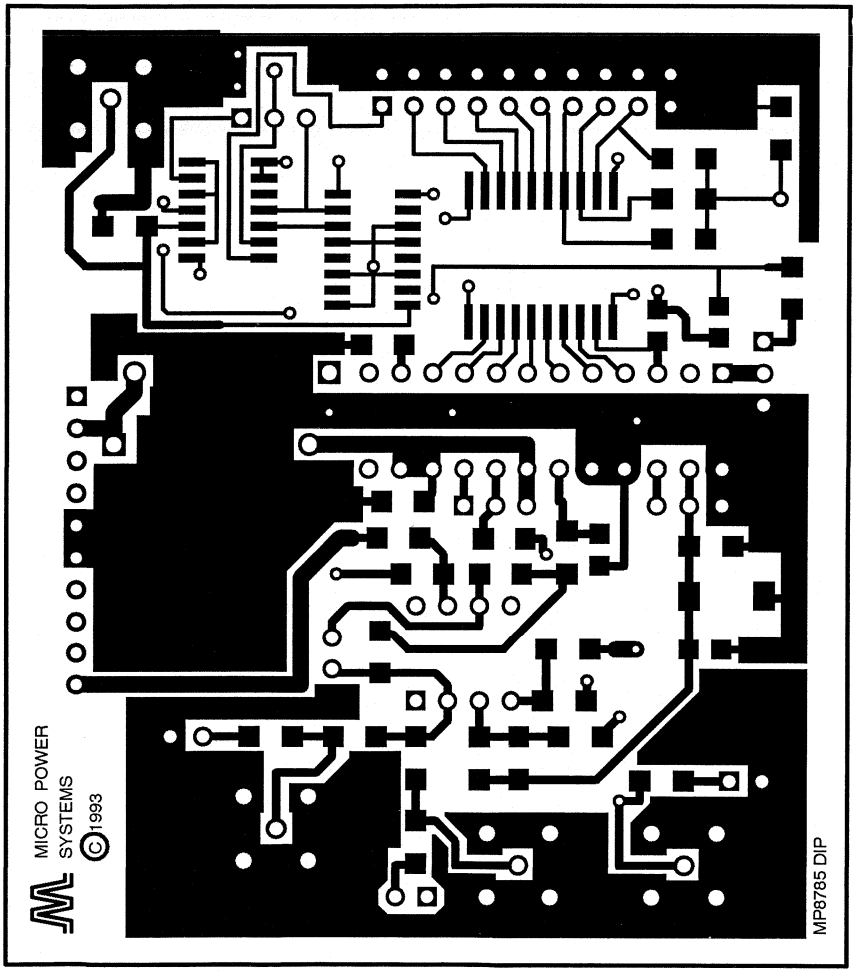

Figure 7. Top Trace

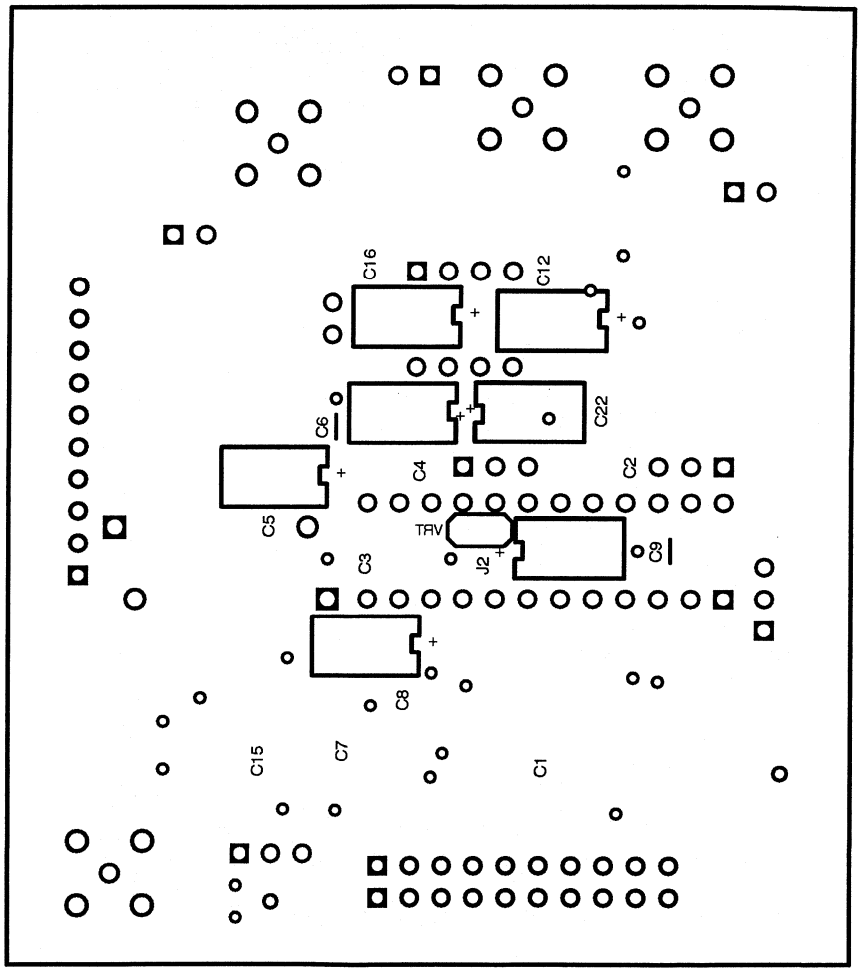

Figure 8. Bottom Silk (Bottom View)

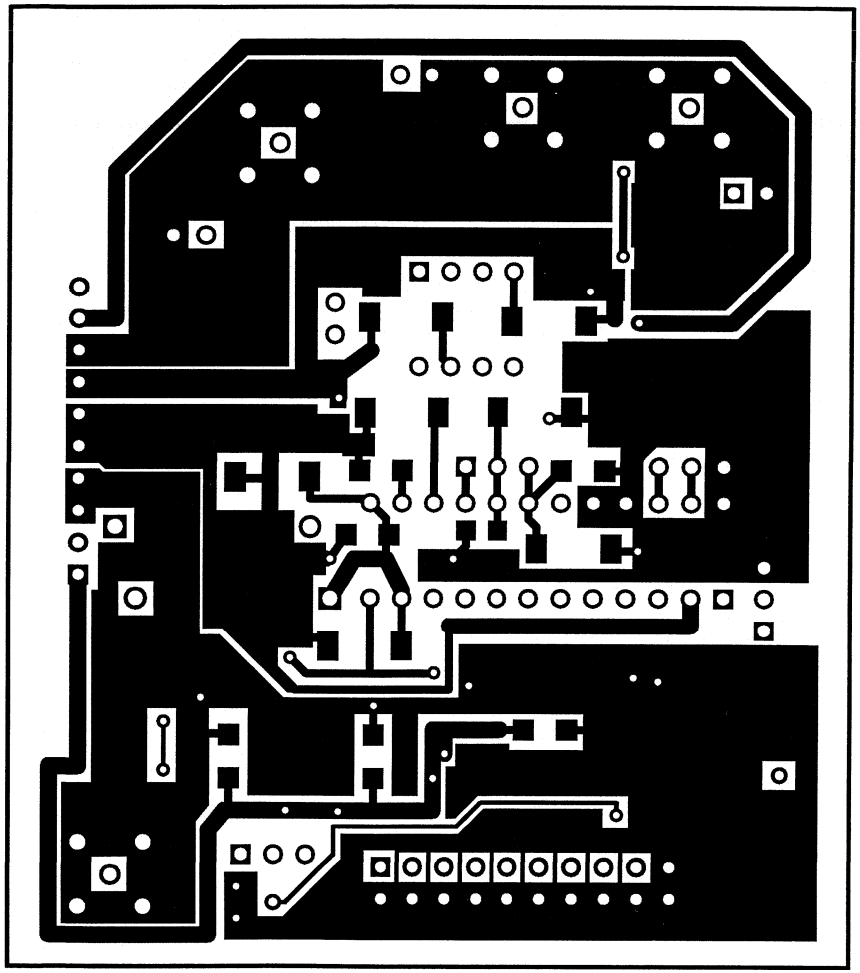

Figure 9. Bottom Trace (Bottom View)

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MP8791AB APPLICATION BOARD DOCUMENTATION

Evaluation Kit Parts List

This kit contains the following:

- One MP8791AB Applications Board with sample MP8791
- MP8791AB Documentation
- Circuit Diagram
- Layout Diagrams

Its uses provide the following features:

- Easy Evaluation of MP8791
- Optimized Printed Circuit Board Design
- Optimized Support Circuits
- User Friendly Interface
- Layout Applicable to Final Design

Introduction

The MP8791AB is a complete printed circuit test board designed to permit quick and accurate evaluation of EXAR's MP8791, 12-bit 2 MSPS analog-to-digital converter. This applications board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested (MP8791), operational amplifiers for input buffers, control logic and latches, and numerous connectors and jumper options.

With external laboratory equipment, complete DC and AC performance of the part can be evaluated.

Flexible user interface is provided by selectable jumper options and convenient connectors. Observation test points are available at commonly used locations.

A Preview of a Common Test Configuration

The board is set up as a general A/D test circuit where the references are fixed. *Figure 2.* shows the overall circuit, *Figure 5.* shows the PC board layout and jumper locations, also listed in Table 1. There are many other circuit possibilities built into the universal test board; however, starting with the default circuit is recommended.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.

System Configuration

Two complete evaluation circuit block diagrams showing the MP8791AB with typical external test equipment is shown in *Figure 2. and Figure 3.* The following is a more detailed description of the major on-board and external components used in these systems as seen in *Figure 2., Figure 3., and Figure 6.*

Application Board Circuitry

The application board support circuitry is shown in *Figure 6.* The major components supporting the A/D under test are:

1. V_{REF} BUFFER – A dual op amp (EL2224C) can be used to isolate the externally supplied $V_{REF(+)}$ and $V_{REF(-)}$ from the device under test and provides a low source impedance. These buffers can be bypassed with onboard jumpers (J6 and J13). If voltage feedback op amps are used, holes for optional compensation caps are provided.
2. ANALOG INPUT AMPLIFIER – An operational amplifier (AD847) is used in an instrumentation amp configuration (gain –5) to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input. Holes for optional compensation caps are provided on-board.
3. DATA LATCHES – The digital output of the A/D drive on-board latches which buffer the device under test from the external test equipment.
4. CONTROL LOGIC – Allows control of the data latch clocks as well as the $\overline{OE}$ pin of the DUT.

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External Equipment Required

The system block diagrams (*Figure 2. and Figure 3.)* shows the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES – ±15 volt and one (or two) +5 volt external power supplies are needed. Decoupling circuits are provided on the applications board, however, low noise, low output impedance supplies are necessary for best performance. A connector (CON3) is used for all power and ground connections. This connector is the 10 pin connector located next to the $V_{REF(-)}$ input. For best results, twist the power supply cable pairs. This minimizes coupling to and from these to unrelated sections of the setup.
2. CLOCK GENERATOR – A 1 KHz to 2 MHz symmetrical clock signal must be applied to the SMB coax connector labeled CLOCK. Note the 50Ω input impedance.
3. REFERENCE SUPPLIES – A positive and negative reference voltage is connected through the SMB coax connectors labeled $V_{REF(+)}$ and $V_{REF(-)}$ (typically +5 and 0 volts respectively). The external reference voltages can be configured to go through op amp buffers or go directly to the A/D by using jumpers J6 and J13. Note that $V_{REF(+)}$ must be more positive than $V_{REF(-)}$, since V_{RT} must be $>V_{RB}$ on chip.
4. INPUT SIGNAL GENERATOR – A clean, low distortion sine wave generator is used as a signal source. A band pass filter is sometimes required to further reduce harmonics and bandlimit noise as shown. The SMB coax connector labeled A_{IN} accepts the analog input. An on board op amp (AD847) is used to amplify this input (gain of –5) and provide low source impedance to drive the A/D under test. The socket has a standard 741 type pinout which allows experimentation with alternative amplifiers.
5. DITHER INPUT – The cross plot test configuration (later described) requires a triangle wave signal source. This signal is added to a DC input signal through the SMB connector labeled DITHER (an inverting input with gain of 1/50). J7 connects this point to ground via a 50Ω resistor.
6. A_{IN} COMMON – An alternate, non inverting input (gain of five). Connect to ground when not used. J11 connects A_{IN} COMMON to ground via a 50 Ω resistor. This input allows use of differential inputs or used for applying a DC offset for level shifting the A_{IN}.
7. OSCILLOSCOPE – The output of a dither DAC, TP3, is used to drive the vertical input of the oscilloscope for manual linearity testing using the "cross plot" method described on the following page.
8. DSP – Evaluation of dynamic and static performance is done by external processing devices that perform histogram and harmonic analysis to determine characteristics like linearity, noise, distortion, intermodulation effects, etc. The data is available at the CON1 connector, which is the inside column of jumper connectors labelled D0 through D11.

Optional Equipment

1. Precision External Output DAC – As an alternative to DSP, a high speed precision digital to analog converter can reconstruct the output in analog form. The analog measurements can be used to evaluate the A/D's performance using conventional analog instrumentation. Use the DACEN output at CON1 to load the reconstruction DAC.
2. Reference Control DACS – The reference voltage at the top (V_{RT}) and bottom (V_{RB}) of the A/D can be changed by external DACs on alternate CLOCK cycles to change offset and scale factor. Data can be loaded into the DACs by using the logic signal DACEN on the output connector. The two DACs must have resolution and settling time characteristics consistent with the application. Note that C14, C13, C21, and C22 are decoupling capacitors at the reference pins. These have to be removed when V_{RT} and V_{RB} are driven dynamically.

SYSTEM OPERATION

Reference Inputs

With the reference op amps in circuit, the ADC's reference pins (V_{RB} and V_{RT}) are driven in an offset and range mode:

$V_{RB} = V_{REF(-)}$, $V_{RT} = V_{REF(-)} + V_{REF(+)}$

Hence $V_{REF(-)}$ defines the offset and $V_{REF(+)}$ defines the span.

Analog Inputs

A_{IN} and A_{IN} COMMON Input Only

Differential input can be achieved by using A_{IN} and (A_{IN} COMMON). If the DITHER input is left floating, then the differential input to the ADC is given by:

ADCIN – $V_{REF(-)}$ = 5 (A_{IN} COMMON) – 5 A_{IN}

under the assumption of ideal components. This allows reduction of common mode signals between A_{IN} and (A_{IN} COMMON).

DITHER and A_{IN} COMMON Input Only

With A_{IN} floating and a signal applied to DITHER:

ADCIN = 0.875 • A_{IN} COMMON – 0.05 • DITHER + 0.175 • $V_{REF(-)}$,
where ADCIN = A_{IN} (MP8791 pin 3).

Outputs

The parallel digital output of the A/D can be accessed on connector "CON1". A system clock (PTSCLK) and an external DAC enable (DACEN) are also available on that connector. This output data, in conjunction with various input stimuli, is used to evaluate the A/D and timing performance. The three common methods are described below.

Digital Signal Processing

A comprehensive dynamic performance evaluation is most often done by using external hardware capable of fast data acquisition and storage. The computation of integral linearity, differential linearity, signal to noise and distortion ratios, the effective number of bits, and other useful figures of merit is done using software having histogram and FFT capability. The accuracy of the test results depends upon the quality of the input sine wave. A low distortion sine wave generator with a band pass filter will be necessary.

Commercial software packages with the needed computational features are available. The Tektronix PTS101 is used by EXAR to acquire and analyze the ADC data.

Analog Testing with External DAC

The logic output of the system can be converted back to analog by using a high performance digital to analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D's dynamically. In addition to a high quality sine wave input, the output D/A converter must be significantly more accurate than the A/D under test. The filtering effects of adding a zero order "hold" in the signal path are described in EXAR Application Note MPSAN27 which can be found in the 1993 data book.

Cross Plot

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave generator and a low noise DC signal source. Input jacks are provided on the board so this "cross plot" method can be conveniently implemented (See *Figure 3.*). The oscilloscope must be set in the X-Y display mode.

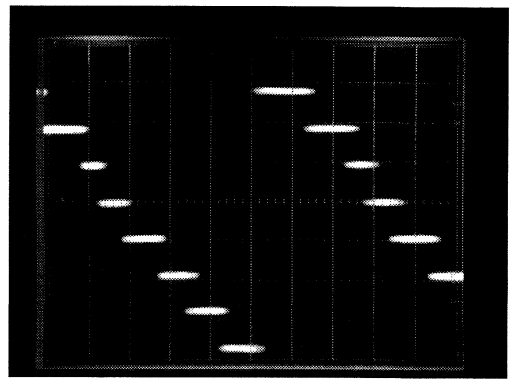

Figure 1. Cross Plot

A triangle wave (100 Hz) with a peak-to-peak amplitude of approximately 160 LSBs peak is supplied to the "DITHER" input. This is attenuated to 8 LSB's by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that ±4 divisions are swept. Look at Test Point 3 (TP3) with the vertical input. Set the horizontal gain for 1 LSB per division.

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A stair step waveform will result (See *Figure 1.*) By changing the DC input, eight code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the endpoint thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are off-centered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

Since the conversion speed is much faster than the dither frequency, multiple readings are taken at each threshold. The horizontal variation of each threshold gives a qualitative measure of noise (in LSB's).

Using this "cross plot" method is a good way to prove out the lab setup prior to more sophisticated DSP test.

Jumper Options

The MP8791AB offers flexibility through configuration determining jumpers. These optional jumpers furnish choices for (1) input termination resistors, (2) bypassing of the reference input buffers, and (3) the selection of several logic and clock options. *Table I., Figure 4., and Figure 5.* show the jumper functions along with the default configuration set-up prior to shipment.

Termination Options

Termination resistors (50 Ω) can be added to the five analog input coax SMB connectors as indicated in *Table I.* (J11, J4, J7, J9, and J12). Note that the CLOCK input is not optional. A permanent 50 Ω termination is connected from its input to digital ground (DGND). The default configuration for the other five coax inputs is — no termination resistors are connected.

Bypass Options

The reference input buffers can be bypassed with J6 and J13 or the V_{RB} pin of the A/D grounded if J8 is inserted. Remove U4, the dual op amp (EL2224C) when using these unbuffered modes. The default mode is — buffers are out.

Logic Options

The logic options are selected using the five jumpers as listed in *Table I.* and shown in detail in *Figure 6.* Note that three of these jumpers have multiple combinations. Note also that the clock connected to the A/D being tested is always the same as the external clock after a two inverter delay. A simplified logic diagram is given in *Figure 4.* The logic control jumpers are primarily set for two basic test configurations. The standard evaluation mode is shown in *Figure 4.*

Final Design Considerations

After the MP8791AB has been used to demonstrate that the MP8791, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices. Where this is not possible, the following advice should be heeded:

1. Be generous with analog and digital ground planes. Repeat as closely as possible the ground plane system on the application board.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the MP8791AB.
3. Coupling between logic signals and analog circuitry can easily change a 12-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations for example.
4. Tri-state the output latches and the A/D enable during the A_{IN} sample time.
5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front, i.e. use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application.
7. For sampling of high frequency signals, a sample and hold amplifier like the AD783 is recommended.
8. Decoupling capacitors on pins R1, R2 and R3 do not improve the ADC's performance.

Additional Documentation

A set of drawings showing the details of the electrical circuit and board layout are given in *Figure 8. Figure 10. Figure 7. and Figure 9. Figure 6.* is the complete electrical circuit. *Figure 5.* shows the jumper locations.

Technical Hotline

For any application hints, please call our hotline at (408) 562-3615.

Table I. Jumper Options

Termination of Input Coax Cables		
Jumper	**Description**	**Default**
J11	Connecting adds 50 Ω from A_{IN} COM to AGND	
J4	Connecting adds 50 Ω from A_{IN} to AGND	✔
J7	Connecting adds 50 Ω from DITHER to AGND	
J9	Connecting adds 50 Ω from $V_{REF(+)}$ to AGND	
J12	Connecting adds 50 Ω from $V_{REF(-)}$ to AGND	
Reference Amplifer/Buffer Bypass		
J6	Connecting shorts coax $V_{REF(+)}$ Jack to V_{REF}T of ADC	✔
J13	Connecting shorts coax $V_{REF(-)}$ Jack to V_{REF}B of ADC	
J8	Connecting shorts V_{REF}B (on ADC) to AGND	✔
Logic and Clock Jumpers		
J2 (2, 3)	Connecting makes the latch clock the same or inverted as the ADC clock. Dependent on J12A.	
J2 (2, 1)	Connecting delays latch clock by 2 prop delays	✔
J3	Divides latch clock by 2 for dynamic V_{REF} control	
J5	Usually connected – except for dynamic V_{REF} control	✔
J12A (2, 1)	Latch clock is inverted ADC clock	
J12A (2, 3)	Latch clock is same as ADC clock	✔
J12A (2, 4)	Used for dynamic V_{REF} control	
J13A (2, 1)	Connects clock to $\overline{OE}$ through 4.7kΩ (delays $\overline{OE}$)	✔
J13A (2, 4)	Connects Latch CLK to $\overline{OE}$	
J13A (2, 3)	Connects Aperture to $\overline{OE}$	

Notes:
1. J*x* (a, b) means short pin a and pin b of jumper *x*.
2. The ADC clock is not affected by the jumper combinations and is the same as the external clock – except for 2 inverter delay.
3. Connect either J3 or J5 but not both simultaneously.
4. When using the amplifier bypass jumpers, remove the op amps from the sockets.

Table II. Test Points

TP1	CLK into MP8791
TP2	V_{REFT} via 100Ω resistor
TP3	Crossplot output
TP6	D0 output of MP8791 i.e. LSB
TP7	$\overline{OE}$ of MP8791
TP9	V_{REFB} via 100Ω resistor

Table III. List of Components

Qty	Value	Ref Designators
1	74HC02	U2
1	74HC04	U1
3	74HC174	U3,U5,U6
1	MP8791	U7
1	AD847	U8
1	EL22224C or equiv.	U4 (optional)
7	10µF	C13, C20, C21, C27, C4, C8, C9
13	0.1µF	C11, C14, C19, C2, C22, C23, C24, C25, C3, C5, C6, C7
6	1.5KΩ	R1, R10, R19, R2, R22, R8
1	20KΩ	R11
1	10KΩ	R12
1	5.1KΩ	R13
4	10Ω	R14, R18, R25, R3
1	150KΩ	R15
7	49.9Ω	R17, R20, R26, R29, R31, R4, R6
3	39Ω	R21, R28, R7
1	4.7KΩ	R24
2	1KΩ	R27, R9
2	100Ω	R30, R5
2	7.5KΩ	R16, R23
6	SMB CONNECTOR	A_{IN}, A_{IN} COM, CLOCK, DITHER, $V_{REF(+)}$, $V_{REF(-)}$
6	TESTPOINT	TP1, TP2, TP3, TP6, TP7, TP9
3	50 Ω Cables	BNC Male to SMB Jack. Can be purchased from Pasternack, Irvine, CA.
7	Jumpers	J4, J6, J5, J8, J2, J12A, J13A
2	8 Pin DIP Socket	SU4, SU8
28	IC Socket Pins	
1	10 Pin Header Connector	CON3
1	30 Pin Header Connector	CON1, CON2
1	PCB–Rev 1	MP8791AB PC Board

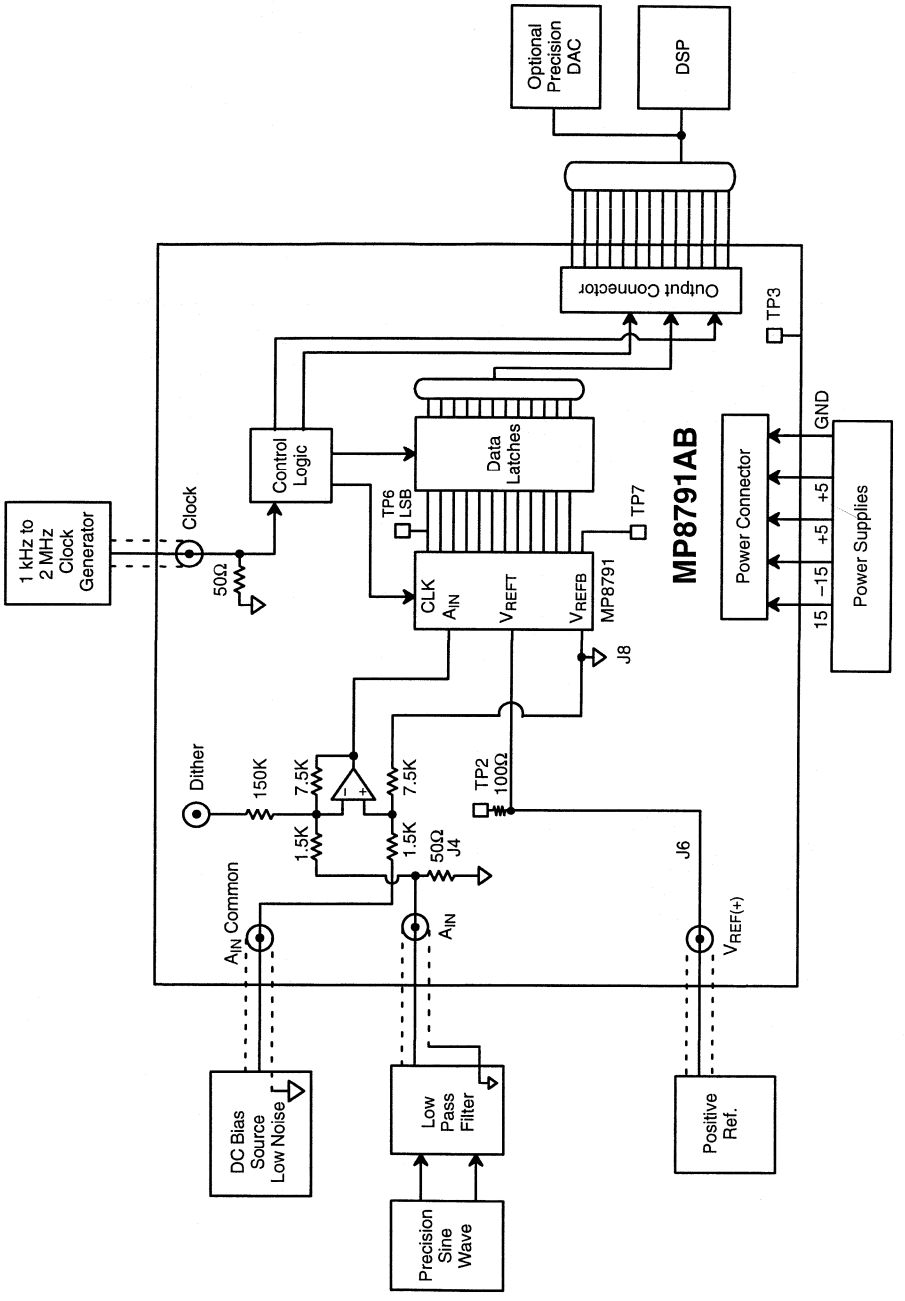

Figure 2. General A/D Test Circuit with Fixed Reference

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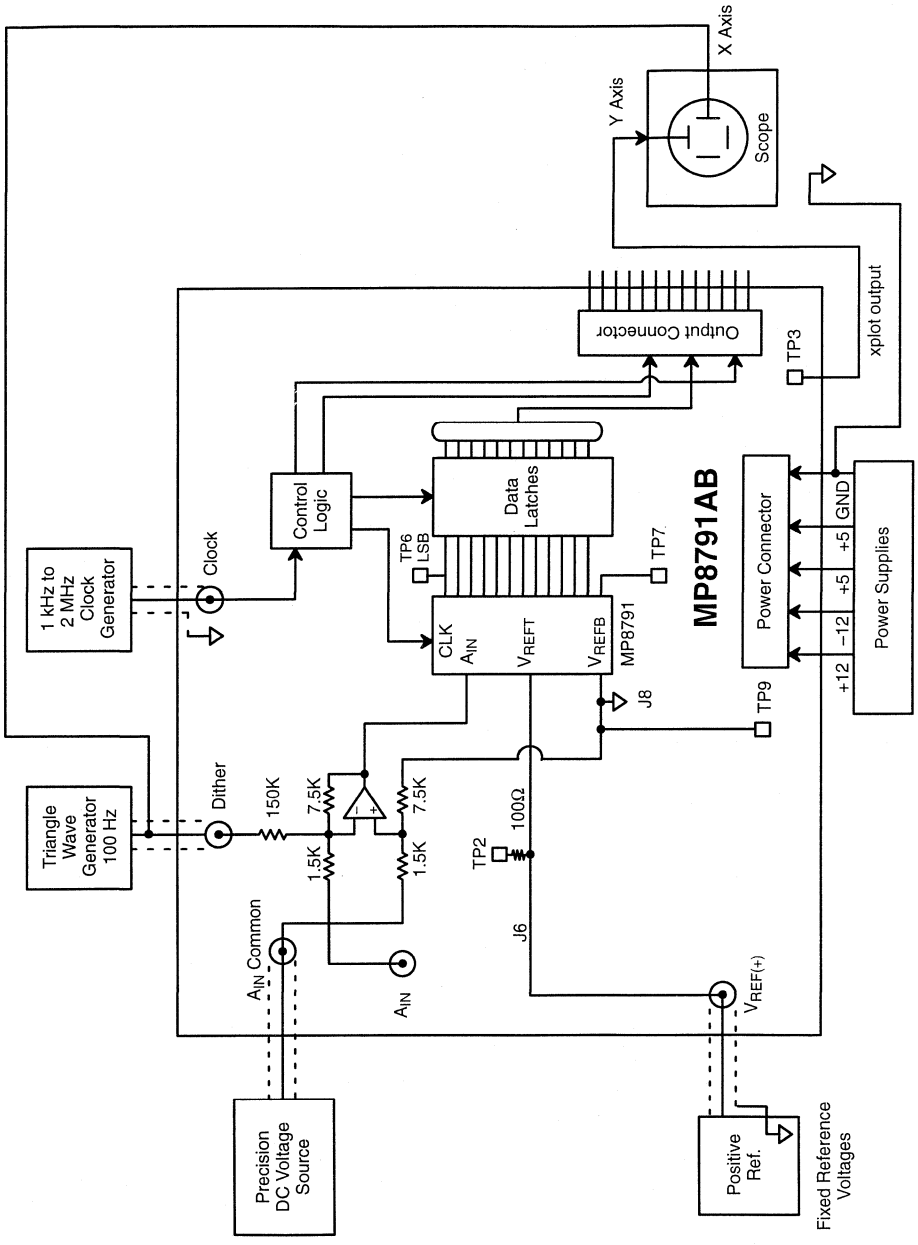

Figure 3. "Cross Plot" Set-Up

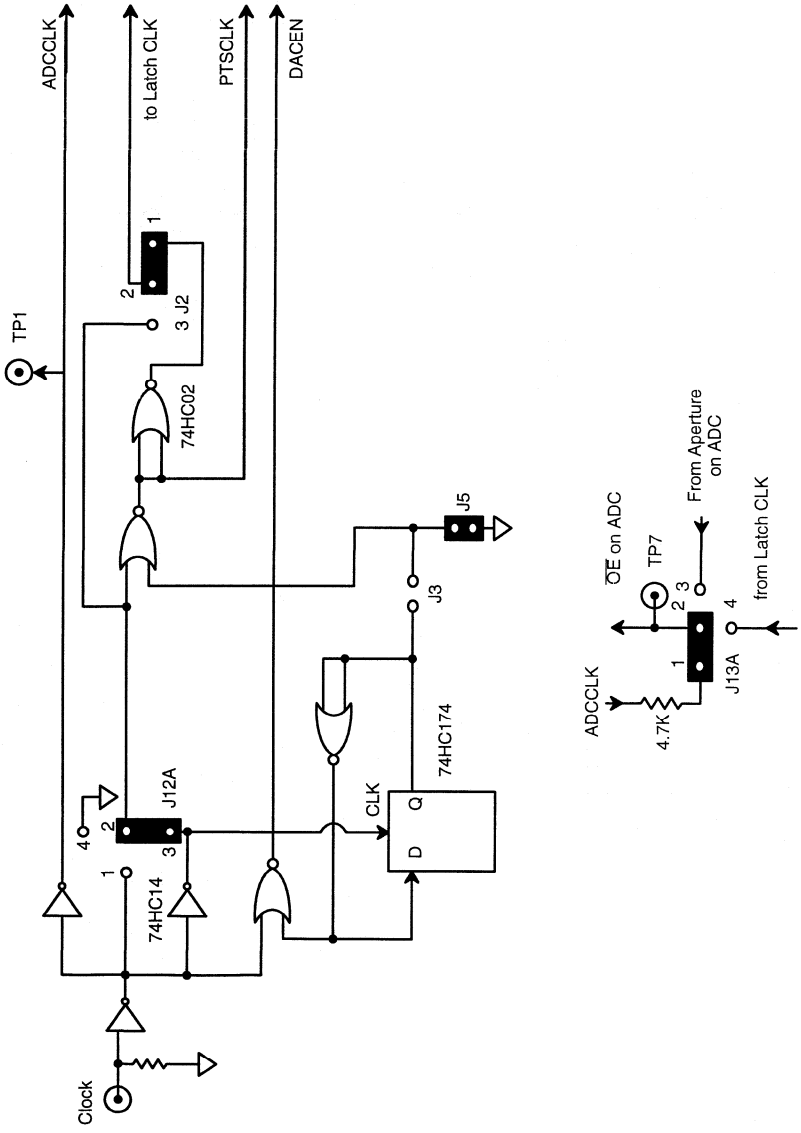

Figure 4. Default Jumper Configuration

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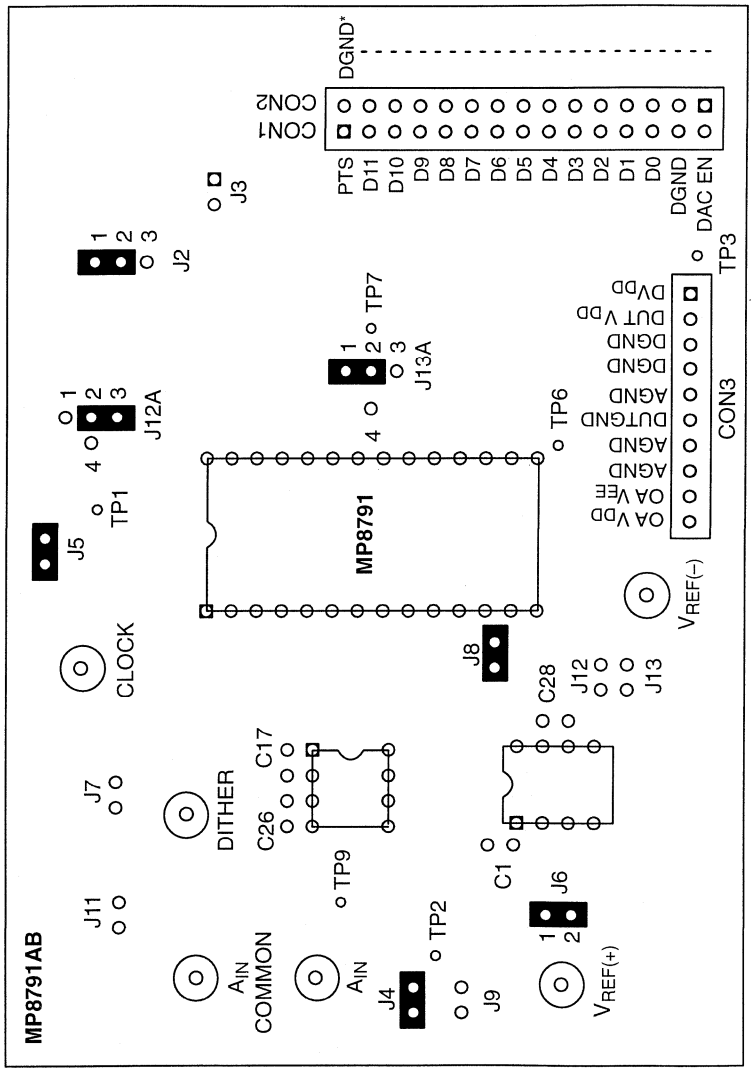

*Note: All pins of CON2 are DGND.

Figure 5. MP8791AB Standard Jumper Settings

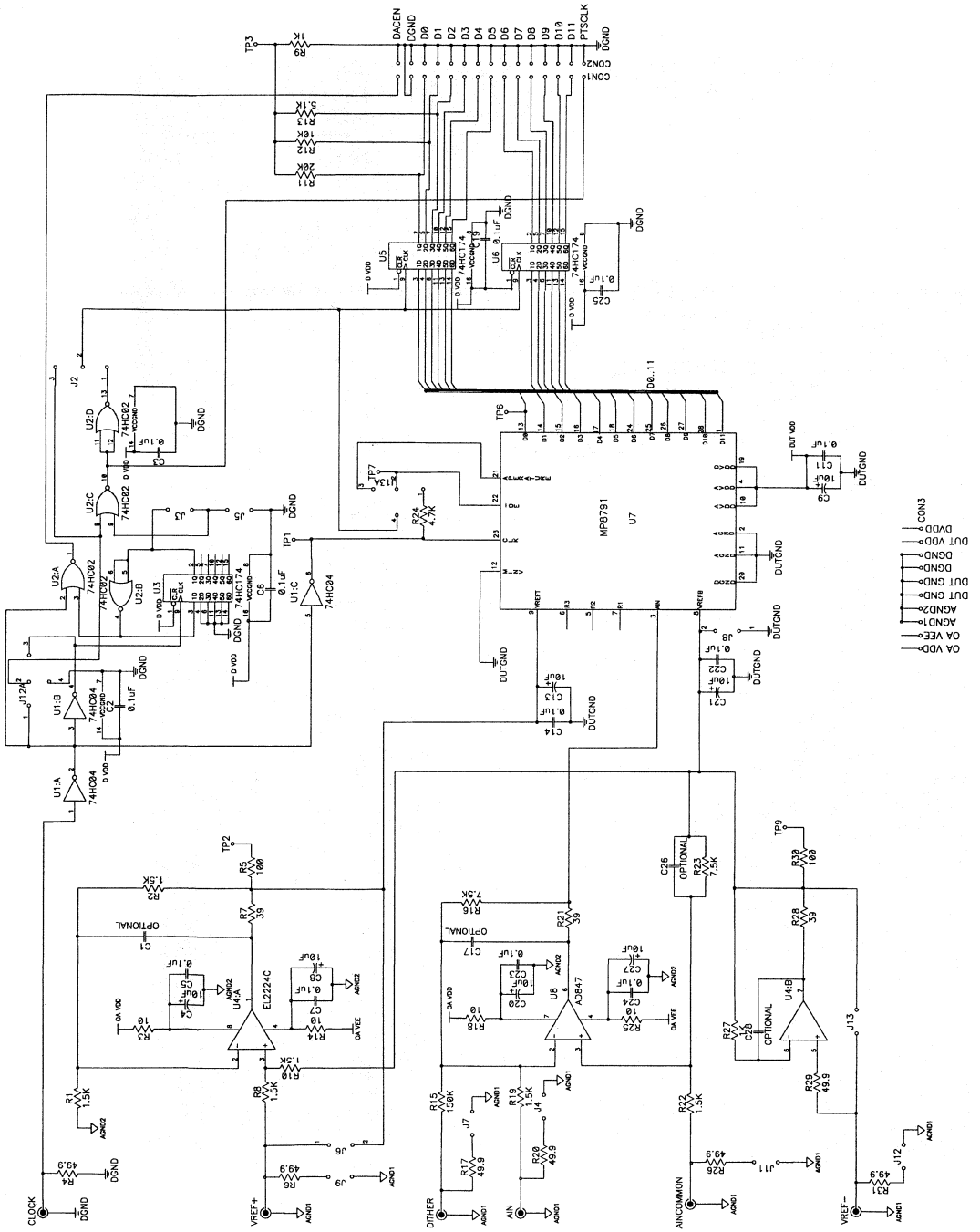

Figure 6. MP8791AB Schematic

8

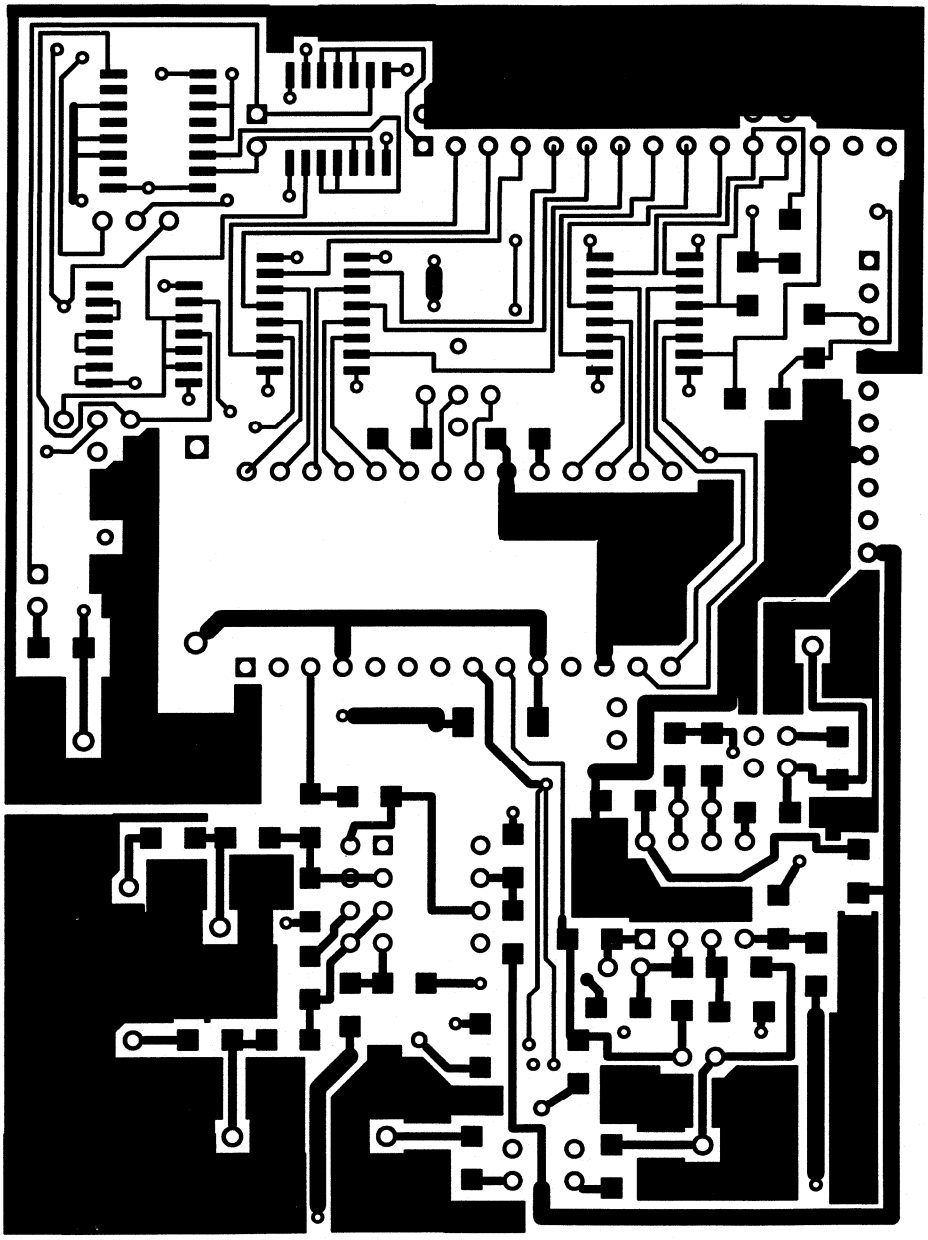

Figure 7. Top Trace

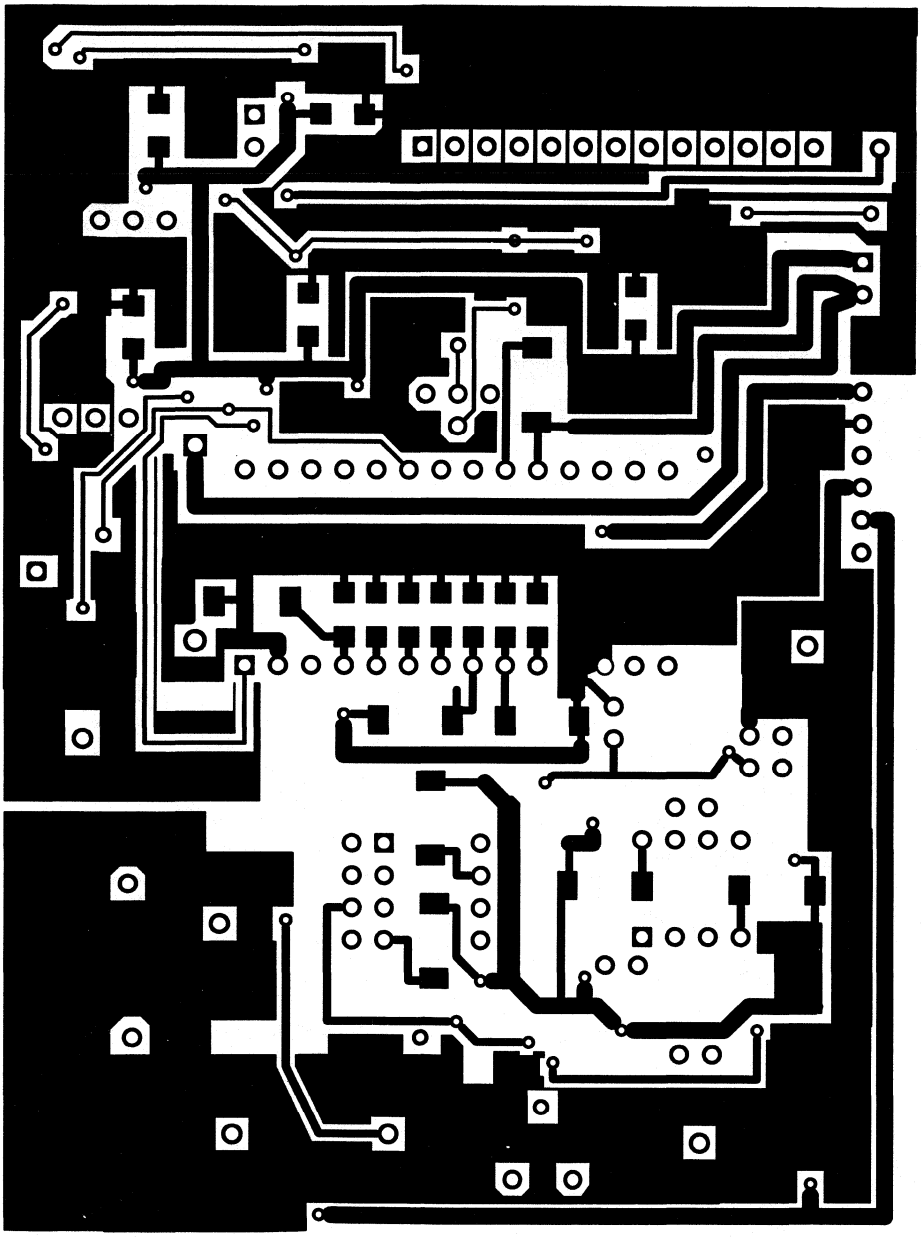

Figure 8. Bottom Trace

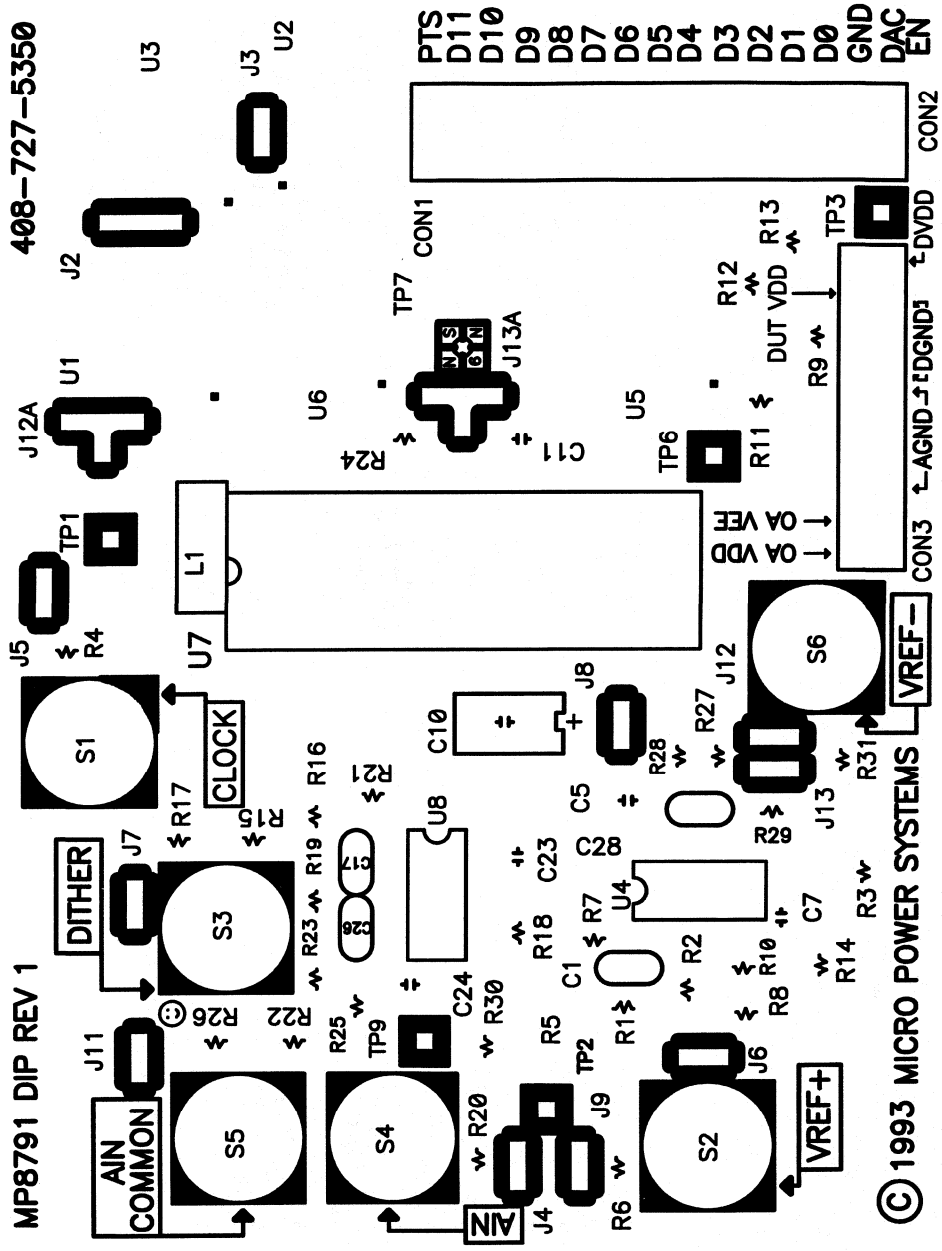

Figure 9. Top Silk

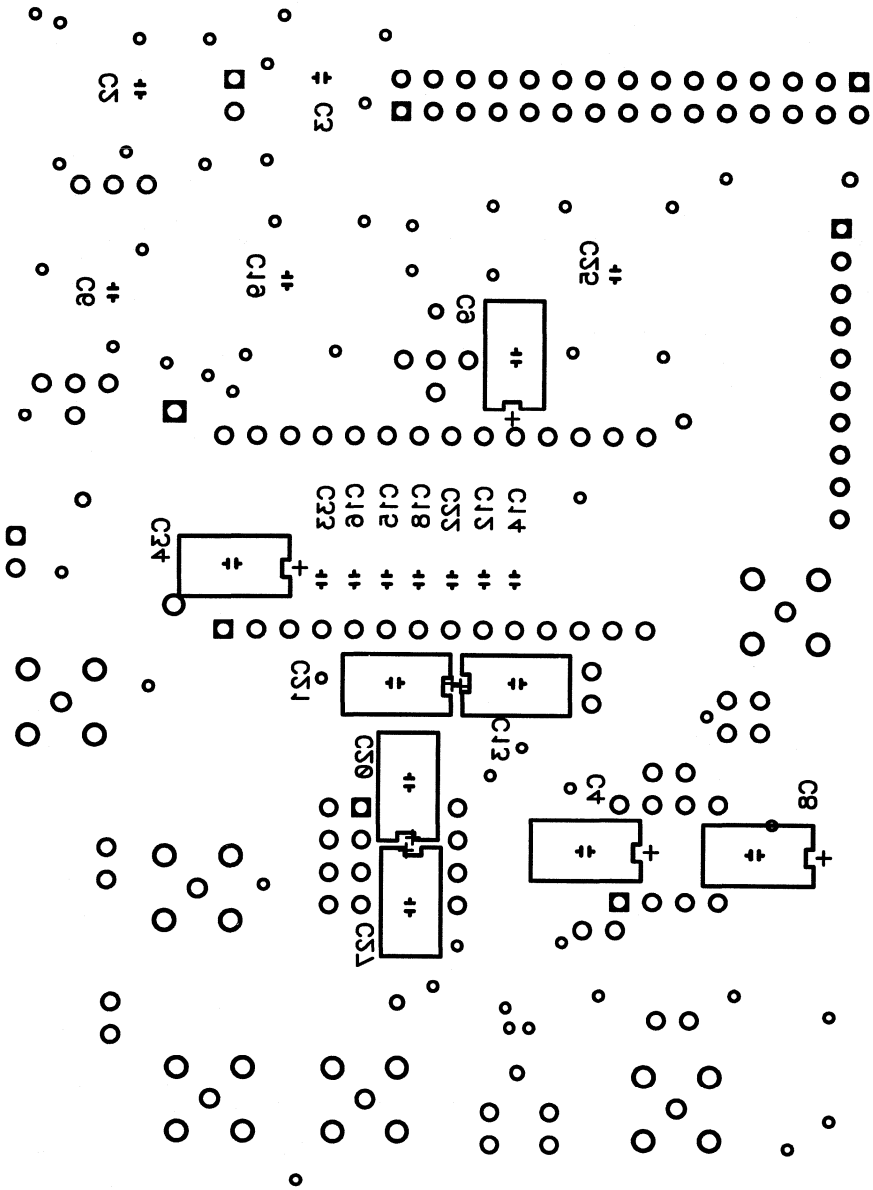

Figure 10. Bottom Silk – Top View

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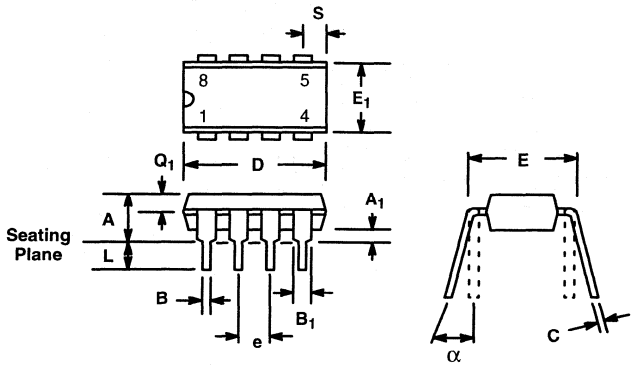
Section 9

Package Dimensions

Package Dimensions

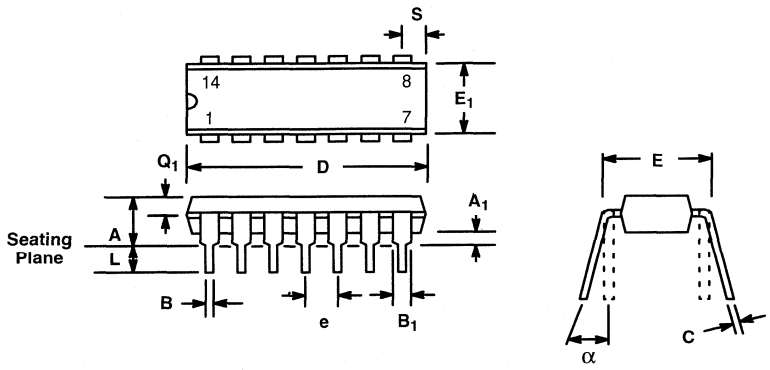
8 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N8



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.350	0.405	8.89	10.29
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.055	0.51	1.40

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

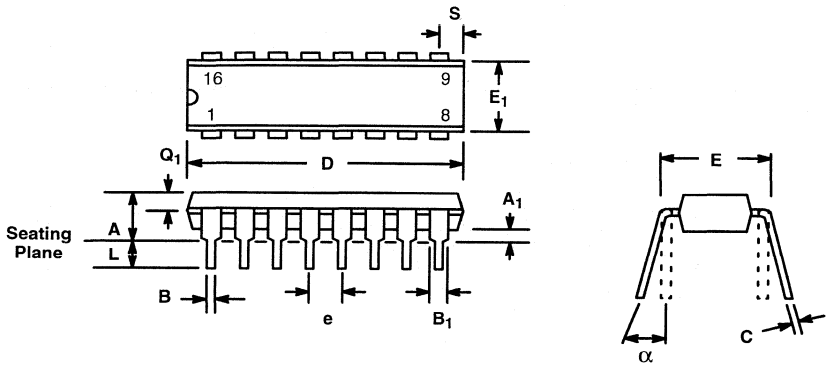
14 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N14



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.005	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.745	0.785	18.92	19.94
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.060	0.098	0.51	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

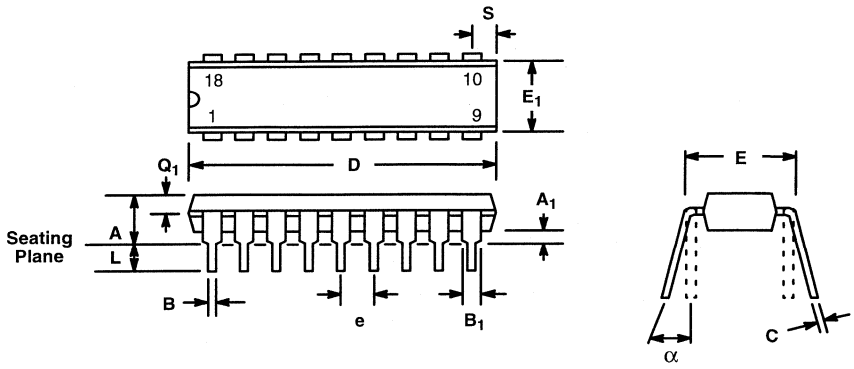
16 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N16



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.745	0.785	18.92	19.94
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.080	0.51	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

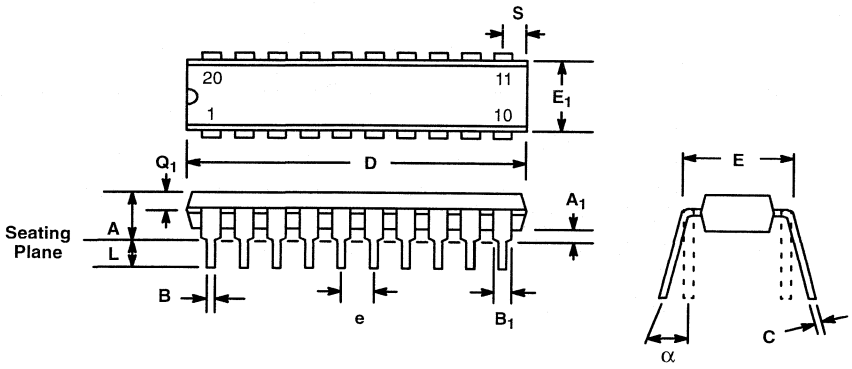
18 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N18



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.845	0.925	21.46	23.50
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.098	1.02	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

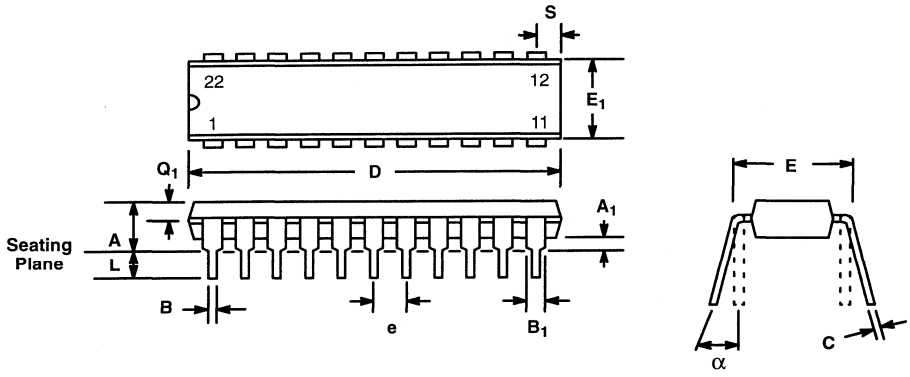
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

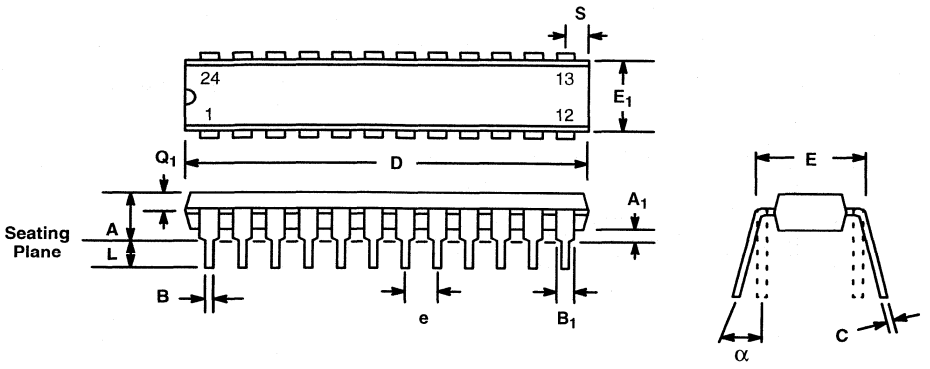
22 LEAD PLASTIC DUAL-IN-LINE
(400 MIL PDIP)
N22



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.050	1.110	26.67	28.19
E	0.385	0.425	9.78	10.80
E_1	0.330	0.380	8.38	9.65
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

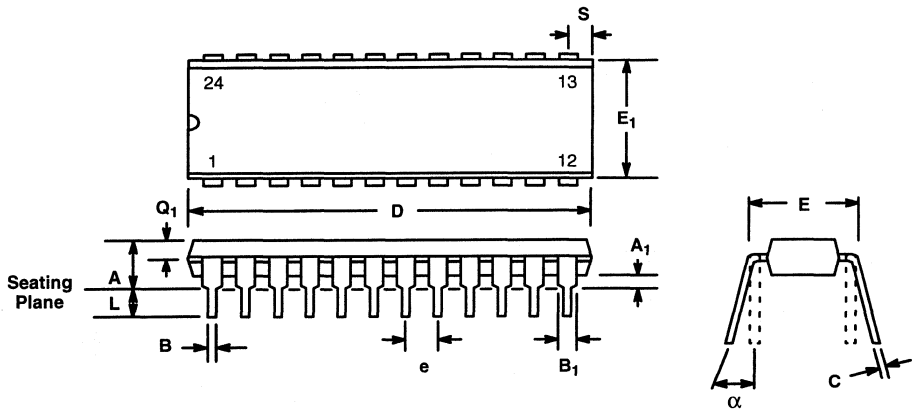
24 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.16	1.280	29.46	32.51
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.028	0.098	0.711	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

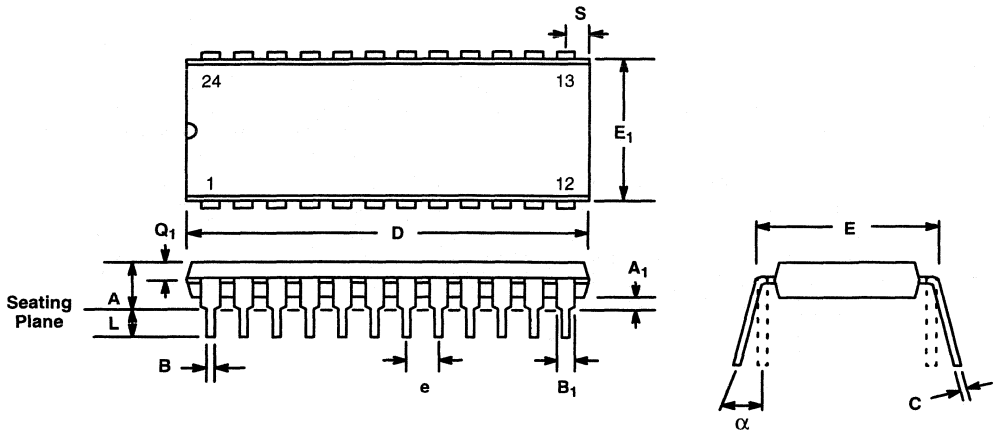
24 LEAD PLASTIC DUAL-IN-LINE
(400 MIL PDIP)
NW24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.130	0.230	3.30	5.84
A_1	0.015	—	0.381	—
B	0.014	0.024	0.356	0.6
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.18	1.26	30.0	32.0
E	0.400	0.425	10.16	10.8
E_1	0.331	0.385	8.4	9.78
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	0.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

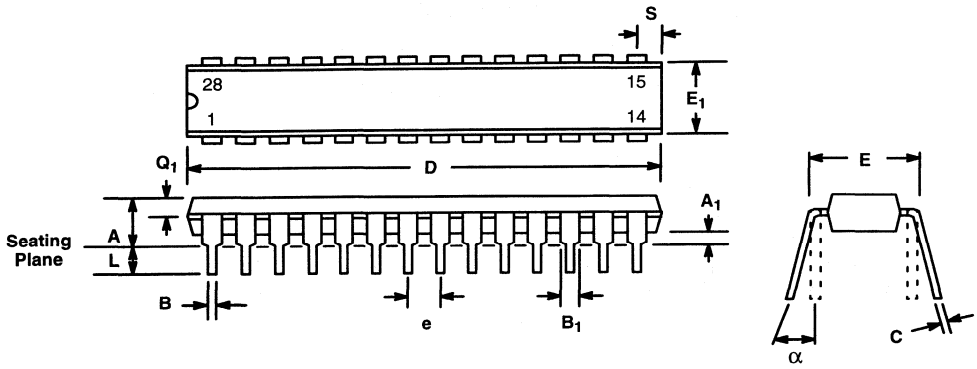
24 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.160	1.290	29.46	32.77
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.098	1.02	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

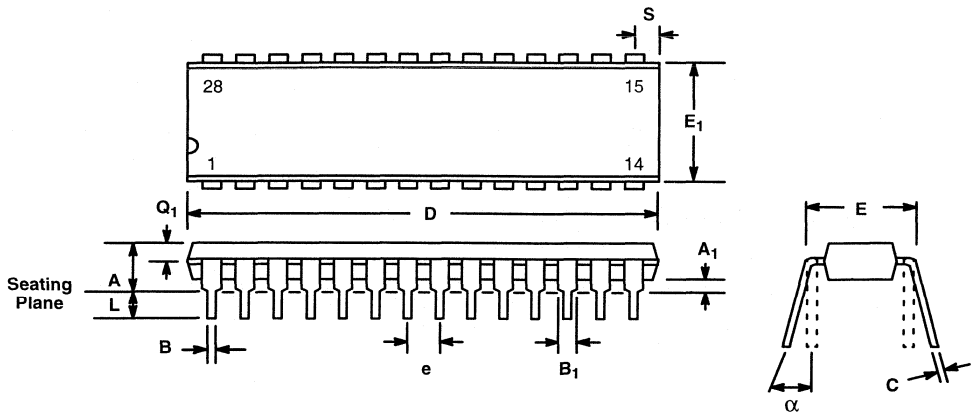
28 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.130	0.230	3.30	5.84
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.340	1.485	34.04	37.72
E	0.290	0.325	7.37	8.26
E_1	0.240	0.310	6.10	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	0.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

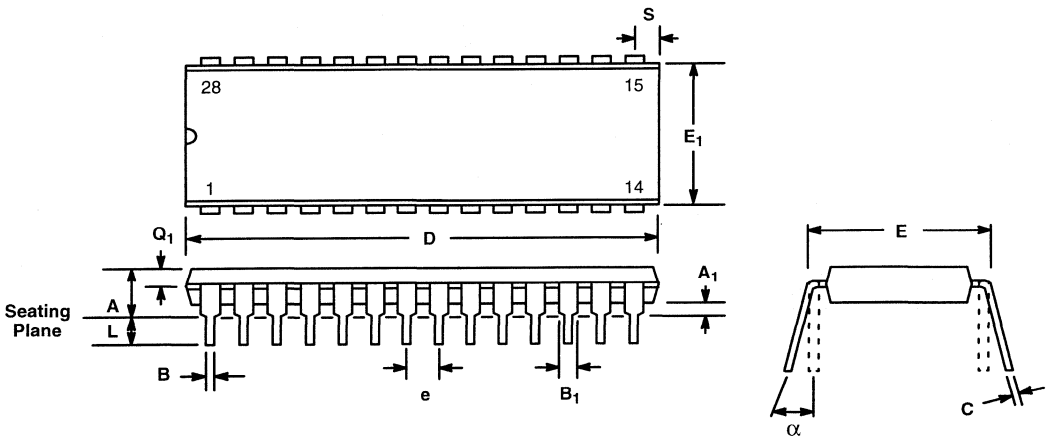
28 LEAD PLASTIC DUAL-IN-LINE
(400 MIL PDIP)
NW28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.130	0.230	3.30	5.84
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.340	1.485	34.04	37.72
E	0.400	0.425	10.16	10.8
E_1	0.265	0.385	9.27	9.78
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	0.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

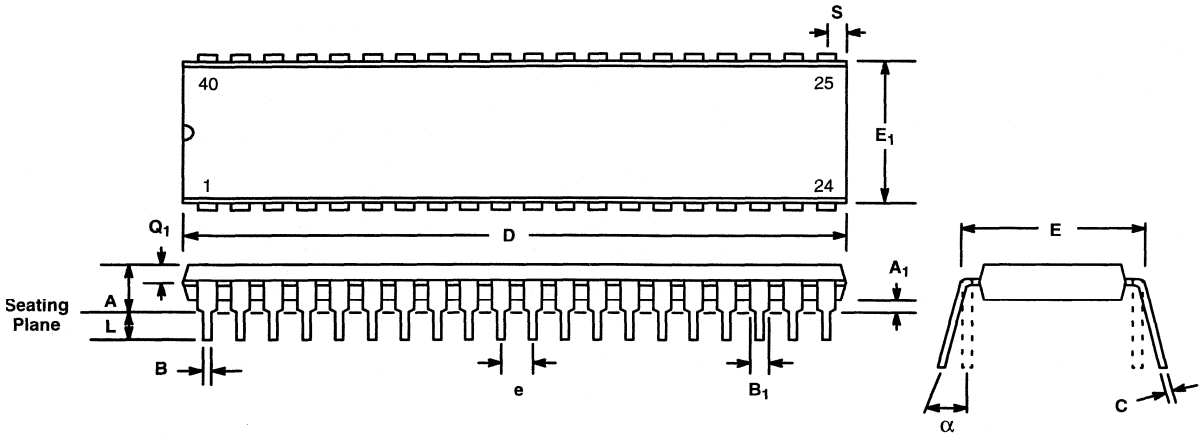
28 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.232	—	5.893
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.380	1.490	35.05	37.85
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	1.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

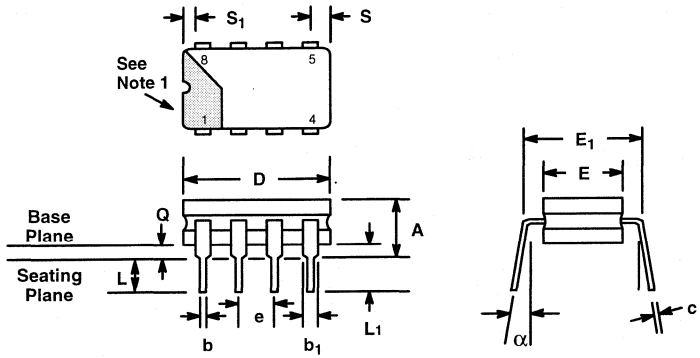
40 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N40



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.980	2.095	50.3	53.2
E	0.585	0.625	14.86	15.88
E_1	0.510	0.620	12.95	15.75
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.098	0.508	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

8 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D8



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	0.405	—	10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.055	—	1.40	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1 Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.

2 The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.

3 Dimension Q shall be measured from the seating plane to the base plane.

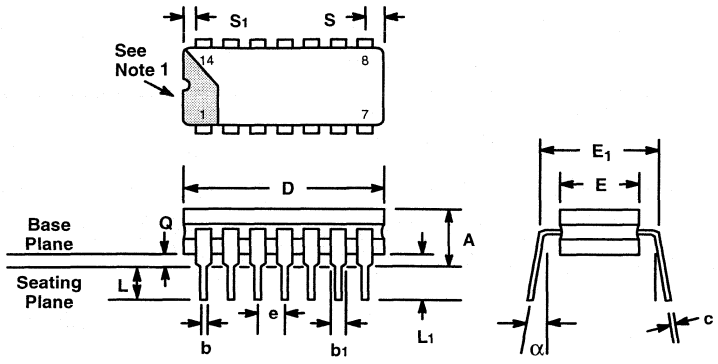
4 This dimension allows for off-center lid, meniscus and glass overrun.

5 The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.

6 Applies to all four corners.

7 This is measured to outside of lead, not center.

14 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D14

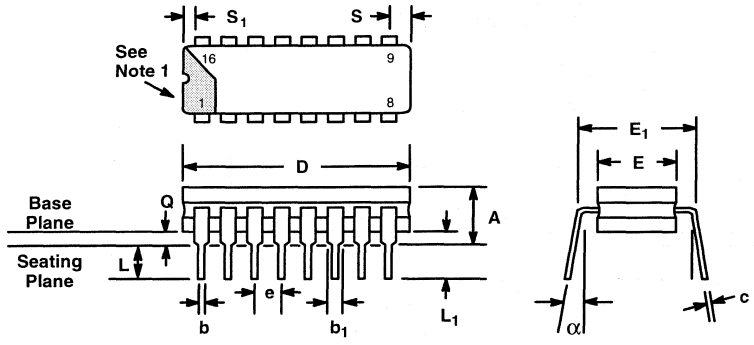


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

16 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D16

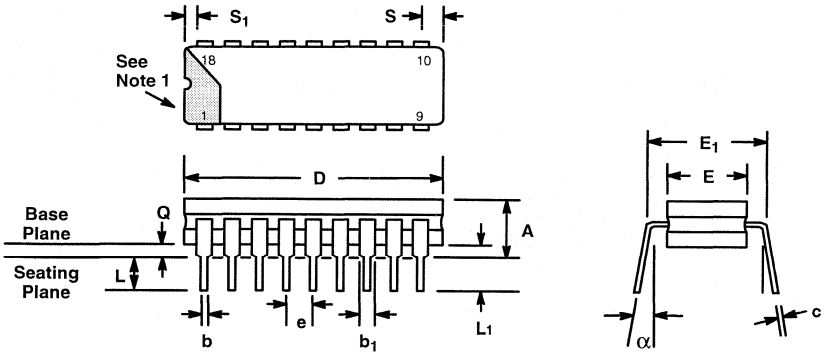


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

18 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D18

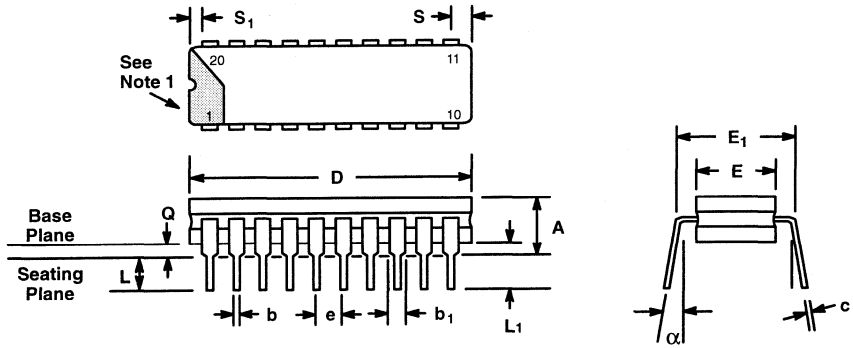


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

20 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D20

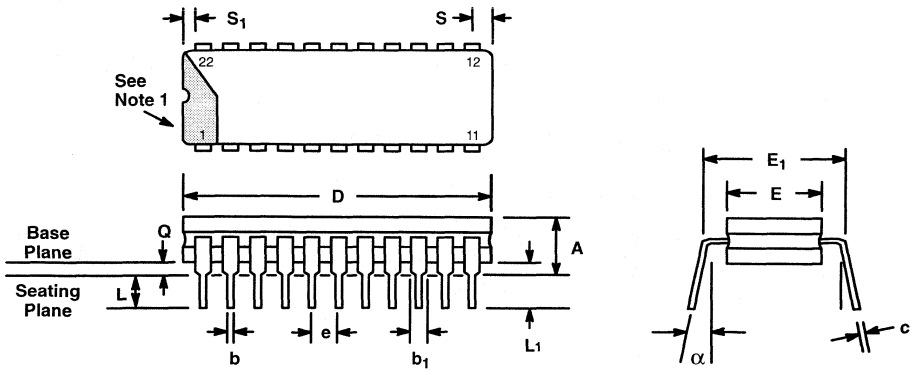


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

22 LEAD CERAMIC DUAL-IN-LINE
(400 MIL CDIP)
D22

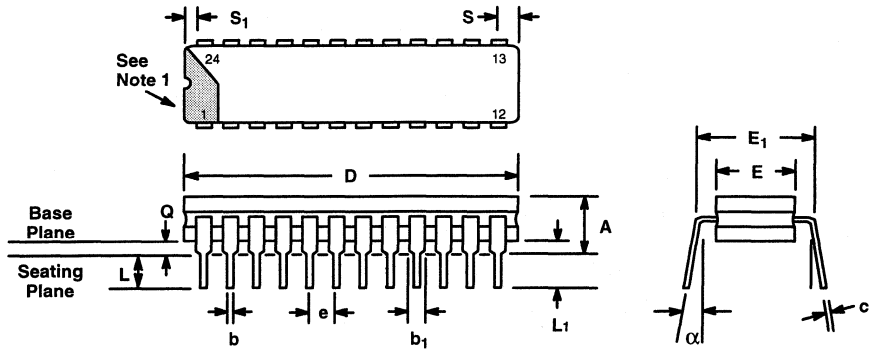


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.111	—	28.22	4
E	0.350	0.410	8.89	10.41	4
E_1	0.390	0.420	9.91	10.67	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

24 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
DN24

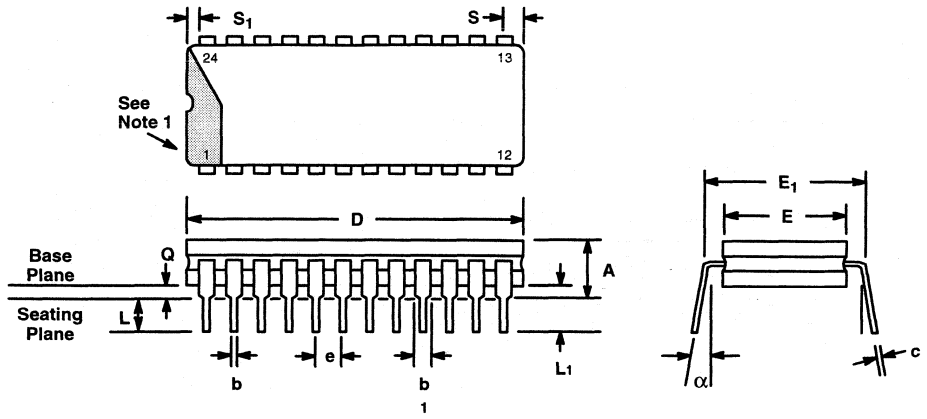


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.280	—	32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

24 LEAD CERAMIC DUAL-IN-LINE
(600 MIL CDIP)
D24

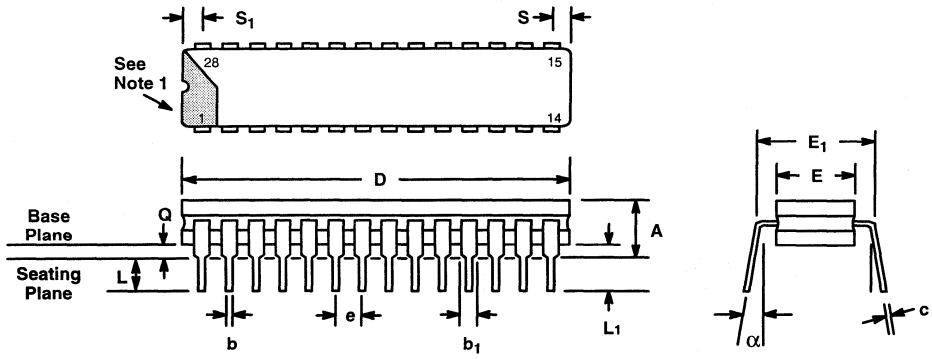


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.381	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

28 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
DN28

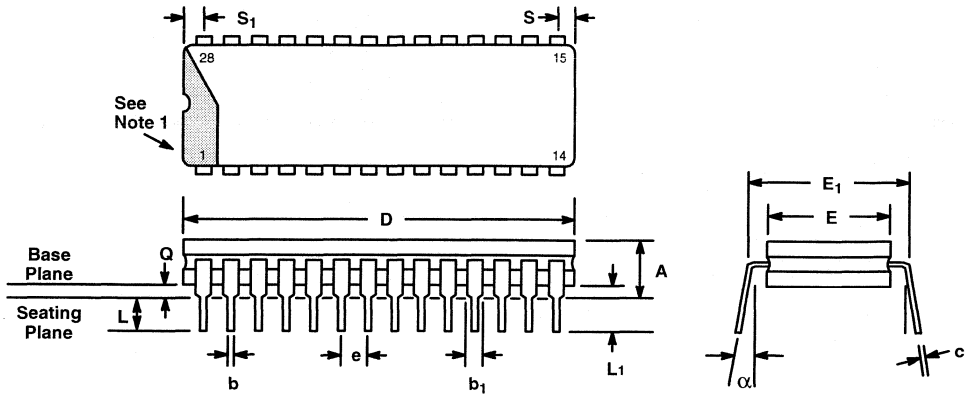


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.130	0.230	3.30	5.84	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.651	2
c	0.008	0.015	0.203	0.381	—
D	—	1.485	—	37.72	4
E	0.240	0.310	6.10	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.115	0.200	2.92	5.08	—
L_1	0.130	—	3.30	—	—
Q	0.015	0.100	0.381	2.54	3
S	—	0.100	—	2.54	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

28 LEAD CERAMIC DUAL-IN-LINE
(600 MIL CDIP)
D28

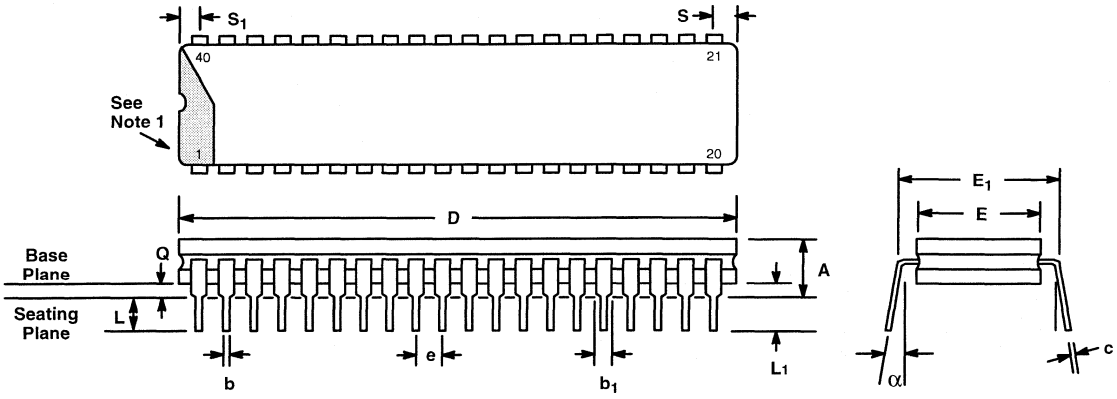


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.232	—	5.89	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.100	—	2.54	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

40 LEAD CERAMIC DUAL-IN-LINE
(600 MIL CDIP)
D40

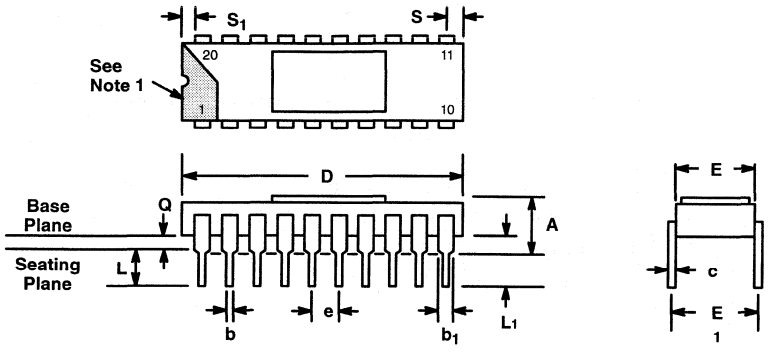


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	2.096	—	53.24	4
E	0.510	0.620	12.95	15.75	4
E_1	0.590	0.630	14.99	16.00	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

20 LEAD CERAMIC SIDE-BRAZED DUAL-IN-LINE
(300 MIL S/B DIP)
C20

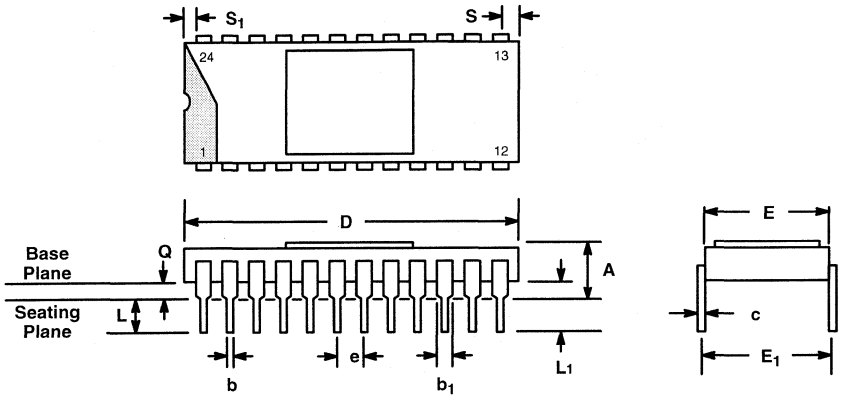


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 inch (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. E_1 shall be measured at the centerline of the leads.

24 LEAD CERAMIC SIDE-BRAZED DUAL-IN-LINE (600 MIL S/B DIP) C24

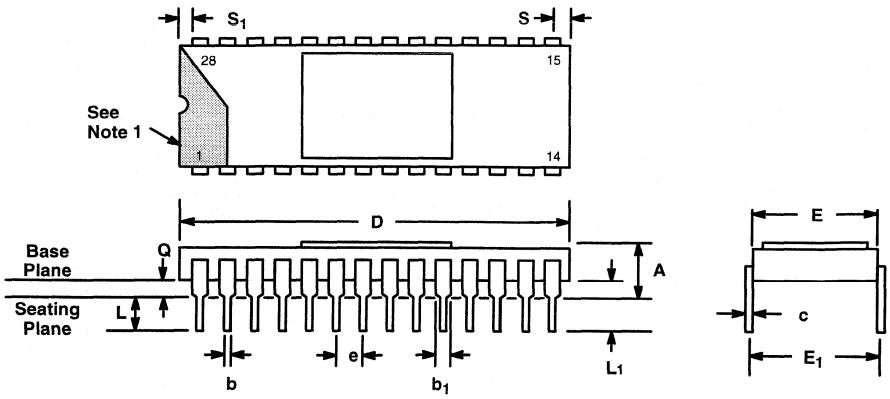


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.381	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. E_1 shall be measured at the centerline of the leads.

28 LEAD CERAMIC SIDE-BRAZED DUAL-IN-LINE (600 MIL S/B DIP) C28

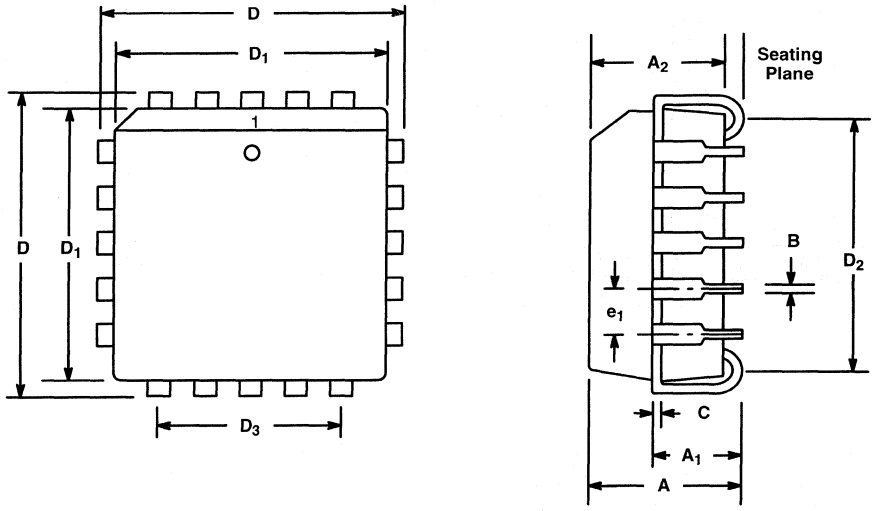


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.232	—	5.89	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.100	—	2.54	6
S_1	0.005	—	0.13	—	6

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 inch (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. E_1 shall be measured at the centerline of the leads.

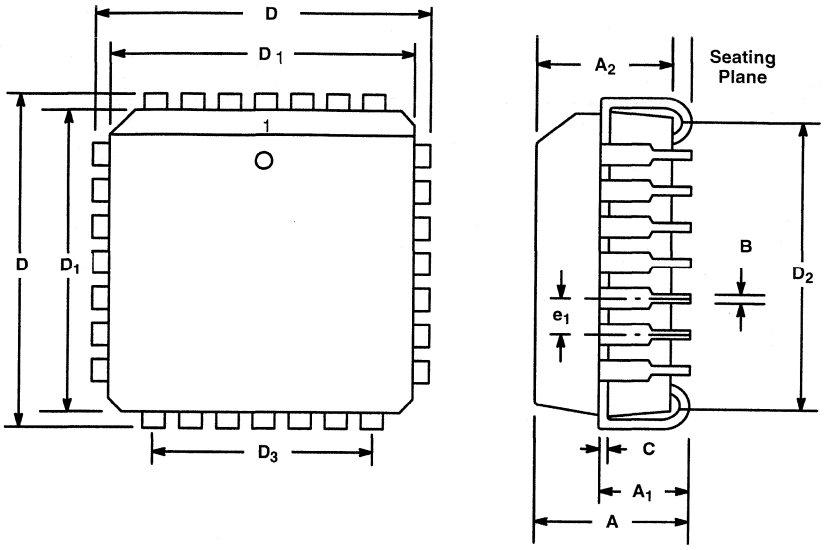
20 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.385	0.395	9.78	10.03
D_1 (1)	0.350	0.354	8.89	8.99
D_2	0.290	0.330	7.37	8.38
D_3	0.200 Ref		5.08 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

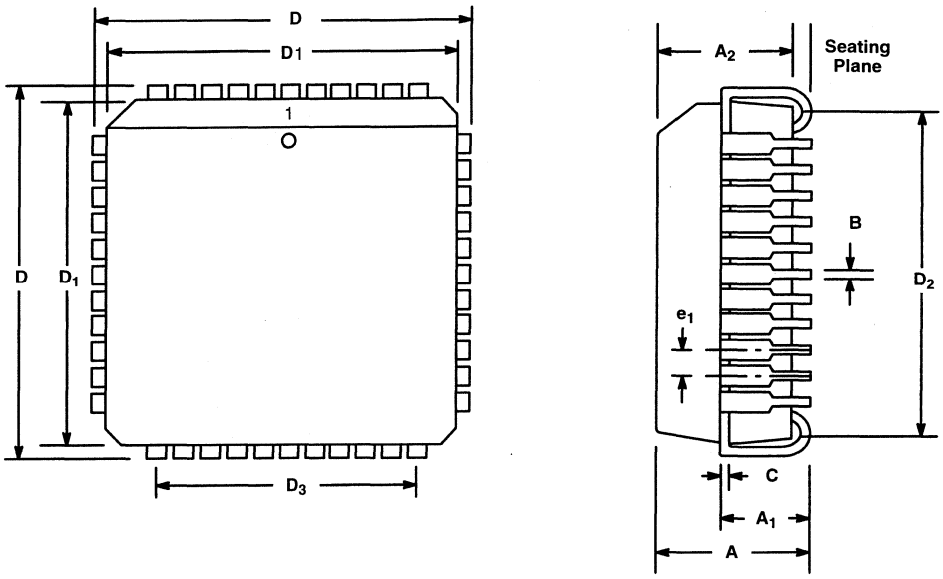
28 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.485	0.495	12.32	12.57
D_1 (1)	0.450	0.454	11.43	11.53
D_2	0.390	0.430	9.91	10.92
D_3	0.300 Ref		7.62 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

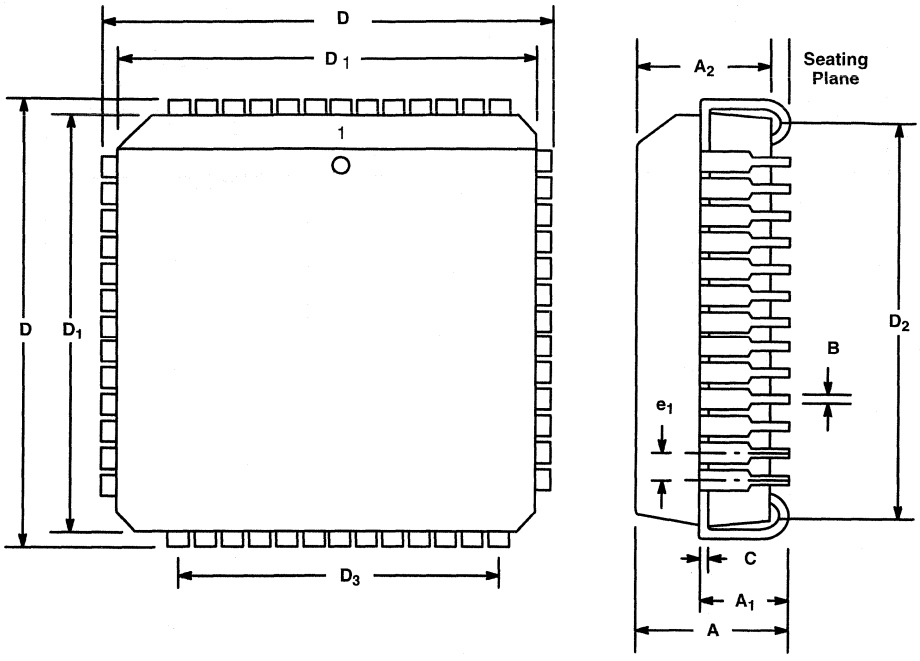
44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P44



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.553
C	0.097	0.0103	0.246	0.261
D	0.685	0.695	17.40	17.65
D_1 (1)	0.650	0.654	16.51	16.61
D_2	0590	0.630	14.99	16.00
D_3	0.500 Ref		12.70 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

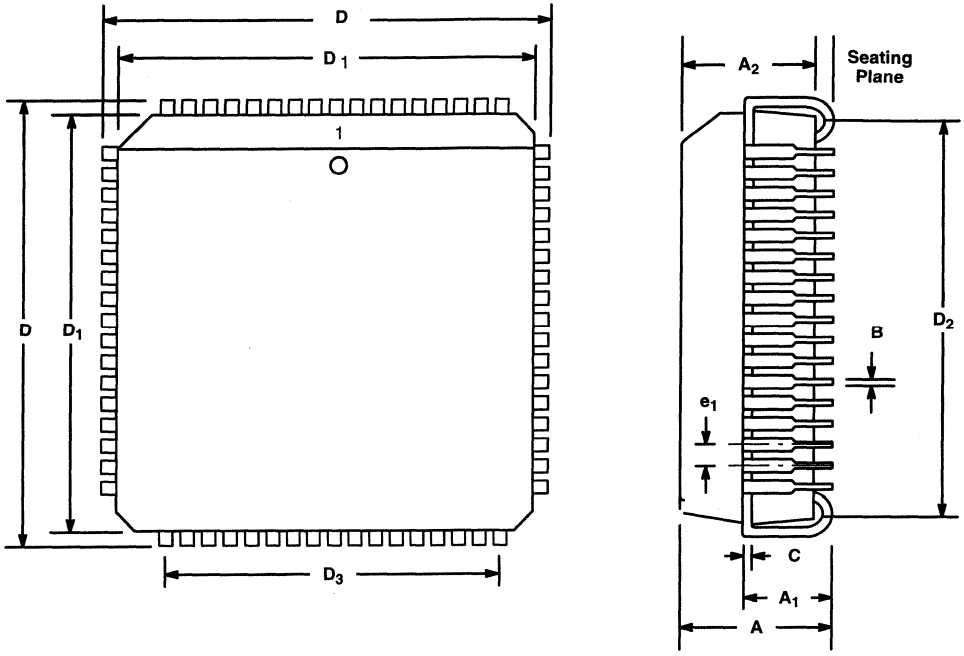
52 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P52



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.165	.180	4.19	4.57
A_1	.100	.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.553
C	0.097	0.0103	0.246	0.261
D	.785	.795	19.94	20.19
D_1 (1)	..750	.754	19.05	19.15
D_2	690	.730	17.53	18.54
D_3	0.600 Ref		15.24 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

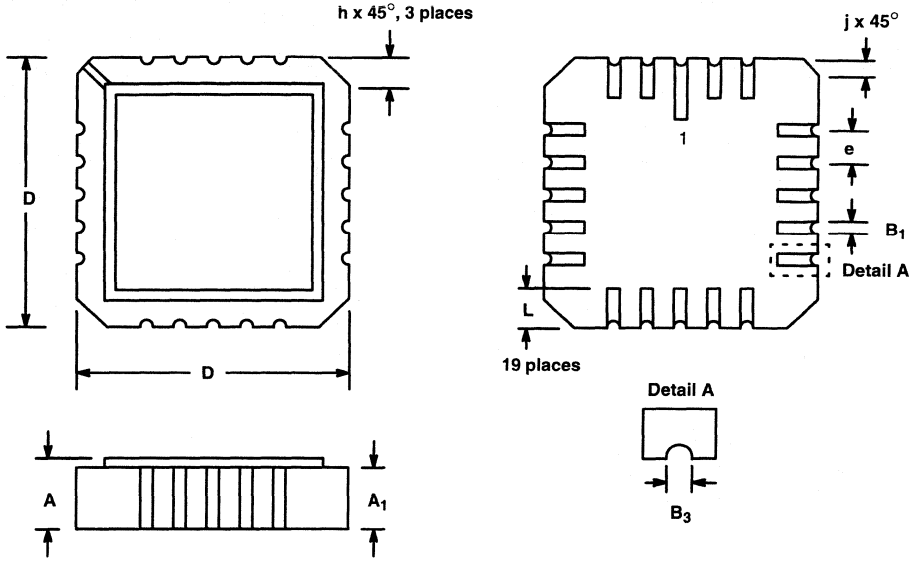
68 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P68



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.165	.180	4.19	4.57
A_1	.095	.118	2.51	3.00
A_2	0.146	0.154	3.71	3.91
B	0.013	0.021	0.330	0.553
C	0.097	0.0103	0.246	0.261
D	.985	.995	25.02	25.27
D_1 (1)	.950	.954	24.13	24.23
D_2	.890	.930	22.60	23.62
D_3	0.800 Ref		20.32 Ref.	
e_1	0.050 BSC		1.27 BSC	

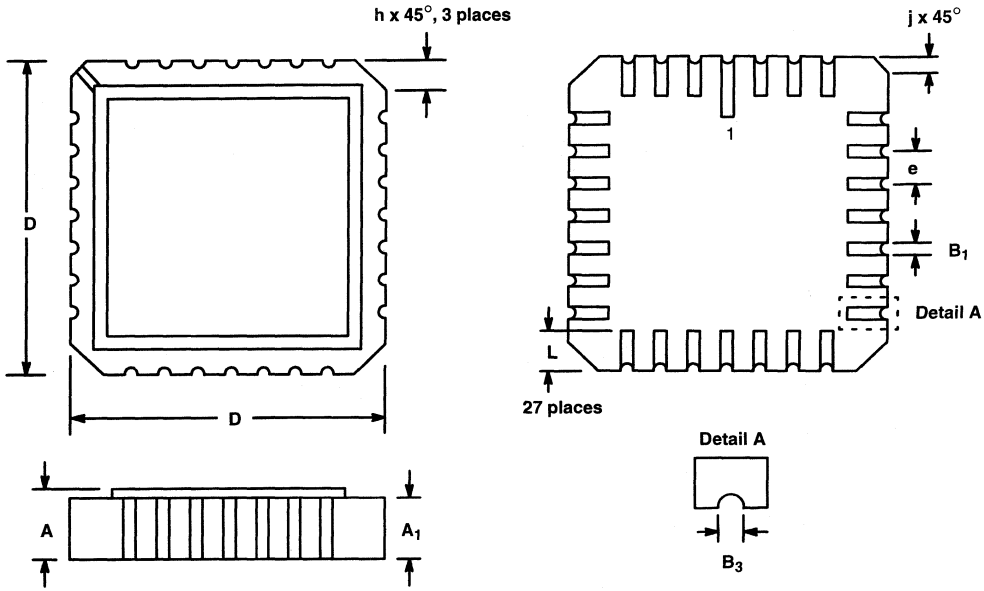
Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

20 TERMINAL LEADLESS CHIP CARRIER (LCC) L20



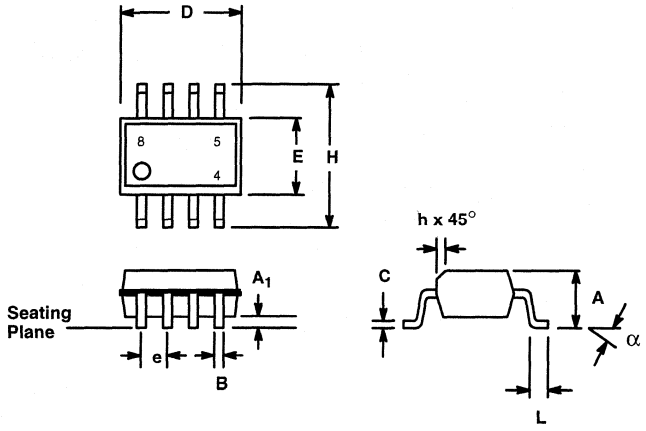
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.064	0.078	1.625	1.981
A_1	0.054	0.066	1.37	1.676
B_1	0.020	0.030	0.508	0.762
B_3	0.006	0.022	0.152	0.559
D	0.342	0.358	8.69	9.09
e	0.050 BSC		1.27 BSC	
h	0.035	0.045	0.889	1.143
j	0.015	0.025	0.381	0.635
L	0.040	0.050	1.02	1.27

28 TERMINAL LEADLESS CHIP CARRIER (LCC) L28



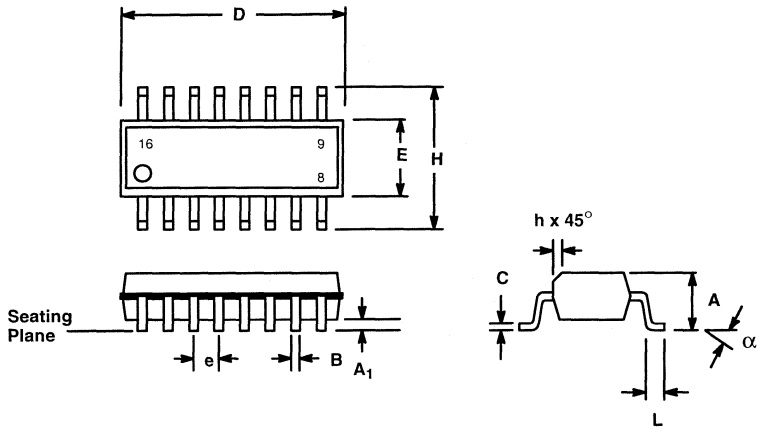
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.064	0.078	1.625	1.981
A_1	0.054	0.066	1.37	1.676
B_1	0.020	0.030	0.508	0.762
B_3	0.006	0.022	0.152	0.559
D	0.445	0.455	11.30	11.56
e	0.050 BSC		1.27 BSC	
h	0.035	0.045	0.889	1.14
j	0.015	0.025	0.381	0.635
L	0.040	0.050	1.02	1.27

8 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)
S8



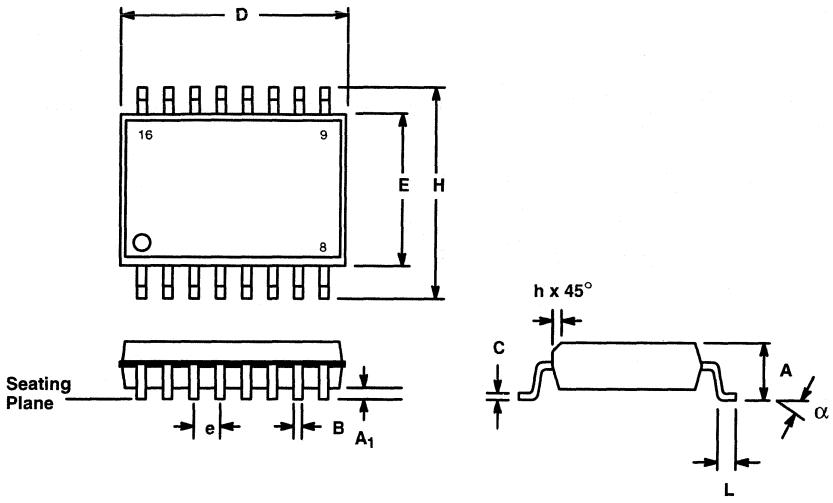
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	.068	1.55	1.73
A_1	.004	.0098	0.102	0.249
B	.0138	.0192	0.351	0.488
C	.0075	.0098	0.191	0.249
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	.230	.244	5.84	6.20
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

16 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)
SN16



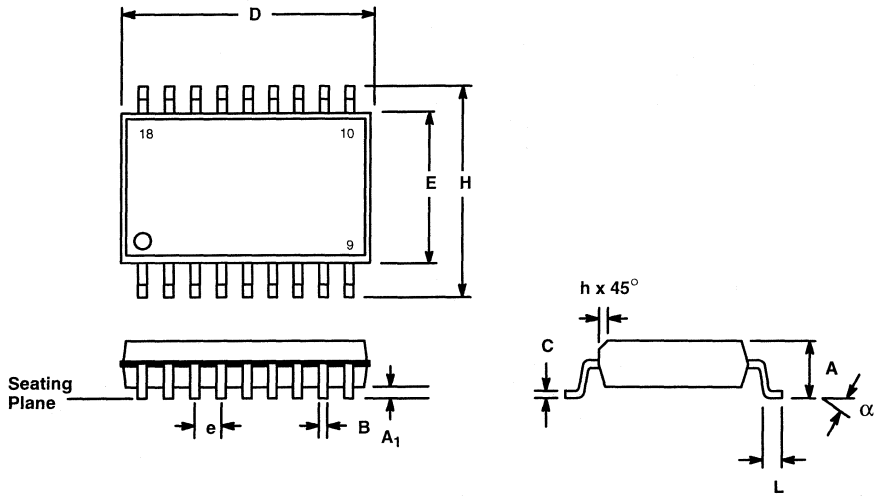
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A_1	0.004	0.0098	0.102	0.249
B	0.0138	0.0192	0.351	0.488
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.89
α	0°	8°	0°	8°

16 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S16



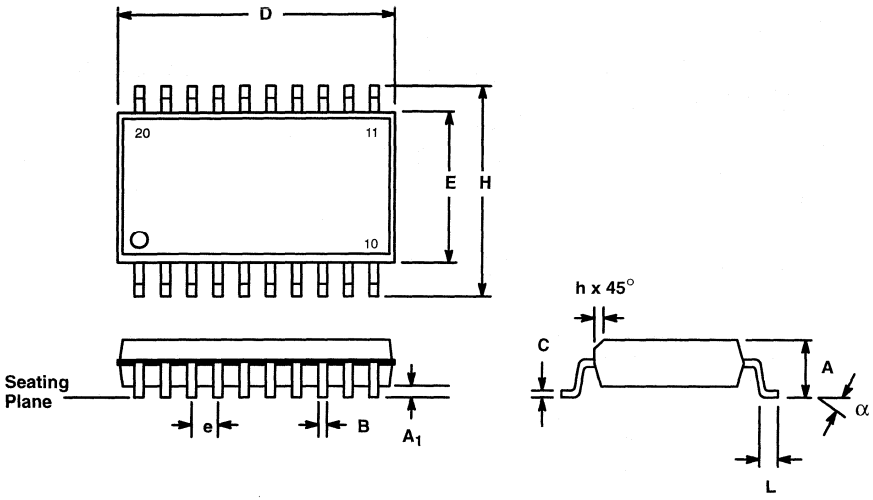
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.46	2.64
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.482
C	0.0091	0.0125	0.231	0.318
D	0.402	0.412	10.21	10.46
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

18 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S18



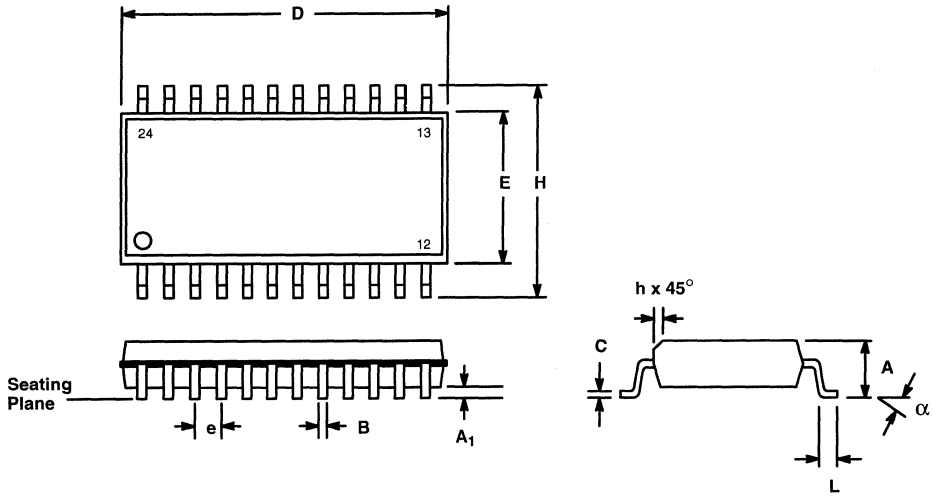
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.641
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.451	0.461	11.46	11.71
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



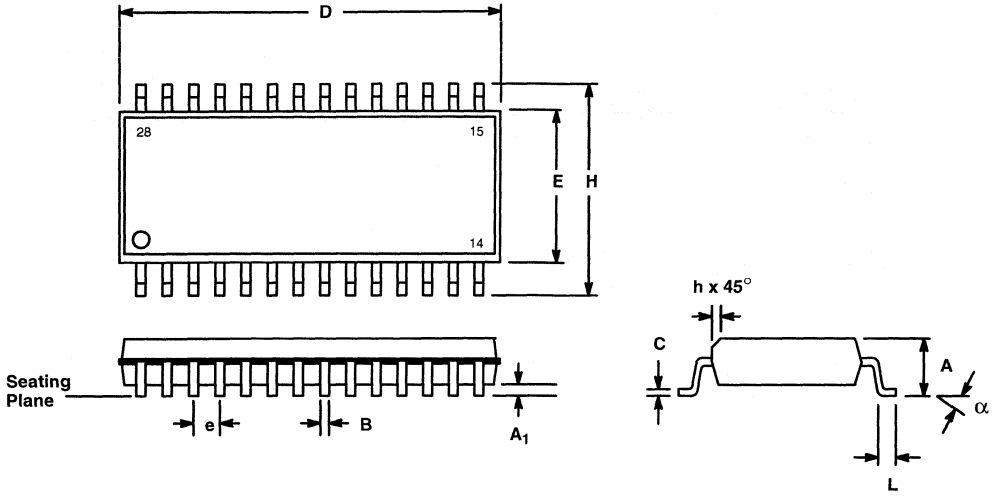
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S24



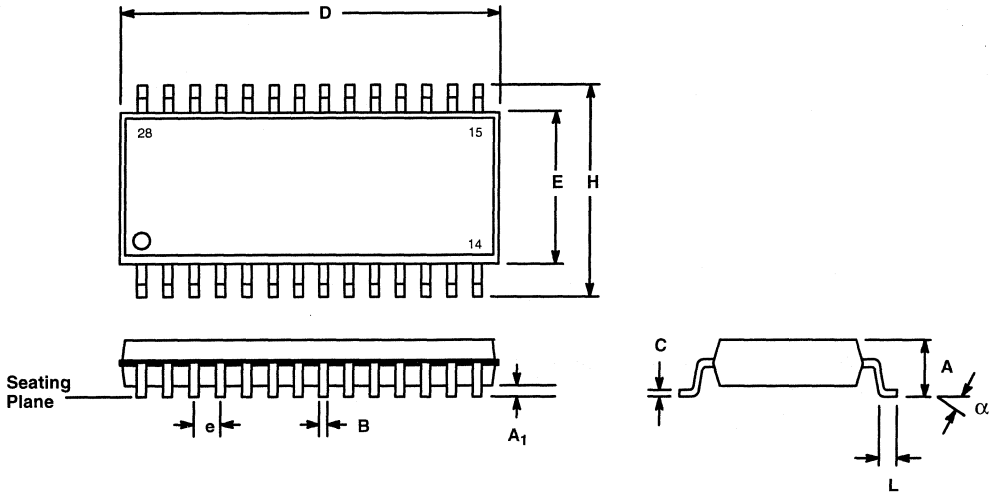
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

28 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S28



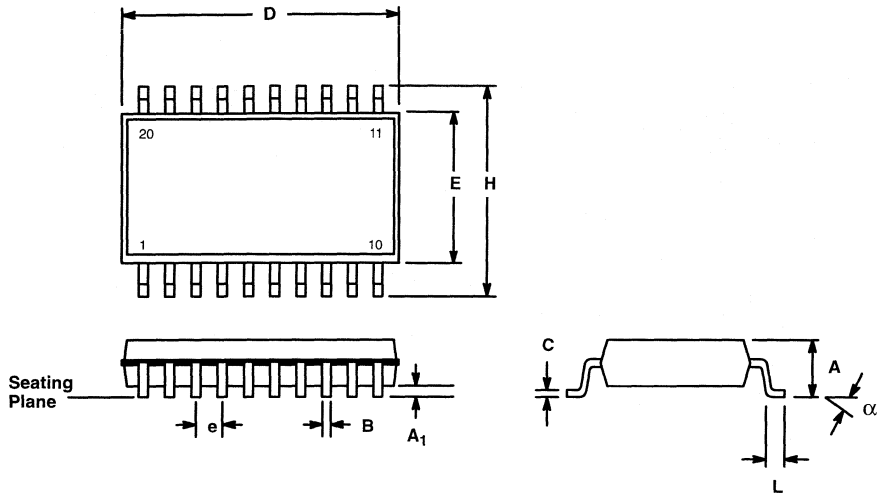
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.701	0.711	17.81	18.06
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

28 LEAD SMALL OUTLINE
(346 MIL JEDEC SOIC)
SW28



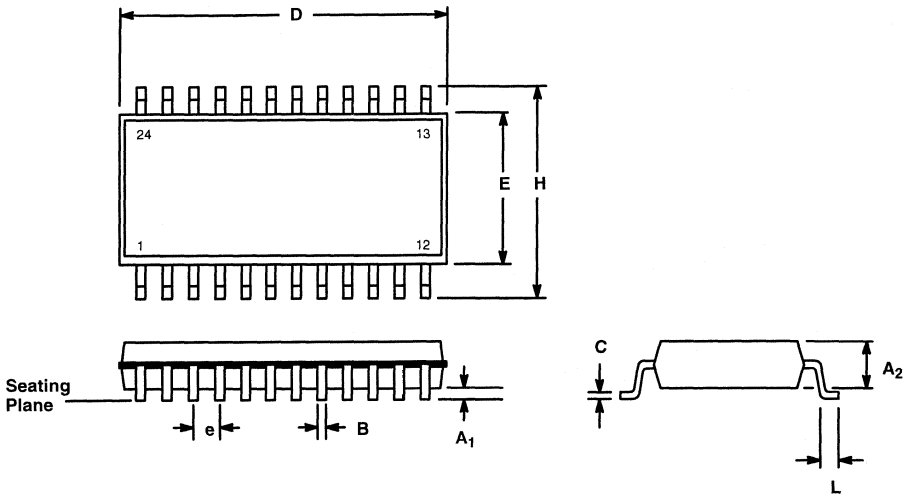
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.090	0.100	2.286	2.54
A1	0.004	0.010	0.102	0.279
B	0.014	0.020	0.356	0.508
C	0.006	0.0125	0.152	0.318
D	0.706	0.718	17.93	18.24
E	0.340	0.350	8.64	8.89
e	0.050 BSC		1.27 BSC	
H	0.463	0.477	11.76	12.12
h	0.010	0.016	0.254	0.406
L	0.020	0.042	0.406	0.889
α	0°	8°	0°	8°

20 LEAD SMALL OUTLINE PACKAGE
(300 MIL EIAJ SOIC)
RN20



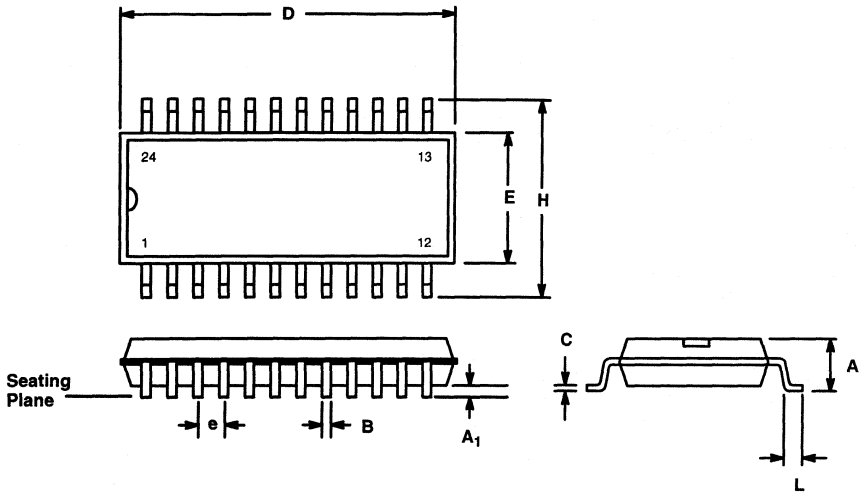
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.92	2.28	0.075	0.090
A_1	0.02	0.18	0.001	0.007
B	0.25	0.55	0.01	0.022
C	0.13	0.20	0.005	0.008
D	12.7	13.1	0.50	0.516
E	6.3	6.7	0.248	0.264
e	1.27 BSC		0.05 BSC	
H	9.45	10.15	0.372	0.4
L	0.40	0.80	0.024	0.031
α	0°	5°	0°	5°

24 LEAD SMALL OUTLINE PACKAGE
(300 MIL EIAJ SOIC)
RN24



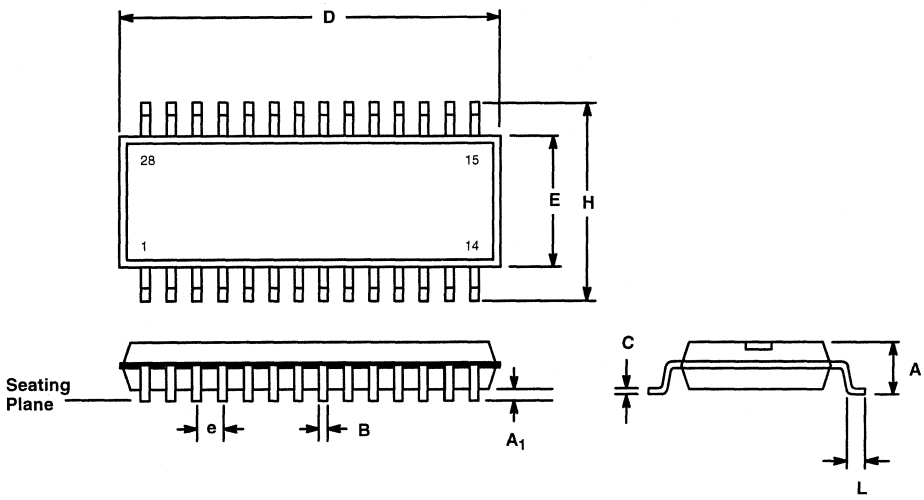
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A_2	1.7	1.9	0.067	0.075
A_1	0.0	0.1	0.000	0.004
B	0.3	0.5	0.012	0.02
C	0.1	0.25	0.004	0.01
D	14.9	15.5	0.588	0.608
E	5.2	5.6	0.205	0.221
e	1.27 BSC		0.05 BSC	
H	7.5	8.1	0.297	0.317
L	0.3	0.7	0.012	0.028

24 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R24



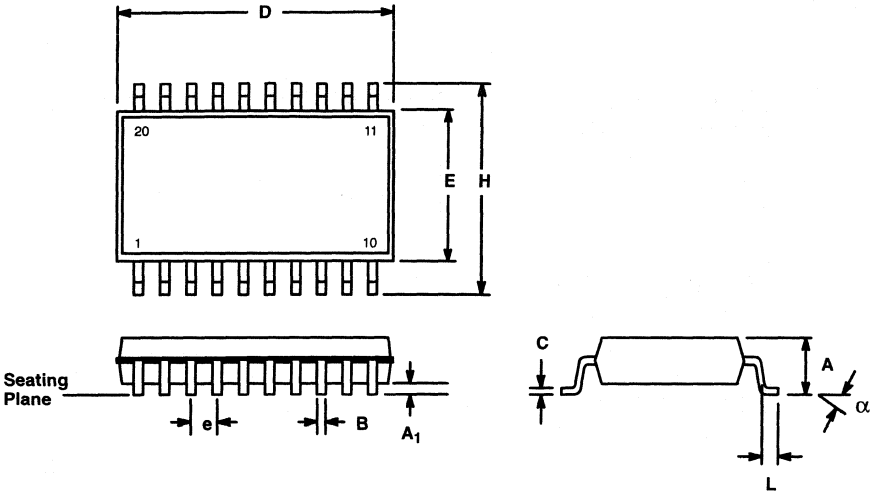
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.50	.012	0.020
C	0.10	0.20	0.004	0.008
D	15.0	15.4	0.590	0.606
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

28 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R28



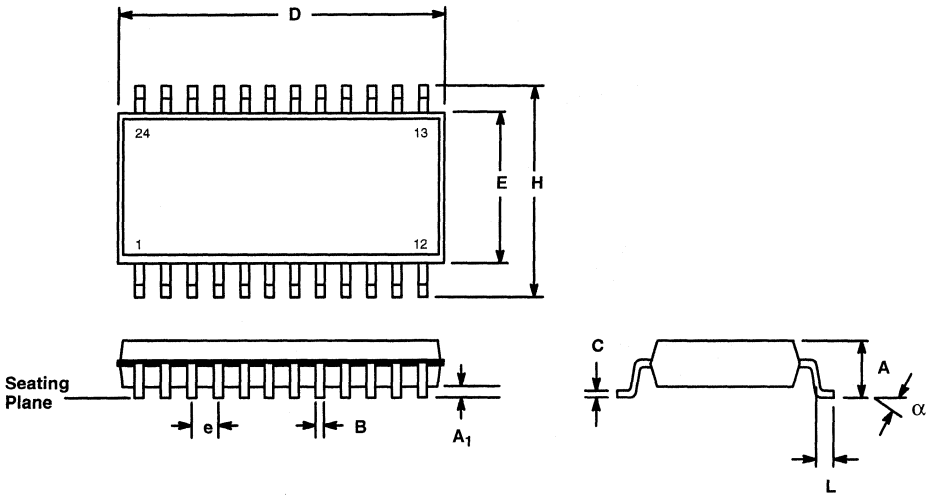
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A_1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

20 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP) A20



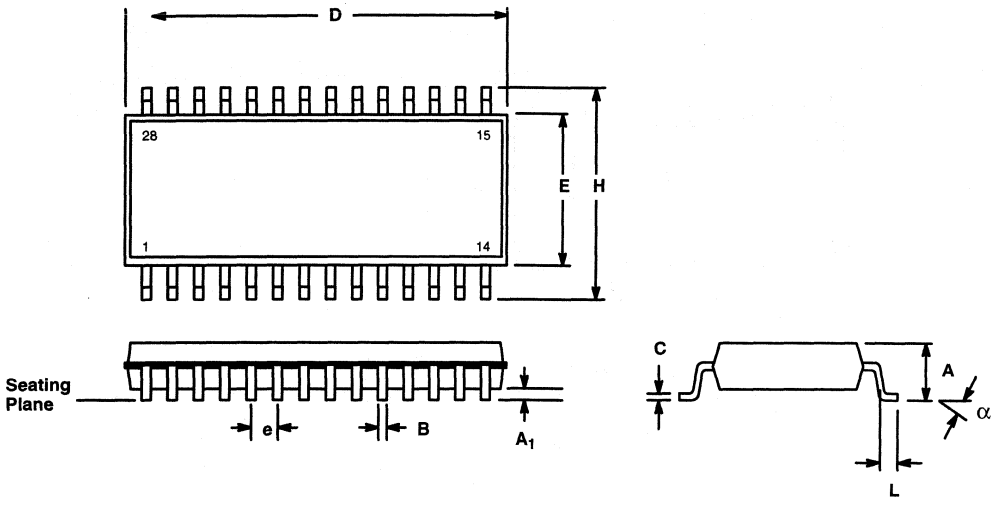
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	7.07	7.40	0.278	0.291
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

24 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP) A24



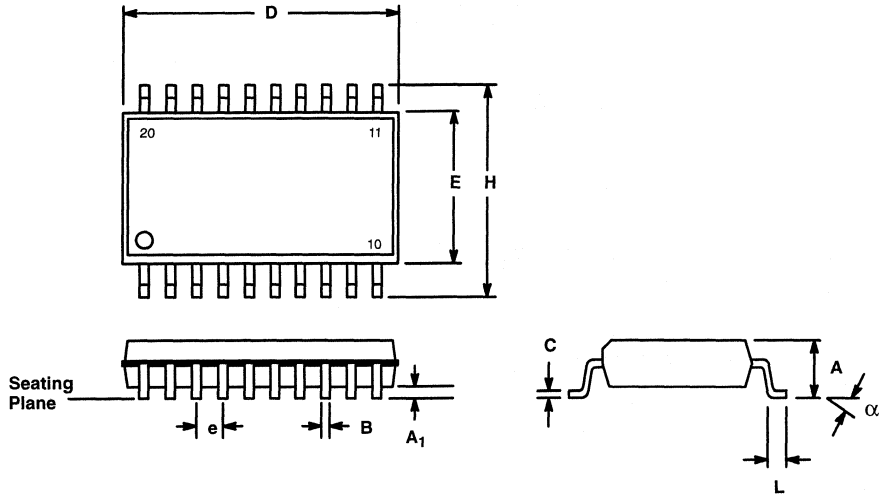
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	8.07	8.40	0.318	0.331
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

28 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP) A28



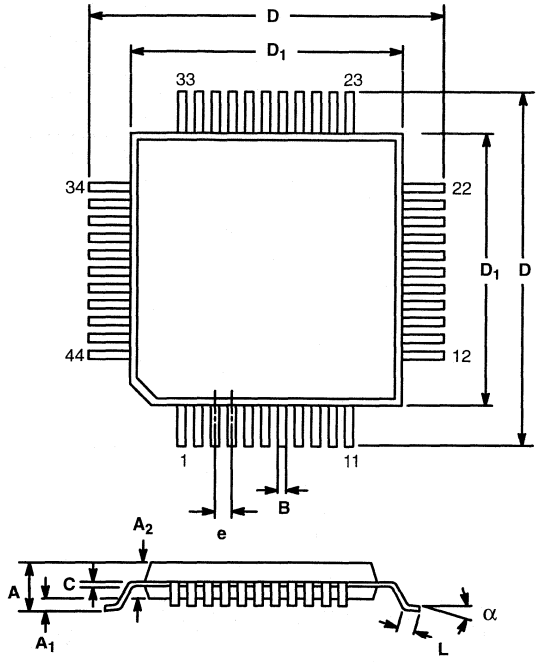
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	10.07	10.40	0.397	0.409
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

20 LEAD THIN SHRUNK SMALL OUTLINE
(300 MIL TSSOP)
B20



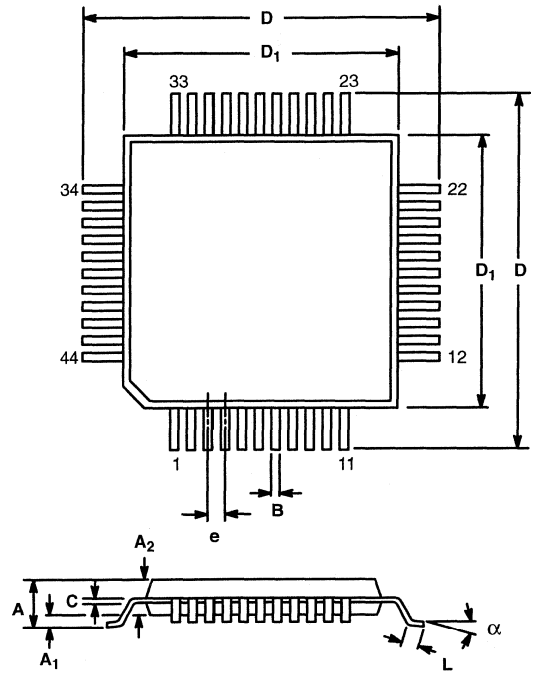
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	1.00	—	0.0394
A_1	0.05	0.15	0.002	0.006
B	0.18	0.30	0.0071	0.0118
C	0.09	0.18	0.0035	0.0071
D	6.4	6.6	0.252	0.26
E	4.3	4.48	0.169	0.176
e	0.65 BSC		0.0256 BSC	
H	6.25	6.50	0.246	0.256
L	0.5	0.7	0.02	0.028
α	0°	8°	0°	8°

44 LEAD PLASTIC QUAD FLAT PACK
(14mm x 14mm PQFP, METRIC)
Q44



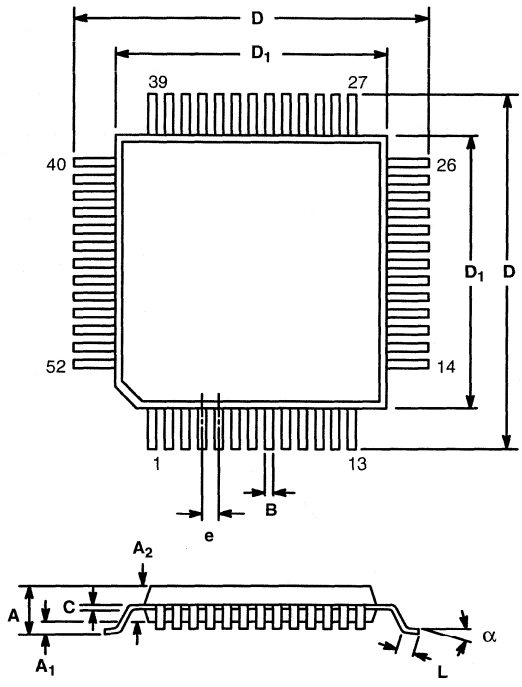
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.1	0.547	0.555
e	1.00 BSC		0.039 BSC	
L	0.65	1.03	0.026	0.040
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

44 LEAD PLASTIC QUAD FLAT PACK
(10mm X 10mm PQFP, METRIC)
QN44



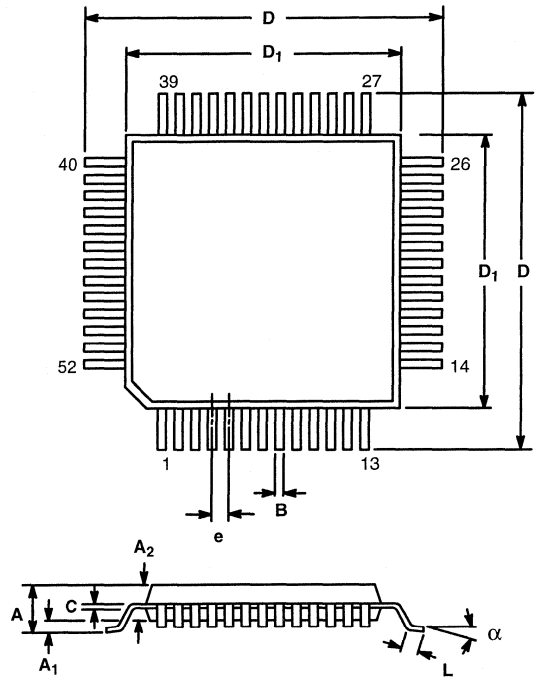
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.45	—	0.096
A_1	0.25	—	0.01	—
A_2	1.9	2.1	0.100	0.108
B	0.3	0.4	0.012	0.018
C	0.13	0.23	0.005	0.009
D	12.95	13.45	0.510	0.530
D_1	9.9	10.1	0.392	0.396
e	0.8 BSC		0.0315 BSC	
L	0.65	1.03	0.026	0.037
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

52 LEAD PLASTIC QUAD FLAT PACK
(14mm x 14mm PQFP, METRIC)
Q52



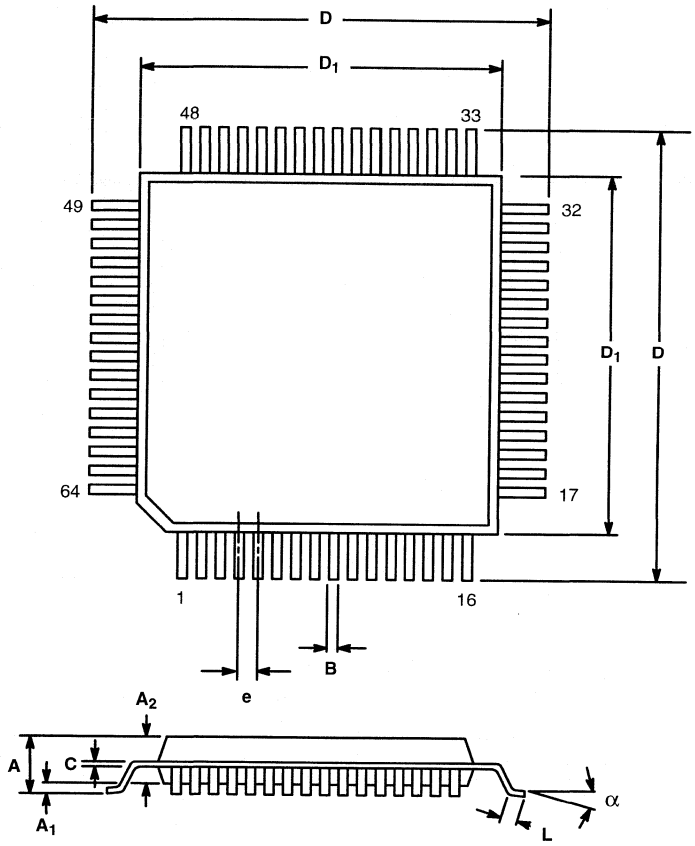
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.10	0.547	0.555
e	1.00 BSC		0.0394 BSC	
L	0.65	1.03	0.026	0.04
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

52 LEAD PLASTIC QUAD FLAT PACK
(10mm x 10mm PQFP, METRIC)
QN52



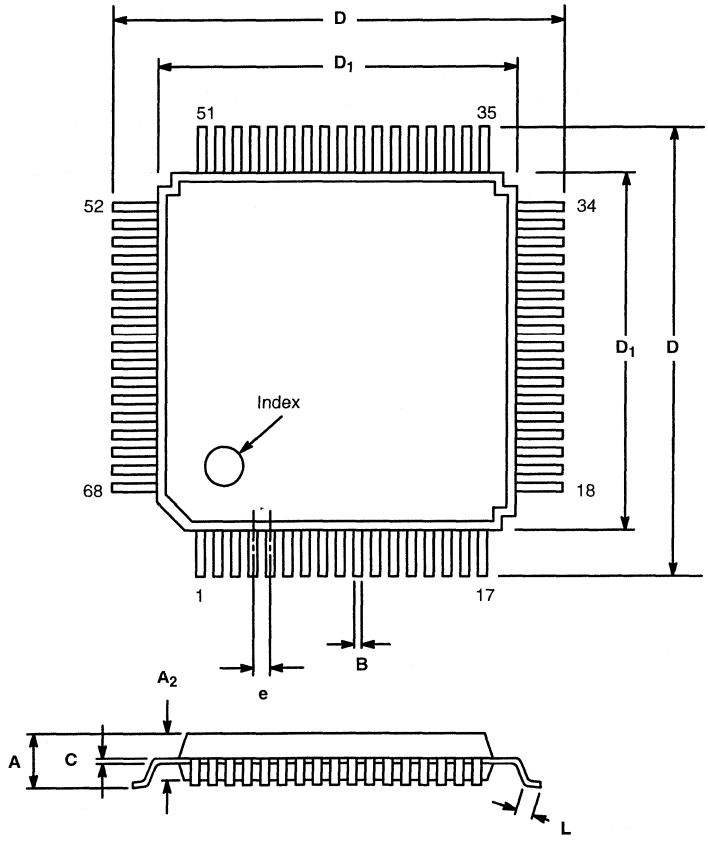
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.45	—	0.096
A_1	0.25	—	0.01	—
A_2	1.9	2.1	0.075	0.083
B	0.22	0.38	0.009	0.015
C	0.13	0.23	0.005	0.009
D	12.95	13.45	0.51	0.53
D_1	9.9	10.1	0.39	0.398
e	0.65 BSC		0.0256 BSC	
L	0.65	1.03	0.0026	0.041
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

64 LEAD PLASTIC QUAD FLAT PACK
(14mm x 14mm PQFP, METRIC)
Q64



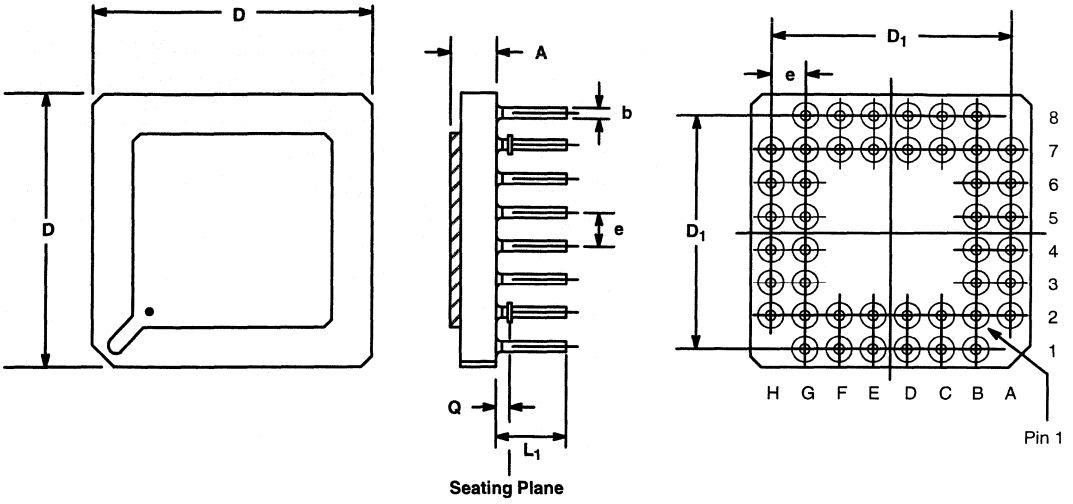
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.1	0.547	0.555
e	0.80 BSC		0.0315 BSC	
L	0.65	1.03	0.026	0.040
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

68 LEAD CERAMIC QUAD FLAT PACK
(CQFP)
F68



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.117	0.155	2.97	3.94
A_2	0.113	0.143	2.87	3.63
B	0.010	0.014	0.254	0.356
C	0.004	0.010	0.10	0.25
D	0.725	0.741	18.4	18.8
D_1	0.544	0.556	13.8	14.1
e	0.025 BSC		0.635 BSC	
L	0.052	0.068	1.32	1.73

44 LEAD PIN GRID ARRAY
(PGA)
G44

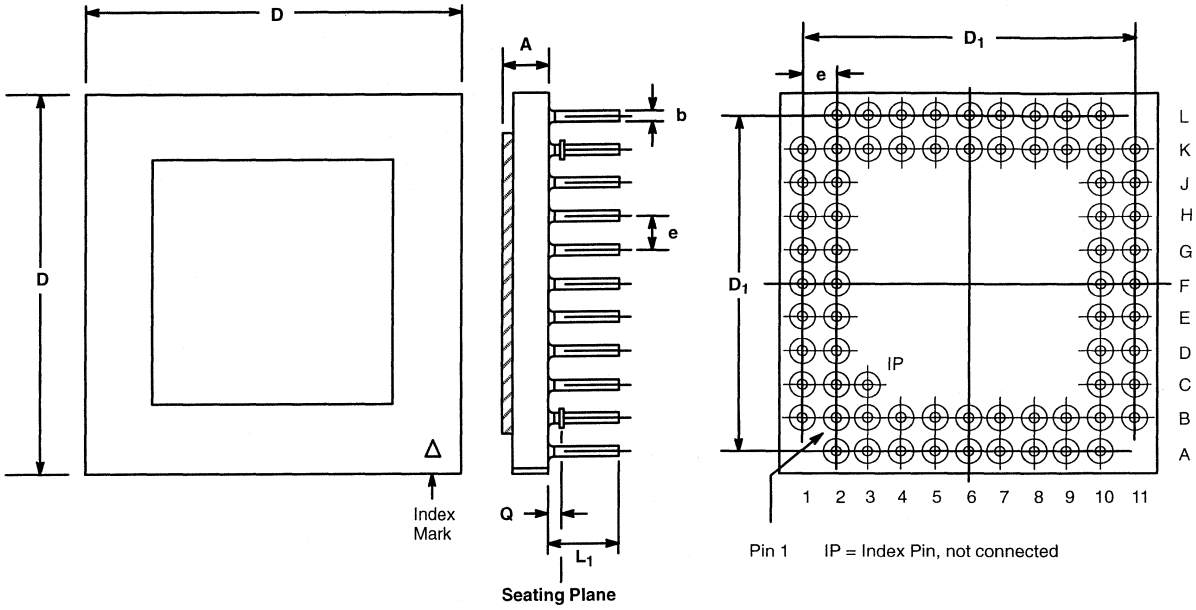


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.082	0.10	2.08	2.54
b	0.016	0.020	0.406	0.508
D	0.841	0.859	21.4	21.8
D_1	0.688	0.712	17.5	18.1
e	0.100 typ.		2.54 typ.	
L_1	0.170	0.190	4.32	4.83
Q	0.050 typ.		1.27 typ.	

CONNECTION TABLE					
PAD	PIN	PAD	PIN	PAD	PIN
1	B2	16	G4	31	C8
2	B1	17	H4	32	C7
3	C2	18	H5	33	B8
4	C1	19	G5	34	B7
5	D2	20	H6	35	A7
6	D1	21	G6	36	B6
7	E1	22	H7	37	A6
8	E2	23	G7	38	B5
9	F1	24	G8	39	A5
10	F2	25	F7	40	A4
11	G1	26	F8	41	B4
12	G2	27	E7	42	A3
13	H2	28	E8	43	B3
14	G3	29	D8	44	A2
15	H3	30	D7		

Note: The letters A-H and numbers 1-8 are the coordinates of a grid. For example, pin 1 is at the intersections of the "B" vertical line and the "2" horizontal line.

68 LEAD PIN GRID ARRAY
(PGA)
G68

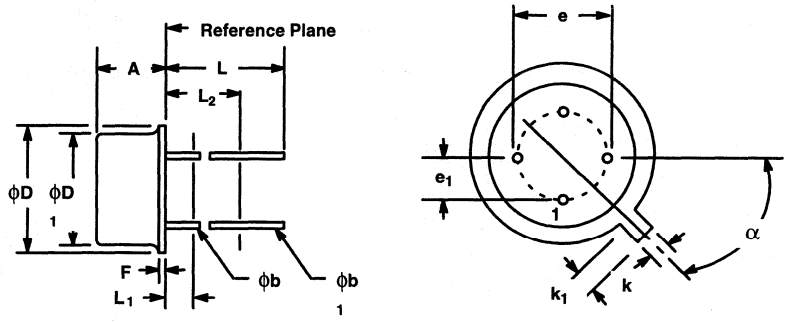


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.079	0.095	2.00	2.41
b	0.016	0.020	0.406	0.508
D	1.086	1.110	27.6	28.2
D_1	0.788	0.812	20.0	20.6
e	0.100 typ.		2.54 typ.	
L_1	0.170	0.190	4.32	4.83
Q	0.050 typ.		1.27 typ.	

CONNECTION TABLE							
PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN
1	B2	18	K2	35	K10	52	B10
2	B1	19	L2	36	K11	53	A10
3	C2	20	K3	37	J10	54	B9
4	C1	21	L3	38	J11	55	A9
5	D2	22	K4	39	H10	56	B8
6	D1	23	L4	40	H11	57	A8
7	E2	24	K5	41	G10	58	B7
8	E1	25	L5	42	G11	59	A7
9	F2	26	K6	43	F10	60	B6
10	F1	27	L6	44	F11	61	A6
11	G2	28	K7	45	E10	62	B5
12	G1	29	L7	46	E11	63	A5
13	H2	30	K8	47	D10	64	B4
14	H1	31	L8	48	D11	65	A4
15	J2	32	K9	49	C10	66	B3
16	J1	33	L9	50	C11	67	A3
17	K1	34	L10	51	B11	68	A2

Note: The letters A-H and numbers 1-8 are the coordinates of a grid. For example, pin 1 is at the intersections of the "B" vertical line and the "2" horizontal line.

2 LEAD TO-52 METAL CAN
TM2

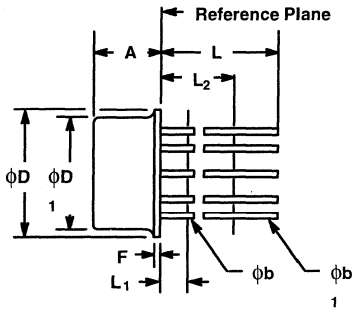


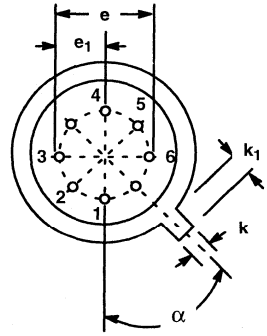
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.115	0.150	2.92	3.81	—
ϕ_b	0.016	0.019	0.406	0.483	1, 5, 3
ϕb_1	0.016	0.021	0.406	0.533	1, 5, 3
ϕD	0.209	0.230	5.31	5.84	—
ϕD_1	0.178	0.195	4.52	4.95	—
e	0.100 BSC		2.54 BSC		3
e_1	0.050 BSC		1.27 BSC		3
F	—	0.030	—	0.762	—
k	0.036	0.046	0.914	1.17	—
k_1	0.028	0.048	0.711	1.22	2
L	0.500	0.750	12.70	19.05	1
L_1	—	0.050	—	1.27	1
L_2	0.250	—	6.35	—	1
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500 (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500 (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019 (0.48 mm) measured in gauging plane. 0.054 (1.37 mm) + 0.001 (0.03 mm) – 0.000 (0.00 mm) below the base plane of the product shall be within 0.007 inch (0.18 mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – Increase maximum limit by 0.003 (0.08 mm) when lead finish A or B is applied.

6 LEAD TO-52 METAL CAN
TM6



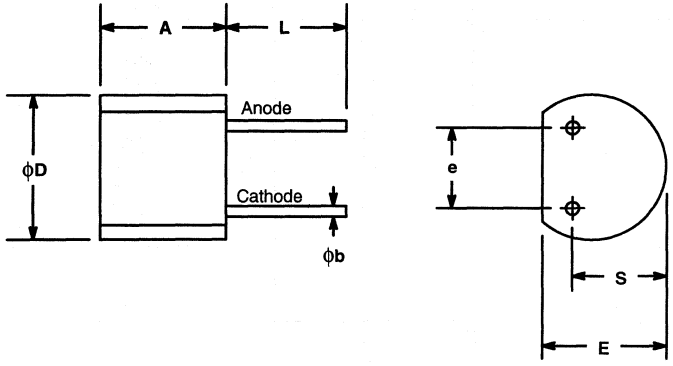


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.115	0.150	2.92	3.81	—
ϕ_b	0.016	0.019	0.406	0.483	1, 5, 3
ϕb_1	0.016	0.021	0.406	0.533	1, 5, 3
ϕD	0.209	0.230	5.31	5.84	—
ϕD_1	0.178	0.195	4.52	4.95	—
e	0.100 BSC		2.54 BSC		3
e_1	0.050 BSC		1.27 BSC		3
F	—	0.030	—	0.762	—
k	0.036	0.046	0.914	1.17	—
k_1	0.028	0.048	0.711	1.22	2
L	0.500	0.750	12.70	19.05	1
L_1	—	0.050	—	1.27	1
L_2	0.250	—	6.35	—	1
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500 (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500 (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019 (0.48 mm) measured in gauging plane. 0.054 (1.37 mm) + 0.001 (0.03 mm) – 0.000 (0.00 mm) below the base plane of the product shall be within 0.007 inch (0.18 mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – Increase maximum limit by 0.003 (0.08 mm) when lead finish A or B is applied.

2 LEAD PLASTIC TO-92
TP2



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.210	4.32	5.33
ϕb	0.016	0.021	0.406	0.533
ϕD	0.175	0.205	4.44	5.21
E	0.125	0.165	3.18	4.19
e	0.095	0.105	2.41	2.67
L	0.500	—	12.7	—
S	0.080	0.105	2.03	2.67

Thermal Data for Packages

Package Type	Lead Count	Body Width	Theta JA (°C/W)
PDIP (Cu Leadframe)	14 16 18 20 22 24 24 24 28 28 28 40	0.300" 0.300" 0.300" 0.300" 0.400" 0.300" 0.400" 0.600" 0.300" 0.400" 0.600" 0.600"	76 75 67 66 60 62 60 57 60 57 55 45
CERDIP (Alloy 42 Leadframe)	14 16 18 20 22 24 24 28 28 28 40	0.300" 0.300" 0.300" 0.300" 0.400" 0.300" 0.600" 0.300" 0.400" 0.600" 0.600"	95 90 85 76 72 68 65 63 62 60 50
SIDE BRAZED (Alloy 42)	20 24 28	0.300" 0.600" 0.600"	63 57 53
PLCC (Cu)	20 28 44 52 68		82 70 60 50 40
LCC (Leadless)	20 28		60 52
SOIC JEDEC (Cu)	8 16 16 18 20 24 28 28	0.150" 0.150" 0.300" 0.300" 0.300" 0.300" 0.300" 0.346"	160 103 92 87 82 74 70 65
SOIC EIAJ (Cu)	20	0.300"	87
SOIC EIAJ (Alloy 42)	24 24 28	0.330" 0.335" 0.335"	85 75 70
SSOP (Cu)	20 24		110 100
TSSOP	20		130
PQFP	44 44 52 64	(10 x 10) (Cu) (14 x 14) (Alloy 42) (14 x 14) (Cu) (14 x 14) (Cu)	110 100 80 65
PGA (Alloy 42)	44 68		50 32

Note: Theta JA and derating factors are nominal values; they can vary up to ±20%

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Section 9

Data Conversion Terminology

Digital-to-Analog Converter Terms

Definitions of the performance specifications and related information are provided in alphabetical order as follows:

Absolute Accuracy: The difference between the expected output voltage/current and the actual output.

Channel-to-Channel Isolation: For multiple DACs, the proportion of input signal from one DACs reference input which appears at the other DAC output. Normally expressed as a ratio in dB.

Differential Nonlinearity (DNL): The difference (in LSB) between the actual and the ideal code transitions between any two adjacent codes.

Digital Crosstalk: For multiple DACs, the glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV-Seconds, with V_{REF}-A and V_{REF}-B equal to AGND.

Digital-to-Analog Converter (DAC): A device which converts a digital input to an analog output (either voltage or current).

Feedthrough Error: A signal which results from undesired coupling from input to output. Variously specified in units of ppm, percent, mV, or fraction of LSB.

Four Quadrant Multiplication: A multiplying DAC which can operate with reference inputs and analog outputs of either positive or negative polarity.

Full Scale Output (Span): The maximum amount of output the DAC can provide when the full scale digital input code is used.

Gain: Ratio of the DACs operational amplifier output voltage to the reference voltage. "Zero" Gain is defined when V_{OUT} equals $|V_{REF}| - 1$ LSB|.

Gain Error: the difference between the actual and ideal output voltage/current measured at full scale. Also called Full Scale Error. Specified in mV, LSB, or percent of Full Scale. The ideal full scale output for a DAC of "n" bits is:

$$V_{REF}\left(\frac{2^n - 1}{2^n}\right)$$

Glitch Energy: The glitch "impulse" injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Seconds or nV-Seconds.

Harmonic Distortion (and Total Harmonic Distortion): The DAC is driven by the digitized representation of a sine wave and the resulting lower order harmonics are measured. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. The lower order harmonics are included, i.e. second through fifth:

$$THD = 20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V1 is the rms amplitude of the fundamental and V_2, V_3, V_4, and V_5 are the rms amplitudes of the individual harmonics.

Integral Nonlinearity (INL): See Relative Accuracy.

Intermodulation Distortion: The DAC is driven by the digitized representation of two combined sine waves of frequencies fa and fb. As with any imperfectly linear device, distortion products (of order m + n) are produced at sum and difference frequencies of mfa $\pm$ nfb where m, n = 0, 1, 2, 3, . . . Intermodulation terms are those for which m or n is not equal to zero. The second order terms include (fa + fb) and (fa – fb) and the third order terms are (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). IMD is defined as:

$$IMD = 20 \log \frac{\text{(rms sum of the sum and difference distortion products)}}{\text{rms amplitude of the fundamental}}$$

Latch-up Free: See Latch-Up Proof.

Latch-Up Proof: The device inputs and outputs are designed to withstand 200 mA surge currents without sustaining latch-up.

Latch-Up: A state in which a low-impedance path results from and persists following an input, output, or supply overvoltage that triggers a parasitic structure. Latch-up is identified by supply current increases that remain after

removing the trigger source. Latch-up is rated by the trigger current applied to the tested terminal.

Least Significant Bit (LSB): The bit that carries the smallest weight or value. Also refers to the smallest analog change that can be produced by the converter (a change of 1 digital input code).

Monotonicity: A property of a DAC whose analog output either increases or stays the same for an increasing digital input. A DAC with a maximum DNL of ±1 LSB is monotonic.

Most Significant Bit (MSB): The digital input bit that carries the largest weight or value.

Multiplying DAC: A DAC whose reference input can be changed. The DAC output becomes the product of the reference input and the digital output code.

Offset Error: See Zero Code Error.

Power-Supply Sensitivity: The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value per % dc change in the power supply voltage (e.g., 0.05%/1%ΔVs). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed +1/2 LSB for a 3% change in power supply. Even better performance is needed for converters designed for battery operation.

Propagation Delay (Switching Time): The time between an input code change until the DAC output reaches 90% of its final value. This is normally specified for a Full Scale output step.

R-2R Ladder: A resistor ladder network in DAC and ADC circuits which generates binary-weighted voltages or currents.

Relative Accuracy: Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale, and is normally specified in LSBs or as a percentage of Full Scale reading.

Resolution: The maximum number of discrete analog increments that a DAC can make. A DAC with n-bits of resolution is capable of 2^{n-1} increments.

Settling Time: The time required for a DAC output to settle to within a specified range (usually ±1/2 LSB) of the final value.

Signal-to-Noise Ratio (SNR): The measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the non-fundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization noise. The theoretical SNR for a sine wave is given by:

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, SNR = 50dB.

Slew Rate (or Slewing Rate): The slew rate of a device or circuit is the maximum rate of change of output voltage. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

Stability: The stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. Stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

Temperature Coefficient (Tempco): The change in amount of nonlinearity that occurs as the operating temperature of the device changes. Usually specified as %/°C or ppm/°C for parameters such as Zero Error, Linearity, or Full Scale Gain. Applies to both DACs and ADCs.

Zero Code Error: The DAC output (in mV or LSBs) when the digital input code set to zero. Also called Offset Error.

Analog-to-Digital Converter Terms

Absolute Accuracy: The difference between the expected digital output code and the actual output for a given range of inputs.

Analog-to-Digital Converter (ADC): A device which converts an analog signal to a digital code.

Bipolar: An ADC which accepts either polarity of input signal.

Differential Nonlinearity (DNL): The worst case deviation from the ideal 1 LSB step between any two adjacent digital codes in an ADC. Differential Nonlinearity greater than 1 LSB will cause missing codes in an ADC, and a non-monotonic transfer function in a DAC.

Gain Error: The difference between the actual and ideal ADC output measured with an analog multitude 1 1/2 LSB below nominal full scale input. Specified as percent of FSR, or LSB. Also called Full Scale Error.

Flash Converter: An ADC configured such that all bit comparisons are made simultaneously. The advantage of this scheme is high conversion speed.

Integral Nonlinearity (INL): The worst case deviation from a line between the ADC end points (zero and Full Scale). Specified either in terms of LSBs or percent of Full Scale.

Latch-up Free: See Latch-Up Proof.

Latch-Up Proof: The device inputs and outputs are designed to withstand 200 mA surge currents without sustaining latch-up.

Latch-Up: A state in which a low-impedance path results from and persists following an input, output, or supply overvoltage that triggers a parasitic structure. Latch-up is identified by supply current increases that remain after removing the trigger source. Latch-up is rated by the trigger current applied to the tested terminal.

Least Significant Bit (LSB): The output bit that carries the smallest weight or value. Also refers to the amount of analog input change required to cause an output code change of 1.

Most Significant Bit (MSB): The output bit that carries the largest weight or value.

No Missing Codes: The ability of an ADC to generate every possible output code as the analog input is swept through its range.

Ratiometric Conversion: A ratiometric converter derives the input signal from a reference voltage that is also used as a reference for the ADC. Typical applications include transducers and bridge circuits.

Relative Accuracy: The deviation of the ADCs actual code transition points form a straight line drawn between the devices' measured zero and measured full scale transition points. Relative Accuracy, therefore, is a measure of code position. Also called Integral Nonlinearity.

Resolution: The maximum number of analog levels which can be resolved by the ADC. An ADC with n-bits of resolution is capable of 2^n increments or levels.

Sample and Hold: A circuit which when given a command instantly "samples" a changing input signal and outputs a DC signal representing the voltage level of the sampled input.

Unipolar: An ADC which accepts only one polarity of input signal.

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